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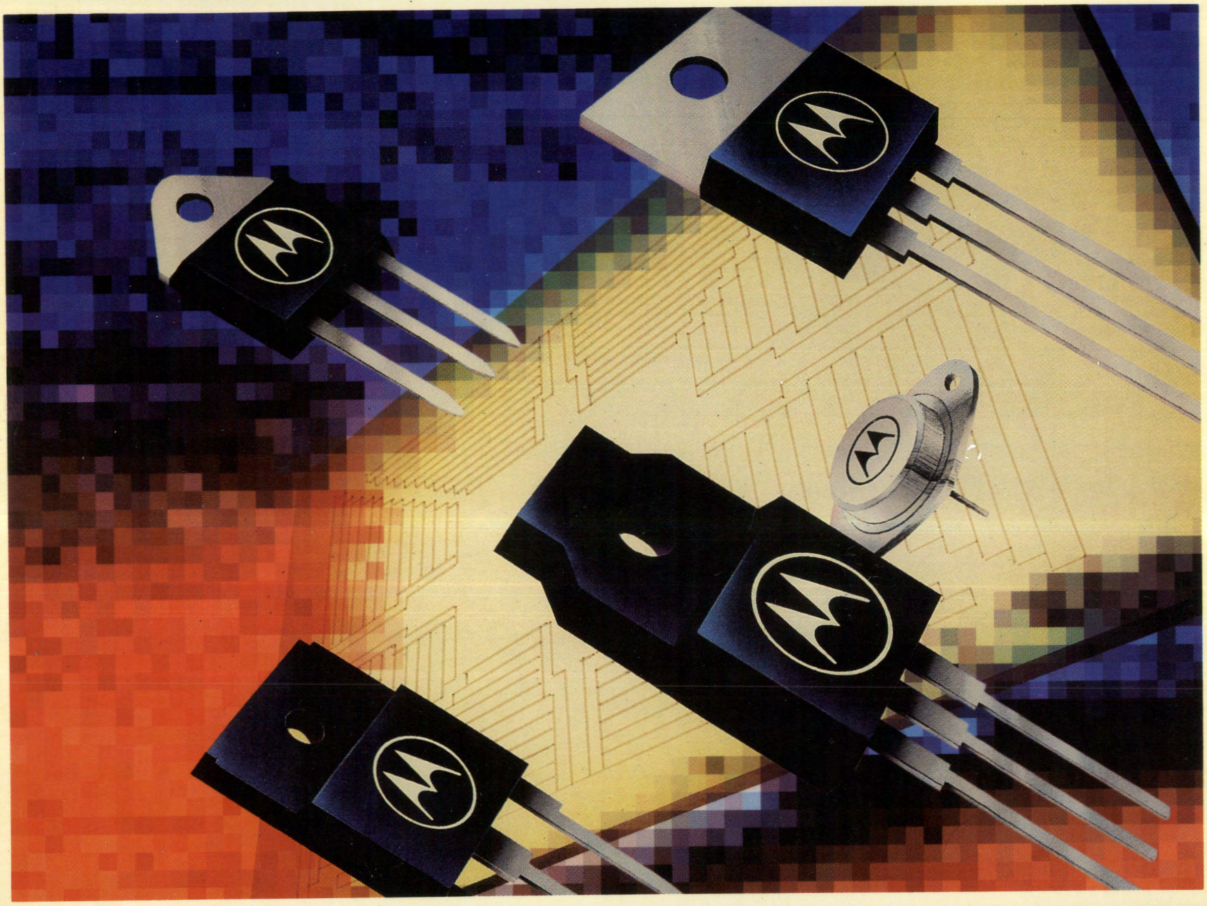
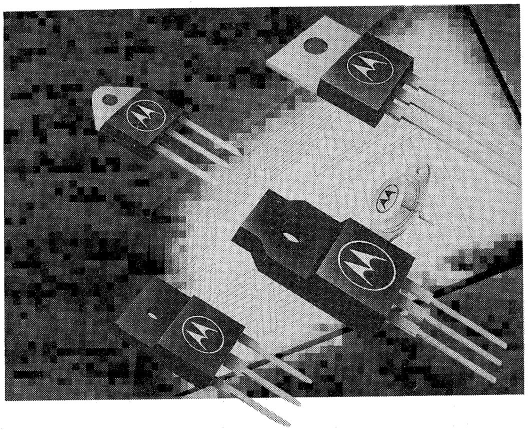


BIPOLAR POWER TRANSISTOR DATA



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MOTOROLA

POWER DEVICE DATA

Prepared by
Technical Information Center

This book presents technical data for Motorola's broad line of silicon power transistors. Complete specifications are provided in the form of data sheets and accompanying selection guides provide a quick comparison of characteristics to simplify the task of choosing the best device for a circuit.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

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Fifth Edition

Printed in U.S.A.

MOTOROLA POWER TRANSISTORS IN BRIEF

Wide Range of Transistor Specifications

Bipolar transistors, NPNs and PNPs, single and multiple (Darlington) transistor structures, metal and plastic packages, Motorola's inventory of more than 1100 standard (off-the-shelf) power transistors covers the widest range of specifications for virtually every potential applications requirement.

Current Range — 0.5 to 100 Amperes
Voltage Range — 25 to 1800 Volts
Power Dissipation Range — 5 to 250 Watts.

Darlingtons

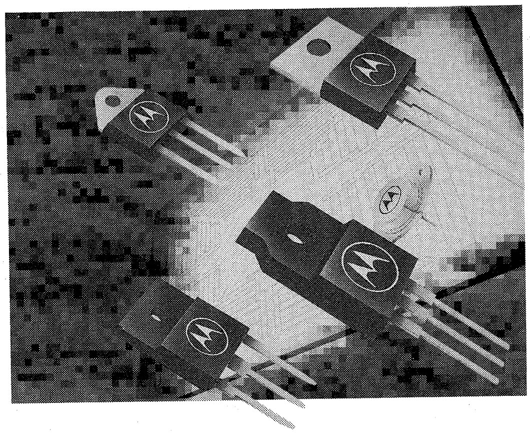
Consisting of two transistors, up to two resistors, and (up to) two diodes on a single chip, Darlington transistors achieve gain figures up to 20,000 in a single package. Rapid line expansion, and the resulting widespread implementation make Motorola Darlingtons highly cost-effective in a fast growing number of applications.

Chips, Chips, Chips!

Designing a hybrid? Motorola's wide range of power transistors is available. . . . UNENCAPSULATED through authorized chip distributors: Check with your Motorola Sales representative for the chip distributor in your area, preferred parts list, price and delivery.

Specials

Need a unique transistor with specifications not available off-the-shelf? Chances are Motorola can produce it quickly and inexpensively. Routine use of four major power processes and more than two decades of experience in the pioneering of new structures and geometries provide the insight and capability to meet any required specification within the limits of today's technology. Specials will require minimum order quantities and minimum yearly run rates. Check with your local Motorola representative for more information on special devices.



Alphanumeric Index and Cross Reference

1

The table on the subsequent pages contains an Alphanumeric index of Silicon power transistors currently manufactured and available to the industry.

The column headed "Similar" lists units with characteristics that might represent suitable replacements. In cases where such a replacement is contemplated, the Motorola device data sheet should be carefully compared with one for the device being replaced to determine any variations that could affect circuit performance.

ALPHANUMERIC INDEX — CROSS-REFERENCE

The following table represents an index and cross-reference guide for all low-frequency power transistors which are either manufactured directly by Motorola or for which Motorola manufactures a suitable equivalent. Where the Motorola part number differs from the Industry part number, the Motorola device is a "form, fit and function" replacement for the industry type number — however, subtle differences in characteristics and/or specifications may exist.

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2N3867SJAN	2N3867SJAN		3-32
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*Consult Motorola if a direct replacement is necessary.

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2N5335		2N5337	3-100
2N5336	2N5336		3-100
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*Consult Motorola if a direct replacement is necessary.

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MJ10025	MJ10025		3-723
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*Consult Motorola if a direct replacement is necessary.
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CM Consult Motorola if a direct replacement is necessary.

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SVT7543		MJ13080	3-810
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*Consult Motorola if a direct replacement is necessary.

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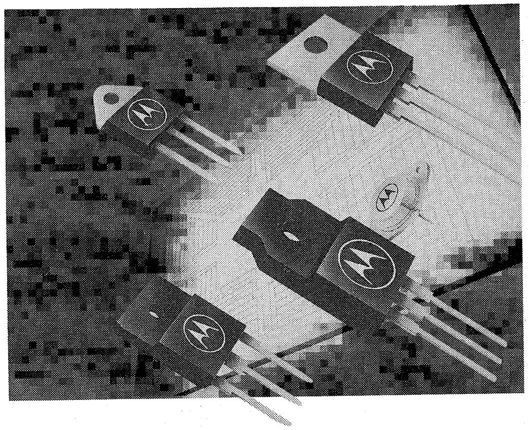

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Selector Guide

The selector guides on the subsequent pages offer a quick "first-selection" capability for devices that fit specific applications categories.

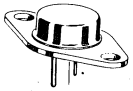
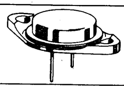
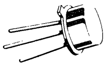
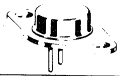
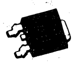
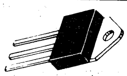
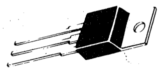
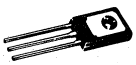
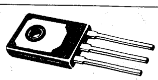
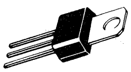
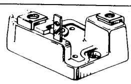
Because designers have different application prerequisite, the devices are categorized in three ways:

1. *by package*
2. *by major product category*
3. *by major applications*

In each case, pertinent electrical characteristics are supplied to permit rapid comparison of potentially suitable devices.

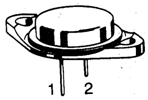
Selection By Package

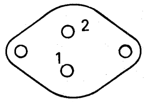
Motorola power transistors are available in a wide variety of metal and plastic packages to match thermal, electrical and cost requirements. The following table compares the basic packages from the standpoint of current, voltage and power capabilities. The devices available in the various packages are tabulated on the succeeding pages.

Package		I_C Range (Amps)	V_{CE} Range (Volts)	P_D (Watts)	Page #
	TO-204AA (TO-3) Case 1 Case 11	2.5–30	40–1500	36–250	2-3
	TO-204AE Case 197	2.5–70	40–1500	36–350	2-3
	TO-205AA Case 31 (TO-5)	3.0	40–800	6.0	2-8
	TO-205AD (TO-39) Case 79	0.5–5.0	40–400	5.0–10	2-8
	TO-213AA (TO-66) Case 80	1.0–10	40–325	20–90	2-9
	DPAK Case 369-03	0.5–10	40–400	12.5–20	2-18
	DPAK Case 369A-04	0.5–10	40–400	12.5–20	2-18
	TO-218AC Case 340	5.0–25	40–1500	80–150	2-10
	TO-220AB Case 221A	0.5–15	30–1800	15–125	2-12
	TO-225AA TYPE Case 77	0.3–5.0	25–400	12.5–40	2-15
	TO-225AB Case 90	5.0–15	40–100	65–100	2-17
	Case 152	0.5–2.0	30–300	10	2-17
	Case 353	25–100	250–850	250	2-18

Bipolar Power Transistors

TABLE 1 — METAL TO-204AA (Formerly TO-3) — TO-204AE (Type)





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

CASE 11-01, 11-3 — 40 mil pins
CASE 1-04, 1-05 — 40 mil pins
MODIFIED TO-3
CASE 197-01 — 60 mil pins

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
2.5	800	MJ8501		7.5 min	0.5	4	2	1		125
	1500*	BU205		2 min		2	0.75 typ	2	4 typ	36
		MJ12002		1.11 min	2		1	2	4 typ	75
3.5	325	2N3902		30/90	1	1.2 typ	0.1 typ	1	2.8	100
4	1500*	MJ12003		2.5 min	3		1	3		100
5	200	MJ410		30/90	1				2.5	100
	250	MJ3029		30 min	0.4		1	3		125
	300	MJ411		30/90	1				2.5	100
	400	2N6543		7/35	3	4	0.8	3	6	100
		MJ13070		8 min	3	1.5	0.5	3		125
	450	MJ13071		8 min	3	1.5	0.5	3		125
		MJ16002		5 min	5	3	0.3	3		125
		MJ16004		7 min	5	2.7	0.35	3		125
		2N6834		10/30	3	2.7	0.35	3	15	125
	500	MJ16002A		5 min	5	3	0.3	3		125
	700	MJ8502		7.5 min	1	4	2	2.5		150
	800	MJ8503		7.5 min	1	4	2	2.5		150
	850*	MJ12020		5 min	5		0.13 typ	3	15	125
	1500*	BU208		2.25 min	4.5		0.6 typ	4.5	4 typ	60
		BU208A		2.25 min	4.5	8 typ	0.4 typ	4.5	4 typ	90
		BU208D†		2.25 min	4.5		0.6 typ	4.5	4 typ	60
		MJ12004		2.5 min	4.5		1	4.5	4	100
6	100	2N5758	2N6226	25/100	3	0.7 typ	0.5 typ	3	1	150
	120	2N5759	2N6227	20/80	3	0.7 typ	0.5 typ	3	1	150
	140	2N5760	2N6228	15/60	3	0.7 typ	0.5 typ	3	1	150

(continued)

$|h_{fe}|$ @ 1 MHz, ## Darlington
* $V_{(BR)CEX}$ or $V_{(BR)CES}$
† D Suffix on this device signifies internal C-E Diode

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TABLE 1 — METAL TO-204AA — TO-204AE (Type) (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
6	375	BU326		30 typ	0.6	3.5	1**	2.5	6	90
	400	BU326A		30 typ	0.6	3.5	1**	2.5	6	90
7	300	MJ3041##		250 min	2.5					175
	350	MJ3042##		250 min	2.5					175
7.5	60	2N3447		40/120	5	2	0.35	5	10	115
	80	2N3448		40/120	5	2	0.35	5	10	115
8	60	MJ1000##	MJ900##	1k min	3					90
		2N6055##	2N6053##	750/18k	4	1.5 typ	1.5 typ	4	4#	100
	80	MJ1001##	MJ901##	1k min	3					90
		2N6056##	2N6054##	750/18k	4	1.5 typ	1.5 typ	4	4#	100
	250	2N6306		15/75	3	1.6	0.4	3	5	125
	300	2N6307		15/75	3	1.6	0.4	3	5	125
	350	2N6308		12/60	3	1.6	0.4	5	5	125
	400	2N6545		7/35	5	4	1	5	6	125
			MJ6503	15 min	2	2	0.5	4		125
		MJ13080		8 min	5	1.5	0.5	5		150
	450	MJ13081		8 min	5	1.5	0.5	5		150
		MJ16006		5 min	8	2.5	0.25	5		150
		MJ16008		7 min	8	2.2	0.25	5		150
		2N6835		10/30	5	2.5	0.25	5	10	150
	500	MJ16006A		5 min	8	3	0.4	5		150
	850*	MJ12021		5 min	8		0.1 typ	5		150
	1400*	MJ10011##		20 min	4		1	4		80
	1500*	MJ12005		5 min	5		1	5		100
9	400	BUS47		7 min	6	2	0.4	6		150
	450	BUS47A		7 min	5	2	0.4	5		150
10	40	2N6383##	2N6648##	1k/20k	5				20#	100
	60	BD311	BD312	25 min	5				4	115
			2N3789	15 min	3	0.3 typ	0.4 typ	5	4	150
		2N3715	2N3791	30 min	3	0.3 typ	0.4 typ	5	4	150
		2N5877	2N5875	20/100	4	1	0.8	4	4	150
		2N6384##		1k/20k	5				20#	100
		MJ3000##	MJ2500##	1k min	5					150
	80	2N3714	2N3790	15 min	3	0.3 typ	0.4 typ	5	4	150
		2N3716	2N3792	30 min	3	0.3 typ	0.4 typ	5	4	150
		2N5878	2N5876	20/100	4	1	0.8	4	4	150
		2N6385##		1k/20k	5				20#	100
		MJ3001##	MJ2501##	1k min	5					150
	140	2N5634		15/60	5	0.9 typ	0.9 typ	5	1	150
		2N3442		20/70	4					117

* $V_{(BR)CEX}$, # $|h_{fe}|$ @ 1 MHz, ## Darlington

(continued)

JAN, JTX, JTXV Available

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TABLE 1 — METAL TO-204AA — TO-204AE (Type) (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
10	250	MJ15011	MJ15012	20/100	2					200
	325	BUX43		8 min	5	2.2	0.9	5	8	120
		MJ413		20/80	0.5				2.5	125
		MJ423		30/90	1				2.5	125
		MJ431		15/35	2.5				2.5	125
	350	BU323##		150 min	6	7.5 typ	5.2 typ	6		175
		MJ13014		8/20	5	2	0.5	5		150
		MJ10002##		3/300	5	2.5	1	5	10#	150
		MJ10006##		30/300	5	1.5	0.5	5	10#	150
	400	BU323A##		150 min	6	7.5 typ	5.2 typ	6		175
		MJ10007##		30/300	5	1.5	0.5	5	10#	150
		MJ10012##		100/2k	6	15	15	6		175
		MJ13015		8/20	5	2	0.5	5		150
	600	MJ10014##		10/250	10	2.5	0.8	10		175
	700	MJ8504		7.5 min	1.5	4	2	5		175
	800	MJ8505		7.5 min	1.5	4	2	5		175
		MJ16018		4 min	5	4.5 typ	0.2 typ	5		150
	950*	MJ12010		4.2 min	5		1	5		100
12	60	2N6057##	2N6050##	750/18k	6	1.6 typ	1.5 typ	6	4#	150
	80	2N6058##	2N6051##	750/18k	6	1.6 typ	1.5 typ	6	4#	150
	100	2N6059##	2N6052##	750/18k	6	1.6 typ	1.5 typ	6	4#	150
	250	BUX42		8 min	6	2	0.4	6	8	120
	1000	BUT16##		5 min	8	3.3	1.5	8		150
15	60	2N3055	MJ2955	20/70	4	0.7 typ	0.3 typ	4	2.5	115
		2N3055A	MJ2955A	20/70	4				0.8	115
		2N6576##		2k/20k	4	2	7	10	10–200#	120
		2N5881	2N5879	20/100	6	1	0.8	6	4	160
	80	2N5882	2N5880	20/100	6	1	0.8	6	4	160
	90	2N6577##		2k/20k	4	2	7	10	10-200#	120
	120	MJ15015	MJ15016	20/70	4				1	180
		2N6578##		2k/20k	4	2	7	10	10-200#	120
	140	MJ15001	MJ15002	25/150	4				2	200
	150	MJ11018##	MJ11017##	100 min	15				3#	175
	200	BUX41		8 min	8	1.5	0.4	8	8	120
		2N6249		10/50	10	3.5	1	10	2.5	175
		MJ11020##	MJ11019##	100 min	15				3#	175
	250	MJ11022##	MJ11021##	100 min	15				3#	175
	275	2N6250		8/50	10	3.5	1	10	2.5	175
	300	2N6546		6/30	10	4	0.7	10	6 to 24	175
		2N6676		8 min	15	2.5	0.5	15	3	175
	325	BUX13		8 min	8	2.5	0.8	8	8	150
	400	BUS48		8 min	10	2	0.4	10		175
		BUX48				3	0.8	10		175
		2N6547		6/30	10	4	0.7	10	6 to 24	175
		2N6678		8 min	15	2.5	0.5	15	3	175
		MJ13090		8 min	10	2.5	0.5	10		175
	450	BUS48A		8 min	10	2	0.4	10		175
		BUX48A				3	0.8	8		175
		MJ13091		8 min	10	2.5	0.5	10		175
		MJ16010		5 min	15	1.2 typ	0.2 typ	10		175

(continued)

[shaded box] JAN, JTX, JTXV Available

* $V_{(BR)CEX}$, # $|h_{fe}|$ @ 1 MHz, ## Darlington

2

TABLE 1 — METAL TO-204AA — TO-204AE (Type) (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	t_f μs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
15		MJ16012 2N6836		7 min 10/30	15 10	0.9 typ 3	0.15 typ 0.35	10 10	 10	175 175
	500	MJ16010A		5 min	15	3	0.4	10		175
	850*	MJ12022		5 min	15		0.1 typ	10		175
16	60	MJ4033##	MJ4030##	1k/	10					150
	80	BD315 MJ4034##	BD316 MJ4031##	25 min 1k/	5 10				1	200 150
	100	BD317 2N5629 MJ4035##	BD318 2N6029 MJ4032##	25 min 25/100 1k/	5 8 10	 1.2 typ	 1.2 typ	 8	1 1	200 200 150
	120	2N5630	2N6030	20/80	8	1.2 typ	1.2 typ	8	1	200
	140	2N3773 2N5631	2N6609 2N6031	15/60 15/60	8 8	1.1 typ 1.2 typ	1.5 typ 1.2 typ	8 8	4 1	150 200
	200	MJ15022	MJ15023	15/60	8				5	250
	250	MJ15024	MJ15025	15/60	8				5	250
18	160	BUX41N		8 min	12	1.2	0.25	12	8	120
20	60	2N3772 2N6282##	 2N6285##	15/60 750/18k	10 10	 2.5 typ	 2.5 typ	 10	2 4#	150 160
	75	2N5039		20/100	10	1.5	0.5	10	60	140
	80	2N5303 2N6283##	2N5745 2N6286##	15/60 750/18k	10 10	2 2.5 typ	1 2.5 typ	10 10	2 4#	200 160
	90	2N5038		20/100	12	1.5	0.5	12	60	140
	100	2N6284##	2N6287##	750/18k	10	2.5 typ	2.5 typ	10	4#	160
	125	BUX40		8 min	15	1	0.25	15	8	120
	140	MJ15003	MJ15004	25/150	5				2	250
	160	BUV11N		10 min	15	1.2	0.25	15	8	150
	200	BUV11 MJ13330		10 min 8/40	12 10	1.8 3.5	0.4 0.7	12 10	8 5 to 40	150 175
	250	BUV12 MJ13331		10 min 8/40	10 10	1.5 3.5	0.5 0.7	10 10	8 5 to 40	150 175
	350	MJ10000## MJ10004##		40/400 40/400	10 10	3 1.5	1.8 0.5	10 10	10# 10#	175 175
	400	BUV24 MJ10001## MJ10005## MJ13333		8 min 40/400 40/400 10/60	12 10 10 5	3 3 1.5 4	0.9 1.8 0.5 0.7	12 10 10 10	8 10# 10#	250 175 175 175
	450	MJ10008## MJ16014 MJ16016 2N6837		30/300 5 min 7 min 10/30	10 20 20 15	2 2.7 2.2 2.5	0.6 0.35 0.25 0.25	10 20 20 15	8#	175 250 250 250
	500	MJ10009## MJ13335		30/300 10/60	10 5	2 4	0.6 0.7	10 10	8#	175 175
	700	BUT15##		15 min	12	2.5	0.8	12		175
	750	MJ10024##		50/600	20	5	1.8	10		250
	850	MJ10025##		50/600	20	5	1.8	10		250

* $V_{(BR)CEX}$, # $|h_{fe}|$ @ 1 MHz, ## Darlington

JAN, JTX, JTXV Available

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TABLE 1 — METAL TO-204AA — TO-204AE (Type) (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
24	1000	BUT36##		5 min	16	6	2.5	16		250
25	60	2N5885	2N5883	20/100	10	1	0.8	10	4	200
	80	2N5886	2N5884	20/100	10	1	0.8	10	4	200
			2N6436	30/120	10	1	0.25	10	40	200
	100	2N6338	2N6437	30/120	10	1	0.25	10	40	200
	120	2N6339	2N6438	30/120	10	1	0.25	10	40	200
	125	BUV10		10 min	20	1.2	0.25	20	8	150
		BUV10N		10 min	20	1.55	0.45	15	10	175
	140	2N6340		30/120	10	1	0.25	10	40	200
	150	2N6341		30/120	10	1	0.25	10	40	200
	500	BUT14##		15 min	16	2.8	0.8	16		175
28	400	BUT13##		20 min	20	2.6	0.8	18		175
30	40	2N3771		15/60	15				2	150
		2N5301	2N4398	15/60	15	2	1	10	2	200
	60	2N5302	2N4399	15/60	15	2	1	10	2	200
		MJ11012##	MJ11011##	1k min	20				4#	200
	90	BUX39		8 min	20	1	0.25	20	8	120
		MJ11014##	MJ11013##	1k min	20				4#	200
	100	2N6328		6/30	30				3	200
		MJ802	MJ4502	25/100	7.5				2	200
	120	MJ11016##	MJ11015##	1k min	20				4#	200
	325	BUV23•		8 min	16	1.8	0.4	16	8	250
	400	BUS98•		8 min	20	2.3	0.4	20		250
		BUX98				3	0.8	20		250
	450	BUS98A•		8 min	16	2.3	0.4	16		250
		BUX98A				3	0.8	16		250
		MJ16020•		5 min	30	1.8	0.2	20		250
		MJ16022•		7 min	30	1.5	0.15	20		250
40	160	BUV21N•		10 min	40	1	0.2	40	8	250
	200	BUV21•		10 min	25	1.8	0.4	25	8	150
	250	BUS52•		15 min	40					350
		BUV22•		10 min	20	1.1	0.35	20	8	250
	350	MJ10022•##		50/600	120	2.5	0.9	20		250
	400	MJ10023•##		50/600	10	2.5	0.9	20		250
	700	BUT35•##		15 min	24	4	1.2	24		250
50	60	2N5685•	2N5683•	15/60	25	0.5 typ	0.3 typ	25	2	300
		MJ11028•##	MJ11029•##	400 min	50					300
	80	2N5686•	2N6584•	15/60	25	0.5 typ	0.3 typ	25	2	300
			2N6377•	30/120	20	0.8	0.25	20	30	250
	90	MJ11030•##	MJ11031•##	400 min	50					300
	100	2N6274•	2N6378•	30/120	20	0.8	0.25	20	30	250
	120	2N6275•	2N6379•	30/120	20	0.8	0.25	20	30	250
		MJ11032•##	MJ11033•##	400 min	50					300
	125	BUV20•		10 min	50	1.2	0.25	50	8	250
	150	2N6277•		30/120	20	0.8	0.25	20	30	250

• Modified TO-3, 60 mil pins, # $|h_{fe}|$ @ 1 MHz, ## Darlington

▒ JAN, JTX, JTXV Available

2

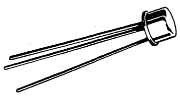
TABLE 1 — METAL TO-204AA — TO-204AE (Type) (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
50	200	BUS51●		15 min	50					350
	400	MJ10015●##		10 min	40	2.5	1	20		250
	500	BUT34●## MJ10016●##		15 min 10 min	32 40	3 2.5	1.5 1	32 20		250 250
56	400	BUT33●##		20 min	36	3.3	1.6	36		250
60	60	MJ14000●	MJ14001●	15/100	50					300
	80	MJ14002●	MJ14003●	15/100	50					300
	200	MJ10020●##		75 min	15	3.5	0.5	30		250
	250	MJ10021●##		75 min	15	3.5	0.5	30		250
70	125	BUS50●		15 min	50					350

● Modified TO-3, 60 mil pins, # $|h_{fe}|$ @ 1 MHz, ## Darlington

TABLE 2 — METAL TO-205AA PACKAGE (Formerly TO-5)

CASE 31-03



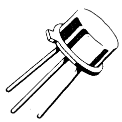
STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

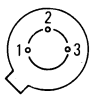
I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
3	40		2N3719 2N3867	25/180 40/200	1 1.5	0.4* 0.4*		1 1.5	60 60	6 6
	60		2N3720 2N3868	25/180 30/150	1 1.5	0.4* 0.4*		1 1.5	60 60	6 6
	80		2N6303	30/150	1.5	0.4*		1.5	60	6

*t_{off}

TABLE 3 — METAL TO-205AD PACKAGE (Formerly TO-39)

CASE 79-02





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(Pin 3 connected to case)

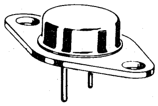
I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.5	300		MJ4646	20 min	0.5	0.72*		0.05	40	5
	400		MJ4647	20 min	0.5	0.72*		0.05	30	5
4	60	2N4877		20/100	4	1.5	0.5	4	4	10
5	80	2N5336 2N5337	2N6190 2N6191	30/120 60/240	2 2	2 2	0.2 0.2	2 2	30 30	6 6
	100	2N5338 2N5339	 2N6193	30/120 60/240	2 2	2 2	0.2 0.2	2 2	30 30	10 6

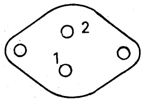
JAN, JTX, JTXV Available

*t_{off}

TABLE 4 — METAL TO-213AA PACKAGE (Formerly TO-66)

CASE 80-02





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
1	40		2N4898	20/100	0.5	0.6 typ	0.3 typ	0.5	3	25
	60		2N4899	20/100	0.5	0.6 typ	0.3 typ	0.5	3	25
	80	2N4912	2N4900	20/100	0.5	0.6 typ	0.3 typ	0.5	3	25
	175	2N3583	2N6420	40/200	0.5	2 typ	0.23 typ	0.5	10	35
	225	2N3738		40/200	0.1	3 typ	0.3 typ	0.1	10	20
	250		2N5344	25/100	0.5	0.6	0.1	0.5	60	40
	300	2N3739		40/200	0.1	3 typ	0.3 typ	0.1	10	20
2	225		2N6211	10/100	1	2.5	0.6	1	20	35
	250	2N3584	2N6421	25/100	1	4	3	1	10	35
	300		2N6212	10/100	1	2.5	0.6	1	20	35
		2N3585	2N6422	25/100	1	4	3	1	10	35
		2N4240		30/150	0.75	6	3	0.75	15	35
	350		2N6213	10/100	1	2.5	0.6	1	20	35
3	140	2N3441		25/100	0.5				0.2	25
4	60		2N3740	30/100	0.25	1.3 typ	0.27 typ	0.25	4	25
		2N3054,A	2N6049	25/100	0.5	1 typ	0.3 typ	0.5	3	75
		2N3766		40/160	0.5	0.9 typ	0.09 typ	0.5	10	20
		2N6294##	2N6296##	750/18k	2	0.9 typ	0.7 typ	2	4#	50
	80		2N3741	30/100	0.25	1.3 typ	0.27 typ	0.25	4	25
		2N3767		40/160	0.5	0.9 typ	0.09 typ	0.5	10	20
		2N6295##	2N6297##	750/18k	2	0.9 typ	0.7 typ	2	4	50
5	80	2N4233A		25/100	1.5	0.5 typ	0.2 typ	1.5	4	75
	275	2N6233		25/125	1	3.5	0.5	1	20	50
	325	2N6235		25/125	1	3.5	0.5	1	20	50
7	60	2N6315	2N6317	20/100	2.5	1	0.8	2.5	4	90
	80	2N5428		60/240	2	2	0.2	2	30	40
		2N6316	2N6318	20/100	2.5	1	0.8	2.5	4	90
	100	2N5429		30/120	2	2	0.2	2	30	40
		2N5430		60/240	2	2	0.2	2	30	40
8	60	2N6300##	2N6298##	750/18k	4	1.5 typ	1.5 typ	4	4#	75
	80	2N6301##	2N6299##	750/18k	4	1.5 typ	1.5 typ	4	4#	75
10	80	2N6495		10/60	10	0.15 typ	0.05 typ	10	25	70

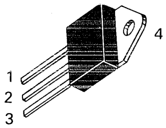
$|h_{fe}|$ @ 1 MHz, ## Darlington

JAN, JTX, JTXV Available

2

TABLE 5 — PLASTIC TO-218AC PACKAGE

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



CASE 340-01

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
3	750	MJH16032		4 min	3	2	1.5	2		125
	850	MJH16034		4 min	3	2	1.5	2		125
5	400	BUW11		6 min	3	4	0.8	3		125
	450	BUW11A		6 min	2.5	4	0.8	2.5		125
		MJH16002		5 min	5	3	0.3	3		100
		MJH16004		7 min	5	2.7	0.35	3		100
	500	MJH16002A		5 min	5	3	0.3	3		100
	1500*	MJH12004		2.5 min	4.5	—	1	4.5	4	100
6	375	BU426		30 typ	0.6	2 typ	0.5 typ	2.5	6 typ	113
	400	BU426A		30 typ	0.6	2 typ	0.5 typ	2.5	6 typ	113
8	400	BUW12		6 min	6	4	0.8	5		125
	450	BUW12A		6 min	5	4	0.8	5		125
		MJH16006		5 min	8	2.5	0.25	5		125
		MJH16008		7 min	8	2.2	0.25	5		125
	500	BUT50P##		30 min	2	0.75 typ	0.1 typ	5		100
		MJH16006A		5 min	8	2.5	0.25	5		125
	700	BU508,A		2.25 min	4.5	8 typ	0.5 typ	4.5	7	125
		BU508D,AD		2.25 min	4.5	8 typ	0.5 typ	4.5	7	125
	750	MJH12005					0.4 typ	5	4	100
9	400	BUS47P		7 min	5	2	0.4	6		128
	450	BUS47AP		7 min	6	2	0.4	6		128
10	40	TIP33	TIP34	20 min	3				3	80
	60	BDV65##	BDV64##	1k min	5					125
		TIP33A	TIP34A	20 min	3				3	80
		TIP140##	TIP145##	500 min	10	2.5 typ	2.5 typ	5	4#	125
	80	BDV65A##	BDV64A##	1k min	5					125
		TIP33B	TIP34B	20 min	3				3	80
		TIP141##	TIP146##	500 min	10	2.5 typ	2.5 typ	5	4#	125
	100	BDV65B##	BDV64B##	1k min	5					125
		TIP33C	TIP34C	20 min	3				3	80
		TIP142##	TIP147##	500 min	10	2.5 typ	2.5 typ	5	4#	125
	120	BDV65C##	BDV64C##	1k min	5					125
	200	BU323P##		150 min	6	15	15	6		125
	250	BU323AP##		150 min	6	15	15	6		125
	400	MJH10012##		100/2k	6	15	15	6		118
	800	MJH16018		4 min	5	4.5 typ	0.2 typ	5		150
15	60	TIP3055	TIP2955	5 min	10				2.5	80
	150	MJH11018	MJH11017	400/15k	10				3#	150

$|h_{fe}|$ @ 1 MHz, ## Darlington
* $V_{(BR)CEX}$ or $V_{(BR)CES}$

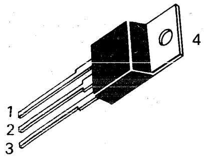
(continued)

TABLE 5 — PLASTIC TO-218AC PACKAGE (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
15	200	**MJH11020**	**MJH11019**	400/15k	10				3#	150
	250	**MJH11022**	**MJH11021**	400/15k	10				3#	150
	300	**MJH6676**		8 min	15	2.5	0.5	15		125
	350	**MJH6677**		8 min	15	2.5	0.5	15		125
	400	**BUS48P**		8 min	10	2	0.4	10		150
		BUW13				4	0.8	10		175
		MJH6678		8 min	15	2.5	0.5	15		125
		MJH13090		8 min	10	2.5	0.5	10		125
	450	**BUS48AP**		8 min	8	2	0.4	10		150
		BUW13A				4	0.8	8		175
		MJH13091		8 min	10	2.5	0.5	10		125
		MJH16010		5 min	15	1.2	0.2	10		150
		MJH16012		7 min	15	0.9	0.15	10		150
	500	**BUT51P##**		40 min	5	1.1	0.16	10		125
		MJH16010A		5 min	15	3	0.4	10		150
16	100	**MJE4340**	**MJE4350**	15 min	8	1.2 typ	1.2 typ	8	1	125
	120	**MJE4341**	**MJE4351**	15 min	8	1.2 typ	1.2 typ	8	1	125
	140	**MJE4342**	**MJE4352**	15 min	8	1.2 typ	1.2 typ	8	1	125
	160	**MJE4343**	**MJE4353**	15 min	8	1.2 typ	1.2 typ	8	1	125
20	60	**MJH6282##**	**MJH6285##**	750/18k	10				4#	125
	80	**MJH6283##**	**MJH6286##**	750/18k	10				4#	125
	100	**MJH6284##**	**MJH6287##**	750/18k	10				4#	125
25	40	**TIP35**	**TIP36**	10/75	15	0.6 typ	0.3 typ	10	3	125
	45	**BD249**	**BD250**	10 min	15				3	125
	60	**BD249A**	**BD250A**	10 min	15				3	125
		TIP35A	**TIP36A**	10/75	15	0.6 typ	0.3 typ	10	3	125
	80	**BD249B**	**BD250B**	10 min	15				3	125
		TIP35B	**TIP36B**	10/75	15	0.6 typ	0.3 typ	10	3	125
	100	**BD249C**	**BD250C**	10 min	15				3	125
		TIP35C	**TIP36C**	10/75	15	0.6 typ	0.3 typ	10	3	125

$|h_{fe}|$ @ 1 MHz, ## Darlington

TABLE 6 — PLASTIC TO-220AB PACKAGE



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-02

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
0.5	350	MJE2360T MJE2361T		15 min 40 min	0.1 0.1				10 typ 10 typ	30 30
1	40	TIP29	TIP30	15/75	1	0.6 typ	0.3 typ	1	3	30
	60	TIP29A	TIP30A	15/75	1	0.6 typ	0.3 typ	1	3	30
	80	TIP29B	TIP30B	15/75	1	0.6 typ	0.3 typ	1	3	30
	100	TIP29C	TIP30C	15/75	1	0.6 typ	0.3 typ	1	3	30
	250	TIP47		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	300	TIP48		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	350	TIP49		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	400	TIP50		30/150	0.3	2 typ	0.18 typ	0.3	10	40
2	45	BD239	BD240	15 min	1				3	30
	60	BD239A TIP110##	BD240A TIP115##	15 min 500 min	1 2	1.7 typ	1.3 typ	2	3 25#	30 50
	80	BD239B TIP111##	BD240B TIP116##	15 min 500 min	1 2	1.7 typ	1.3 typ	2	3 25#	30 50
	100	BD239C TIP112##	BD240C TIP117##	15 min 500 min	1 2	1.7 typ	1.3 typ	2	3 25#	30 50
	400	BUX84		30 min	0.1	3.5	1.4	1	4	50
	450	BUX85		30 min	0.1	3.5	1.4	1	4	50
	900	MJE1320		3 min	1	4 typ	0.8 typ	1		80
2.5	700	MJE8500		7.5 min	0.5	4	2	1		65
	750	MJE12007		1.1 min	2		1	2	4 typ	65
	800	MJE8501		7.5 min	0.5	4	2	1		65
3	40	TIP31	TIP32	25 min	1	0.6 typ	0.3 typ	1	3	40
	45	BD241	BD242	25 min	1				3	40
	60	BD241A TIP31A	BD242A TIP32A	25 min 25 min	1 1	0.6 typ	0.3 typ	1	3 3	40 40
	80	BD241B TIP31B	BD242B TIP32B	25 min 25 min	1 1	0.6 typ	0.3 typ	1	3 3	40 40
	100	BD241C TIP31C	BD242C TIP32C	25 min 25 min	1 1	0.6 typ	0.3 typ	1	3 3	40 40
	750	MJE16032		4 min	3	2	1.5	2		80
	850	MJE16034		4 min	3	2	1.5	2		80
4	45	2N6121 BD533	2N6124 BD534	25/100 25 min	1.5 2	0.4 typ	0.3 typ	1.5	2.5 3	40 50
	60	2N6122 BD535 MJE800T##	2N6125 BD536 MJE700T##	25/100 25 min 750 min	1.5 2 1.5	0.4 typ	0.3 typ	1.5	2.5 3 1#	40 50 40
	80	2N6123 BD537	 BD538	20/80 15 min	1.5 2	0.4 typ	0.3 typ	1.5	2.5 3	40 50
	300	MJE13004		6/30	3	3	0.7	3	4	60
	400	MJE13005		6/30	3	3	0.7	3	4	60
5	60	TIP120##	TIP125##	1k min	3	1.5 typ	1.5 typ	3	4#	65
	80	TIP121##	TIP126##	1k min	3	1.5 typ	1.5 typ	3	4#	65
	100	TIP122##	TIP127##	1k min	3	1.5 typ	1.5 typ	4	4#	75

$|h_{fe}|$ @ 1 MHz, ## Darlington

(continued)

TABLE 6 — PLASTIC TO-220AB PACKAGE (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
5	250	2N6497		10/75	2.5	1.8	0.8	2.5	5	80
	300	2N6498		10/75	2.5	1.8	0.8	2.5	5	80
	400	MJE13070		8 min	3	1.5	0.5	3		80
	450	BUS46P		7 min	3	1.5	0.5	2		75
		MJE13071		8 min	3	1.5	0.5	3		80
		MJE16002		5 min	5	3	0.3	3		80
		MJE16004		7 min	5	2.7	0.35	3		80
	700	MJE8502		7.5 min	1	4	2	2.5		80
	800	MJE8503		7.5 min	1	4	2	2.5		80
6	40	TIP41	TIP42	15/75	3	0.4 typ	0.15 typ	3	3	65
	45	BD243	BD244	15 min	3				3	65
	60	BD243A	BD244A	15 min	3				3	65
		TIP41A	TIP42A	15/75	3	0.4 typ	0.15 typ	3	3	65
	80	BD243B	BD244B	15 min	3				3	65
		TIP41B	TIP42B	15/75	3	0.4 typ	0.15 typ	3	3	65
	100	BD243C	BD244C	15 min	3				3	65
		TIP41C	TIP42C	15/75	3	0.4 typ	0.15 typ	3	3	65
7	30	2N6288	2N6111	30/150	3	0.4 typ	0.15 typ	3	4	40
	45	BD795	BD796	25 min	3				3	65
	50	2N6290	2N6109	30/150	2.5	0.4 typ	0.15 typ	3	4	40
	60	BD797	BD798	25 min	3				3	65
	70	2N6292	2N6107	30/150	3	0.4 typ	0.15 typ	3	4	40
	80	BD799	BD800	15 min	3				3	65
	100	BD801	BD802	15 min	3				3	65
	150	BU407,D		30 min	1.5		0.75	5	10	60
	200	BU406,D		30 min	1.5		0.75	5	10	60
	375	BU522##		250 min	2.5				7.5	75
	425	BU522A##		250 min	2.5				7.5	75
	450	BU522B##		250 min	2.5				7.5	75
8	40	2N6386##		1k/20k	3				20#	65
	45	BDX53##	BDX54##	750 min	3				4#	60
		BD895##	BD896##	750 min	3				1#	70
		BD895A##	BD896A##	750 min	4				1#	70
	60	2N6043##	2N6040##	1k/10k	4	1.5 typ	1.5 typ	3	4#	75
		BDX53A##	BDX54A##	750 min	3				4#	60
		BD897##	BD898##	750 min	3				1#	70
		BD897A##	BD898A##	750 min	4				1#	70
		TIP100##	TIP105##	1k/20k	3	1.5 typ	1.5 typ	3	4#	80
	80	2N6044##	2N6041##	1k/10k	4	1.5 typ	1.5 typ	3	4#	75
		BDX53B##	BDX54B##	750 min	3				4#	60
		BD899##	BD900##	750 min	3				1#	70
		BD899A##	BD900A##	750 min	4				1#	70
		TIP101##	TIP106##	1k/20k	3	1.5 typ	1.5 typ	3	4#	80
	100	2N6045##	2N6042##	1k/10k	3	1.5 typ	1.5 typ	3	4#	75
		BDX53C##	BDX54C##	750 min	3				4#	60
		BD901##	BD902##	750 min	3				1#	70
		TIP102##	TIP107##	1k/20k	3	1.5 typ	1.5 typ	3	4#	80

(continued)

$|h_{fe}|$ @ 1 MHz, ## Darlington

2

TABLE 6 — PLASTIC TO-220AB PACKAGE (continued)

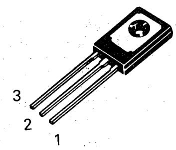
I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
8	120	BDX53D##	BDX54D##	750 min	3				4#	60
		MJE15028	MJE15029	20 min	4				30	50
	150	MJE15030	MJE15031	20 min	4				30	50
		BU807##		100 min	5	0.55 typ	0.2 typ	5		60
	200	BU806##		100 min	5	0.55 typ	0.2 typ	5		60
	300	MJE13006		5/30	5	3	0.7	5	4	80
		MJE5740##		200 min	4	8 typ	2 typ	6		80
			MJE5850	15 min	2	2	0.5	4		80
	350	MJE5741##		200 min	4	8 typ	2 typ	6		80
			MJE5851	15 min	2	2	0.5	4		80
	400	MJE5742##		200 min	4	8 typ	2 typ	6		80
		MJE13007		5/30	5	3	0.7	5	4	80
			MJE5852	15 min	2	2	0.5	4		80
		MJE16080		5 min	8	2	0.5	5		80
	450	MJE16080		5 min	8	2	0.5	5		80
10	30		D45H1	20 min	4					50
			D45H2	40 min	4					50
	40	D44E1##		1000 min	5	2 typ	0.5 typ	10		50
	45	BDX33##	BDX34##	750 min	4				3	70
		BD805	BD806	15 min	4				1.5	90
			D45H4	20 min	4					50
		D44H5	D45H5	40 min	4					50
	60	BDX33A##	BDX34A##	750 min	4				3	70
		BD807	BD808	15 min	4				1.5	90
		D44H7	D45H7	20 min	4					50
		D44H8	D45H8	40 min	4					50
			D45H9	40 min	4					50
		MJE2801T		25/100	3					75
		MJE3055T	MJE2955T	20/70	4					75
		2N6387##	2N6667##	1k/20k	5				20#	65
		SE9300	SE9400	1k min	4				1#	70
	80	BDX33B##	BDX34B##	750 min	3				3	70
		BD809	BD810	15 min	4				1.5	90
		D44E3##		1000 min	5	2 typ	0.5 typ	10		50
			D45H12	40 min	4					50
		2N6388##	2N6668##	1k/20k	5				20#	65
		D44H10	D45H10	20 min	4	0.5 typ	0.14 typ	5	50 typ	50
		D44H11	D45H11	40 min	4	0.5 typ	0.14 typ	5	50 typ	50
		SE9301	SE9401	1k min	4				1#	70
	100	BDX33C##	BDX34C##	750 min	3				3	70
		SE9302	SE9402	1k min	4				1#	70
12	300	MJE13008		6/30	8	3	0.7	8	4	100
	400	MJE13009		6/30	8	3	0.7	8	4	100
15	30	D44VH1	D45VH1	20 min	4	0.7	0.09	8	50 typ	83
	40	2N6486	2N6489	20/150	5	0.6 typ	0.3 typ	5	5	75
	45	D44VH4	D45VH4	20 min	4	0.5	0.09	8	50 typ	83
	60	2N6487	2N6490	20/150	5	0.6 typ	0.3 typ	5	5	75
		D44VH7		20 min	4	0.5	0.09	8	50 typ	83
	80	2N6488	2N6491	20/150	5	0.6 typ	0.3 typ	5	5	75
		D44VH10	D45VH10	20 min	4	0.5	0.09	8	50 typ	83

$|h_{fe}|$ @ 1 MHz, ## Darlington

2

TABLE 7 — PLASTIC TO-225AA PACKAGE (Formerly TO-126)

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE



STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

CASE 77-04
PLASTIC

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.3	250	MJE3440		40/160	0.02				15	15
	350	MJE3439		40/160	0.02				15	15
0.5	150	MJE341		25/200	0.05				15	20.8
	200	MJE344		30/300	0.05				15	20.8
	250	2N5655		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
		BD157		30/240	0.05					20
	300	BD158		30/240	0.05					20
		BD232		20 min	0.15					20
		MJE340	MJE350	30/240	0.05					20.8
		2N5656		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
	350	2N5657		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
		BD159		30/240	0.05					20
1	40	2N4921	2N4918	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
	60	2N4922	2N4919	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
	80	2N4923	2N4920	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
1.5	40	MJE720		8 min	1					20
	45	BD165	BD166	15 min	0.5				6	20
		BD135	BD136	40/250	0.15					12.5
		BD135.6	BD136.6	40/100	0.15					12.5
		BD135.10	BD136.10	63/160	0.15					12.5
		BD135.16	BD136.16	100/250	0.15					12.5
	60	BD167	BD168	15 min	0.5				6	20
		BD137	BD138	40/250	0.15					12.5
		BD137.6	BD138.6	40/100	0.15					12.5
		BD137.10	BD138.10	63/160	0.15					12.5
		BD137.16	BD138.16	100/250	0.15					12.5
	80	BD169	BD170	15 min	0.5				6	20
		BD139	BD140	40/250	0.15					12.5
		BD139.6	BD140.6	40/100	0.15					12.5
		BD139.10	BD140.10	63/160	0.15					12.5
		BD139.16	BD140.16	100/250	0.15					12.5
	300	MJE13002●		5/25	1	4	0.7	1	5	40
	400	MJE13003●		5/25	1	4	0.7	1	5	40
2	45	BD233	BD234	25 min	1				3	25
	60	BD235	BD236	25 min	1				3	25
	80	BD237	BD238	25 min	1				3	25
	100	MJE270	MJE271	1.5k min	0.12				6	15
3	30	MJE520	MJE370	25 min	1					25

● Case 77 (Style 3), # $|h_{fe}|$ @ 1 MHz, ## Darlington

(continued)

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TABLE 7 — PLASTIC TO-225AA PACKAGE (Formerly TO-126) (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
3	40	MJE180	MJE170	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	45	BD175	BD176	40/250	0.15				3	30
		BD175.6	BD176.6	40/100	0.15				3	30
		BD175.10	BD176.10	63/160	0.15				3	30
		BD175.16	BD176.16	100/250	0.15				3	30
	60	BD177	BD178	40/250	0.15				3	30
		BD177.6	BD178.6	40/100	0.15				3	30
		BD177.10	BD178.10	63/160	0.15				3	30
		BD177.16	BD178.16	100/250	0.15				3	30
		MJE181	MJE171	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	80	BD179	BD180	40/250	0.15				3	30
		BD179.6	BD180.6	40/100	0.15				3	30
		BD179.10	BD180.10	63/160	0.15				3	30
		BD179.16	BD180.16	100/250	0.15				3	30
		MJE182	MJE172	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	200	BUY49P		30 min	0.5				25	20
4	20	BD433	BD434	50 min	2				3	36
	30	BD185	BD186	15 min	2				20	40
		BD435	BD436	50 min	2				3	36
	40	2N5190	2N5193	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		MJE521	MJE371	40 min	1					40
		2N6037##	2N6034##	750/18k	2	1.7 typ	1.2 typ	2	25	40
	45	BD187	BD188	15 min	2				20	40
		BD437	BD438	40 min	2				3	36
		BD675##	BD676##	750 min	1.5					40
		BD675A##	BD676A##	750 min	2					40
		BD785	BD786	20 min	2				50	15
		BD775##	BD776##	750 min	2				20	15
	60	BD189	BD190	15 min	2				20	40
		BD439	BD440	25 min	2				3	36
		BD677##	BD678##	750 min	1.5					40
		BD677A##	BD678A##	750 min	2					40
		BD787	BD788	20 min	2				50	15
		BD777##	BD778##	750 min	2				20	15
		2N5191	2N5194	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		MJE800##	MJE700##	750 min	1.5				1#	40
		MJE801##	MJE701##	750 min	2				1#	40
		2N6038##	2N6035 ##	750/18k	2	1.7 typ	1.2 typ	2	25	40
	80	2N5192	2N5195	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		BD441	BD442	15 min	2				3	36
		BD679##	BD680##	750 min	1.5					40
		BD679A##	BD680A##	750 min	2					40
		BD789	BD790	10 min	2				40	15
		BD779##	BD780##	750 min	2				20	15
		MJE802##	MJE702##	750 min	1.5				1#	40
		MJE803##	MJE703##	750 min	2				1#	40
		2N6039##	2N6036##	750/18k	2	1.7 typ	1.2 typ	2	25	40
	100	BD681##	BD682##	750 min	1.5					40
		BD791	BD792	10 min	2				40	15
		MJE243	MJE253	40/120	0.2	0.7 typ	0.08 typ	0.2	40	15
5	25	MJE200	MJE210	45/180	2	0.13 typ	0.035 typ	2	65	15

• Case 77 (Style 3), # $|h_{fe}|$ @ 1 MHz, ## Darlington

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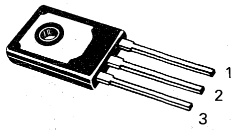
TABLE 8 — PLASTIC TO-225AB (Formerly TO-127)

STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE



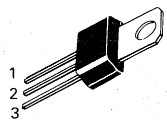
CASE 90-05
PLASTIC

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
5	50		MJE105	25/100	2					65
	60	MJE1100## MJE1101##	MJE1090##	750 min 750 min	3A 4A				1 1	70 70
	80	MJE1102## MJE1103##	MJE1092## MJE1093##	750 min 750 min	3A 4A				1 1	70 70
8	60	MJE6043##	MJE6040##	1k/20k	4	1.5 typ	1.5 typ	4	4#	75
	80	MJE6044##	MJE6041##	1k/20k	4	1.5 typ	1.5 typ	4	4#	75
	100	MJE6045##		1k/20k	4	1.5 typ	1.5 typ	4	4#	75
10	45		BD206	15 min	4				1.5	90
	60	BD207 MJE2801 MJE3055	BD208 MJE2901 MJE2955	15 min 25/100 20/70	4 3 4				1.5 2	90 90 90
12	40	2N5989	2N5986	20/120	6	0.5 typ	0.25 typ	6	2	100
	60		2N5987	20/120	6	0.5 typ	0.25 typ	6	2	100
	80	2N5991	2N5988	20/120	6	0.5 typ	0.25 typ	6	2	100
15	40	MJE1660		20/100	5				3	90
	60	MJE1661		20/100	5				3	90

$|h_{fe}|$ @ 1 MHz, ## Darlington

TABLE 9 — PLASTIC CASE 152

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)



I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
0.5	300	MPS-U10	MPS-U60	30 min	0.03				60	10
0.8	40	MPS-U02	MPS-U52	30 min	0.5				150	10
1	120	MPS-U03		40 min	0.01				100	10
	180	MPS-U04		40 min	0.01				100	10
2	20	BD505	BD506	40 min	1				50	10
	30	BD507 MPS-U01	BD508 MPS-U51	40 min 50 min	1 1				50 50	10 10
	40	BD509 MPS-U01A MPS-U45##	BD510 MPS-U51A MPS-U95##	40 min 50 min 4k min	1 1 1				50 50 100	10 10 10

(continued)

Darlington

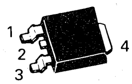
TABLE 9 — PLASTIC CASE 152 (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
2	45	BD515	BD516	25 min	0.5				50	10
	60	BD517 MPS-U05	BD518 MPS-U55	25 min 60 min	0.5 0.25				50 50	10 10
	80	BD519 MPS-U06	BD520 MPS-U56	25 min 60 min	0.5 0.25				50 50	10 10
	100	BD529 MPS-U07	BD530 MPS-U57	30 min 30 min	0.25 0.25				50 50	10 10

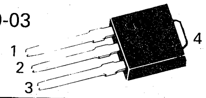
Darlington

TABLE 10 — DPAK — SURFACE MOUNT POWER PACKAGE

CASE 369A-04



CASE 369-03



STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type* NPN	PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Typ	t_f µs Typ	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.5	300	MJD340	MJD350	30/240	0.05					15
1	40	MJD29	MJD30	15/75	1	0.6	0.3	1	3	15
	100	MJD29C	MJD30C	15/75	1	0.6	0.3	1	3	15
	250	MJD47		30/150	0.3	2	0.2	0.3	10	15
	400	MJD50		30/150	0.3	2	0.2	0.3	10	20
1.5	400	MJD13003		5/25	1	4 max	0.7 max	1	4	15
2	100	MJD112##	MJD117##	500 min	2	1.7	1.3	2	25#	20
3	40	MJD31	MJD32	25 min	1	0.6	0.3	1	3	15
	100	MJD31C	MJD32C	25 min	1	0.6	0.3	1	3	15
4	80	MJD6039##	MJD6036##	1k/12k	2	1.7	1.2	2	25	20
5	25	MJD200	MJD210	45/180	2	0.15	0.04	2	65	12.5
6	100	MJD41C	MJD42C	15/75	3	0.4	0.15	3	3	20
8	80	MJD44H11	MJD45H11	40 min	4	0.5	0.14	5	50 typ	20
	100	MJD122##	MJD127##	1k/12k	4	1.5	2	4	4#	20
10	60	MJD3055	MJD2955	20/100	4	1.5	1.5	3	2	20
	80	MJD44E3##		1k min	5	2	0.5	10		20

Darlington
* Case 369-03 may be ordered by adding -1 suffix to part number.

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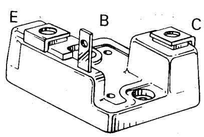
TABLE 11 — PLASTIC MO-040AA†

CASE 353-01



I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	PNP	h_{FE} Min/Max	@ I_C Amp	t_s µs Max	t_f µs Max	@ I_C Amp	P_D (Case) Watts @ 25°C
50	450	MJ10044##		50 min	50	3.8	1.3	50	250
100	250	MJ10047## MJ10048##		75 min 75 min	100 100	4 20	1 8	100 100	250 250

Darlington † Not recommended for new designs — consult Motorola.

Selection By Major Product Categories

TABLE 12 — MILITARY SPECIFIED POWER TRANSISTORS

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN/#	Device Type PNP/#	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
1	300	2N3739J,/402A TX, TXV		40/200	0.1	3.5*		0.5	10	20	TO-213AA/80
3	40		2N3867J,/350A TX, TXV	40/200	1.5	0.5	0.1	1.5	60	10	TO-205AA/31
			2N3867SJ,350A TX, TXV	40/200	1.5	0.5	0.1	1.5	60	10	TO-205AD/79
	60		2N3868J,/350A TX, TXV	30/150	1.5	0.5	0.1	1.5	60	10	TO-205AA/31
			2N3868SJ,/350A TX, TXV	30/150	1.5	0.055	0.035	1.5	60	5	TO-205AD/79
4	60		2N3740J,/441A TX, TXV	30/100	0.25	1*		1	5	25	TO-213AA/80
		2N3766J,/518 TX, TXV		40/160	0.5	2.5*		0.5	10	25	TO-213AA/80
	80		2N3741J,/441A TX, TXV	30/100	0.25	1*		1	5	25	TO-213AA/80
		2N3767J,/518 TX, TXV		40/160	0.5	2.5*		0.5	10	25	TO-213AA/80
5	100	2N5339J/560 TX, TXV	2N6193J/561 TX, TXV	60/240	2	2	0.2	2	30	6	TO-205AD/79
8	60	2N6300J,/540** TX, TXV	2N6298J,/540** TX, TXV	750/18k	4	8*		4	25	75	TO-213AA/80
	80	2N6301J,/540** TX, TXV	2N6299J,/540** TX, TXV	750/18k	4	8*		4	25	75	TO-213AA/80
	250	2N6306J,/498		15/75	3	3*		3	5	125	TO-204/1
	350	2N6308J,/498		12/60	3	3*		3	5	125	TO-204/1
10	40	2N6383J,/523** TX, TXV	2N6648J,527 TX, TXV	1k/20k	5	10*		5	20	100	TO-204/1
			2N6648J,/527** TX, TXV	1k/20k	5	10*		5	50	85	TO-204/1
	60	2N3715J,/408B TX, TXV	2N3791J,/379B TX, TXV	30/120	3	2*		5	4	150	TO-204/1
		2N6384J,/523** TX, TXV		1k/20k	5	10*		5	20	100	TO-204/1
			2N6649J,/527 TX, TXV	1k/20k	5	10*		5	50	85	TO-204/1
	80	2N3716J,/408B TX, TXV	2N3792J,/379B TX, TXV	30/120	3	2*		5	4	150	TO-204/1
		2N6385J,/523** TX, TXV		1k/20k	5	10*		5	20	100	TO-204/1
			2N6650J,/527** TX, TXV	1k/20k	5	10*		5	50	85	TO-204/1
12	80	2N6058J,/502** TX, TXV	2N6051J,/501** TX, TXV	1k/18k	6	10*		5	10	150	TO-204/1
	100	2N6059J,/502** TX, TXV	2N6052J,/501** TX, TXV	1k/18k	6	10*		5	10	150	TO-204/1
15	300	2N6546J,/525 TX		12/60	5	4.7*		10	6	175	TO-204/1

MIL-S-19500 Detailed Spec. shown by Device Type

* t_{off}

** Consult Factory for qualification status.

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TABLE 12 — MILITARY SPECIFIED POWER TRANSISTORS (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN/#	PNP/#	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
15	400	2N6547J,/525 TX		12/60	5	4.7*		10	6	175	TO-204/1
20	75	2N5039J,/439 TX, TXV**		30/150	2	2*		10	60	140	TO-204/1
	80	2N5303J,/456A TX, TXV	2N5745J,/433 TX, TXV	15/60	10	3*		10	2	200	TO-204/1
		2N6283J,/504** TX, TXV	2N6286J,/505** TX, TXV	1250/18k	10	10*		10	8	175	TO-204/1
	90	2N5038J/439 TX, TXV**		50/200	2	2*		12	60	140	TO-204/1
	100	2N6284J,/504** TX, TXV	2N6287J,/505 TX, TXV	1250/18k	10	10*		10	8	175	TO-204/1
25	100	2N6338J,/509 TX, TXV**		30/120	10	1		10	40	200	TO-204/1
			2N6437J,/508 TX, TXV**	30/120	10	1		10	40	200	TO-204/1
	120		2N6438J,/509 TX, TXV**	30/120	10	1		10	40	200	TO-204/1
	150	2N6341J,/509 TX, TXV**		30/120	1	1		10	40	200	TO-204/1
30	60	2N5302J,/456A TX, TXV	2N4399J,/433 TX, TXV	15/60	15	3*		10	2	200	TO-204/1
50	60	2N5685J,/464 TX, TXV	2N5683J,/466 TX, TXV	15/60	25	3*		25	2	300	TO-204/197 MOD
	80	2N5686J,/464 TX, TXV	2N5684J,/466 TX, TXV	15/60	25	3*		25	2	300	TO-204/197 MOD
	100	2N6274J,/514 TX, TXV**	2N6378J,/515 TX, TXV**	30/120	20	1.05*		20	30	250	TO-204/197 MOD
	120		2N6379J,/515 TX, TXV**	30/120	20	1.05*		20	30	250	TO-204/197 MOD
	150	2N6277J,/514 TX, TXV**		30/120	20	1.05*		20	30	250	TO-204/197

MIL-S-19500 Detailed Spec. shown by Device Type

* t_{off}

** Consult Factory for qualification status.

TABLE 13 — POWER DARLINGTONS

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	$\|h_{fe}\|$ @ 1 MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
2	40	MPS-U45	MPS-U95	4k min	1				100	10	/152
	60	TIP110	TIP115	1k min	1	2 typ	1 typ	1	25	50	TO-220/221A
	80	TIP111	TIP116	1k min	1	2 typ	1 typ	1	25	50	TO-220/221A
	100	TIP112 MJE270	TIP117 MJE271	1k min 1.5k min	1 0.12	2 typ	1 typ	1	25 6	50 25	TO-220/221A TO-225AA/77

(continued)

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TABLE 13 — POWER DARLINGTONS (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	$\|h_{fe}\|$ @ 1 MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
4	40	MJE3300	MJE3310	1k min	1				20	15	TO-225AA/77R
		2N6037	2N6034	750/1k	2	1.7 typ	1.2 typ	2	25	40	TO-225AA/77
	45	BD675	BD676	750 min	1.5					40	TO-225AA/77
		BD675A	BD676A	750 min	2					40	TO-225AA/77
		BD775	BD776	750 min	2				20	15	TO-225AA/77
	60	BD677	BD678	750 min	1.5					15	TO-225AA/77
		BD677A	BD678A	750 min	2					40	TO-225AA/77
		BD777	BD778	750 min	2				20	40	TO-225AA/77
		MJE3301		1k min	1				20	15	TO-225AA/77R
		MJE800	MJE700	750 min	1.5				1	40	TO-225AA/77
		MJE800T	MJE700T	750 min	1.5				1	40	TO-220/221A
		MJE801	MJE701	750 min	2				1	40	TO-225AA/77
		2N6038	2N6035	750/18k	2	1.7 typ	1.2 typ	2	25	40	TO-225AA/77
		2N6294	2N6296	750/18k	2	0.9 typ	0.7 typ	2	4	50	TO-213AA/80
	80	BD679	BD680	750 min	1.5					40	TO-225AA/77
		BD679A	BD680A	750 min	2					40	TO-225AA/77
		BD779	BD780	750 min	2				20	15	TO-225AA/77
		MJE802	MJE702	750 min	1.5					40	TO-225AA/77
		MJE803	MJE703	750 min	2					40	TO-225AA/77
		2N6039	2N6036	750/18k	2	1.7 typ	1.2 typ	2	25	40	TO-225AA/77
		2N6295	2N6297	750/18k	2	0.9 typ	0.7 typ	2	4	50	TO-213AA/80
	100	BD681	BD682	750 min	1.5					40	TO-225AA/77
5	60	MJE1100	MJE1090	750 min	3A				1	70	TO-225AB/90
		MJE1101	MJE1091	750 min	4A				1	70	TO-225AB/90
		TIP120	TIP125	1k min	3	1.5 typ	1.5 typ	3	4	65	TO-220/221A
	80	MJE1102	MJE1092	750 min	3A				1	70	TO-225AB/90
		MJE1103	MJE1102	750 min	4A				1	70	TO-225AB/90
		TIP121	TIP126	1k min	3	1.5 typ	1.5 typ	3	4	65	TO-220/221A
	100	TIP122	TIP127	1k min	3	1.5 typ	1.5 typ	3	4	65	TO-220/221A
7	300	MJ3041		250 min	2.5					100	TO-204/1
	350	MJ3042		250 min	2.5					100	TO-204/1
	375	BU522		250 min	2.5				7.5	75	TO-220/221A
	425	BU522A		250 min	2.5				7.5	75	TO-220/221A
	450	BU522B		250 min	2.5				7.5	75	TO-220/221A
8	40	2N6386		1k/20k	3				20	65	TO-220/221A
	45	BDX53	BDX54	750 min	3				4	60	TO-220/221A
		BD895	BD896	750 min	3				1	70	TO-220/221A
		BD895A	BD896A	750 min	4				1	70	TO-220/221A
	60	BDX53A	BDX54A	750 min	3				4	60	TO-220/221A
		BD897	BD898	750 min	3				1	70	TO-220/221A
		BD897A	BD898A	750 min	4				1	70	TO-220/221A
		MJ1000	MJ900	1k min	3					90	TO-204/11
		TIP100	TIP105	1k/20k	3	1.5 typ	1.5 typ	3	4	80	TO-220/221A
		2N6043	2N6040	1k/10k	4	1.5 typ	1.5 typ	3	4	75	TO-220/221A
		2N6300	2N6298	750k/18k	4	1.5 typ	1.5 typ	4	4	75	TO-213AA/80
		2N6055	2N6053	750k/18k	4	1.5 typ	1.5 typ	4	4	100	TO-204/11
		MJE6043	MJE6040	1k/20k	4	1.5 typ	1.5 typ	4	2	75	TO-225AB/90
	80	BDX53B	BDX54B	750 min	3				4	60	TO-220/221A
		BD899	BD900	750 min	3				1	70	TO-220/221A
		BD899A	BD900A	750 min	4				1	70	TO-220/221A
		MJ1001	MJ901	1k min	3					90	TO-204/11
		TIP101	TIP106	1k/20k	3	1.5 typ	1.5 typ	3	4	80	TO-220/221A

(continued)

TABLE 13 — POWER DARLINGTONS (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	t_f μs Max	@ I_C Amp	$\|h_{fe}\|$ @ 1 MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
8		2N6044	2N6041	1k/10k	4	1.5 typ	1.5 typ	3	4	75	TO-220/221A
		2N6301	2N6299	750k/18k	4	1.5 typ	1.5 typ	4	4	75	TO-213A/80
		2N6056	2N6054	750k/18k	4	1.5 typ	1.5 typ	4	4	100	TO-204A/11
		MJE6044	MJE6041	1k/20k	4	1.5 typ	1.5 typ	4	2	75	TO-225AB/90
	100	BDX53C	BDX54C	750 min	3				4	60	TO-220/221A
		BD901	BD902	750 min	3				1	70	TO-220/221A
		MJE6045		1k/20k	4	1.5 typ	1.5 typ	4	2	75	TO-225AB/90
		TIP102	TIP107	1k/20k	3	1.5 typ	1.5 typ	3	4	80	TO-220/221A
		2N6045	2N6042	1k/10k	4	1.5 typ	1.5 typ	3	4	75	TO-220/221A
	120	BDX53D	BDX54D	750 min	3				4	60	TO-220/221A
	150	BU807•		100 min	5	0.55 typ	0.2 typ	5		60	TO-220/221A
	200	BU806•		100 min	5	0.55 typ	0.2 typ	5		60	TO-220/221A
	300	MJE5740		200/400	4	8 typ	2 typ	6		80	TO-220/221A
	350	MJE5741		200/400	4	8 typ	2 typ	6		80	TO-220/221A
	400	MJE5742		200/400	4	8 typ	2 typ	6		80	TO-220/221A
	500	BUT50P•		30 min	2	0.75 typ	0.1 typ	5		100	TO-218/340
	1400*	MJ10011		20 min	4			1	4	80	TO-204/1
10	40	2N6383	2N6648	1k/20k	5				20	100	TO-204/11
		D44E1		1000 min	5	2 typ	0.5 typ	10		50	TO-220/221A
	45	BDX33	BDX34	750 min	4				3	70	TO-220/221A
	60	BDV65	BDV64	1k min	5					125	TO-218/340
		BDX33A	BDX34A	750 min	4				3	70	TO-220/221A
		MJ3000	MJ2500	1k min	5					150	TO-204/1
		2N6387	2N6667	1k/20k	5				20	65	TO-220/221A
		2N6384		1k/20k	5				20	100	TO-204/11
		D44E2		1000 min	5	2 typ	0.5 typ	10		50	TO-220/221A
		TIP140	TIP145	500 min	10	2.5 typ	2.5 typ	5	4	125	TO-218/340
	80	2N6388	2N6668	1k/20k	5				20	65	TO-220/221A
		2N6385		1k/20k	5				20	100	TO-204/11
		BDV65A	BDV64A	1k min	5					125	TO-218/340
		BDX33B	BDX34B	750 min	3				3	70	TO-220/221A
		D44E3		1000 min	5	2 typ	0.5 typ	10		50	TO-220/221A
		TIP141	TIP146	500 min	10	2.5 typ	2.5 typ	5	4	125	TO-218/340
	100	BDV65B	BDV64B	1k min	5					125	TO-218/340
		BDX33C	BDX34C	750 min	3				3	70	TO-220/221A
		TIP142	TIP147	500 min	10	2.5 typ	2.5 typ	5	4	125	TO-218/340
	120	BDV65C	BDV64C	1k min	5					125	TO-218/340
		BDX33D	BDX34D	750 min	3				3	70	TO-220/221A
	200	BU323P		150 min	6	15	15	6		125	TO-218/340
	250	BU323AP		150 min	6	15	15	6		125	TO-218/340
	350	BU323		150 min	6	7.5 typ	5.2 typ	6		175	TO-204/1
		MJ10002		30/300	5	2.5	1	5	10	150	TO-204/1
		MJ10006•		30/300	5	1.5	0.5	5	10	150	TO-204/1
	400	BU323A		150 min	6	7.5 typ	5.2 typ	6		175	TO-204/1
		MJH10012		100/2k	6	15	15	6		118	TO-218/340
		MJ10007•		30/300	5	1.5	0.5	5	10	150	TO-204/1
		MJ10012		100/2k	6	15	15	6		175	TO-204/1
	600	MJ10014•		10/250	10	2.5	0.8	10		175	TO-204/1

• Darlington with speed-up diode.

(continued)

TABLE 13 — POWER DARLINGTONS (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	$\lvert h_{fe} \rvert$ @ 1 MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
12	60	2N6057	2N6050	750/18k	6	1.6 typ	1.5 typ	6	4	150	TO-204/1
	80	2N6058	2N6051	750/18k	6	1.6 typ	1.5 typ	6	4	150	TO-204/1
	100	2N6059	2N6052	750/18k	6	1.6 typ	1.5 typ	6		150	TO-204/11
	1000	BUT16•		5 min	8	3.3	1.5	8		150	TO-204/1
15	60	2N6576		2k/20k	4	2	7	10	10/200	120	TO-204/11
	90	2N6577		2k/20k	4	2	7	10	10/200	120	TO-204/11
	120	2N6578		2k/20k	4	2	7	10	10/200	120	TO-204/11
	150	MJ11018 MJH11018	MJ11017 MJH11017	100 min 100 min	15 15				3 3	175 150	TO-204/1 TO-218/340
	200	MJ11020 MJH11020	MJ11019 MJH11019	100 min 100 min	15 15				3 3	175 150	TO-204/1 TO-218/340
	250	MJ11022 MJH11022	MJ11021 MJH11021	100 min 100 min	15 15				3 3	175 150	TO-204/1 TO-218/340
	500	BUT51P		40 min	5	1.1	0.16	10		125	TO-218/340
16	60	MJ4033	MJ4030	1k min	10					150	TO-204/1
	80	MJ4034	MJ4031	1k min	10					150	TO-204/1
	100	MJ4035	MJ4032	1k min	10					150	TO-204/1
20	60	2N6282 MJH6282	2N6285 MJH6285	750/18k 750/18k	10 10	2.5 typ 2.5 typ	2.5 typ 2.5 typ	10 10	4 4	160 125	TO-204/1 TO-218/340
	80	2N6283 MJH6283	2N6286 MJH6286	750/18k 750/18k	10 10	2.5 typ 2.5 typ	2.5 typ 2.5 typ	10 10	4 4	160 125	TO-204/1 TO-218/340
	100	2N6284 MJH6284	2N6287 MJH6287	750/18k 750/18k	10 10	2.5 typ 2.5 typ	2.5 typ 2.5 typ	10 10	4 4	160 125	TO-204/1 TO-218/340
	350	MJ10000 MJ10004•		40/400 40/400	10 10	3 1.5	1.8 0.5	10	10 10	175 175	TO-204/1 TO-204/1
	400	MJ10001 MJ10005•		40/400 40/400	10 10	3 1.5	1.8 0.5	10	10 10	175 175	TO-204/1 TO-204/1
	450	MJ10008•		30/300	10	2	0.6	10	8	175	TO-204/1
	500	MJ10009•		30/300	10	2	0.6	10	8	175	TO-204/1
	700	BUT15•		15 min	12	2.5	0.8	12		175	TO-204/1
	750	MJ10024•		50/600	5	5	1.8	10		250	TO-204/1
	850	MJ10025•		50/600	5	5	1.8	10		250	TO-204/1
24	1000	BUT36•		5 min	16	6	2.5	16		250	TO-204 Mod/197
25	500	BUT14•		15 min	16	2.8	0.8	16		175	TO-204/1
28	400	BUT13•		20 min	20	2.6	0.8	18		175	TO-204/1
30	60	MJ11012	MJ11011	1k min	20				4	200	TO-204/1
	90	MJ11014	MJ11013	1k min	20				4	200	TO-204/1
	120	MJ11016	MJ11015	1k min	20				4	200	TO-204/1
40	350	MJ10022•		50/600	10	2.5	0.9	20		250	TO-204 Mod/197
	400	MJ10023•		50/600	10	2.5	0.9	20		250	TO-204 Mod/197
	700	BUT35•		15 min	24	4	1.2	24		250	TO-204 Mod/197
50	60	MJ11028	MJ11029	400 min	50					300	TO-204 Mod/197

• Darlington with speed-up diode.

(continued)

TABLE 13 — POWER DARLINGTONS (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	$\lvert h_{fe} \rvert$ @ 1 MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
50	90	MJ11030	MJ11031	400 min	50					300	TO-204 Mod/197
	120	MJ11032	MJ11033	400 min	50					300	TO-204 Mod/197
	400	MJ10015●		10 min	40	2.5	0.5	20	10	250	TO-204 Mod/197
	450	MJ10044●		50 min	50	3.8	1.3	50		250	— /353
	500	BUT34● MJ10016●		15 min 10 min	32 40	3 2.5	1.5 0.5	32 20	 10	250 250	TO-204 Mod/197 TO-204 Mod/197
56	400	BUT33●		20 min	36	3.3	1.6	36		250	TO-204 Mod/197
60	200	MJ10020●		75/1k min	15	3.5	0.5	30		250	TO-204 Mod/197
	250	MJ10021●		75/1k min	15	3.5	0.5	30		250	TO-204 Mod/197
100	250	MJ10047● MJ10048●		75 min 75 min	100 100	4 20	1 8	100 100		250 250	— /353 — /353

● Darlington with speed-up diode.

TABLE 14 — POWER SWITCHING TRANSISTORS

V_{CEO} < 200 V

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
0.8	40	MPS-U02	MPS-U52	30 min	0.5				150	10	—/152
1	120	MPS-U03		40 min	0.1				100	10	—/152
	180	MPS-U04		40 min	0.1				100	10	—/152
2	20	BD505	BD506	40 min	1				50	10	—/152
	30	BD507 MPS-U01	BD508 MPS-U51	40 min 50 min	1 1				50 50	10 10	—/152 —/152
	40	BD509 MPS-U01A MPS-U45#	BD510 MPS-U51A MPS-U95#	40 min 50 min 4k min	1 1 1				50 50 100	10 10 10	—/152 —/152 —/152
	45	BD515	BD516	25 min	0.5				50	10	—/152
	60	BD517 MPS-U05	BD518 MPS-U55	25 min 60 min	0.5 0.25				50 50	10 10	—/152 —/152
	80	BD519 MPS-U06	BD520 MPS-U56	25 min 60 min	0.5 0.25				50 50	10 10	—/152 —/152
	100	BD529 MPS-U07	BD530 MPS-U57	30 min 60 min	0.25 0.25				50 50	10 10	—/152 —/152
	150	2N5051		25/100	0.75	3.5	1.2	0.75	10	40	TO-213AA/80
3	40		2N3719 2N3867	25/180 40/200	2 2	0.4* 0.4*		1 1	60 60	6 6	TO-205AA/31 TO-205AA/31
	60		2N3720 2N3868	25/180 30/150	2 2	0.4* 0.4*		1 1	60 60	6 6	TO-205AA/31 TO-205AA/31
	80		2N6303	30/150	2	0.4*		1	60	6	TO-205AA/31

Darlington

* t_{off} @ 1 MHz

(continued)

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TABLE 14 — POWER SWITCHING TRANSISTORS (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
4	30	BD185	BD186	15 min	2				20	40	TO-225AA/77
	45	BD187	BD188	15 min	2				20	40	TO-225AA/77
		BD785	BD786	20 min	2				50	15	TO-225AA/77
	60	2N4877		20/100	4	1.5	0.5	4	30	10	TO-205AD/79
		BD189	BD190	15 min	2				20	40	TO-225AA/77
		BD787	BD788	20 min	2				50	15	TO-225AA/77
	80	BD789	BD790	10 min	2				40	15	TO-225AA/77
	100	BD791	BD792	10 min	2				40	15	TO-225AA/77
5	60		MJ8100	25/180	2	1	0.15	2	30	10	TO-205AD/79
	80	2N5337	2N6191	60/240	2	2	0.2	2	30	10	TO-205AD/79
	100	2N5339	2N6193	60/240	2	2	0.2	2	30	10	TO-205AD/79
7	60	2N6315	2N6317	20/100	2.5	1	0.8	2.5	4	90	TO-213AA/80
	80	2N5428		60/240	2	2	0.2	2	30	60	TO-213AA/80
		2N5347	2N6187	60/240	2	2	0.2	2	30	60	TO-210AA/160
		2N6316	2N6318	20/100	2.5	1	0.8	2.5	4	90	TO-213AA/80
	100	2N5430		60/240	2	2	0.2	2	30	60	TO-213AA/80
		2N5349	2N6189	60/240	2	2	0.2	2	30	60	TO-210AA/160
7.5	60	2N3447		40/120	5	2	0.35	5	10	115	TO-204/11
	80	2N3448		40/120	5	2	0.35	5	10	115	TO-204/11
8	120	MJ3247	MJ3237	40 min	3	0.4 typ	0.18 typ	5	20	75	TO-213AA/80
		MJ4247	MJ4237	40 min	3	0.4 typ	0.18 typ	5	20	90	TO-204/11
		MJE15028	MJE15029	20 min	4	0.4 typ	0.18 typ	5	30	50	TO-220/221A
	150	MJ3248	MJ3238	40 min	3	0.4 typ	0.18 typ	5	20	75	TO-213AA/80
		MJ4248	MJ4238	40 min	3	0.4 typ	0.18 typ	5	20	90	TO-204/11
		MJE15030	MJE15031	20 min	4	0.4 typ	0.18 typ	5	30	50	TO-220/221A
10	60		MJ6700	25/180	2	1	0.15	2	30	60	TO-210AA/160
		2N5877	2N5875	20/100	4	1	0.8	4	4	150	TO-204/11
	80	2N5878	2N5876	20/100	4	1	0.8	4	4	150	TO-204/11
15	60	2N5881	2N5879	20/100	6	1	0.8	6	4	160	TO-204/11
	80	2N5882	2N5880	20/100	6	1	0.8	6	4	160	TO-204/11
18	160	BUX41N		8 min	12	1.2	0.25	12	8	120	TO-204/1
20	75	2N5039		20/100	10	1.5	0.5	10	60	140	TO-204/1
	80	2N5303	2N5745	15/60	10	2	1	10	2	200	TO-204/11
	90	2N5038		20/100	12	1.5	0.5	12	60	140	TO-204/1
	125	BUX40		8 min	15	1	0.25	15	8	120	TO-204/1
	160	BUV11N		10 min	15	1.2	0.25	15	8	150	TO-204/1
25	60	2N5885	2N5883	20/100	10	1	0.8	10	4	200	TO-204/11
	80	2N5886	2N5884	20/100	10	1	0.8	10	4	200	TO-204/11
			2N6436	30/120	10	1	0.25	10	40	200	TO-204/1
	100	2N6338		30/120	10	1	0.25	10	40	200	TO-204/1
			2N6437	30/120	10	1	0.25	10	40	200	TO-204/1
	120	2N6339		30/120	10	1	0.25	10	40	200	TO-204/1
			2N6438	30/120	10	1	0.25	10	40	200	TO-204/1
	125	BUV10		10 min	20	1.2	0.25	20	8	150	TO-204/1
		BUV10N		10 min	20	1.55	0.45	15	10	175	TO-204/1

(continued)

TABLE 14 — POWER SWITCHING TRANSISTORS (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
25	140	2N6340		30/120	10	1	0.25	10	40	200	TO-204/1
	150	2N6341		30/120	10	1	0.25	10	40	200	TO-204/1
30	40	2N5301	2N4398	15/60	15	2	1	10	2	200	TO-204/11
	60	2N5302	2N4399	15/60	15	2	1	10	2	200	TO-204/11
	90	BUX39		8 min	20	1	0.25	20	8	120	TO-204/1
40	160	BUV21N		10 min	40	1	0.2	40	8	250	TO-204 Mod/197
50	80		2N6377	30/120	20	0.8					TO-204 Mod/197
	100	2N6274	2N6378	30/120	20	0.8	0.25	20	30	250	TO-204 Mod/197
	120	2N6275	2N6379	30/120	20	0.8	0.25	20	30	250	TO-204 Mod/197
	125	BUV20		10 min	50	1.2	0.25	50	8	250	TO-204 Mod/197
	140	2N6276		30/120	20	0.8	0.25	20	30	250	TO-204 Mod/197
	150	2N6277		30/120	20	0.8	0.25	20	30	250	TO-204 Mod/197
70	125	BUS50		15 min	50					350	TO-204 Mod/197

TABLE 15 — SWITCHMODE POWER TRANSISTORS

$V_{CEO} \geq 200$ V

Devices are listed in descending order of $V_{CEO(sus)}$, and I_CCont

$V_{CEO(sus)}$ Volts Min	I_CCont Amps Max	V_{CEV} Volts Min	Device Type NPN unless otherwise noted	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
1000	24	1400	BUT36##	5 min	16	6	2.5	16		250	TO-204 Mod/197
	12	1400	BUT16##	5 min	8	3.3	1.5	8		150	TO-204/1
900	2	1800	MJE1320	3 min	1	4 typ	0.8 typ	1		80	TO-220/221A
850	20	1200	MJ10025##★	50/600	20	5	1.8	10			TO-204/1
	3	1500 1500	MJE16034 MJH16034	4 min 4 min	3 3	2 2	1.5 1.5	2 2		80 125	TO-220/221A TO-218/340
800	10	1400 1500 1500	MJ8505★ MJ16018★ MJH16018★	7.5 min 4 min 4 min	1.5 5 5	4 4.5 typ 4.5 typ	2 0.2 typ 0.2 typ	5 5 5			TO-204/1 TO-204/1 TO-218/340
	5	1400 1400	MJ8503★ MJE8503★	7.5 min 7.5 min	1 1	4 4	2 2	2.5 2.5			TO-204/1 TO-220/221A
	2.5	1400 1400	MJ8501★ MJE8501★	7.5 min 7.5 min	0.5 0.5	4 4	2 2	1 1			TO-204/1 TO-220/221A
750	20	1000	MJ10024##★	50/600	20	5	1.8	10			TO-204/1
	8	1500 1500	MJ12005 MJH12005	5 min	5		1 0.4 typ	5 5	4 typ 4	 100	TO-204/1 TO-218/340
	5	1500	MJ12004★	2.5 min	4.5		1	4.5	4 typ		TO-204/1
	4	1500	MJ12003	2.5 min	3		1	3	4 typ		TO-204/1

★ Designers Data Sheet characterization
Darlington ## Darlington with speed-up diode * t_{off} ** $|h_{fe}|$ @ 1 MHz

(continued)

TABLE 15 — SWITCHMODE POWER TRANSISTORS (continued)

$V_{CEO(sus)}$ Volts Min	I_C Cont Amps Max	V_{CEV} Volts Min	Device Type NPN unless otherwise noted	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	t_f μs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
750	3	1500	MJE16032	4 min	3	2	1.5	2		80	TO-220/221A
		1500	MJH16032	4 min	3	2	1.5	2		125	TO-218/340
	2.5	1500	MJ12002★	1.11 min	2		1	2	4 typ		TO-204/1
		1500	MJE12007★	1.1 min	2		1	2	4 typ		TO-220/221A
700	40	1000	BUT35##	15 min	24	4	1.2	24		250	TO-204 Mod/197
	20	1000	BUT15##	15 min	12	2.5	0.8	12		175	TO-204/1
	10	1200	MJ8504★	7.5 min	1.5	4	2	5			TO-204/1
	8	1400	MJ10011#	20 min	4		1	4			TO-204/1
		1500	BU508,A	2.25 min	4.5	8 typ	0.5 typ	4.5	7	125	TO-218/340
		1500	BU508D,AD	2.25 min	4.5	8 typ	0.5 typ	4.5	7	125	TO-218/340
	5	1200	MJ8502★	7.5 min	1	4	2	2.5			TO-204/1
		1200	MJE8502★	7.5 min	1	4	2	2.5			TO-220/221A
		1500	BU208A	2.25 min	4.5	8 typ	0.4 typ	4.5	4 typ	90	TO-204/1
		1500	BU208D	2.25 min	4.5		0.6 typ	4.5			TO-204/1
	2.5	1200	MJE8500★	7.5 min	0.5	4	2	1			TO-220/221A
600	15	700	MJ10014##★	10/250	10	2.5	0.8	10			TO-204/1
550		650	MJ10013##★	10/250	10	2.5	0.8	10			TO-204/1
500	50	750	MJ10016##★	10 min	40	2.5	1	20			TO-204 Mod/197
		850	BUT34##	15 min	32	3	1.5	32		250	TO-204 Mod/197
	25	850	BUT14##	15 min	16	2.8	0.8	16		175	TO-204/1
	20	600	MJ10009##★	30/300	10	2	0.6	10	8**		TO-204/1
		800	MJ13335★	10/60	5	4	0.7	10			TO-204/1
	15	850	BUT51P##	40 min	5	1.1	0.16	10		125	TO-218/340
		1000	MJ16010A★	5 min	15	3	0.4	10			TO-204/1
		1000	MJH16010A★	5 min	15	3	0.4	10			TO-218/340
	8	850	BUT50P##	30 min	2	0.75 typ	0.1 typ	5		100	TO-218/340
		1000	MJ16006A★	5 min	15	3	0.4	10			TO-204/1
		1000	MJH16006A★	5 min	15	3	0.4	10			TO-218/340
	5	1000	MJ16002A★	5 min	15	3	0.3	3			TO-204/1
		1000	MJH16002A★	5 min	15	3	0.3	3			TO-218/340
450	50	500	MJ10044##★	50 min	50	3.8	1.3	50			—/353
	30	850	MJ16020	5 min	30	1.8	0.2	20		250	TO-204/1
		850	MJ16022	7 min	30	1.5	0.15	20		250	TO-204/1
		1000	BUS98A	8 min	16	2.3	0.4	16		250	TO-204 Mod/197
	20	650	MJ10008##★	30/300	10	2	0.6	10	8**		TO-204/1
		850	2N6837★	10/30	15	2.5	0.25	15	15		TO-204/1
		850	MJ16014★	5 min	20	2.7	0.35	20			TO-204/197
		850	MJ16016★	7 min	20	2.2	0.25	20			TO-204/197
	15	750	MJ13091★	8 min	10	2.5	0.5	10			TO-204/1
		850	2N6836★	10/30	10	3	0.35	10	10		TO-204/1
		850	MJ12022★	5 min	15		0.1 typ	10			TO-204/1
		850	MJ16010★	5 min	15	1.2 typ	0.2 typ	10			TO-204/1
		850	MJ16012★	7 min	15	0.9 typ	0.15 typ	10			TO-204/1
		850	MJH16010★	5 min	15	1.2	0.2	10		175	TO-218/340
		850	MJH16012★	7 min	15	0.9	0.15	10		150	TO-218/340
		1000	BUS48A	8 min	10	2	0.4	10		175	TO-204/1

(continued)

★ Designers Data Sheet characterization
Darlington   ## Darlington with speed-up diode   * t_{off} ** $|h_{fe}|$ @ 1 MHz

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TABLE 15 — SWITCHMODE POWER TRANSISTORS (continued)

$V_{CEO(sus)}$ Volts Min	I_C Cont Amps Max	V_{CEV} Volts Min	Device Type NPN unless otherwise noted	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
450	15	1000	**BUS48AP**	8 min	8	2	0.4	10		150	TO-218/340
		1000	**BUW13A**			4	0.8	8		175	TO-218/340
	9	1000	**BUS47A**	7 min	5	2	0.4	5		150	TO-204/1
		1000	**BUS47AP**	7 min	6	2	0.4	6		128	TO-218/340
	8	750	**MJ13081★**	8 min	5	1.5	0.5	5			TO-204/1
		850	**2N6835★**	7.5/3	5	2.5	0.25	5	10		TO-204/1
		850	**MJE16080**	5 min	8	2	0.5	5		80	TO-220/221A
		850	**MJ12021★**	5 min	8		0.1 typ	8			TO-204/1
		850	**MJ16006★**	5 min	8	2.5	0.25	5			TO-204/1
		850	**MJ16008★**	7 min	8	2.2	0.25	5			TO-204/1
		850	**MJH16006★**	5 min	8	2.5	0.25	5			TO-218/340
		850	**MJH16008★**	7 min	8	2.2	0.25	5			TO-218/340
		1000	**BUW12A**	6 min	5	4	0.8	5		125	TO-218/340
	5	750	**MJ13071★**	8 min	3	1.5	0.5	3			TO-204/1
		750	**MJE13071★**	8 min	3	1.5	0.5	3			TO-220/221A
		850	**2N6834★**	10/30	3	2.7	0.35	3	15		TO-204/1
		850	**MJ12020★**	5 min	5		0.13 typ	3			TO-204/1
		850	**MJ16002★**	5 min	5	3	0.3	3			TO-204/1
		850	**MJ16004★**	8 min	3	2.7	0.35	3			TO-204/1
		850	**MJE16002★**	5 min	5	3	0.3	3			TO-220/221A
		850	**MJE16004★**	7 min	5	2.7	0.35	3			TO-220/221A
		850	**MJH16002★**	5 min	5	3	0.3	3			TO-218/340
		850	**MJH16004★**	7 min	5	2.7	0.35	3			TO-218/340
		1000	**BUW11A**	6 min	2.5	4	0.8	2.5		125	TO-218/340
	3	1000	**BUX85**	30 min	0.1	3.5	1.4	1	4	50	TO-220/221A
400	56	600	**BUT33##**	20 min	36	3.3	1.6	36		250	TO-204 Mod/197
	50	650	**MJ10015##★**	10 min	40	2.5	1	20			TO-204 Mod/197
	40	600	**MJ10023##★**	50/600	10	2.5	0.9	20			TO-204 Mod/197
	30	850	**BUS98**	8 min	20	2.3	0.4	20		250	TO-204 Mod/197
	28	600	**BUT13##**	20 min	20	2.6	0.8	18		175	TO-204/1
	20	450	**BUV24**	8 min	12	3	0.9	12	8	250	TO-204/1
		500	**MJ10001#★**	40/400	10	3	1.8	10	10**		TO-204/1
		500	**MJ10005#★**	40/400	10	1.5	0.5	10	10**		TO-204/1
		500	**MJ13333★**	10/60	5	4	0.7	10			TO-204/1
	15	650	**MJ13090★**	8 min	10	2.5	0.5	10			TO-204/1
		650	**MJH6678**	8 min	15	2.5	0.5	15		125	TO-218/340
		650	**2N6678**	8 min	15	2.5	0.5	15	3		TO-204/1
		850	**2N6547★**	6/30	10	4	0.7	10	6 to 24		TO-204/1
		850	**BUS48**	8 min	10	2	0.4	10		175	TO-204/1
		850	**BUS48P**	8 min	10	2	0.4	10		150	TO-218/340
		850	**BUW13**			4	0.8	10		175	TO-218/340
		850	**BUX48**			3	0.6	10			TO-204/1
	12	700	**MJE13009★**	6/30	8	3	0.7	8	4**		TO-220/221A
	10	950	**MJ12010**	4.2 min	5		1	5	6 typ		TO-204/1
		550	**MJ10012#**	100/2k	6	6	15	15	6		TO-204/1
		500	**MJ10003#★**	30/300	5	2.5	1	5	10**		TO-204/1
		500	**MJ10007##★**	30/300	5	1.1	0.25	5	10**		TO-204/1
		450	**MJ13015★**	8/20	5	2	0.5	5			TO-204/1
	9	850	**BUS47**	7 min	6	2	0.4	6		150	TO-204/1
		850	**BUS47P**	7 min	5	2	0.4	6		128	TO-218/340

★ Designers Data Sheet characterization
Darlington ## Darlington with speed-up diode * t_{off} ** $|h_{fe}|$ @ 1 MHz

(continued)

TABLE 15 — SWITCHMODE POWER TRANSISTORS (continued)

$V_{CEO(sus)}$ Volts Min	I_CCont Amps Max	V_{CEV} Volts Min	Device Type NPN unless otherwise noted	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	t_f μs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
	8	850	2N6545★	7/35	5	4	1	5	6		TO-204/1
		800	MJE5742#	200/400	4	8 typ	2 typ	6			TO-220/221A
		800	MJE16080	5 min	8	2	0.5	5		80	TO-220/221A
		850	BUW12	6 min	6	4	0.8	5		125	TO-218/340
		850	BUX84	30 min	0.1	3.5	1.4	1	4	50	TO-220/221A
		700	MJE13007★	6/30	5	3	0.7	5	4		TO-220/221A
		650	MJ13080★	8 min	5	1.5	0.5	5			TO-204/1
		450	MJ6503-PNP★	15 min	2	2	0.5	4			TO-204/1
		450	MJE5852-PNP★	15 min	2	2	0.5	4			TO-220/221A
	6	900	BU326A	30 typ	0.6	3.5	1**	2.5	6	90	TO-204/1
		900	BU426A	30 typ	0.6	2 typ	0.5 typ	2.5	6 typ	113	TO-218/340
	5	850	2N6543★	7/35	3	4	0.8	3	6		TO-204/1
		850	BUW11	6 min	3	4	0.8	3		125	TO-218/340
		650	MJ13070★	8 min	3	1.5	0.5	3			TO-204/1
		650	MJE13070★	8 min	3	1.5	0.5	3			TO-220/221A
	4	700	MJE13005★	6/30	3	3	0.7	3	4		TO-220/221A
	1.5	700	MJE13003★	5/25	1	4	0.7	1	5		TO-225AA/77R
	0.5	400	MJ4647-PNP	20 min	0.5	0.72*		0.05	40		TO-205AD/79
375	6	800	BU326	30 typ	0.6	3.5	1**	2.5	6	90	TO-204/1
		800	BU426	30 typ	0.6	2 typ	0.5 typ	2.5	6 typ	113	TO-218/340
350	40	450	MJ10022##★	50/600	10	2.5	0.9	20			TO-204 Mod/197
	20	450	MJ10000#★	40/400	10	3	1.8	10	10**		TO-204/1
		450	MJ10004##★	40/400	10	1.5	0.5	10	10**		TO-204/1
	15	550	2N6677	8 min	15	2.5	0.5	15	3		TO-204/1
		375	2N6251	6/50	10	3.5	1	10	2.5		TO-204/1
		550	MJH6677	8 min	15	2.5	0.5	15		125	TO-218/340
	10	450	MJ10002#★	30/300	5	2.5	1	5	10**		TO-204/1
		450	MJ10006##★	30/300	5	1.5	0.5	5	10**		TO-204/1
		400	MJ13014★	8/20	5	2	0.5	5			TO-204/1
	8	700	2N6308	12/60	3	1.6	0.4	5	5		TO-204/1
		700	MJE5741#	200/400	4	8 typ	2 typ	6			TO-220/221A
		400	MJE5851-PNP	15 min	2	2	0.5	4			TO-220/221A
	2	400	2N6213-PNP	10/100	1	2.5	0.6	1	4		TO-213AA/80
325	30	400	BUV23	8 min	16	1.8	0.4	16	8	250	TO-204 Mod/197
	15	400	BUX13	8 min	8	2.5	0.8	8	8	150	TO-204/1
	5	350	2N6235	25/125	1	3.5	0.5	1	20		TO-213AA/80
300	15	650	2N6546★	6/30	10	4	0.7	10	6 to 24		TO-204/1
		450	2N6676	8 min	15	2.5	0.5	15	3		TO-204/1
		450	MJH6676	8 min	15	2.5	0.5	15		125	TO-218/340
	12	600	MJE13008★	6/30	8	3	0.7	8	4**		TO-220/221A
	8	600	2N6307	15/75	3	1.6	0.4	3	5		TO-204/1
		600	MJE13006★	6/30	5	3	0.7	5	4		TO-220/221A
		600	MJE5740	200/400	4	8 typ	2 typ	6			TO-220/221A
		350	MJE5850-PNP★	15 min	2	2	0.5	4			TO-220/221A
	5	400	2N6498	10/75	2.5	1.8	0.8	2.5	5		TO-220/221A
	4	600	MJE13004★	6/30	3	3	0.7	3	4		TO-220/221A
	2	500	2N3585	25/100	1	4	3	1	10		TO-213AA/80
		500	2N6422-PNP	25/100	1	4	3	1	10		TO-213AA/80
		350	2N6212-PNP	10/100	1	2.5	0.6	1	4		TO-213AA/80
	1.5	600	MJE13002★	5/25	1	4	0.7	1	5		TO-225AA/77R

★ Designers Data Sheet characterization
\# Darlington ## Darlington with speed-up diode * t_{off} ** $|h_{fe}|$ @ 1 MHz

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TABLE 15 — SWITCHMODE POWER TRANSISTORS (continued)

$V_{CEO(sus)}$ Volts Min	I_C Cont Amps Max	V_{CEV} Volts Min	Device Type NPN unless otherwise noted	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	t_f μs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
300	1	300	2N5345-PNP	25/100	0.5	0.6	0.1	0.5	60		TO-213AA/80
	0.5	300	MJ4646-PNP	20 min	0.5	0.72*		0.05	40		TO-205AD/79
275	15	300	2N6250	8/50	10	3.5	1	10	2.5		TO-204/1
250	100	300	MJ10047##★	75 min	100	4	1	100			—/353
		300	MJ10048#★	75 min	100	2	8	100			—/353
	60	350	MJ10021##★	25 min	30	3.5	0.5	30			TO-204 Mod/197
	40	300	BUV22	10 min	20	1.1	0.35	20	8	250	TO-204/1
		350	BUS52	15 min	40					350	TO-204/1
	20	300	BUV12	10 min	10	1.5	0.5	10	8	150	TO-204/1
		450	MJ13331★	8/40	10	3.5	0.7	10	5/40		TO-204/1
	15	250	MJ11021#-PNP	100 min	15				3#		TO-204/1
		250	MJ11022#	100 min	15				3#		TO-204/1
	12	300	BUX42	8 min	6	2	0.4	6	8	120	TO-204/1
	8	500	2N6306	15/75	3	1.6	0.4	3	5		TO-204/1
		400	MJ6502-PNP★	15 min	2	2	0.5	4			TO-204/1
	5	500	MJ3029	30 min	0.4		1	3			TO-204/11
		350	2N6497	10/75	2.5	1.8	0.8	2.5	5		TO-220/221A
	2	375	2N3584	25/100	1	4	3	1	10		TO-213AA/80
		375	2N6421-PNP	25/100	1	4	3	1	10		TO-213AA/80
	1	250	2N5344-PNP	25/100	0.5	0.6	0.1	0.5	60		TO-213AA/80
225	2	275	2N6211	10/100	1	2.5	0.6	1	20		TO-213AA/80
200	60	300	MJ10020##★	25 min	30	3.5	0.5	30			TO-204 Mod/197
	50	300	BUS51	15 min	50					350	TO-204/1
	40	250	BUV21	10 min	25	1.8	0.4	25	8	150	TO-204/1
	20	250	BUV11	10 min	12	1.8	0.4	12	8	150	TO-204/1
		400	MJ13330★	8/40	10	3.5	0.7	10	5/40		TO-204/11
	15	225	2N6249	10/50	10	3.5	1	10	2.5		TO-204/11
		250	BUX41	8 min	8	1.5	0.4	8	8	120	TO-204/1
		200	MJ11019#-PNP	100 min	15				3#		TO-204/1
		200	MJ11020#	100 min	15				3#		TO-204/1
	3	250	BUY49P	30 min	0.5				25	20	TO-225AA/77

★ Designers Data Sheet characterization
Darlington ## Darlington with speed-up diode * t_{off} ** $|h_{fe}|$ @ 1 MHz

Application Selector Guides

Application Literature

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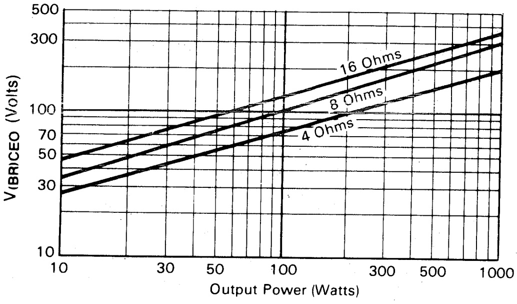
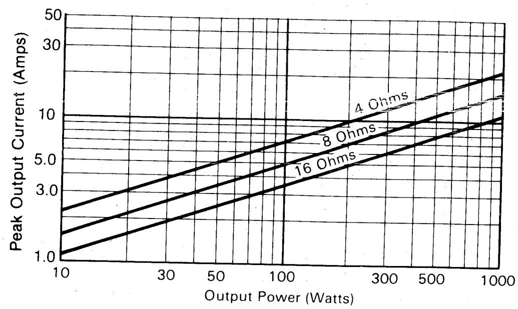
EN-101 Verifying Collector Voltage Ratings

GENERAL DESIGN CURVES FOR POWER AUDIO OUTPUT STAGES

$V_{(BR)CEO}$ Required on Output and Driver Transistors versus Output Power for 4, 8 and 18 Ohm Load



Output Transistor Peak Collector Current versus Output Power for 4, 8 and 16 Ohm Loads



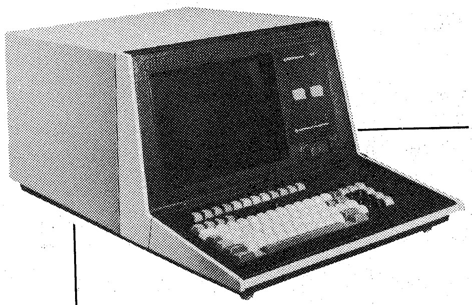
Another important parameter that must be considered before selecting the output transistors is the safe-operating area these devices must withstand. For a complete discussion on these see Application Notes AN-484A and AN-485.

TABLE 16 — RECOMMENDED POWER TRANSISTORS FOR AUDIO/SERVO LOADS

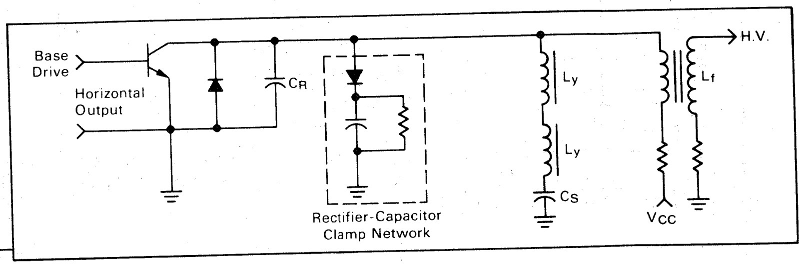
RMS Power Output	NPN	PNP	Case	P_D Watts @ 25°C	V_{CEO}	h_{FE}@ Min/Max	I_C Amps	f_T MHz Typ	ISB Volts/Amps
To 25W	MJE15030	MJE15031	TO-220	50W	150 V	20 min	4A	70	14/3.6
25 to 50W	2N3055A	MJ2955A	TO-204	120W	120 V	20/70	4A	3	60/2
	MJ15001	MJ15002	TO-204	200W	140 V	25/150	4A	3	40/5
50 to 100W	MJ15015	MJ15016	TO-204	180W	120 V	20/70	4A	3	60/3
	MJ15003	MJ15004	TO-204	250W	140 V	25/150	5A	3	100/1
Over 100W	MJ15024	MJ15025	TO-204	250W	250 V	15/60	8A	8	80/2.2

The Power Transistors shown are provided for reference only and show device capability. The final choice of the Power Transistors used is left to the circuit designer and depends upon the particular safe-operating area required and the mounting and heat sinking configuration used.

CRT Deflection



The typical raster scanning television or CRT data monitor normally uses an inductive switched horizontal output stage. The horizontal output switching is accomplished by a high voltage bipolar power transistor. This device switches from 0.5 to 5 A or higher collector current levels and must block a 100 to 1500 V retrace or flyback pulse. The listed Motorola semiconductor power devices will easily handle this task if the circuit electrical parameters have been properly established.



2

TABLE 17 — HORIZONTAL CRT DEFLECTION TRANSISTOR SELECTOR GUIDE

Applications	Retrace Voltage	I_{PK} Amps	Scan Rate	Preferred Devices*	V_{CEX} Volts	I_C Amps
Line Operated T.V. (120 Vac)						
Small Screen B/W	Up to 975	1 to 2	15 k	MJ12002	1500	2.5
Large Screen B/W, or Small Color	Up to 975	2 to 3	15 k	MJ12003	1500	4
Large Screen Color	Up to 975	4 to 5	15 k	BU508,D	1500	8
Battery Operated T.V.	Up to 250	3 to 10	15 k	BU407	350	7
Display Monitors						
Low End	Up to 250	3 to 10	20 k	BU407	350	7
High End	Up to 975	2 to 5	30 k	MJH16018	1500	8

* Additional selections are available for specific circuit requirements — see Device Selection By Package Type.

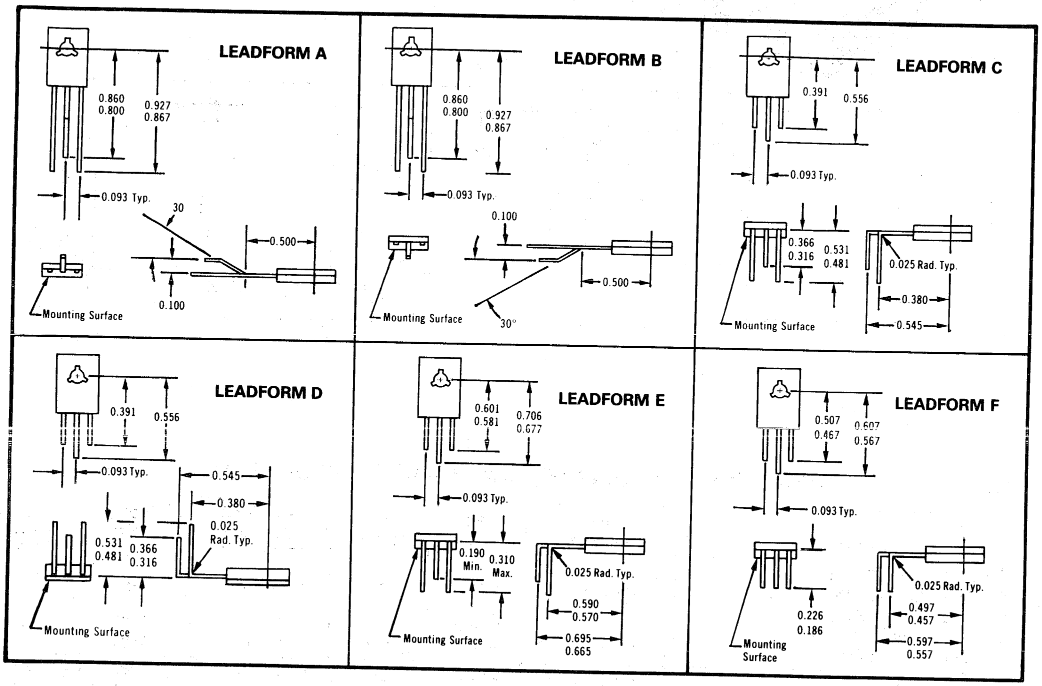
Preferred Leadform Options For Motorola Plastic Power Transistors

ORDERING INFORMATION

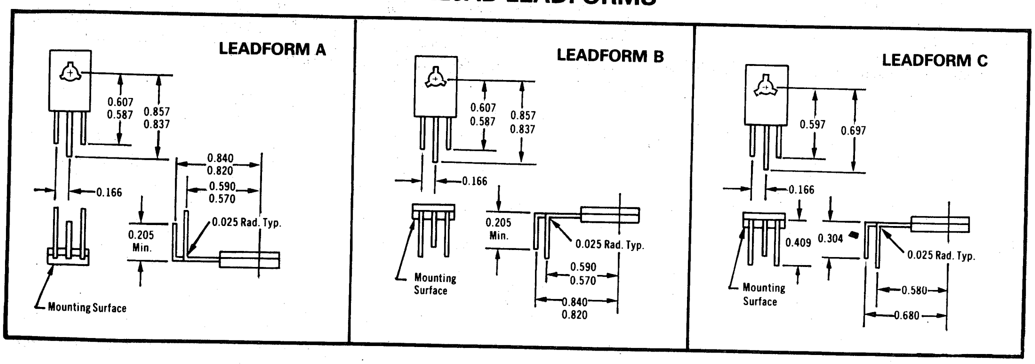
TO-225AA (Case 77), TO-225AB (Case 90), TO-220AB (Case 221A)

Devices may be leadformed by first converting to a special "SJE" number. The factory must be given the designation of the package and the applicable leadform suffix letter. The factory must be consulted.

TO-225AA LEADFORMS



TO-225AB LEADFORMS

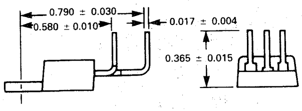


2

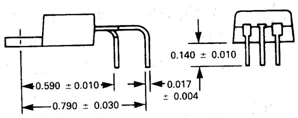
TO-220 LEADFORMS

Options are listed in parenthesis below standard dimensions.

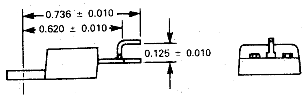
LEADFORM AJ



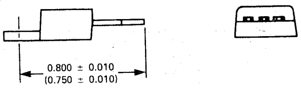
LEADFORM AK



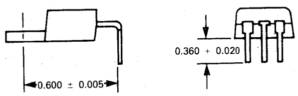
LEADFORM S



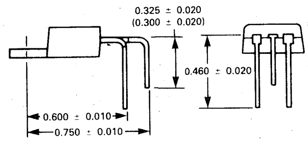
LEADFORMS W & WC



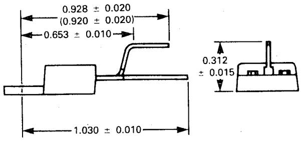
LEADFORM 2A



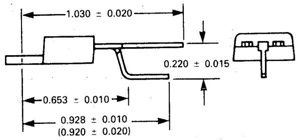
LEADFORMS 3 & 3A



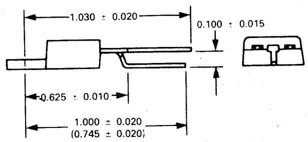
LEADFORMS 5F & 5FA



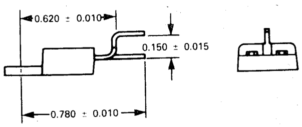
LEADFORMS 5R & 5RA



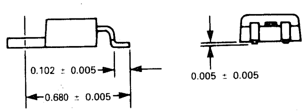
LEADFORMS 10R & 10RC



LEADFORM 15FA



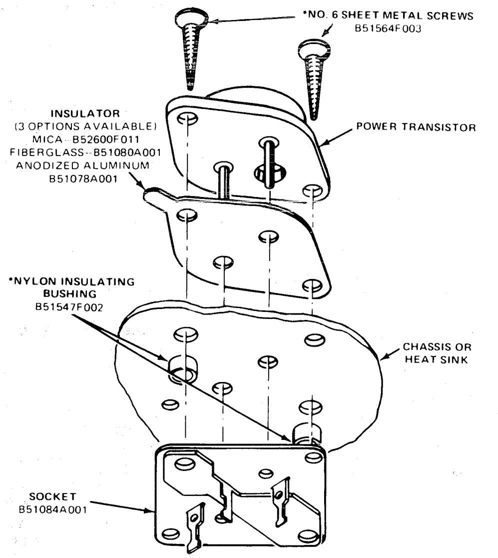
LEADFORM 16



2

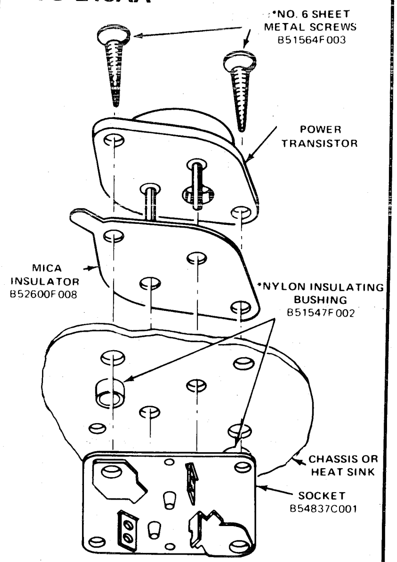
Mounting Hardware

TO-204AA



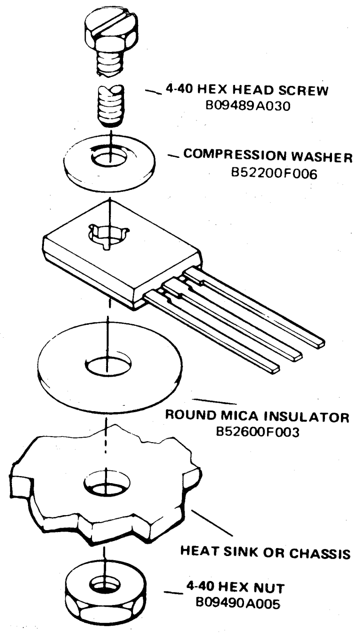
* Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

TO-213AA



* Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

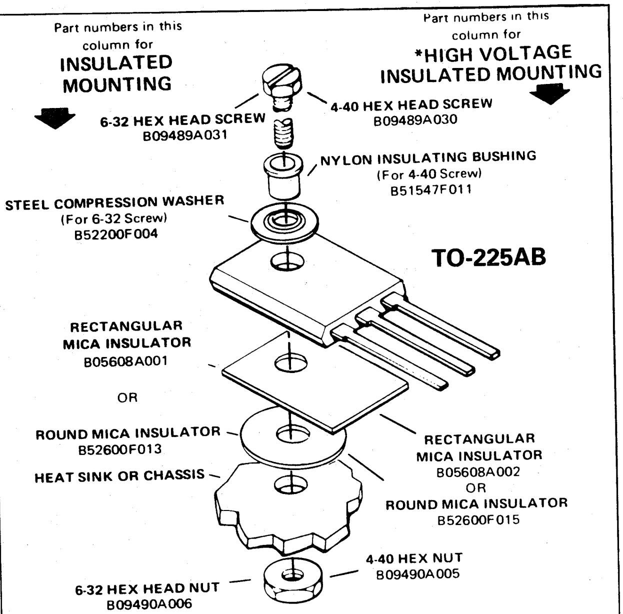
TO-225AA



TORQUE REQUIREMENTS
0.68N-m (6IN-LBS.) MAX.

MOUNTING HARDWARE — continued

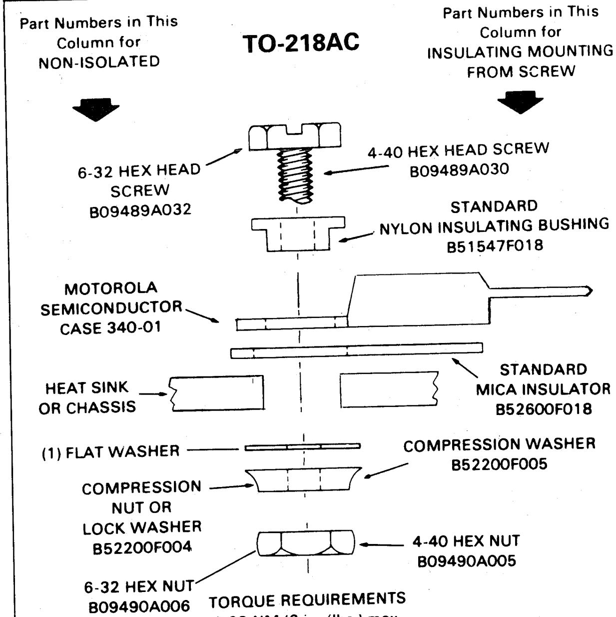
TO-225AB



TORQUE REQUIREMENTS
Insulated 0.68 N-m (6 IN. LBS.) MAX
High Voltage Insulated 0.90 N-m (8 IN. LBS.) MAX

*High voltage mounting requirements depend on use environment. User is encouraged to make his own evaluation.

TO-218AC



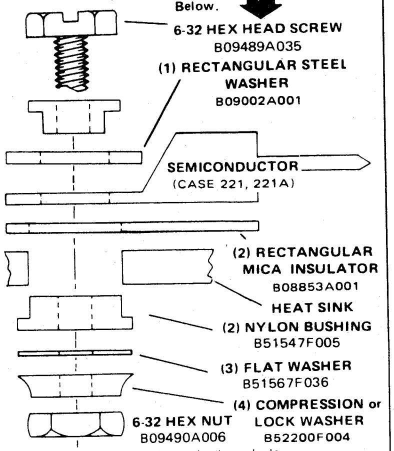
TORQUE REQUIREMENTS
0.68 NM (6 in./lbs.) max.
Recommended Torque: 0.57 Nm/5 in./lbs. - 5.5 kg/cm.
(1) USE WITH LOCK WASHER

TO-220AB

PREFERRED ARRANGEMENT

for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used.

Choose from Parts Listed Below.

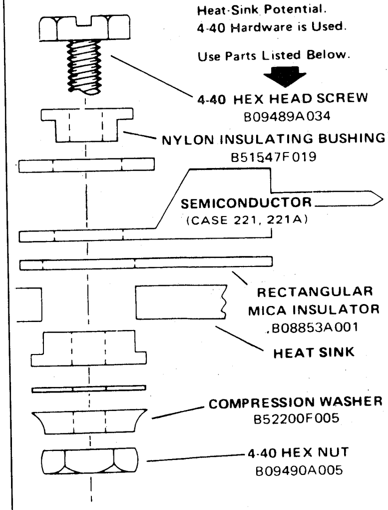


(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing and lock washer are used.
(4) Compression washer preferred when plastic insulating material is used.

ALTERNATE ARRANGEMENT

for Isolated Mounting when Screw must be at Heat-Sink Potential. 4-40 Hardware is Used.

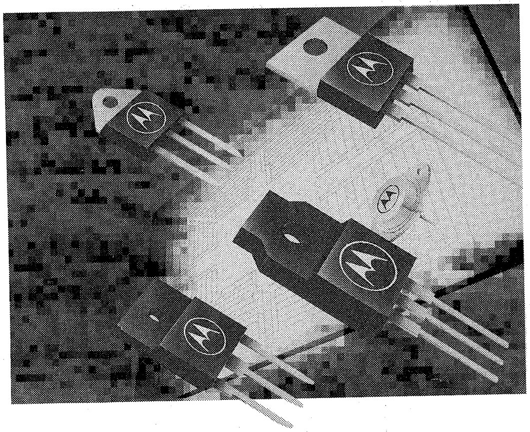
Use Parts Listed Below.



TORQUE REQUIREMENTS
Insulated
0.68 N·M (6 in-lbs) max
Noninsulated
0.9 N·M (8 in-lbs) max*

2

2



Data Sheets

3

The following power transistor data sheets are arranged in alphanumeric sequence, some data sheets may contain information applying to more than one transistor — e.g. 2N4398, 2N4399, 2N5745. To determine if a particular device type is covered by a data sheet in this section, either refer to the alphanumeric listing of the Index and Cross Reference on page 1-2 or simply turn to the proper sequence for indication of where the Data Sheet can be found.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

2N3054
2N3054A

MEDIUM-POWER NPN SILICON TRANSISTORS

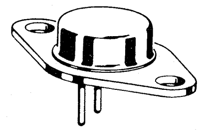
. . . designed for general purpose switching and amplifier applications.

- Excellent Safe Operating Area
- DC Current Gain Specified to 3.0 Amperes
- Complement to PNP Type 2N6049 or 2N4912

4 AMPERE

POWER TRANSISTORS NPN SILICON

55 VOLTS
25 WATTS – 2N3054
75 WATTS – 2N3054A



*MAXIMUM RATINGS

Rating	Symbol	2N3054A	2N3054	Unit
Collector-Emitter Voltage	V_{CEO}	55		Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	60		Vdc
Collector-Base Voltage	V_{CB}	90		Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	4.0 10**		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.43	25 0.143	Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200		°C

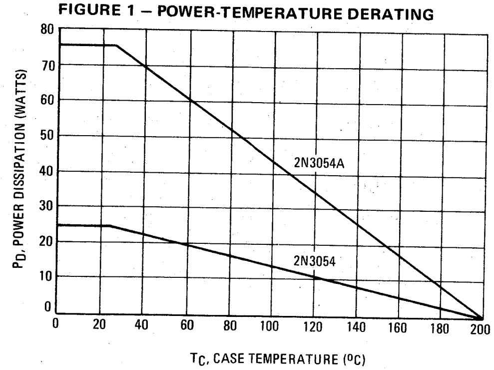
*Indicates JEDEC Registered Data
**Addition to JEDEC Registered Data

3

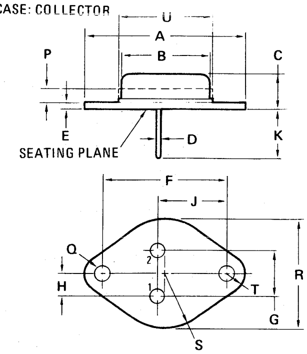
THERMAL CHARACTERISTICS

Characteristic	Symbol	2N3054A	2N3054	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.33	7.0	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	55	—	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, R_{BE} = 100 Ω)	$V_{CER(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	500	μAdc
Collector Cutoff Current (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		—	6.0	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
***ON CHARACTERISTICS** (1)				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	25	150	—
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		5.0	—	
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	—	1.0	Vdc
(I_C = 3.0 Adc, I_B = 1.0 Adc)		—	6.0	
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.7	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc)	f_T	3.0	—	MHz
*Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	25	180	—
*Common-Emitter Cutoff Frequency (I_C = 100 mAdc, V_{CE} = 4.0 Vdc)	f_{hfe}	30	—	kHz

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%

3

FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUIT

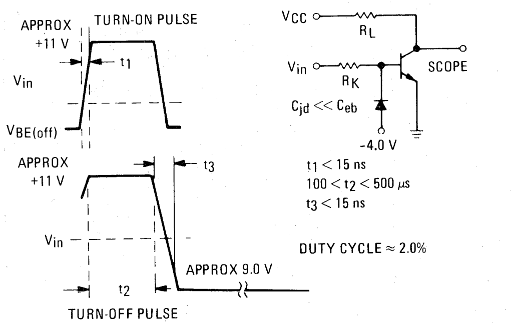


FIGURE 3 – TURN-ON TIME

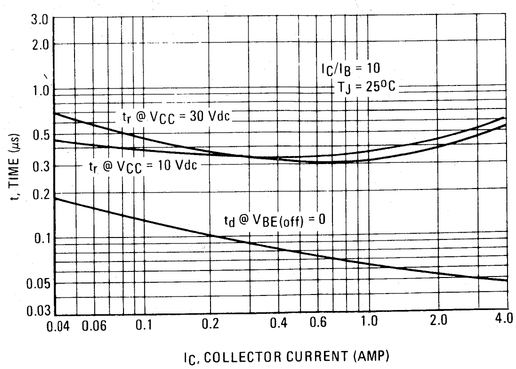


FIGURE 4 – THERMAL RESPONSE

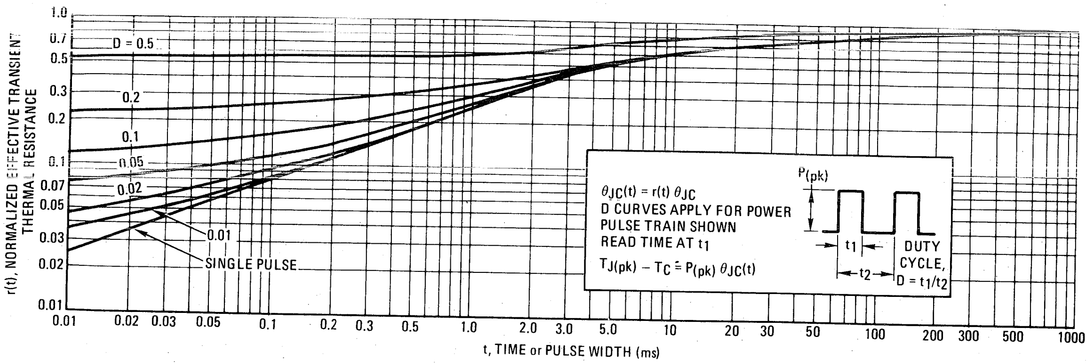
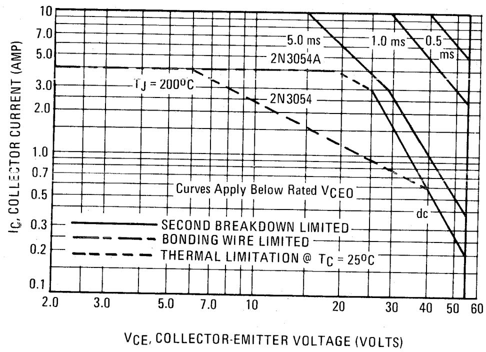


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

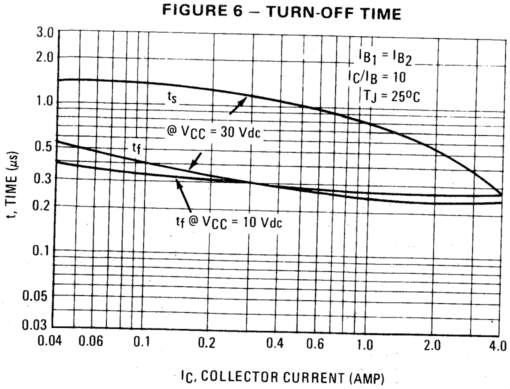


FIGURE 7 – CAPACITANCE

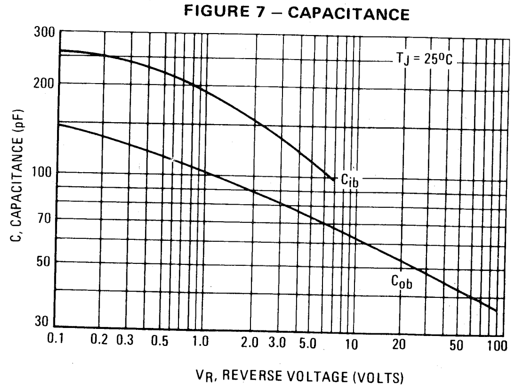


FIGURE 8 – DC CURRENT GAIN

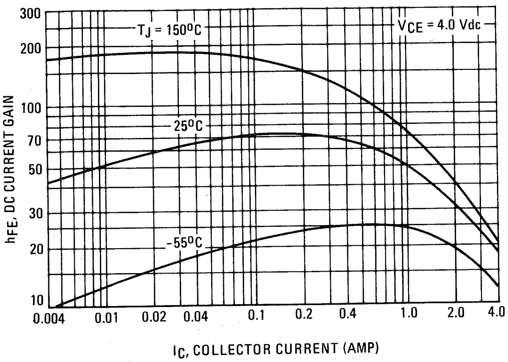


FIGURE 9 – COLLECTOR SATURATION REGION

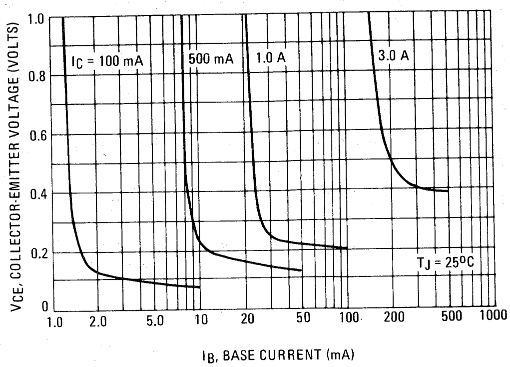


FIGURE 10 – TEMPERATURE COEFFICIENTS

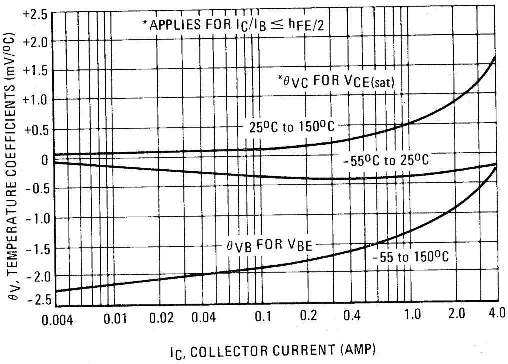


FIGURE 11 – "ON" VOLTAGES

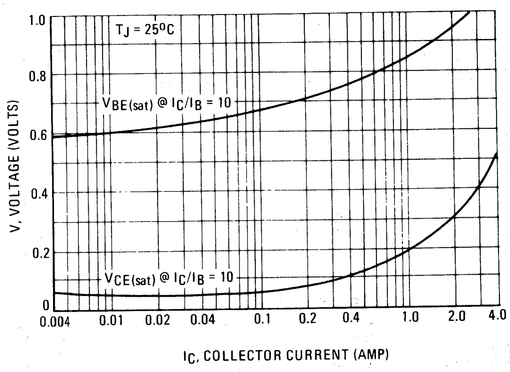


FIGURE 12 – COLLECTOR CUT-OFF REGION

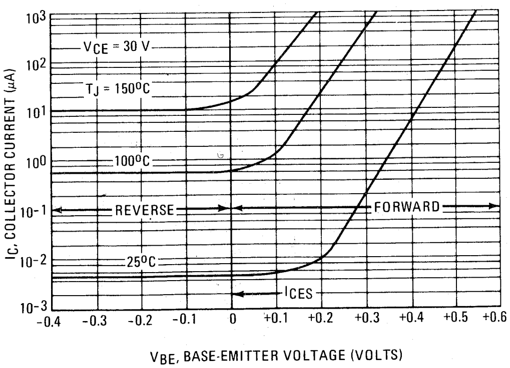
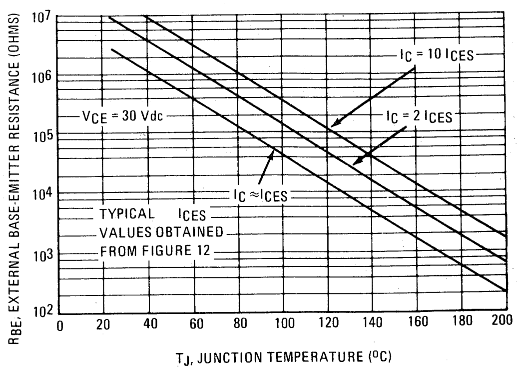


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
2N3055
PNP
MJ2955

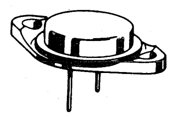
COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose switching and amplifier applications.

- DC Current Gain — h_{FE} = 20-70 @ I_C = 4 Adc
- Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4 Adc
- Excellent Safe Operating Area

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON

60 VOLTS
115 WATTS



MAXIMUM RATINGS

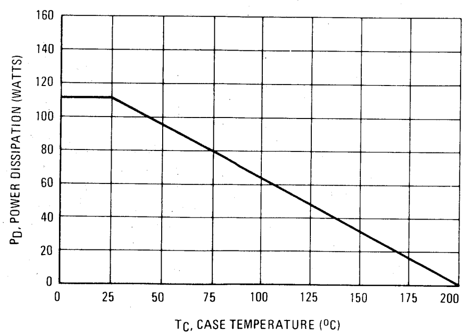
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Emitter Voltage	V_{CER}	70	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	7	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.657	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

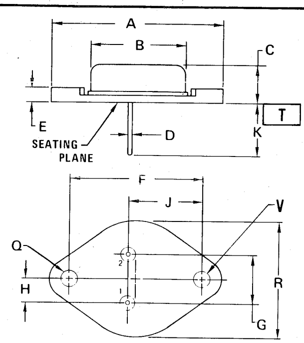
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

3

FIGURE 1 — POWER DERATING





NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⊕ | ϕ 0.25 (0.010) Ⓜ | T | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⊕ | ϕ 0.30 (0.012) Ⓜ | T | V Ⓜ | Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

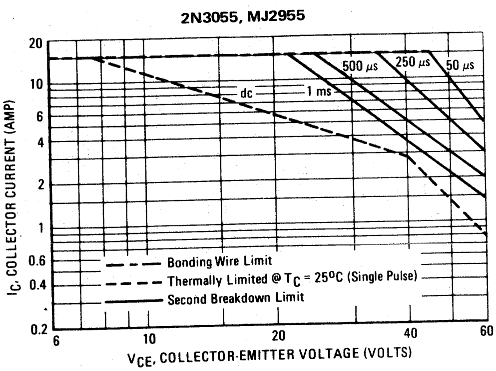
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	70	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
***ON CHARACTERISTICS (1)**				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	70 –	–
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	–	1.1 3.0	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.5	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s; Nonrepetitive)	$I_{s/b}$	2.87	–	Adc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	–	MHz
*Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	15	120	–
*Small-Signal Current Gain Cutoff Frequency (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	f_{hfe}	10	–	kHz

* Indicates Within JEDEC Registration. (2N3055)
(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2.0%.

3

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

NPN
2N3055

PNP
MJ2955

FIGURE 3 – DC CURRENT GAIN

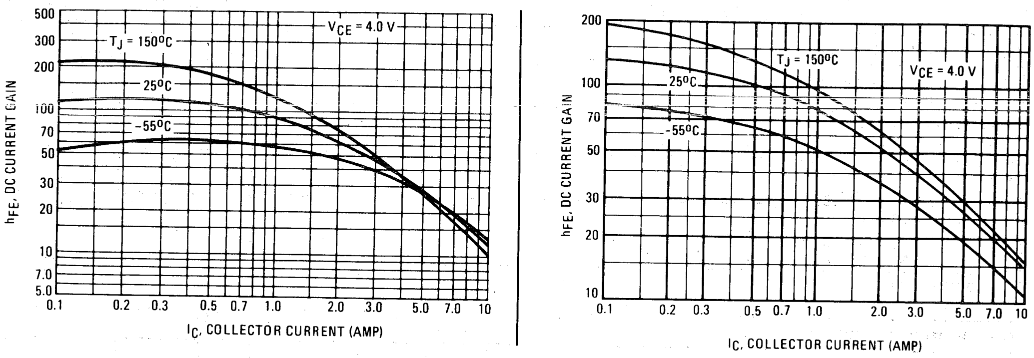


FIGURE 4 – COLLECTOR SATURATION REGION

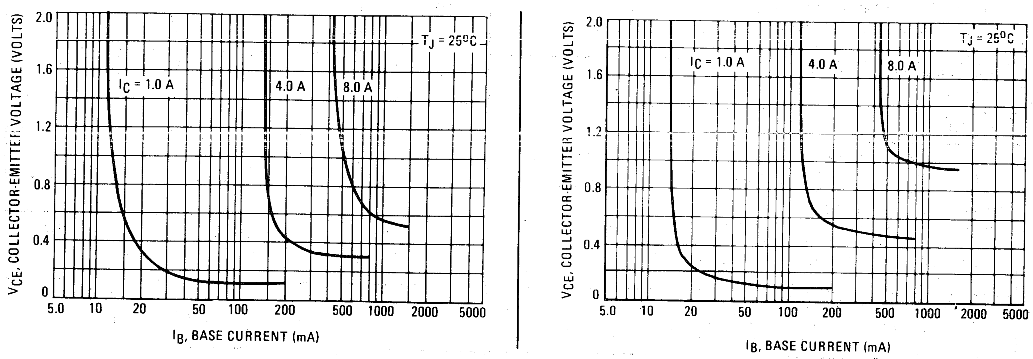
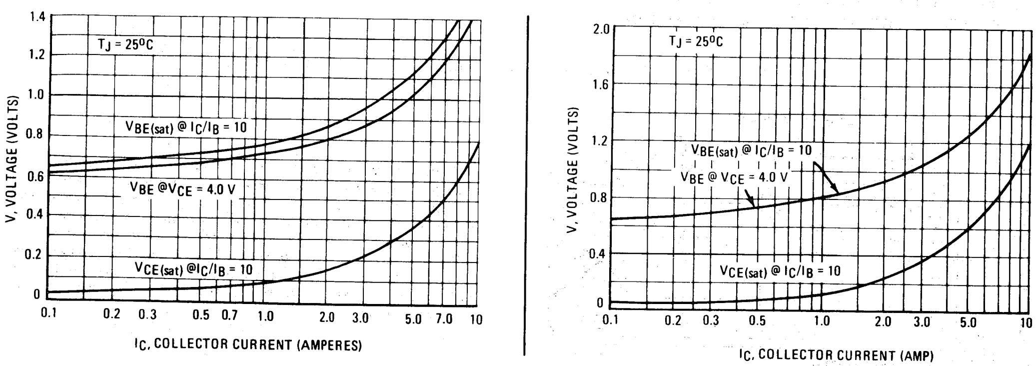


FIGURE 5 – "ON" VOLTAGES



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN | **PNP**
2N3055A | **MJ2955A**
MJ15015 | **MJ16016**

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

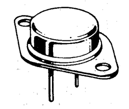
. . . PowerBase complementary transistors designed for high power audio, stepping motor and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc-to-dc converters, inverters, or for inductive loads requiring higher safe operating area than the 2N3055 and MJ2955.

- Current-Gain — Bandwidth-Product @ I_C = 1.0 Adc
  f_T = 0.8 MHz (Min) — NPN
  = 2.2 MHz (Min) — PNP
- Safe Operating Area — Rated to 60 V and 120 V, Respectively

15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60, 120 VOLTS
115, 180 WATTS



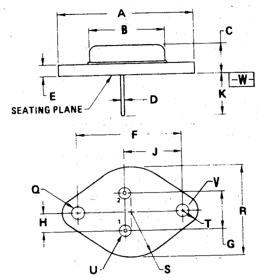
*MAXIMUM RATINGS

Rating	Symbol	2N3055A MJ2955A	MJ15015 MJ15016	Unit
Collector-Emitter Voltage	V_{CEO}	60	120	Vdc
Collector-Base Voltage	V_{CBO}	100	200	Vdc
Collector-Emitter Voltage Base Reversed Biased	V_{CEV}	100	200	Vdc
Emitter-Base Voltage	V_{EBO}	7.0		Vdc
Collector Current — Continuous	I_C	15		Adc
Base Current	I_B	7.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.65	180 1.03	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.52	0.98	°C/W

*Indicates JEDEC Registered Data (2N3055A)



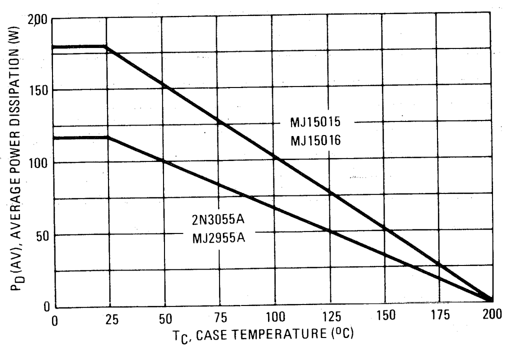
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.
2. DIAMETER V AND SURFACE W ARE DATUMS.
3. POSITIONAL TOLERANCE FOR HOLE Q:
⌖ | ∅ 0.25 (0.010) Ⓜ | W | V Ⓜ
4. POSITIONAL TOLERANCE FOR LEADS:
⌖ | ∅ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

CASE 1-04
TO-204AA

FIGURE 1 — POWER DERATING



3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
*Collector-Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	2N3055A, MJ2955A MJ15015, MJ15016	$V_{CEO(sus)}$	60 120	— —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, $V_{BE(off)}$ = 0 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 0 Vdc)	2N3055A, MJ2955A MJ15015, MJ15016	I_{CEO}	— —	0.7 0.1	mAdc
*Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	2N3055A, MJ2955A MJ15015, MJ15016	I_{CEV}	— —	5.0 1.0	mAdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3055A, MJ2955A MJ15015, MJ15016	I_{CEV}	— —	30 6.0	mAdc
*Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	2N3055A, MJ2955A MJ15015, MJ15016	I_{EBO}	— —	5.0 0.2	mAdc
***SECOND BREAKDOWN**					
Second Breakdown Collector Current with Base Forward Biased (t = 0.5 s non-repetitive) (V_{CE} = 60 Vdc)	2N3055A, MJ2955A MJ15015, MJ15016	$I_{S/b}$	1.95 3.0	— —	Adc
***ON CHARACTERISTICS (1)**					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	10 20 5.0	70 70 —	—
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc) (I_C = 15 Adc, I_B = 7.0 Adc)		$V_{CE(sat)}$	— — —	1.1 3.0 5.0	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	0.7	1.8	Vdc
***DYNAMIC CHARACTERISTICS**					
Current-Gain—Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)	2N3055A, MJ15015 MJ2955A, MJ15016	f_T	0.8 2.2	6.0 18	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	60	600	pF
***SWITCHING CHARACTERISTICS (2N3055A only)**					
RESISTIVE LOAD					
Delay Time	(V_{CC} = 30 Vdc, I_C = 4.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, t_p = 25 μs Duty Cycle ≤ 2%)	t_d	—	0.5	μs
Rise Time		t_r	—	4.0	μs
Storage Time		t_s	—	3.0	μs
Fall Time		t_f	—	6.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.
*Indicates JEDEC Registered Data (2N3055A)

3

FIGURE 2 – DC CURRENT GAIN

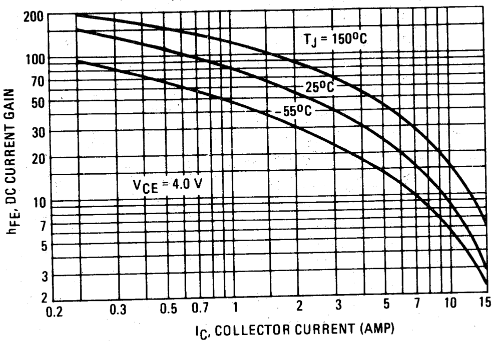


FIGURE 3 – COLLECTOR SATURATION REGION

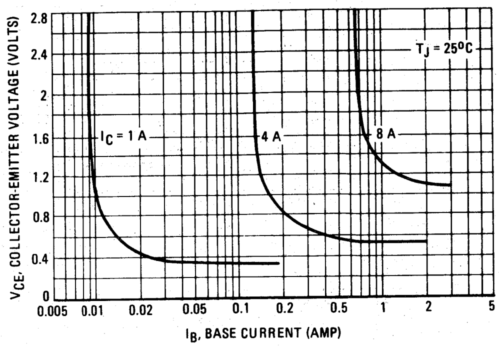


FIGURE 4 – "ON" VOLTAGES

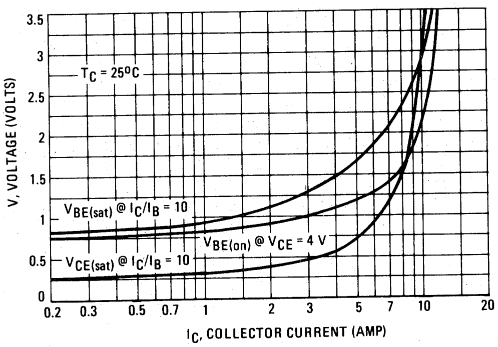


FIGURE 5 – CURRENT-GAIN–BANDWIDTH PRODUCT

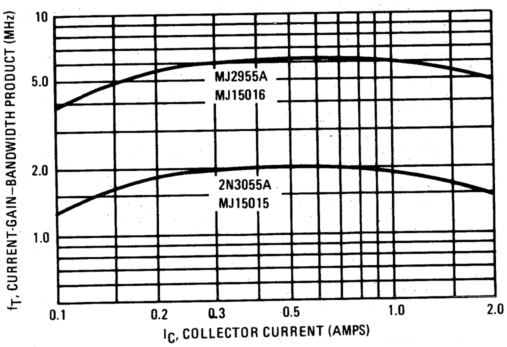


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT
(Circuit shown is for NPN)

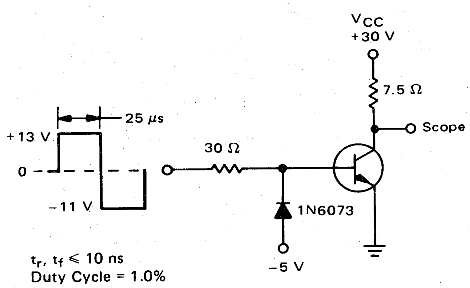


FIGURE 7 – TURN-ON TIME

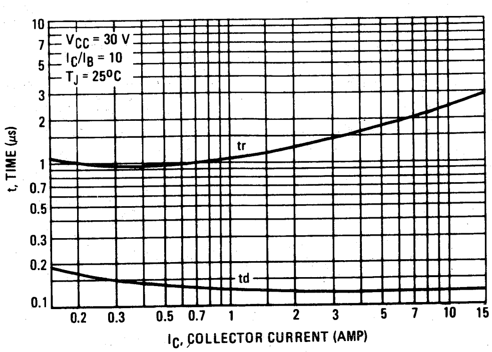


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FIGURE 8 — TURN-OFF TIMES

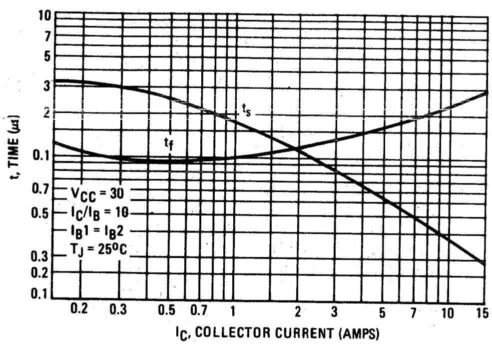
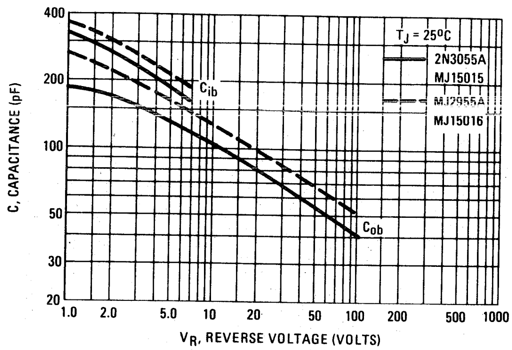
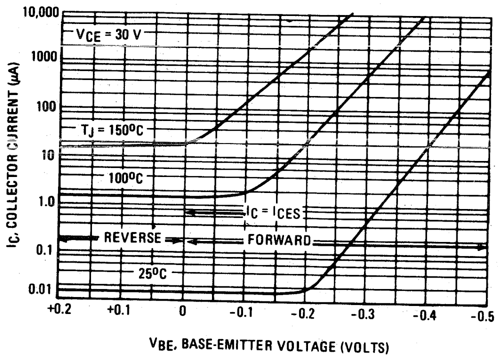


FIGURE 9 — CAPACITANCES



COLLECTOR CUT-OFF REGION

NPN
FIGURE 10 — 2N3055A, MJ15015



PNP
FIGURE 11 — MJ2955A, MJ15016

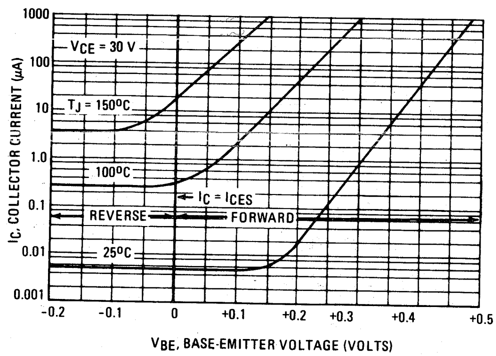


FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA
2N3055A, MJ2955A

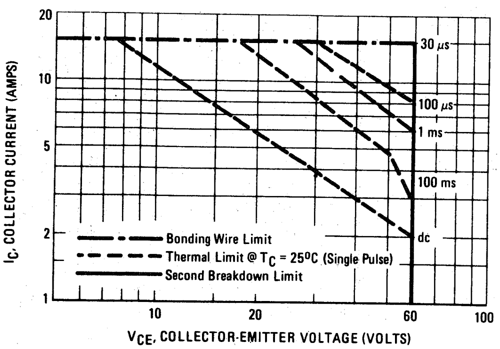
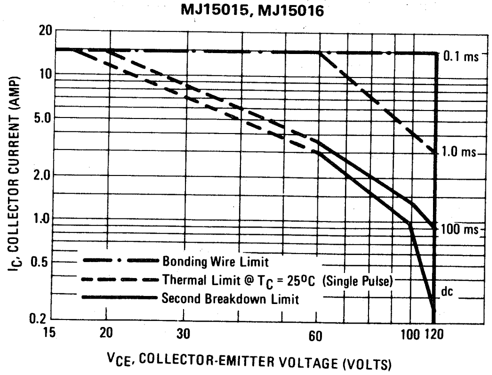


FIGURE 13 — FORWARD BIAS SAFE OPERATING AREA
MJ15015, MJ15016



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe Operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 12 and 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N3441

3 AMPERES

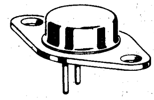
NPN SILICON POWER TRANSISTOR

140 VOLTS
25 WATTS

NPN SILICON POWER TRANSISTOR

. . . 2N3441 transistor is designed for use in general-purpose switching and linear amplifier applications requiring high breakdown voltages. It is characterized for use as:

- Driver for High Power Outputs
- Series and Shunt Regulators
- Audio and Servo Amplifiers
- Solenoid and Relay Drivers
- Power Switching Circuits

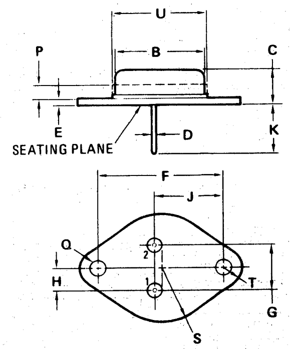


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	140	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector Current — Continuous	I_C	3	Adc
Base Current — Continuous	I_B	2	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	25 0.142	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7	$^oC/W$



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

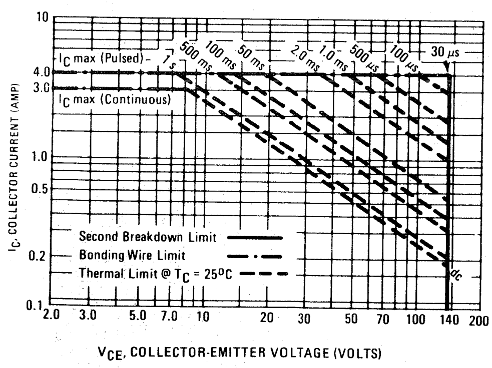
CASE 80-02
TO-213AA

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Adc, I_B = 0)	I_{CEO}	–	100	mA
Collector Cutoff Current	I_{CEX}			mA
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 V)		–	5.0	
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 V @ 150°C)		–	6.0	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mA
ON CHARACTERISTICS				
DC Current Gain (1)	h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 4.0 V)		25	100	
(I_C = 2.7 Adc, V_{CE} = 4.0 V)		5.0	–	
Collector-Emitter Saturation Voltage (1) (I_C = 2.7 Adc, I_B = 0.9 Adc)	$V_{CE(sat)}$	–	6.0	Vdc
Base-Emitter On Voltage (1) (I_C = 2.7 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	6.7	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1 kHz)	h_{fe}	15	75	–
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f_{test} = 0.4 MHz)	$\|h_{fe}\|$	5.0	–	–

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N3442
2N4347

3

HIGH-POWER INDUSTRIAL TRANSISTORS

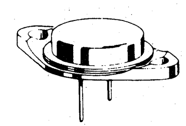
NPN silicon power transistors designed for applications in industrial and commercial equipment including high fidelity audio amplifiers, series and shunt regulators and power switches.

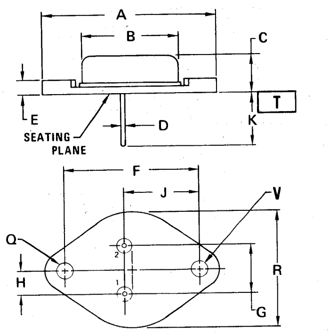
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 2.0 Adc – 2N4347
- Collector-Emitter Sustaining Voltage – $V_{CEO(sus)}$ = 120 Vdc (Min) – 2N4347
  140 Vdc (Min) – 2N3442
- Excellent Second-Breakdown Capability

5.0 AND 10 AMPERE

POWER TRANSISTORS
NPN SILICON

120, 140 VOLTS
100, 117 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⊕ | ϕ 0.25 (0.010) Ⓜ | T | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⊕ | ϕ 0.30 (0.012) Ⓜ | T | V Ⓜ | Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

*MAXIMUM RATINGS

Rating	Symbol	2N4347	2N3442	Unit
Collector-Emitter Voltage	V_{CEO}	120	140	Vdc
Collector-Base Voltage	V_{CB}	140	160	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current – Continuous Peak	I_C	5.0 10	10 15**	Adc
Base Current – Continuous Peak	I_B	3.0 8.0	7.0 –	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.57	117 0.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N4347	2N3442	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	1.5	°C/W

*Indicates JEDEC Registered Data.
**This data guranteed in addition to JEDEC registered data.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

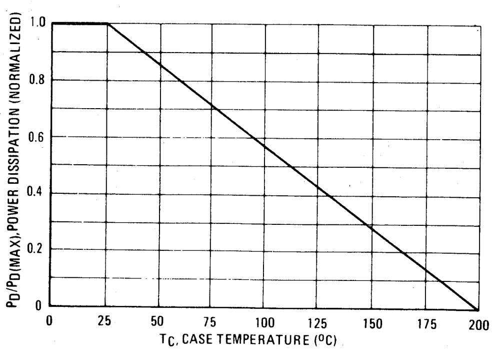
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	2N4347	$V_{CEO(sus)}$	120	–	Vdc
	2N3442		140	–	
Collector Cutoff Current (V_{CE} = 100 Vdc, I_B = 0)	2N4327	I_{CEO}	–	200	mAdc
(V_{CE} = 140 Vdc, I_B = 0)	2N3422		–	200	
Collector Cutoff Current (V_{CE} = 125 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4347	I_{CEX}	–	2.0	mAdc
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3442		–	5.0	
(V_{CE} = 120 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N4347		–	10	
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3442		–	30	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	2N4347, 2N3442	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)	2N4347	h_{FE}	15	60	–
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	2N4347		10	–	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N3442		20	70	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3442		7.5	–	
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)	2N4347	$V_{CE(sat)}$	–	1.0	Vdc
(I_C = 5.0 Adc, I_B = 0.63 Adc)	2N4347		–	2.0	
(I_C = 10 Adc, I_B = 2.0 Adc)	2N3442		–	5.0	
Base-Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)	2N4347	$V_{BE(on)}$	–	2.0	Vdc
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	2N4347		–	3.0	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3442		–	5.7	
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f_{test} = 50 kHz)	2N4347	f_T	200	–	kHz
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 40 kHz)	2N3442		80	–	
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	2N4347	h_{fe}	40	–	–
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	2N3442		12	72	

*Indicates JEDEC Registered Data

NOTES: 1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
2. $f_T = |h_{fe}| \cdot f_{test}$

3

FIGURE 1 – POWER DERATING



ACTIVE REGION SAFE OPERATING AREA INFORMATION

FIGURE 2 — 2N3442

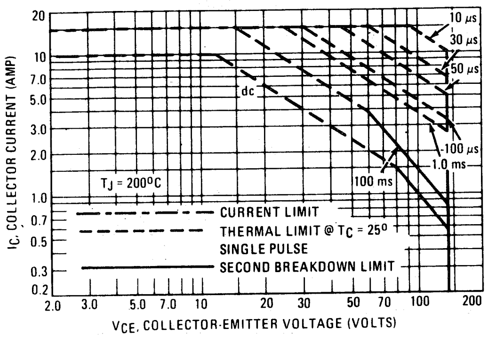
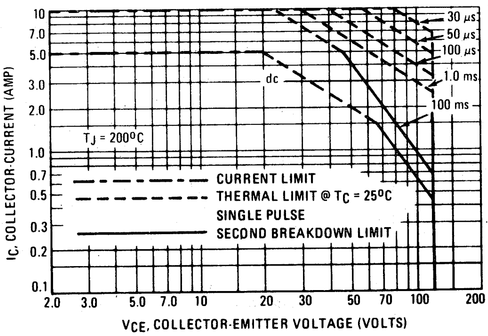


FIGURE 3 — 2N4347



There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 and 3 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 — DC CURRENT GAIN

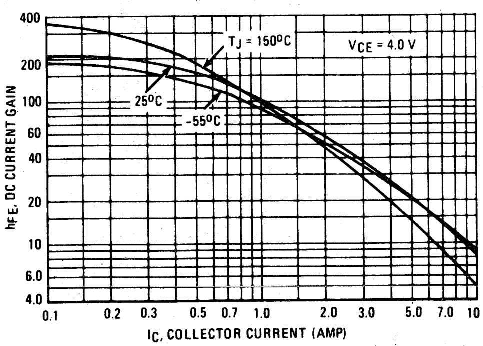
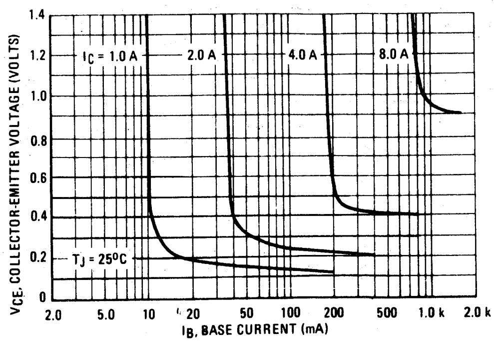


FIGURE 5 — COLLECTOR-SATURATION REGION



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N3447
2N3448

HIGH-SPEED SILICON ANNULAR NPN POWER TRANSISTORS

. . . for switching and amplifier applications

FEATURES

- Fast Switching: Total Switching Time = 1.2 μs (Typ) @ 5.0 A
- High Gain: h_{FE} = 40 to 120 @ 5.0 Amps
- Guaranteed DC Safe Area: 1.5 Amps (Min) @ V_{CE} = 40 Vdc
- Low $V_{CE(sat)}$: 1.0 Volt (Typ), 1.5 Volts (Max) @ 5.0 Amps
- Excellent Beta Linearity

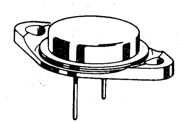
APPLICATIONS

- Specified safe area of this series allows reliable design for inverters, converters, hammer, and servo drivers.
- Fast response makes it ideal for series regulators; high switching speeds enhance its use in switching regulators.
- Wide bandwidth and flat beta hold-up result in exceptional amplifier characteristics.

7.5 AMPERE

POWER TRANSISTORS
SILICON NPN

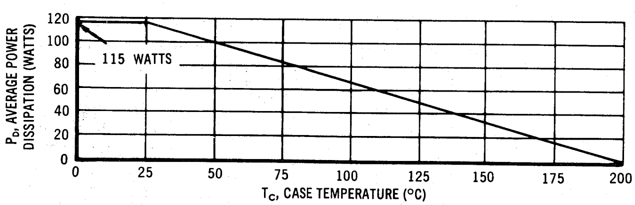
60-80 VOLTS
115 WATTS



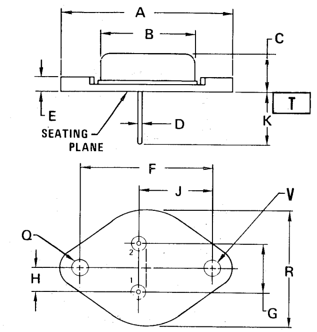
MAXIMUM RATING

Rating	Symbol	2N3447	2N3448	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0	10	Vdc
Collector Current-Continuous	I_C	7.5		Adc
Base Current - Continuous	I_B	4.0		Adc
Total Device Dissipation	P_D	Figure 1, 2	Figure 1, 3	Watts
Operating Junction Temperature Range	T_J	−65 to +200		°C

FIGURE 1 — POWER DERATING CURVE



These transistors are also subject to safe area curves as indicated by Figures 2, 3. Both limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⌖ ∅ 0.25 (0.010) Ⓜ T V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⌖ ∅ 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Emitter-Base Cutoff Current		I_{EBO}				mAdc
(V_{EB} = 6.0 Vdc)	2N3447		—	—	0.25	
(V_{EB} = 10 VDc)	2N3448		—	—	0.25	
Collector-Emitter Cutoff Current		I_{CEX}				mAdc
(V_{CE} = 60 Vdc, V_{BE} = −1.0 Vdc)	2N3447		—	—	0.1	
(V_{CE} = 60 Vdc, V_{BE} = −1.0 Vdc, T_C = 150°C)	2N3447		—	—	1.0	
(V_{CE} = 80 Vdc, V_{BE} = −1.0 Vdc)	2N3448		—	—	0.1	
(V_{CE} = 80 Vdc, V_{BE} = −1.0 Vdc, T_C = 150°C)	2N3448		—	—	1.0	
Collector-Emitter Cutoff Current		I_{CEO}				mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N3447		—	—	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N3448		—	—	1.0	
Collector-Base Breakdown Voltage		$V_{(BR)CBO}$				Vdc
(I_C = 1.0 mAdc, I_E = 0)	2N3447		80	—	—	
	2N3448		100	—	—	
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$				Vdc
(I_C = 100 mAdc, I_B = 0)	2N3447		60	—	—	
	2N3448		80	—	—	
DC Current Gain		h_{FE}				—
(I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)			40	85	—	
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)			40	75	120	
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	—	0.8	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc)		$V_{BE(sat)}$	—	1.0	1.5	Vdc
Base-Emitter Voltage (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)		V_{BE}	—	1.0	1.4	Vdc
Small Signal Current Gain		h_{fe}				—
(V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1.0 kHz)			40	—	200	
(V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 10 MHz)			1.0	1.6	—	
Common Base Output Capacitance (V_{CB} = 10 Vdc, f = 0.1 MHz)		C_{ob}	—	260	400	pF
Switching Times						μs
(V_{CC} = 25 Vdc, R_L = 5.0 ohms, I_C = 5.0 A, I_{B1} = I_{B2} = 0.5 A)						
Delay Time plus Rise Time		$t_d + t_r$	—	0.15	0.35	
Storage Time		t_s	—	0.9	2.0	
Fall Time		t_f	—	0.15	0.35	

3

SAFE OPERATING AREAS

FIGURE 2 — 2N3447

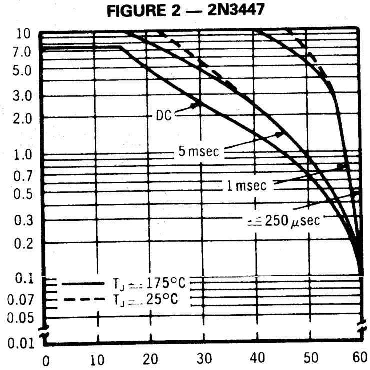
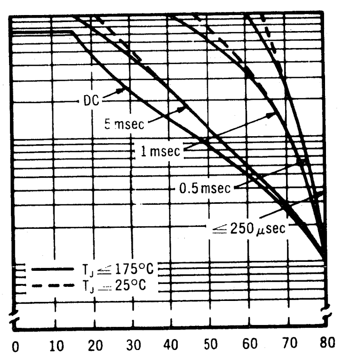


FIGURE 3 — 2N3448



V_{CE}, COLLECTOR-EMITTER VOLTAGE (VOLTS)

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
2N3583 thru 2N3585
2N4240
PNP
2N6420 thru 2N6422

COMPLEMENTARY MEDIUM-POWER HIGH VOLTAGE POWER TRANSISTORS

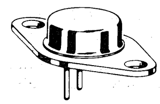
. . . designed for high-speed switching and linear amplifier applications for high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 175 to 300 Vdc @ I_C = 200 mAdc
- Second Breakdown Collector Current —
  $I_{s/b}$ = 350 mAdc @ V_{CE} = 100 Vdc — NPN
  = 150 mAdc @ V_{CE} = 100 Vdc — PNP
- Usable DC Current Gain to 2.0 Adc

1.0 AND 2.0 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

250-500 VOLTS
35 WATTS



*MAXIMUM RATINGS

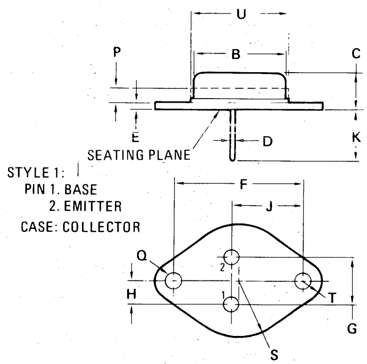
Rating	Symbol	2N3583 2N6420	2N3584 2N6421	2N3585 2N6422	2N4240	Unit
Collector-Emitter Voltage	V_{CEO}	175	250	300	300	Vdc
Collector-Base Voltage	V_{CB}	250	375	500	500	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →				Vdc
Collector Current — Continuous — Peak (1)	I_C	1.0 5.0	← 2.0 → ← 5.0 →			Adc
Base Current	I_B	← 1.0 →				Adc
Total Power Dissipation @ T_C = 25°C, Derate above 25°C	P_D	← 35 → ← 0.2 →				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.0	°C/W

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	NPN	PNP	Symbol	NPN Min	NPN Max	PNP Min	PNP Max	Unit
***OFF CHARACTERISTICS (1)**								
Collector-Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0) NPN	2N3583	2N6420	$V_{CEO(sus)}$	175	—	175	—	Vdc
	2N3584	2N6421		250	—	250	—	
	2N3585	2N6422		300	—	300	—	
(I_C = 50 mAdc, I_B = 0) PNP	2N4240			300	—	300	—	
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	2N3583	2N6420	I_{CEO}	—	10	—	10	mAdc
	2N3584	2N6421		—	5.0	—	5.0	
	2N3585	2N6422		—	5.0	—	5.0	
	2N4240			—	5.0	—	5.0	
Collector Cutoff Current (V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3583	2N6420	I_{CEX}	—	1.0	—	1.0	mAdc
(V_{CE} = 340 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3584	2N6421		—	1.0	—	1.0	
(V_{CE} = 450 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3585	2N6422		—	1.0	—	1.0	
	2N4240			—	2.0	—	2.0	
(V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3583	2N6420		—	3.0	—	3.0	
(V_{CE} = 300 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3584	2N6421		—	3.0	—	3.0	
	2N3585	2N6422		—	3.0	—	3.0	
	2N4240			—	5.0	—	5.0	
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	2N3583	2N6420	I_{EBO}	—	5.0	—	5.0	mAdc
	2N3584	2N6421		—	0.5	—	0.5	
	2N3585	2N6422		—	0.5	—	0.5	
	2N4240			—	0.5	—	0.5	
ON CHARACTERISTICS (1)								
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 10 Vdc)	All	All	h_{FE}	40	—	40	—	—
*(I_C = 0.5 Adc, V_{CE} = 10 Vdc)	2N3583	2N6420		40	200	40	200	
*(I_C = 0.75 Adc, V_{CE} = 2.0 Vdc)	2N4240			10	100	10	100	
(I_C = 0.75 Adc, V_{CE} = 10 Vdc)	2N4240			30	150	30	150	
*(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	2N3584	2N6421		8.0	80	8.0	80	
	2N3585	2N6422		8.0	80	8.0	80	
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)	2N3583*	2N6420		10	—	10	—	
	2N3584	2N6421		25	100	25	100	
	2N3585	2N6422		25	100	25	100	
*Collector-Emitter Saturation Voltage (I_C = 0.75 Adc, I_B = 75 mAdc)	2N4240		$V_{CE(sat)}$	—	1.0	—	1.0	Vdc
(I_C = 1.0 Adc, I_B = 125 mAdc)	2N3583	2N6420		—	5.0	—	5.0	
	2N3584	2N6421		—	0.75	—	0.75	
	2N3585	2N6422		—	0.75	—	0.75	
*Base-Emitter Saturation Voltage (I_C = 0.75 Adc, I_B = 75 mAdc)	2N4240		$V_{BE(sat)}$	—	1.8	—	1.8	Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc)	2N3584	2N6421		—	1.4	—	1.4	
	2N3585	2N6422		—	1.4	—	1.4	
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)	All	All	$V_{BE(on)}$	—	1.4	—	1.4	Vdc

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

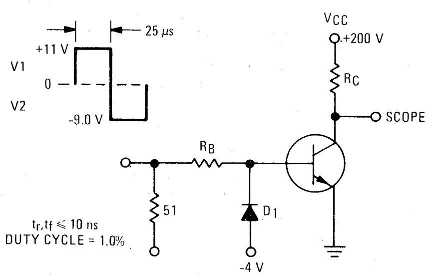
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	NPN	PNP	Symbol	NPN Min	NPN Max	PNP Min	PNP Max	Unit
DYNAMIC CHARACTERISTICS								
*Current Gain — Bandwidth Product[(1)] (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 5.0 MHz)	2N3583 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422	f_T	10 15	— —	10 15	— —	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	All		C_{ob}	—	120	—	120	pF
*Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 30 Vdc, f = 1.0 kHz)	2N3583	2N6420	h_{fe}	25	350	25	350	—
***SWITCHING CHARACTERISTICS**								
Rise Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, R_L = 200 Ohms, I_{B1} = 100 mAdc) (V_{CC} = 200 Vdc, I_C = 0.75 Adc, R_L = 267 Ohms, I_{B1} = 75 mAdc)	2N3584 2N3585 2N4240	2N6421 2N6422	t_r	— —	3.0 0.5	— —	3.0 0.5	μs
Storage Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc) (V_{CC} = 200 Vdc, I_C = 0.75 Adc, I_{B1} = I_{B2} = 75 mAdc)	2N3584 2N3585 2N4240	2N6421 2N6422	t_s	— —	4.0 6.0	— —	4.0 6.0	μs
Fall Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc) (V_{CC} = 200 Vdc, I_C = 0.75 Adc, I_{B1} = I_{B2} = 75 mAdc)	2N3584 2N3585 2N4240	2N6421 2N6422	t_f	— —	3.0 3.0	— —	3.0 3.0	μs
Second Breakdown Collector Current (V_{CE} = 100 Vdc)	All	All	$I_{s/b}$	350	—	150	—	mAdc

*Indicates JEDEC Registered Data
(1) $f_T = |h_{fe}| \bullet f_{test}$.

3

FIGURE 1 — SWITCHING TIME TEST CIRCUIT

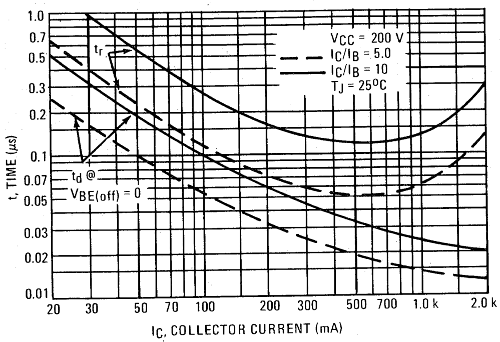


RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS
D1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA
FOR t_d and t_r, D1 IS DISCONNECTED AND V_2 = 0.
FOR PNP TEST CIRCUIT, REVERSE DIODE AND VOLTAGE POLARITIES.

NPN
2N3583 thru 2N3585, 2N4240

PNP
2N6420 thru 2N6422

FIGURE 2 – TURN-ON TIME



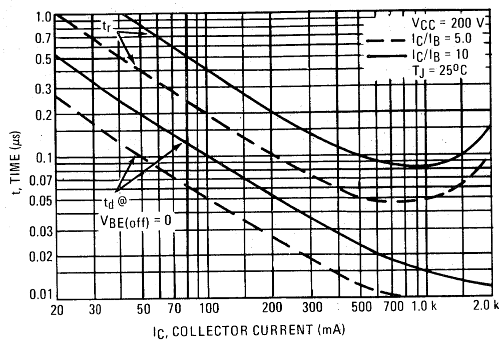
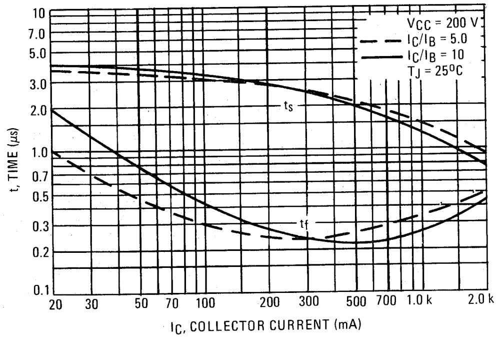


FIGURE 3 – TURN-OFF TIME



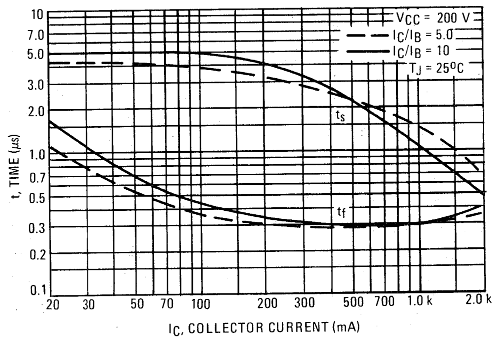


FIGURE 4 – CURRENT-GAIN – BANDWIDTH PRODUCT

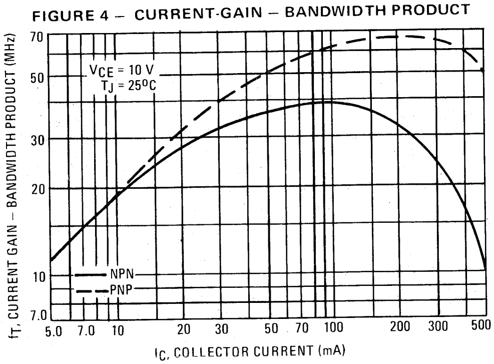


FIGURE 5 – CAPACITANCE

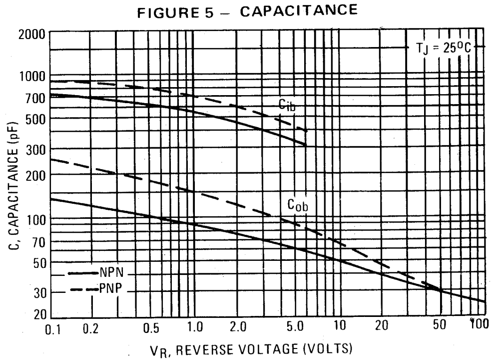
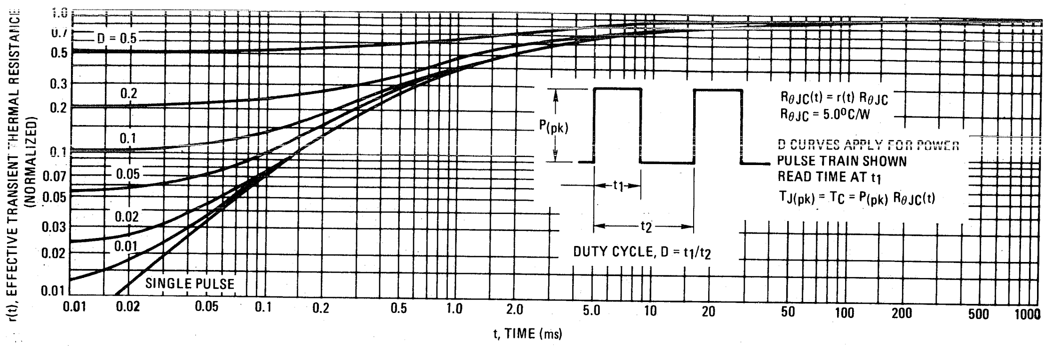


FIGURE 6 — THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 7 — 2N3583 thru 2N3585, 2N4240

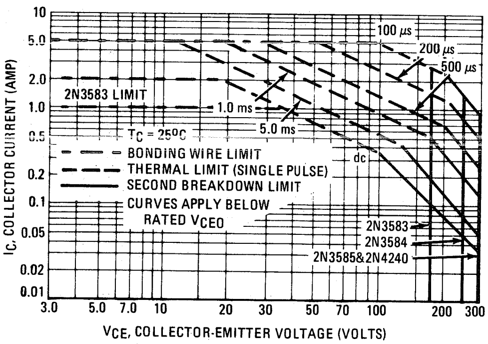
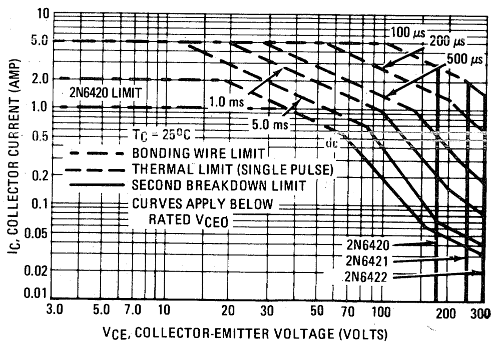
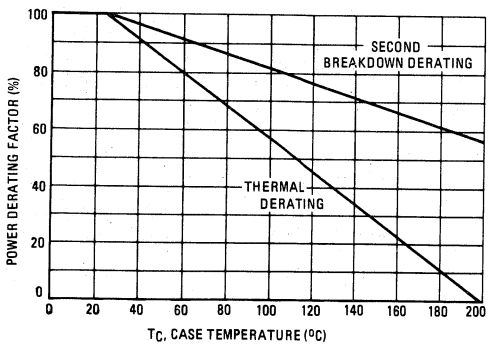


FIGURE 8 — 2N6420 thru 2N6422



3

FIGURE 9 — POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 7 and 8 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 9.

$T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 7 and 8 may be found at any case temperature by using the appropriate curve on Figure 9.

NPN
2N3583 thru 2N3585, 2N4240

PNP
2N6420 thru 2N6422

FIGURE 10 – DC CURRENT GAIN

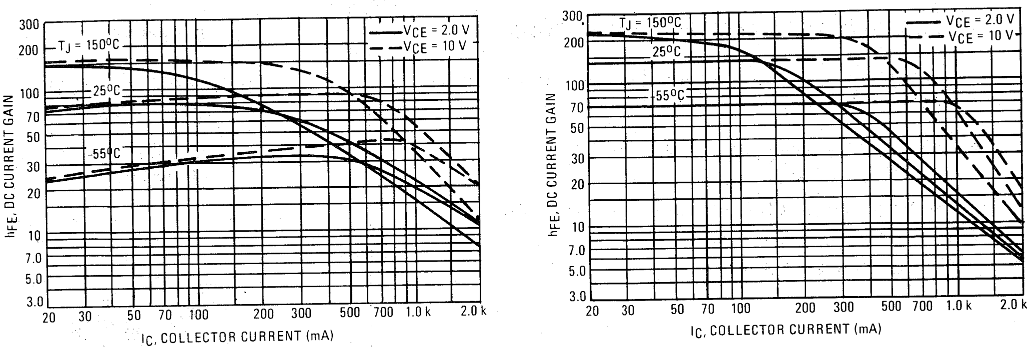


FIGURE 11 – COLLECTOR SATURATION REGION

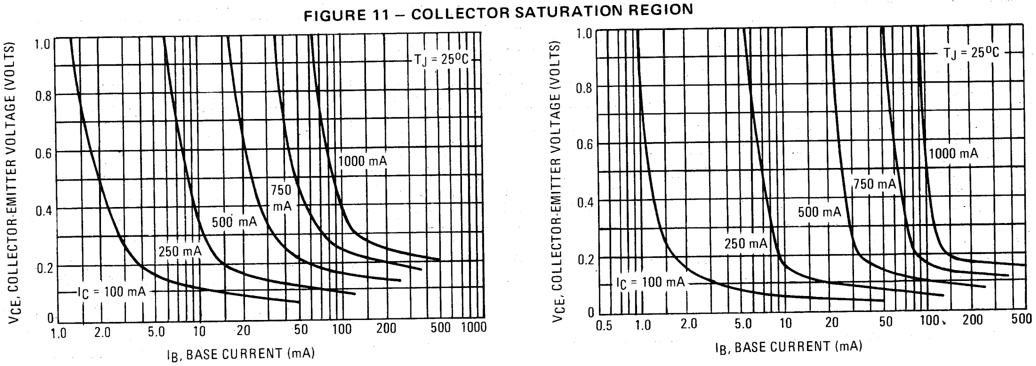
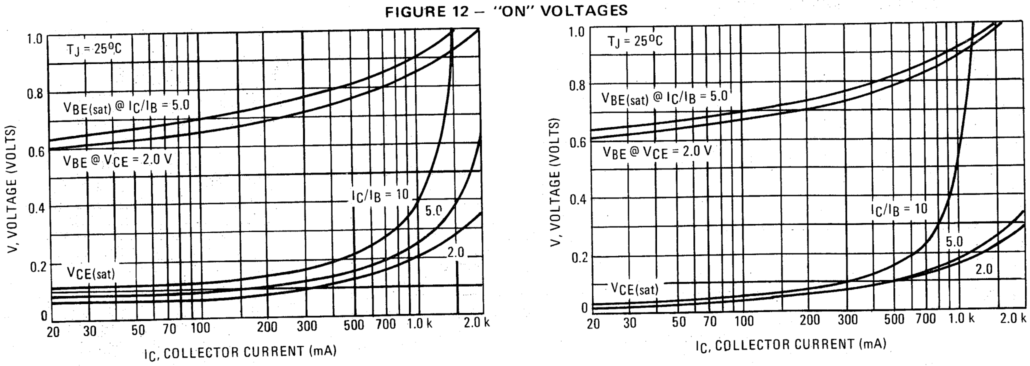


FIGURE 12 – "ON" VOLTAGES



NOTE: DC CURRENT LIMIT FOR 2N3583, 2N6420 is 1.0 Amp.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
2N3714 thru 2N3716

SILICON NPN POWER TRANSISTORS

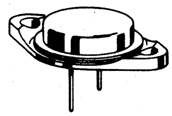
. . . designed for medium-speed switching and amplifier applications. These devices feature:

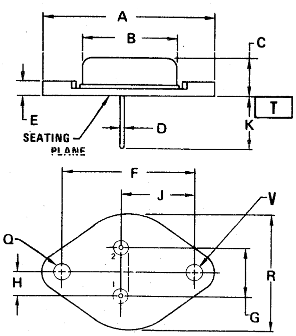
- Total Switching Time at 3 A typically 1.15 μs
- Gain Ranges Specified at 1 A and 3 A
- Low $V_{CE(sat)}$: typically 0.5V at I_C = 5A and I_B = 0.5A
- Excellent Safe Operating Areas
- Complement to 2N3789-92

10 AMPERE

POWER TRANSISTORS
SILICON NPN

60-80 VOLTS
150 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⊕ ∅ 0.25 (0.010) Ⓜ T V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⊕ ∅ 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

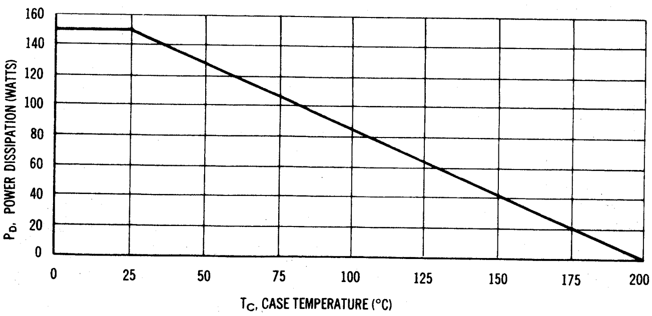
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	2N3715	2N3714 2N3716	Unit
Collector-Base Voltage	V_{CB}	80	100	Volts
Collector-Emitter Voltage	V_{CEO}	60	80	Volts
Emitter-Base Voltage	V_{EB}	7.0	7.0	Volts
Collector Current	I_C	10	10	Amps
Base Current	I_B	4.0	4.0	Amps
Power Dissipation	P_D	150	150	Watts
Thermal Resistance	θ_{JC}	1.17	1.17	°C/W
Operating Junction and Storage Temperature Range	T_J and T_{stg}	-65 to +200		°C

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Limits are indicated by Figures 12, 13. Both limits are applicable and must be observed.

3

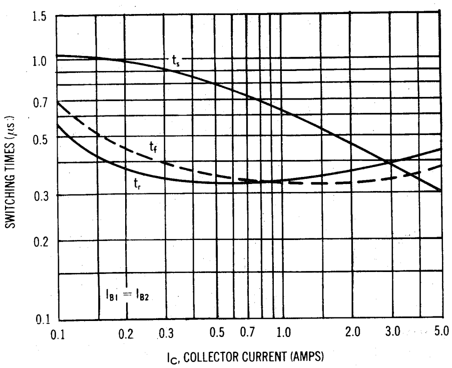
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Emitter-Base Cutoff Current (V_{EB} = 7 Vdc)	All Types	I_{EBO}	—	5	mAdc
Collector-Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc)	2N3715		—	1	
(V_{CE} = 100 Vdc, V_{BE}= -1.5 Vdc)	2N3714, 2N3716		—	1	
(V_{CE} = 60 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3715		—	10	
(V_{CE} =80 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3714, 2N3716		—	10	
Collector-Emitter Sustaining Voltage* (I_C = 200 mAdc, I_B = 0)	2N3715	$V_{CEO(sus)}$*	60	—	Vdc
	2N3714, 2N3716		80	—	
DC Current Gain* (I_C = 1 Adc, V_{CE} = 2 Vdc)	2N3714	h_{FE}*	25	90	—
	2N3715, 2N3716		50	150	
(I_C = 3 Adc, V_{CE} = 2 Vdc)	2N3714		15	—	
	2N3715, 2N3716		30	—	
Collector-Emitter Saturation Voltage* (I_C = 5 Adc, I_B = 0.5 Adc)	2N3714	$V_{CE(sat)}$*	—	1.0	Vdc
	2N3715, 2N3716		—	0.8	
Base-Emitter Saturation Voltage* (I_C = 5 Adc, I_B = 0.5 Adc)	2N3714	$V_{BE(sat)}$*	—	2.0	Vdc
	2N3715, 2N3716		—	1.5	
Base-Emitter Voltage* (I_C = 3 Adc, V_{CE} = 2 Vdc)	All Types	V_{BE}*	—	1.5	Vdc
Small Signal Current Gain (V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1 MHz)	All Types	h_{fe}	4	—	—
Switching Times (Figure 2) (I_C = 5 A, I_{B1} = I_{B2} = 0.5 Adc)			Typ		μs
Rise Time		t_r	0.45		
Storage Time		t_s	0.3		
Fall Time		t_f	0.4		

*Use sweep test to prevent overheating

3

FIGURE 2 — TYPICAL SWITCHING TIMES



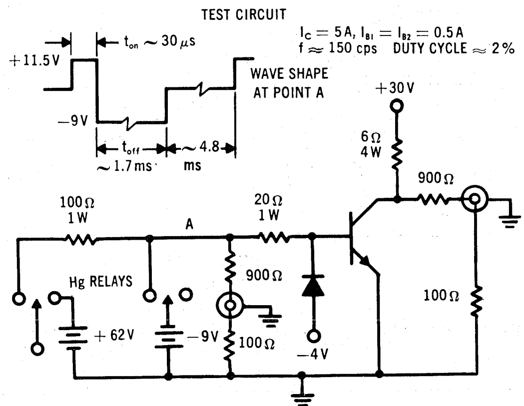


FIGURE 3 – COLLECTOR CURRENT versus BASE CURRENT

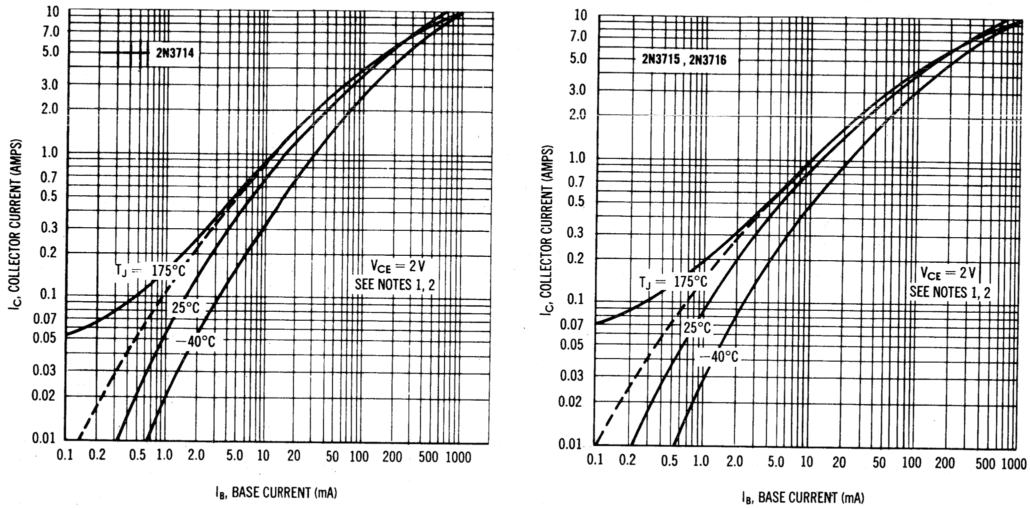


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FIGURE 4 – BASE CURRENT-VOLTAGE VARIATIONS

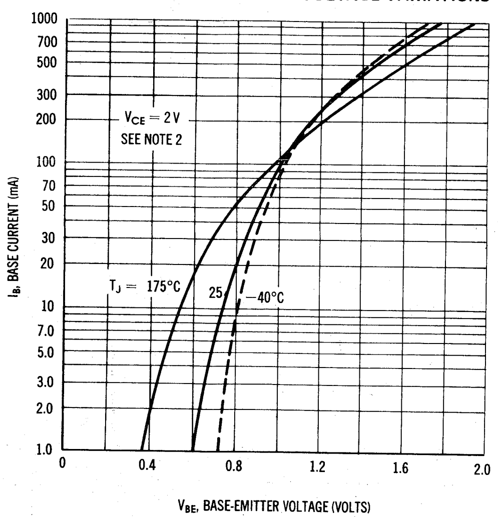
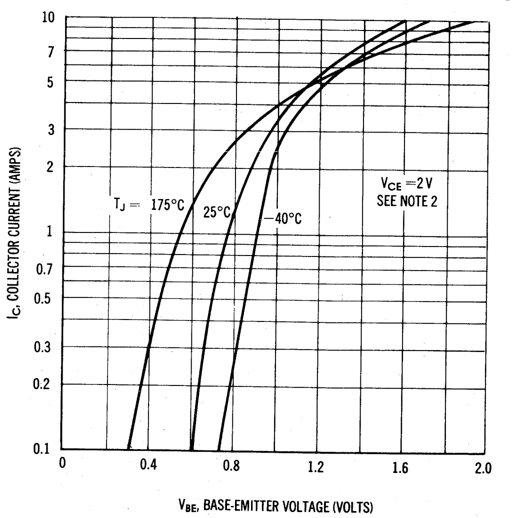


FIGURE 5 – COLLECTOR CURRENT-VOLTAGE VARIATIONS



NOTE 1. Dotted line indicates metered base current plus the I_{CBO} of the transistor at 175°C.

NOTE 2. Pulse test: pulse width ≈ 200 µsec, duty cycle ≈ 1.5%

FIGURE 6 – COLLECTOR-EMITTER SATURATION VOLTAGE VARIATIONS

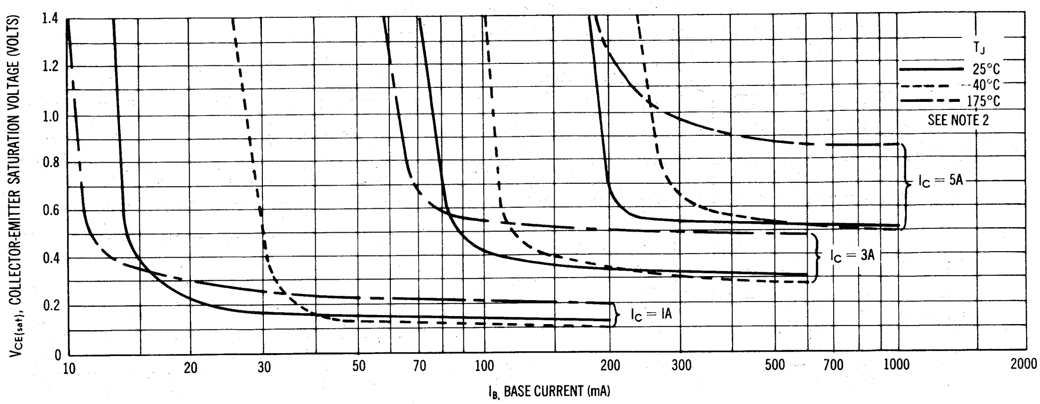


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE VARIATIONS

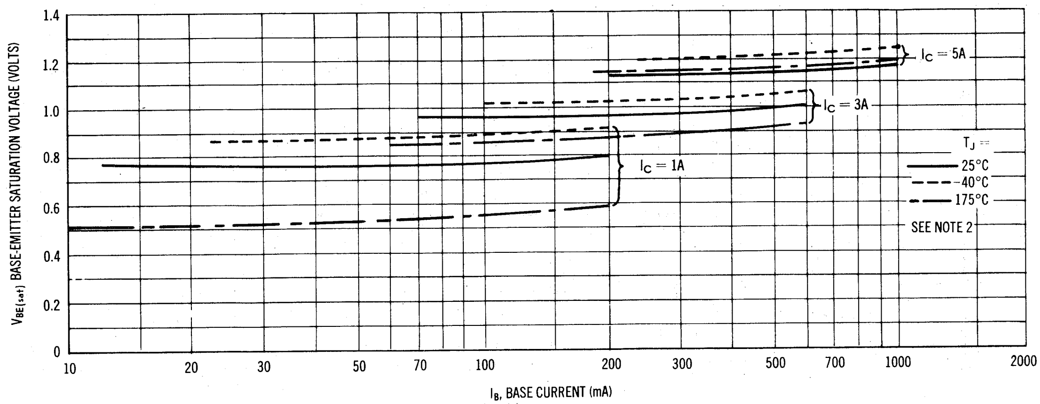


FIGURE 8 – COLLECTOR CURRENT versus BASE-EMITTER VOLTAGE

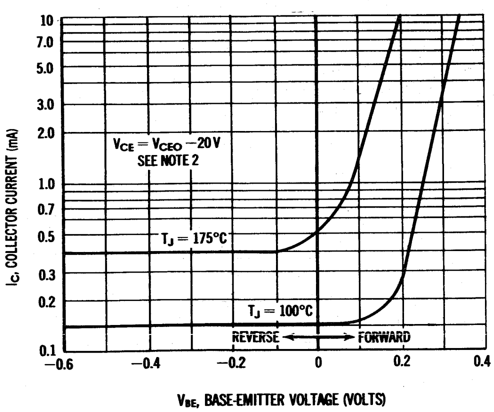


FIGURE 9 – COLLECTOR CURRENT versus BASE-EMITTER RESISTANCE

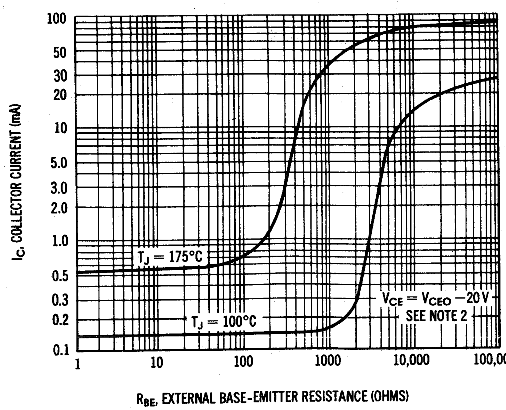


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FIGURE 10 – CURRENT GAIN VARIATIONS

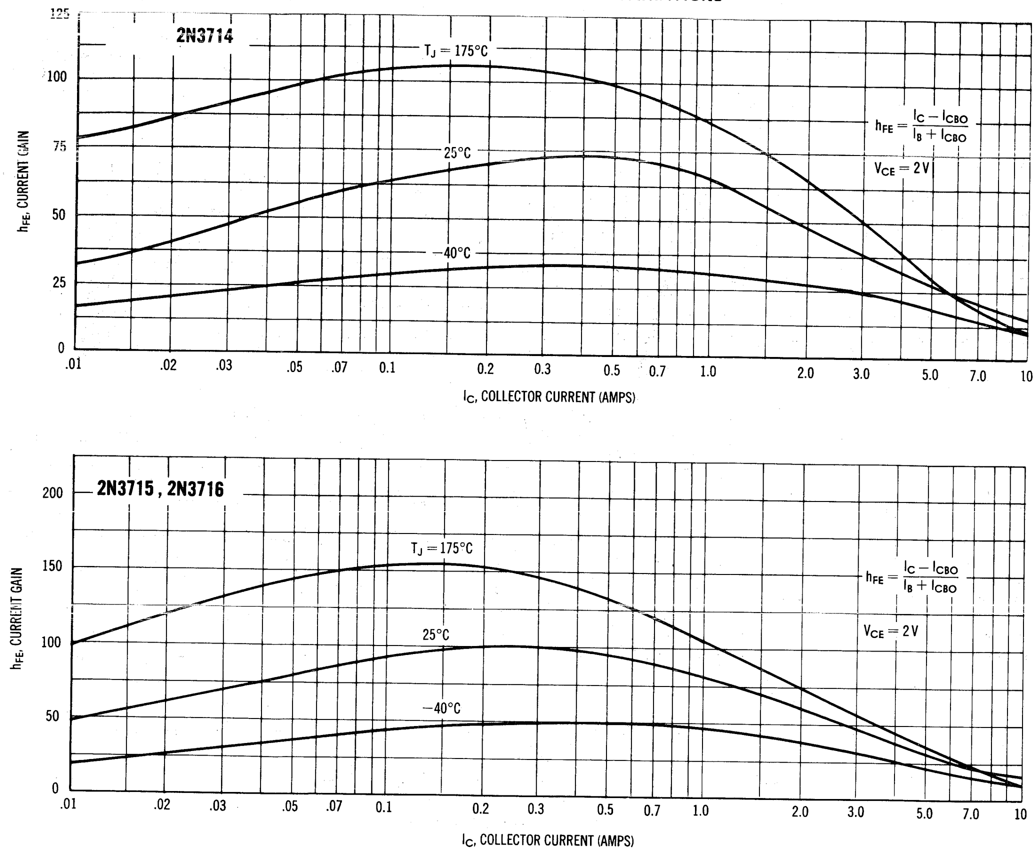

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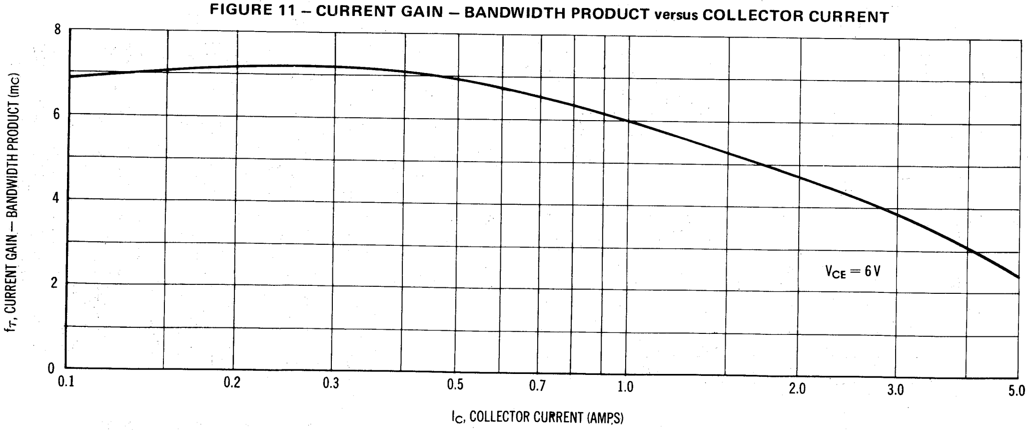
FIGURE 11 – CURRENT GAIN – BANDWIDTH PRODUCT versus COLLECTOR CURRENT



SAFE OPERATING AREAS

FIGURE 12 – 2N3715

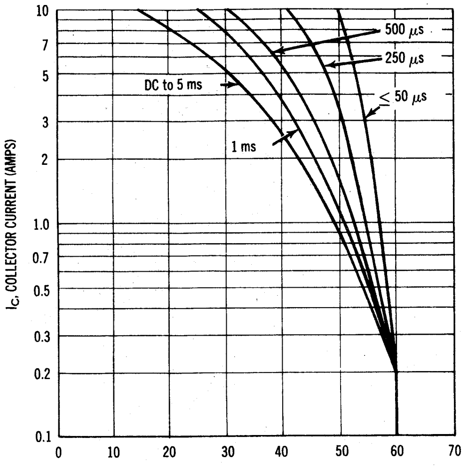
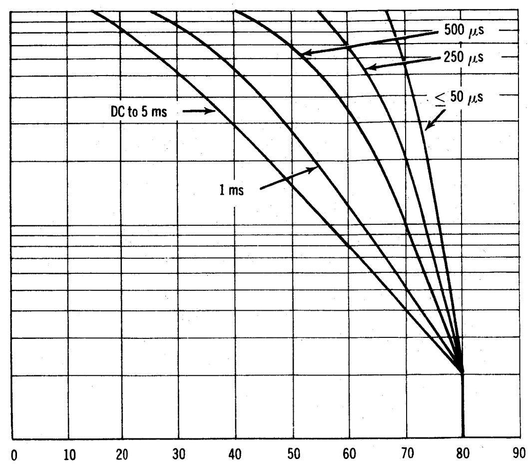


FIGURE 13 – 2N3714, 2N3716



V_{CE}, COLLECTOR-EMITTER VOLTAGE (VOLTS)

The Safe Operating Area Curves indicate I_C — V_{CE} limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

3

2N3719, 2N3720
2N3867, 2N3868
2N6303

SILICON PNP POWER TRANSISTORS

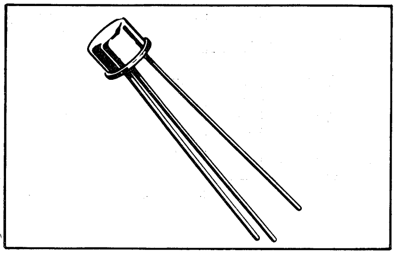
. . . designed for high-speed, medium-current switching and high-frequency amplifier applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc (Min) — 2N3719,2N3867
  = 60 Vdc (Min) — 2N3720,2N3868
  = 80 Vdc (Min) — 2N6303
- DC Current Gain —
  h_{FE} = 25-180 @ I_C = 1.0 Adc — 2N3719,2N3720
  = 40-200 @ I_C = 1.5 Adc — 2N3867
  = 30-150 @ I_C = 1.5 Adc — 2N3868,2N6303
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.75 Vdc @ I_C = 1.0 Adc — 2N3719,2N3720
  = 0.75 Vdc @ I_C = 1.5 Adc — 2N3867,2N3868, 2N6303
- High Current-Gain — Bandwidth Product —
  f_T = 90 MHz (Typ)
- 2N3867 JAN and 2N3868 JAN also Available

3 AMPERE

POWER TRANSISTORS
PNP SILICON

40,60,80 VOLTS
6 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N3719 2N3867	2N3720 2N3868	2N6303	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}		4.0		Vdc
Collector Current — Continuous Peak	I_C		3.0 10		Adc
Base Current	I_B		0.5		Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D		6.0 34.3		Watts mW/°C
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D		1.0 5.71		Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +200		°C

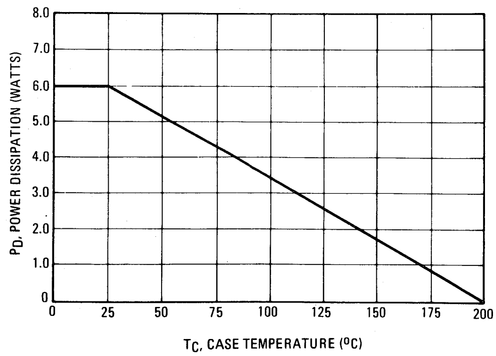
THERMAL CHARACTERISTICS

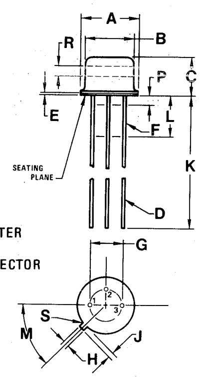
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	29	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	175	°C/W

*Indicates JEDEC Registered Data

3

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.711	0.864	0.028	0.034
J	0.734	1.14	0.029	0.045
K	38.10	44.45	1.500	1.750
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	—		—	
P	–	1.27	–	0.050
R	2.54	–	0.100	–
S	–	0.25	–	0.010

All JEDEC dimensions and notes apply.

CASE 31-03
TO-205AA

*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 20 mAdc, I_B = 0)	2N3867	$V_{CEO(sus)}$	40	–	Vdc
	2N3868		60	–	
	2N6303		80	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	2N3867	$V_{(BR)CBO}$	40	–	Vdc
	2N3868		60	–	
	2N6303		80	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		$V_{(BR)EBO}$	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 2.0 Vdc)		I_{CEX}	–	1.0	μAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0, T_C = 150°C)		I_{CBO}	–	150	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)	2N3867	h_{FE}	50	–	–
	2N3868, 2N6303		35	–	
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N3867		40	200	
	2N3868, 2N6303		30	150	
(I_C = 2.5 Adc, V_{CE} = 3.0 Vdc)	2N3867		25	–	
	2N3868, 2N6303		20	–	
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	2N3867		20	–	
	2N3868, 2N6303				
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)		$V_{CE(sat)}$	–	0.5	Vdc
(I_C = 1.5 Adc, I_B = 150 mAdc)			–	0.75	
(I_C = 2.5 Adc, I_B = 250 mAdc)			–	1.3	
Base-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)		$V_{BE(sat)}$	–	1.0	Vdc
(I_C = 1.5 Adc, I_B = 150 mAdc)			0.9	1.4	
(I_C = 2.5 Adc, I_B = 250 mAdc)			–	2.0	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f_{test} = 20 MHz)		f_T	60	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	120	pF
Input Capacitance (V_{EB} = 3.0 Vdc, I_C = 0, f = 0.1 MHz)		C_{ib}	–	1000	pF
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = 0, I_C = 1.5 Adc, I_{B1} = 150 mAdc)	t_d	–	35	ns
Rise Time		t_r	–	65	ns
Storage Time	(V_{CC} = 30 Vdc, I_C = 1.5 Adc, I_{B1} = I_{B2} = 150 mAdc)	t_s	–	325	ns
Fall Time		t_f	–	75	ns

*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

3

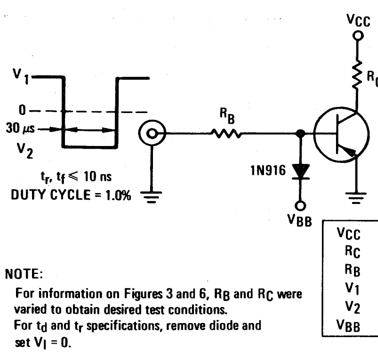
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 20 mAdc, I_B = 0)	2N3719	$V_{CEO(sus)}$	40	–	Vdc
	2N3720		60	–	
Collector Cutoff Current (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 2.0 Vdc)	2N3719	I_{CEX}	–	10	μAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 2.0 Vdc)	2N3720		–	10	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = 150°C)	2N3719		–	1.0	mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = 150°C)	2N3720		–	1.0	
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	2N3719	I_{CBO}	–	10	μAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N3720		–	10	
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 1.5 Vdc)		h_{FE}	20	–	–
(I_C = 1.0 Adc, V_{CE} = 1.5 Vdc)			25	180	
(I_C = 1.0 Adc, V_{CE} = 1.5 Vdc, T_C = −40°C)			15	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc, T_C = −40°C to +100°C)		$V_{CE(sat)}$	–	0.75	Vdc
(I_C = 3.0 Adc, I_B = 300 mAdc, T_C = −40°C to +100°C)			–	1.5	
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc, T_C = −40°C to +100°C)		$V_{BE(sat)}$	–	1.5	Vdc
(I_C = 3.0 Adc, I_B = 300 mAdc, T_C = −40°C to +100°C)			–	2.3	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 30 MHz)		f_T	60	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	120	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 0.1 MHz)		C_{ib}	–	1000	pF
SWITCHING CHARACTERISTICS					
Turn-On Time (V_{CC} = 12 Vdc, $V_{BE(off)}$ = 0, I_C = 1.0 Adc, I_{B1} = 0.1 Adc)		t_{on}	–	100	ns
Turn-Off Time (V_{CC} = 12 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc)		t_{off}	–	400	ns

*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%. (2) $f_T = |h_{fe}| \bullet f_{test}$.

3

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



	2N3719 2N3720	2N3867 2N3868 2N6303
V_{CC}	-12 V	-30 V
R_C	12 Ω	19 Ω
R_B	100 Ω	100 Ω
V_1	+8.0 V	13.6 V
V_2	-11 V	-16.4 V
V_{BB}	≈ 3.0 V	≈ 3.0 V

NOTE:
For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.
For t_d and t_r specifications, remove diode and set V_I = 0.

FIGURE 3 — TURN-ON TIME

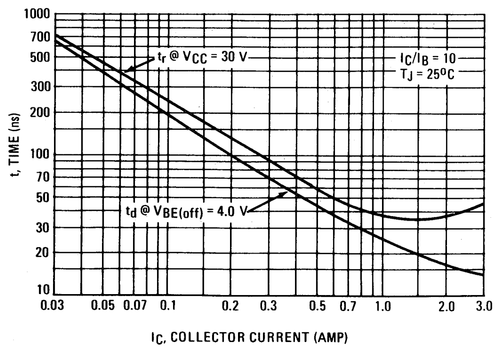


FIGURE 4 – THERMAL RESISTANCE

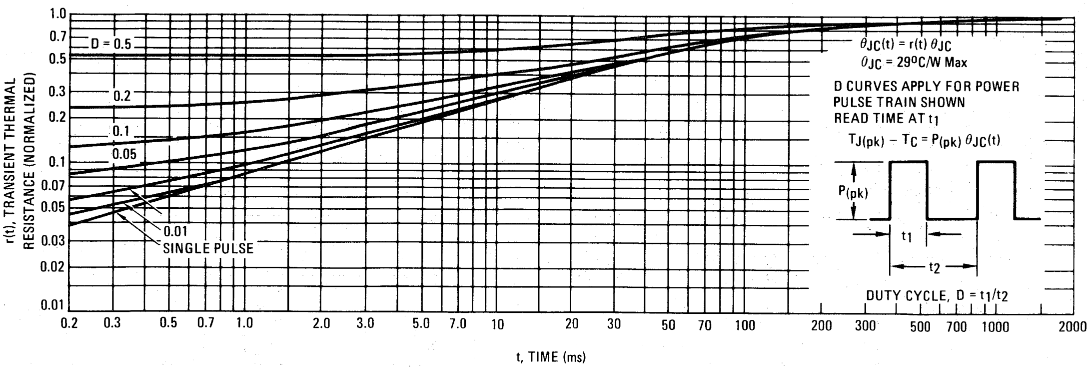
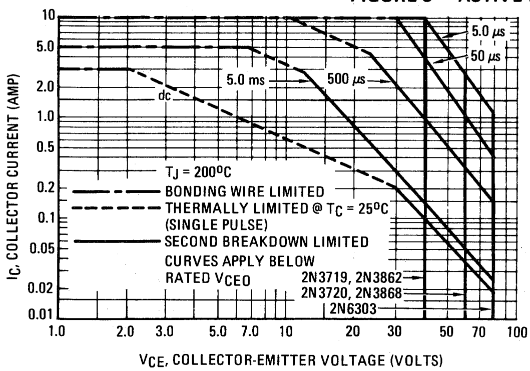


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

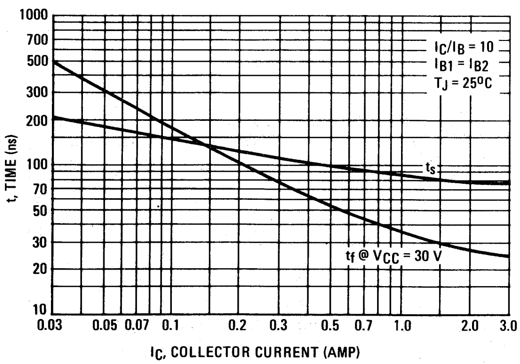
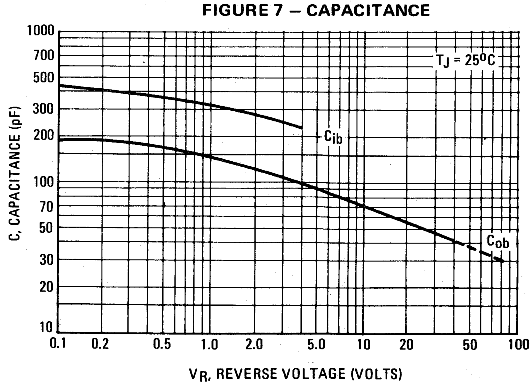


FIGURE 7 – CAPACITANCE



3

FIGURE 8 – DC CURRENT GAIN

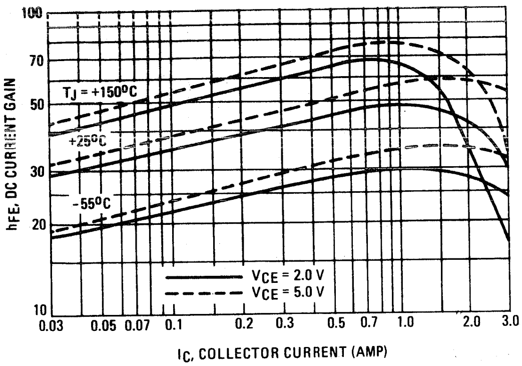


FIGURE 9 – COLLECTOR SATURATION REGION

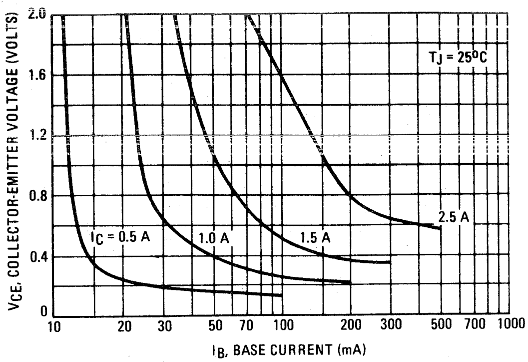


FIGURE 10 – "ON" VOLTAGES

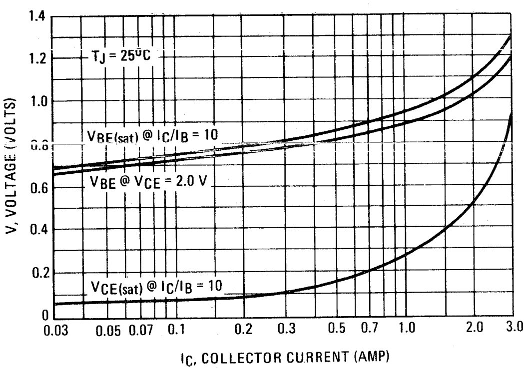


FIGURE 11 – TEMPERATURE COEFFICIENTS

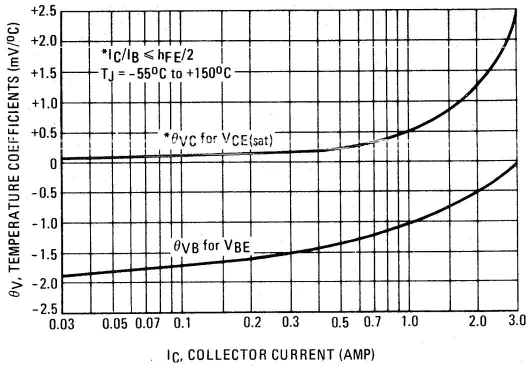


FIGURE 12 – COLLECTOR CUT-OFF REGION

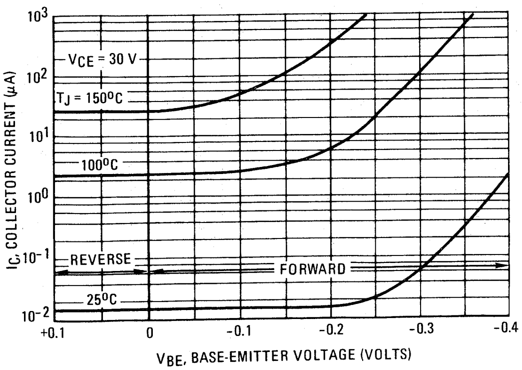
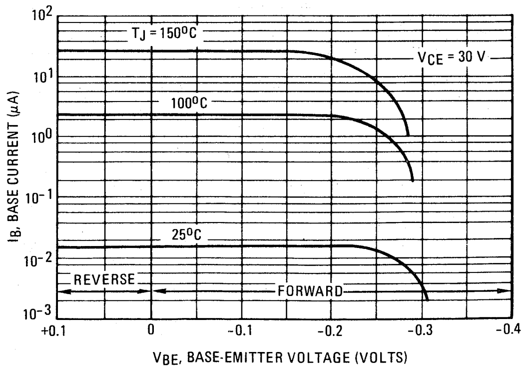


FIGURE 13 – BASE CUT-OFF REGION



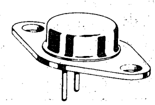
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N3738
2N3739

1.0 AMPERE

POWER TRANSISTORS
NPN SILICON

225, 300 VOLTS
20 WATTS



HIGH VOLTAGE SILICON POWER TRANSISTORS

. . . designed for high-speed switching, linear amplifier applications, high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 225 Vdc @ I_C = 5.0 mAdc (2N3738)
  = 300 Vdc @ I_C = 5.0 mAdc (2N3739)
- DC Current Gain —
  h_{FE} = 40-200 @ I_C = 100 mAdc
- Current-Gain — Bandwidth Product —
  f_T = 10 MHz (Min) @ I_C = 100 mAdc
- $I_{S/b}$ Rated to 2.0 Amperes

*MAXIMUM RATINGS

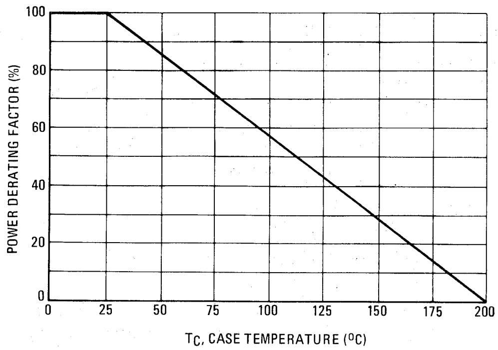
Rating	Symbol	2N3738	2N3739	Unit
Collector-Emitter Voltage	V_{CEO}	225	300	Vdc
Collector-Base Voltage	V_{CB}	250	325	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak	I_C	1.0 2.0		Adc
Base Current — Continuous — Peak	I_B	0.50 1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.133		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

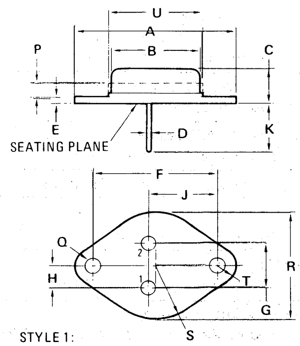
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.5	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

3

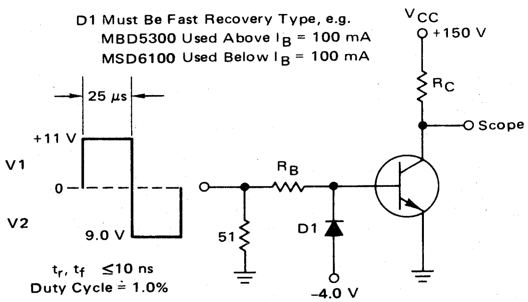
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 5.0 mAdc, I_B = 0)	2N3738		225	–	
	2N3739		300	–	
Collector-Emitter Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 125 Vdc, I_B = 0)	2N3738		–	0.25	
(V_{CE} = 200 Vdc, I_B = 0)	2N3739		–	0.25	
Collector-Base Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 250 Vdc, I_E = 0)	2N3738		–	0.1	
(V_{CB} = 325 Vdc, I_E = 0)	2N3739		–	0.1	
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3738		–	0.5	
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3739		–	0.5	
(V_{CE} = 125 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N3738		–	1.0	
(V_{CE} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N3739		–	1.0	
Emitter-Base Cutoff Current		I_{EBO}			mAdc
(V_{EB} = 6.0 Vdc)			–	0.1	
***ON CHARACTERISTICS**					
DC Current Gain (1)		h_{FE}			–
(I_C = 50 mAdc, V_{CE} = 10 Vdc)			30	–	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)			40	200	
(I_C = 250 mAdc, V_{CE} = 10 Vdc)			25	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 250 mAdc, I_B = 25 mAdc)			–	2.5	
Base-Emitter "ON" Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 100 mAdc, V_{CE} = 10 Vdc)			–	1.0	
SMALL SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (2)		f_T			MHz
(I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)			10	–	
*Output Capacitance		C_{ob}			pF
(V_{CB} = 100 Vdc, I_E = 0, f = 100 kHz)			–	20	
*Small-Signal Current Gain		h_{fe}			–
(I_C = 100 mAdc, V_{CE} = 20 Vdc, f = 1.0 kHz)			35	–	

3

*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.
(2) $f_T = |h_{fe}| \bullet$ frequency

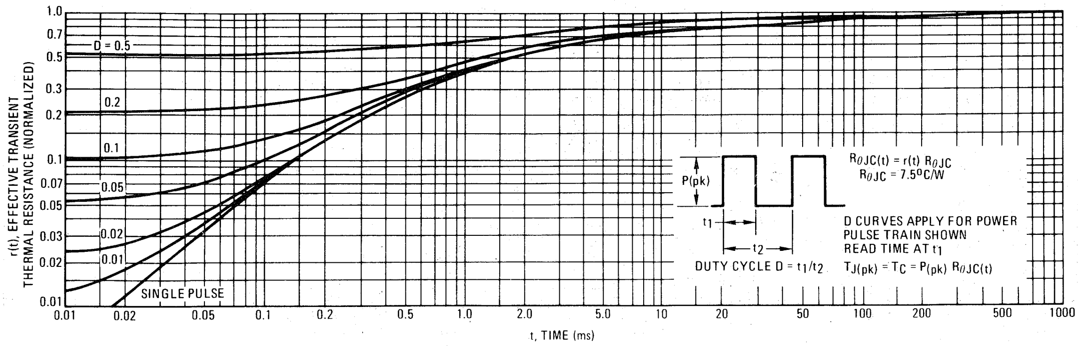
FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



R_B and R_C Varied to Obtain Desired Current Levels

For t_d and t_r, D1 is disconnected and V2 = 0
For PNP test circuit, reverse diode and voltage polarities.

FIGURE 3 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 4 – 2N3738, 2N3739

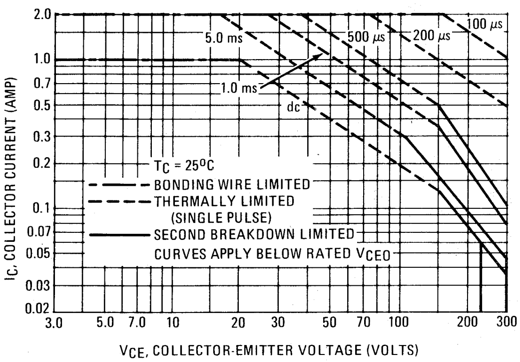
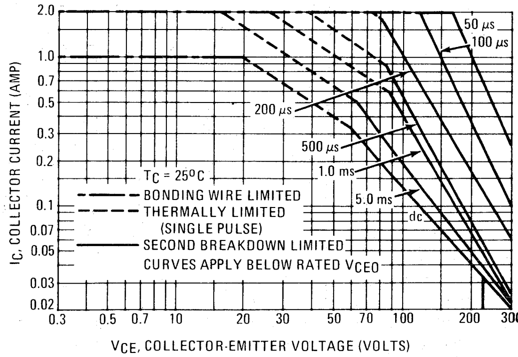


FIGURE 5 — 2N6425



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 4 and 5 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 175^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 4 and 5 may be found at any case temperature by using the appropriate curve on Figure 1.

2N3738, 2N3739

FIGURE 6 – DC CURRENT GAIN

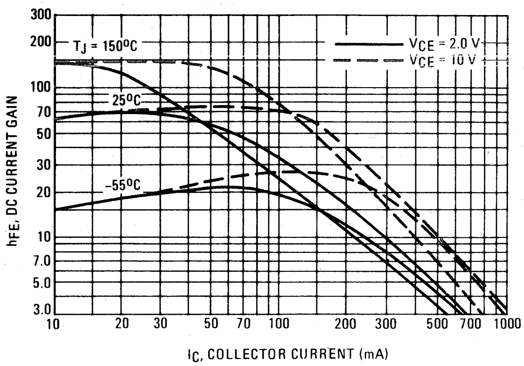


FIGURE 7 – COLLECTOR SATURATION REGION

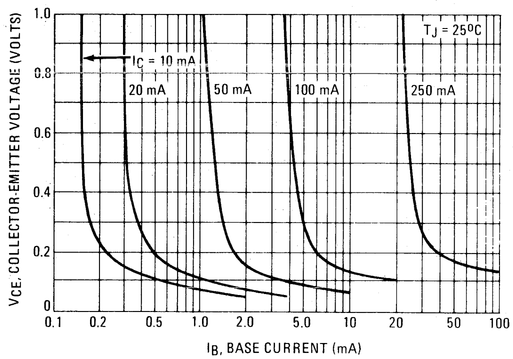
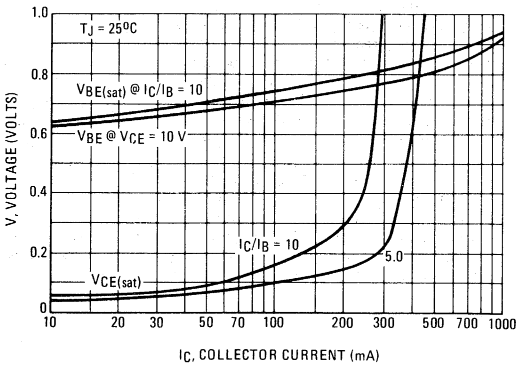


FIGURE 8 – "ON" VOLTAGE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N3740
2N3741,A

MEDIUM-POWER PNP TRANSISTORS

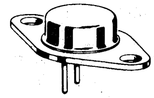
. . . ideal for use as drivers, switches and medium-power amplifier applications. These devices feature:

- Low Saturation Voltage – 0.6 $V_{CE(sat)}$ @ I_C = 1.0 Amp
- High Gain Characteristics – h_{FE}@ I_C = 250 mA: 30–100
- Excellent Safe Area Limits (See Figure 2)
- Low Collector Cutoff Current –
  100 nA (Max) 2N3740, 2N3741A
- Complementary to NPN 2N3766 (2N3740) and 2N3767 (2N3741)

POWER TRANSISTORS

PNP SILICON

60–80 VOLTS
25 WATTS

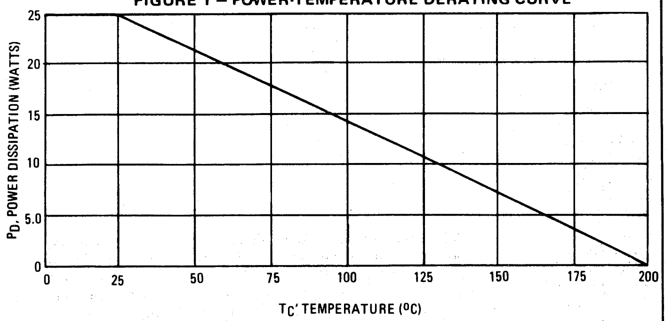


*MAXIMUM RATINGS

Rating	Symbol	2N3740	2N3741 2N3741A	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	7.0	7.0	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Collector Current – Continuous – Peak (Note 1)	I_C	4.0 10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.143		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

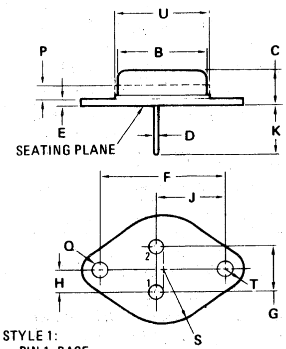
Note 1: See Figure 2

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2.
Both limits are applicable and must be observed.

*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

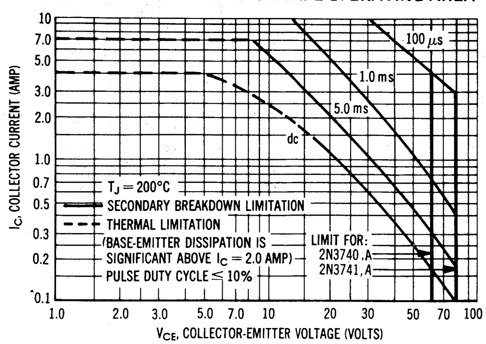
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ①		$V_{CEO(sus)}$ ①			Vdc
(I_C = 100 mAdc, I_B = 0)	2N3740,		60	–	
	2N3741, 2N3741A		80	–	
Emitter Base Cutoff Current		I_{EBO}			
(V_{EB} = 7.0 Vdc)	2N3740, 2N3741		–	0.5	mAdc
	2N3741A			100	nAdc
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3740		–	100	μAdc
			–	100	nAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3741		–	100	μAdc
	2N3741A		–	100	nAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3740		–	1.0	mAdc
			–	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3741		–	1.0	mAdc
	2N3741A		–	0.5	
Collector-Emitter Cutoff Current		I_{CEO}			
(V_{CE} = 40 Vdc, I_B = 0)	2N3740		–	1.0	mAdc
			–	1.0	μAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N3741		–	1.0	mAdc
	2N3741A		–	1.0	μAdc
Collector Base Cutoff Current		I_{CBO}			
(V_{CB} = 60 Vdc, I_E = 0)	2N3740		–	100	μAdc
			–	100	nAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N3741		–	100	μAdc
	2N3741A		–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE} ①			–
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			40	–	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			30	100	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			20	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 125 mAdc)		$V_{CE(sat)}$ ①	–	0.6	Vdc
Base-Emitter Voltage (I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		V_{BE} ①	–	1.0	Vdc
TRANSIENT CHARACTERISTICS					
Current-Gain—Bandwidth Product		f_T			MHz
(I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)			3.0	–	
			4.0†	–	
Common Base Output Capacitance (V_{CB} = 10 Vdc, I_C = 0, f = 100 kHz)		C_{ob}	–	100	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

*Indicates JEDEC Registered Data.

†Motorola guarantees this value in addition to the JEDEC registered data shown.

① Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

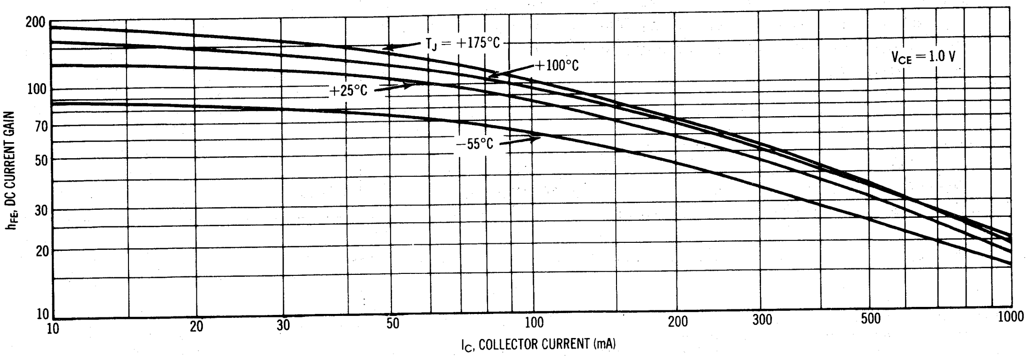
FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

3

FIGURE 3 – CURRENT GAIN



SATURATION REGION CHARACTERISTICS

FIGURE 4 – COLLECTOR SATURATION REGION

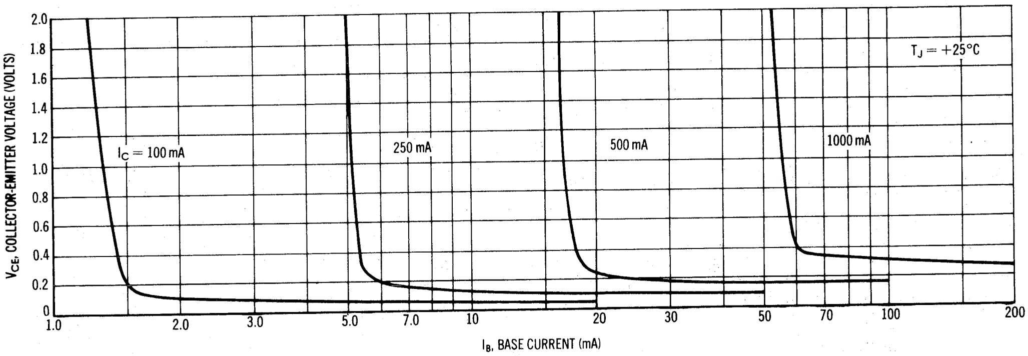


FIGURE 5 – "ON" VOLTAGES

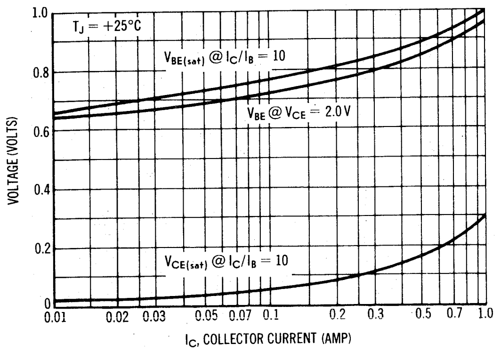
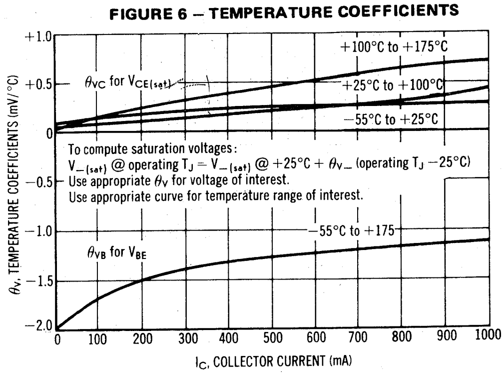


FIGURE 6 – TEMPERATURE COEFFICIENTS



3

2N3766
2N3767

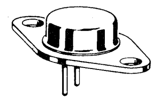
MEDIUM-POWER NPN SILICON TRANSISTORS

. . . for use in driver circuits, switching, and medium-power-amplifiers applications. These high performance devices feature:

- Low Saturation Voltage — 1.0 $V_{CE(sat)}$ @ I_C = 500 mA
- High Gain Characteristics — h_{FE} = 40–160 @ I_C = 500 mA
- Packaged in the Compact, High-Efficiency TO-213AA Package
- Complementary to PNP 2N3740 (2N3766) and 2N3741 (2N3767)

4 AMPERE POWER TRANSISTORS

NPN SILICON
60-80 VOLTS
20 WATTS



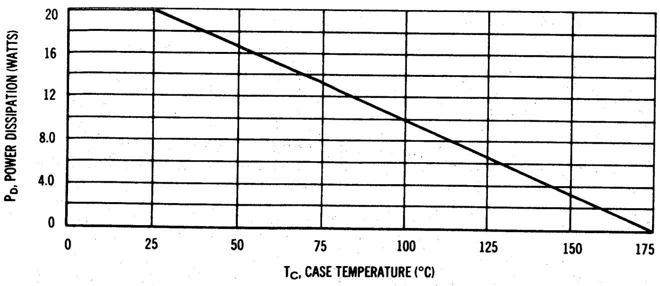
MAXIMUM RATINGS

Rating	Symbol	2N3766	2N3767	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.133		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

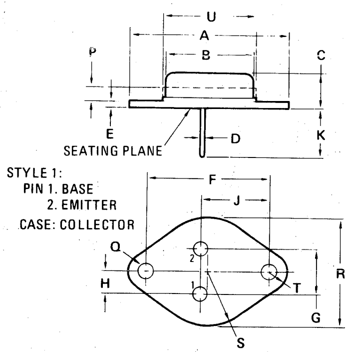
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	7.5	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2. Both limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

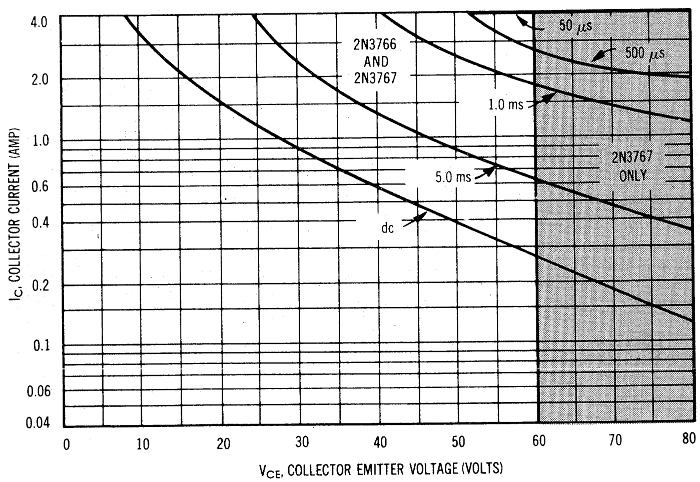
CASE 80-02
TO-213AA

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Voltage [1] (I_C = 100 mAdc, I_B = 0)	2N3766 2N3767		$V_{(BR)CEO}$	60 80	— —	Vdc
Emitter-Base Cutoff Current (V_{EB} = 6.0 Vdc)			I_{EBO}	—	0.75	mAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{BE} = 1.5 Vdc) (V_{CE} = 100 Vdc, V_{BE} = 1.5 Vdc) (V_{CE} = 50 Vdc, V_{BE} = 1.5 Vdc, T_C = 150°C) (V_{CE} = 70 Vdc, V_{BE} = 1.5 Vdc, T_C = 150°C)	2N3766 2N3767 2N3766 2N3767		I_{CEX}	— — — —	0.1 0.1 1.0 1.0	mAdc
Collector-Emitter Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	2N3766 2N3767		I_{CEO}	— —	0.7 0.7	mAdc
Collector-Base Cutoff Current (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	2N3766 2N3767		I_{CBO}	— —	0.1 0.1	mAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc) (I_C = 500 mAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 10 Vdc)			h_{FE}	30 40 20	— 160 —	—
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc) (I_C = 500 mAdc, I_B = 50 mAdc)			$V_{CE(sat)}$	— —	2.5 1.0	Vdc
Base-Emitter Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)			V_{BE}	—	1.5	Vdc
TRANSIENT CHARACTERISTICS						
Current-Gain - Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)			f_T	10	—	MHz
Common-Base Output Capacitance (V_{CB} = 10 Vdc, I_C = 0 Adc, f = 100 kHz)			C_{ob}	—	50	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)			h_{fe}	40	—	—

(1) Pulse Test: Pulse Width ≤300μs, Duty Cycle ≤2.0%.

FIGURE 2 – ACTIVE REGION SAFE AREAS



The Safe Operating Area Curves indicate I_C-V_{CE} limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Case temperature and duty cycle of the excursions make no significant change in these safe areas.) The load line may exceed the BV_{CEO} voltage limit only if the collector current has been reduced to 20 mA or less before or at the BV_{CES} limit; then and only then may the load line be extended to the absolute maximum voltage rating of BV_{CBO}. To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

LARGE SIGNAL CHARACTERISTICS

FIGURE 3 — TRANSCONDUCTANCE

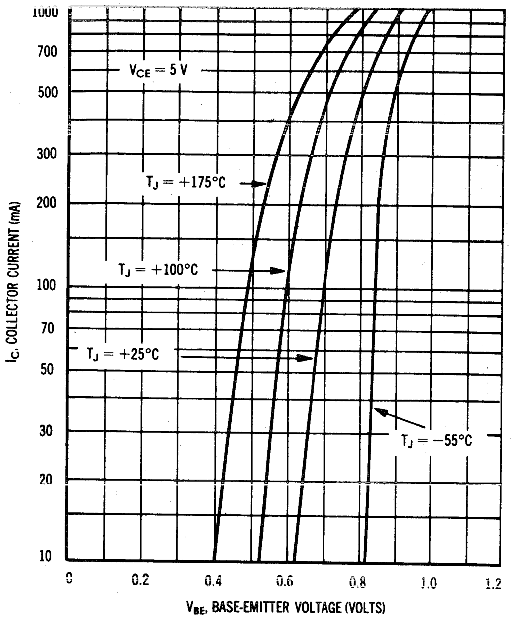
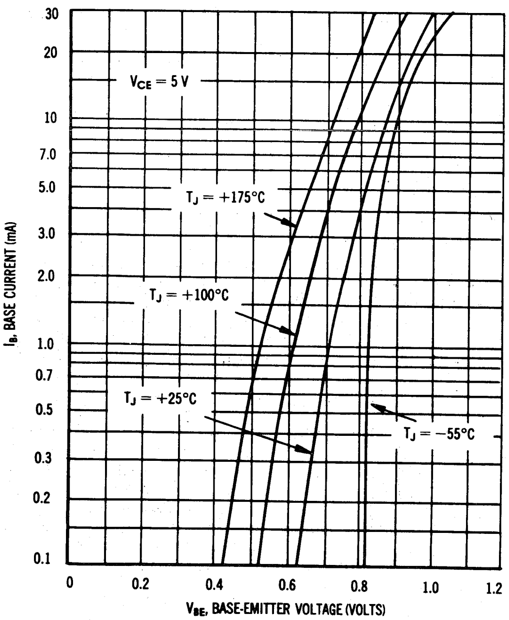


FIGURE 5 — INPUT ADMITTANCE



CUT-OFF CHARACTERISTICS

FIGURE 4 — TRANSCONDUCTANCE

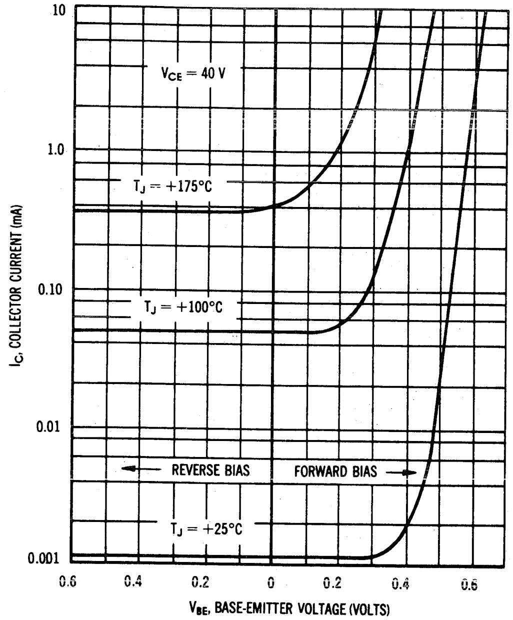


FIGURE 6 — EFFECT OF BASE-EMITTER RESISTANCE

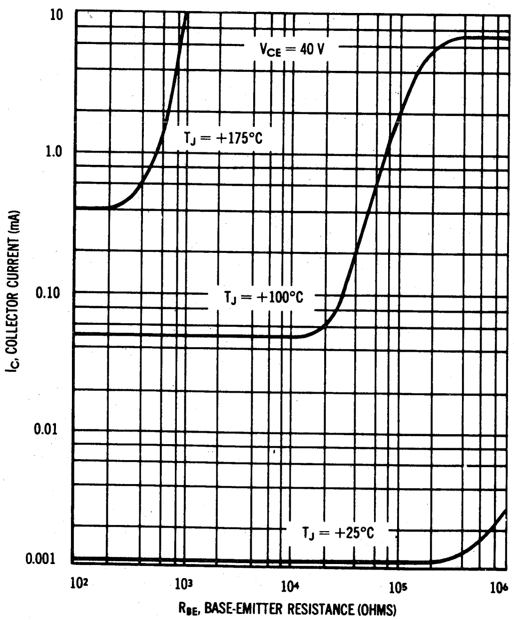


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FIGURE 7 – CURRENT GAIN

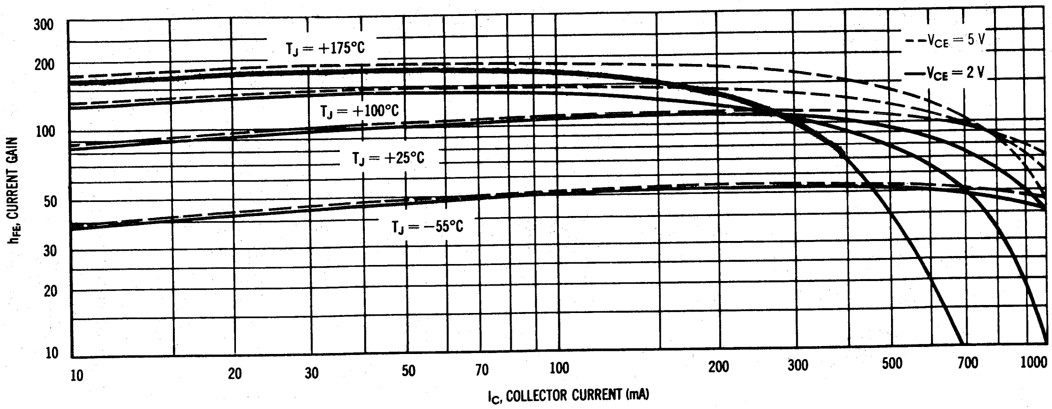


FIGURE 8 – COLLECTOR SATURATION REGION

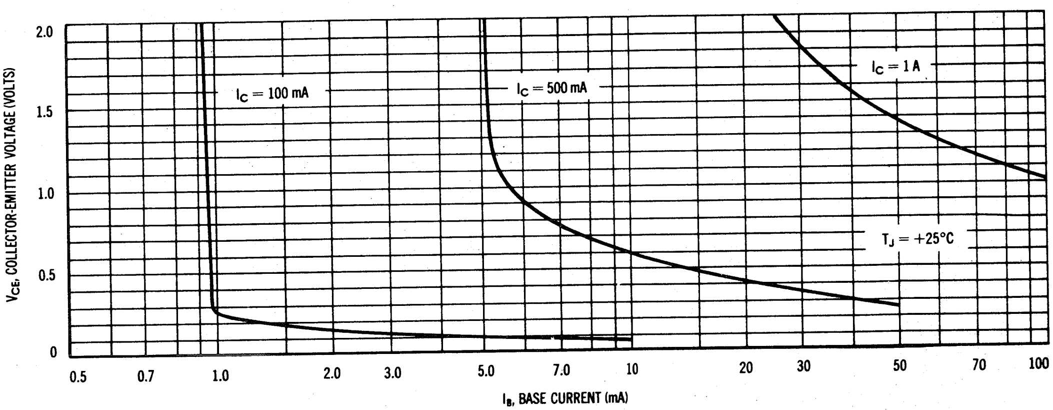


FIGURE 9 – "ON" VOLTAGES

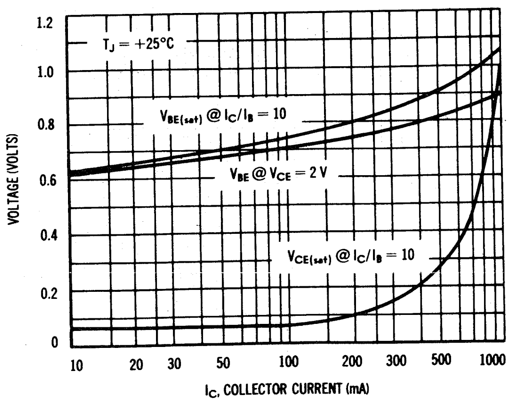
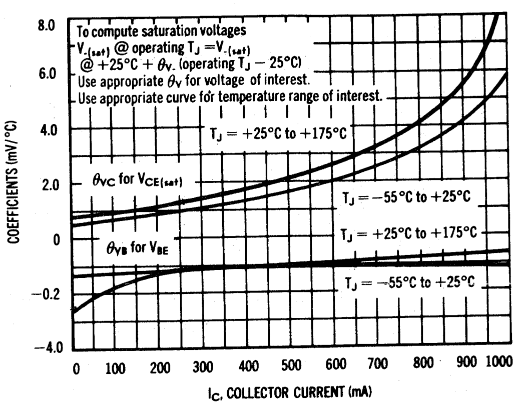


FIGURE 10 – TEMPERATURE COEFFICIENTS



3

2N3771
2N3772

HIGH POWER NPN SILICON POWER TRANSISTORS

. . . designed for linear amplifiers, series pass regulators, and inductive switching applications.

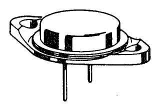
- Forward Biased Second Breakdown Current Capability

  $I_{S/b}$ = 3.75 Adc @ V_{CE} = 40 Vdc – 2N3771
  = 2.5 Adc @ V_{CE} = 60 Vdc – 2N3772

20 and 30 AMPERE

POWER TRANSISTORS
NPN SILICON

40 and 60 VOLTS
150 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N3771	2N3772	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Emitter Voltage	V_{CEX}	50	80	Vdc
Collector-Base Voltage	V_{CB}	50	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0	7.0	Vdc
Collector Current – Continuous Peak	I_C	**30** 30	**20** 30	Adc
Base Current – Continuous Peak	I_B	7.5 15	5.0 15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

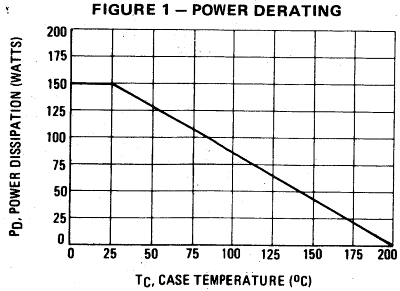
THERMAL CHARACTERISTICS

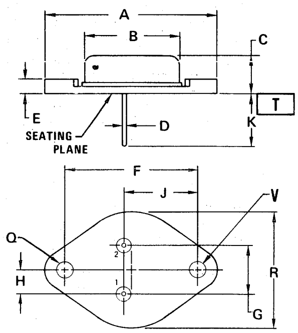
Characteristic	Symbol	2N3771, 2N3772	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data

3

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 3:
PIN 1. ANODE
2. CATHODE

NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⌖ ϕ 0.25 (0.010) Ⓜ T V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ ϕ 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (1)	2N3771	$V_{CEO(sus)}$	40	–	Vdc
(I_C = 0.2 Adc, I_B = 0)	2N3772		60	–	
Collector-Emitter Sustaining Voltage	2N3771	$V_{CEX(sus)}$	50	–	Vdc
(I_C = 0.2 Adc, $V_{EB(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	2N3772		80	–	
Collector-Emitter Sustaining Voltage	2N3771	$V_{CER(sus)}$	45	–	Vdc
(I_C = 0.2 Adc, R_{BE} = 100 Ohms)	2N3772		70	–	
*Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N3771		–	10	
(V_{CE} = 50 Vdc, I_B = 0)	2N3772		–	10	
(V_{CE} = 25 Vdc, I_B = 0)					
*Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3771		–	2.0	
(V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3772		–	5.0	
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6257		–	4.0	
(V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3771		–	10	
	2N3772		–	10	
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)					
*Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 50 Vdc, I_E = 0)	2N3771		–	2.0	
(V_{CB} = 100 Vdc, I_E = 0)	2N3772		–	5.0	
*Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)	2N3771		–	5.0	
(V_{BE} = 7.0 Vdc, I_C = 0)	2N3772		–	5.0	
***ON CHARACTERISTICS**					
DC Current Gain (1)		h_{FE}			–
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)	2N3771		15	60	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3772		15	60	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)					
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N3771		5.0	–	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N3772		5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 1.5 Adc)	2N3771		–	2.0	
(I_C = 10 Adc, I_B = 1.0 Adc)	2N3772		–	1.4	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N3771		–	4.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N3772		–	4.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)	2N3771		–	2.7	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3772		–	2.2	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)					
***DYNAMIC CHARACTERISTICS**					
Current-Gain—Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 50 kHz)		f_T	0.2	–	MHz
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	40	–	–
SECOND BREAKDOWN					
Second Breakdown Energy with Base Forward Biased t = 1.0 s (non-repetitive)		$I_{S/b}$			Adc
(V_{CE} = 40 Vdc)	2N3771		3.75	–	
(V_{CE} = 60 Vdc)	2N3772		2.5	–	

*Indicates JEDEC Registered Data

(1) Pulse Test: 300 μs, Rep. Rate 60 cps.

3

FIGURE 2 – THERMAL RESPONSE – 2N3771, 2N3772

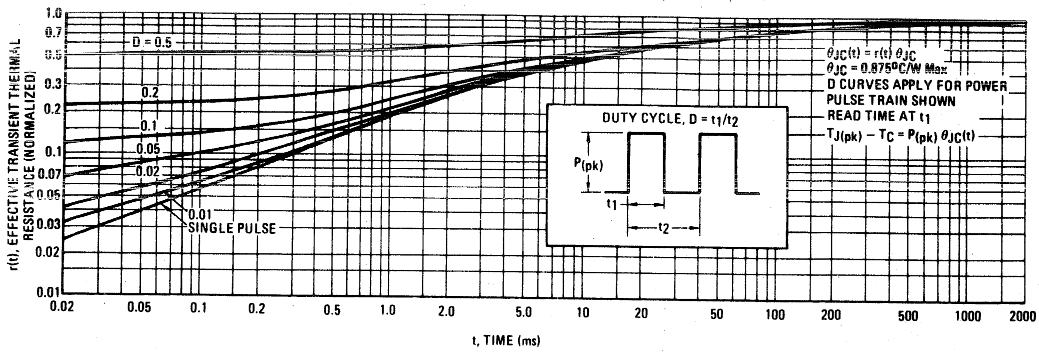
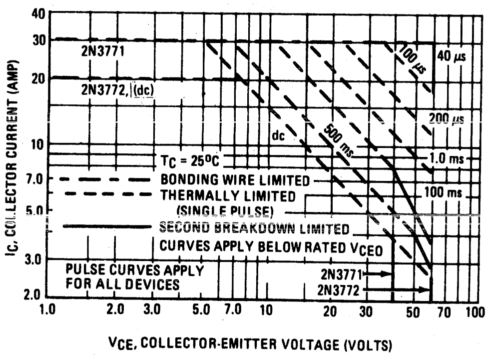


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA – 2N3771, 2N3772

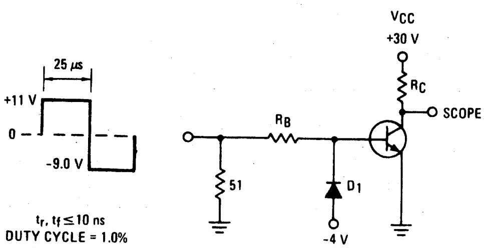


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based upon JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3, $T_{J(pk)}$ will be found to be less than $T_{J(max)}$ for pulse widths of 1 ms and less. When using Motorola transistors, it is permissible to increase the pulse power limits until limited by $T_{J(max)}$.

3

FIGURE 4 – SWITCHING TIME TEST CIRCUIT



R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS.

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

FIGURE 5 – TURN-ON TIME

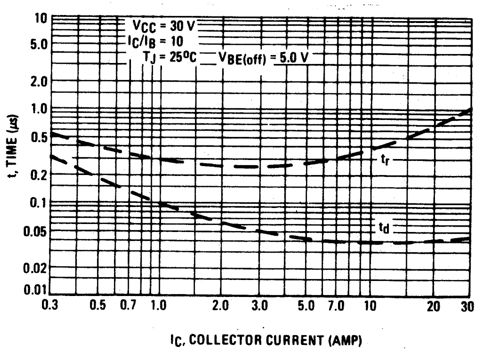


FIGURE 6 — TURN-OFF TIME

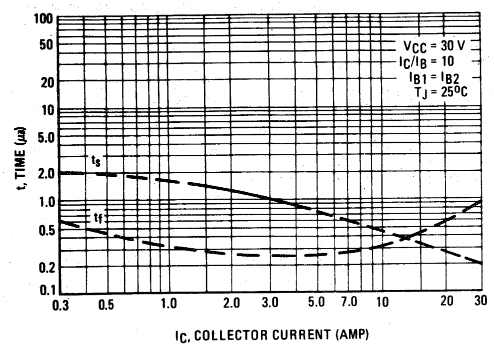


FIGURE 7 — CAPACITANCE

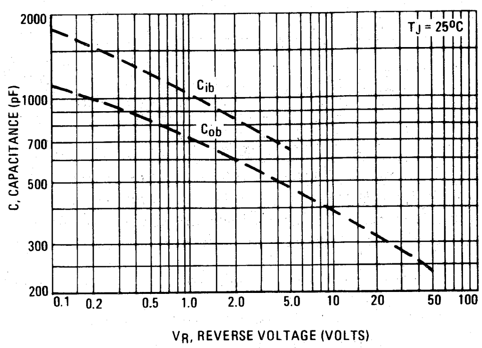


FIGURE 8 — DC CURRENT GAIN

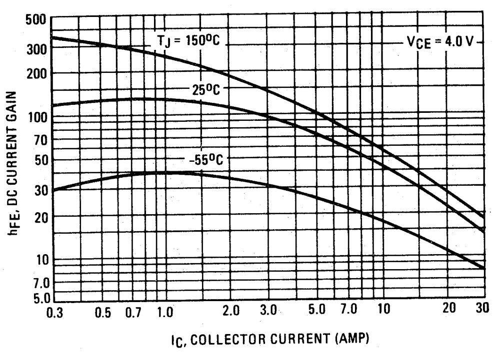
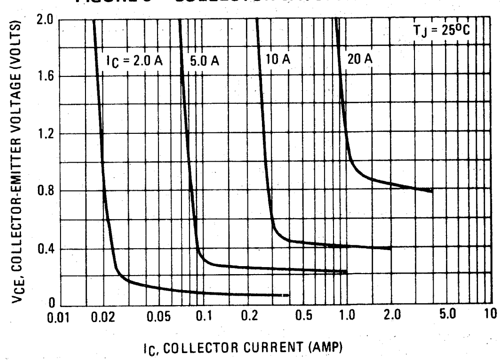


FIGURE 9 — COLLECTOR SATURATION REGION



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
2N3773
PNP
2N6609

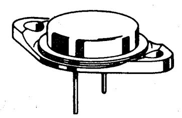
COMPLEMENTARY SILICON POWER TRANSISTORS

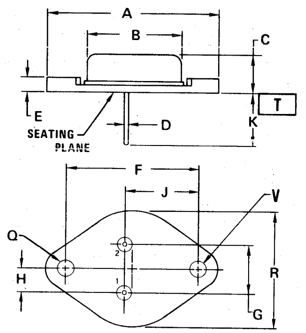
The 2N3773 and 2N6609 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc to dc converters or inverters.

- High Safe Operating Area (100% Tested)
  150 W @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{FE} = 15 (Min) @ 8 A, 4 V
  $V_{CE(sat)}$ = 1.4 V (Max) @ I_C = 8 A, I_B = 0.8 A
- For Low Distortion Complementary Designs

16 AMPERE COMPLEMENTARY POWER TRANSISTORS

140 VOLTS
150 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 3:
PIN 1. ANODE
2. CATHODE

NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⊕ ϕ 0.25 (0.010) Ⓜ T V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⊕ ϕ 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	140	Vdc
Collector-Emitter Voltage	V_{CEX}	160	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector Current — Continuous — Peak (1)	I_C	16 30	Adc
Base Current — Continuous — Peak (1)	I_B	4 15	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
*Collector-Emitter Breakdown Voltage (I_C = 0.2 Adc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
*Collector-Emitter Sustaining Voltage (I_C = 0.1 Adc, $V_{BE(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	$V_{CEX(sus)}$	160	–	Vdc
Collector-Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	150	–	Vdc
*Collector Cutoff Current (V_{CE} = 120 Vdc, I_B = 0)	I_{CEO}	–	10	mAdc
*Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 – –	 2 10	mAdc
Collector Cutoff Current (V_{CB} = 140 Vdc, I_E = 0)	I_{CBO}	–	2	mAdc
*Emitter Cutoff Current (V_{BE} = 7 Vdc, I_C = 0)	I_{EBO}	–	5	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain *(I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)	h_{FE}	 15 5	 60 	–
Collector-Emitter Saturation Voltage *(I_C = 8 Adc, I_B = 800 mAdc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 – –	 1.4 4	Vdc
*Base-Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	–	2.2	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common-Emitter Small-Signal, Short-Circuit, Forward Current Transfer Ratio (I_C = 1 A, f = 50 kHz)	$\|h_{fe}\|$	4	–	–
*Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	40	–	–
SECOND BREAKDOWN CHARACTERISTICS				
Second Breakdown Collector Current with Base Forward Biased t = 1 s (non-repetitive), V_{CE} = 100 V, See Figure 12	$I_{S/b}$	1.5	–	Adc

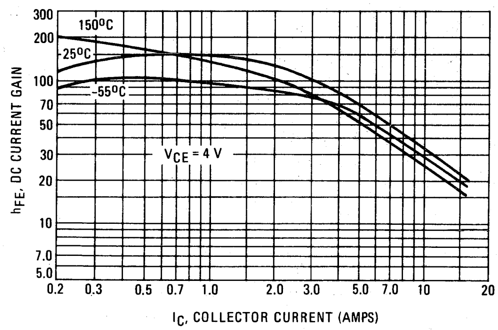
(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

*Indicates JEDEC Registered Data

3

NPN

FIGURE 1 — DC CURRENT GAIN



PNP

FIGURE 2 — DC CURRENT GAIN

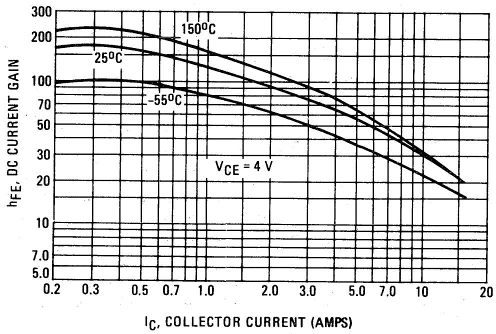


FIGURE 3 — COLLECTOR SATURATION REGION

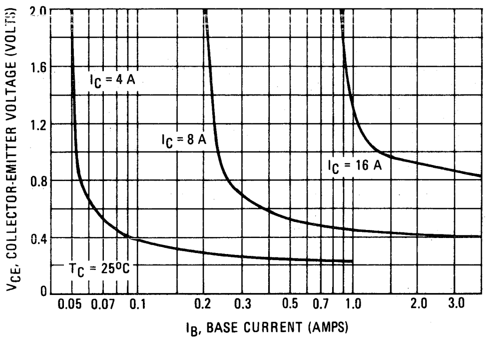
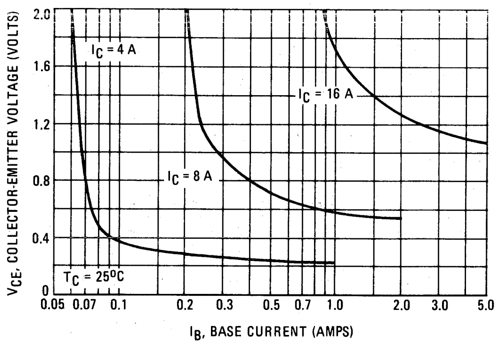


FIGURE 4 — COLLECTOR SATURATION REGION



3

FIGURE 5 — "ON" VOLTAGE

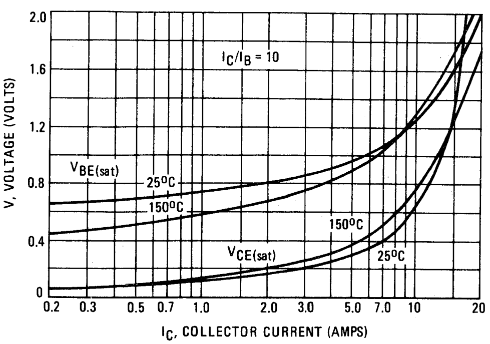


FIGURE 6 — "ON" VOLTAGE

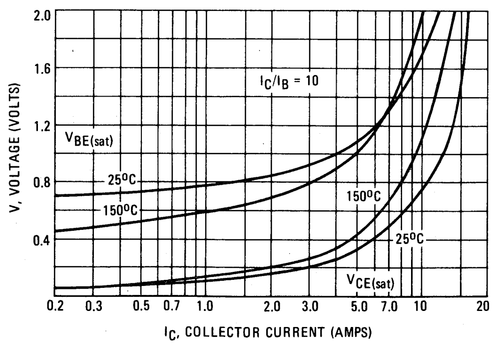
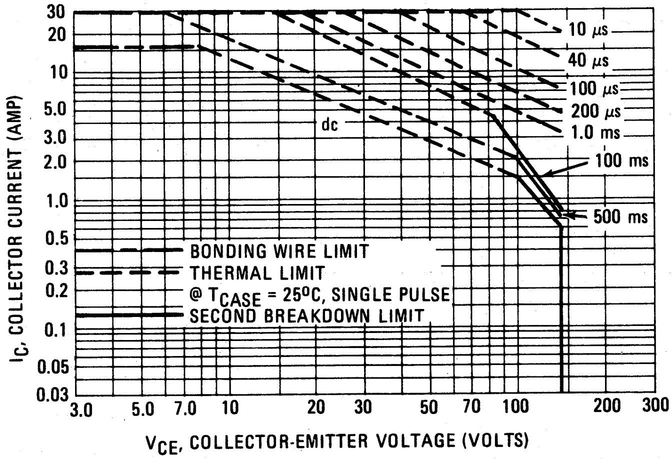


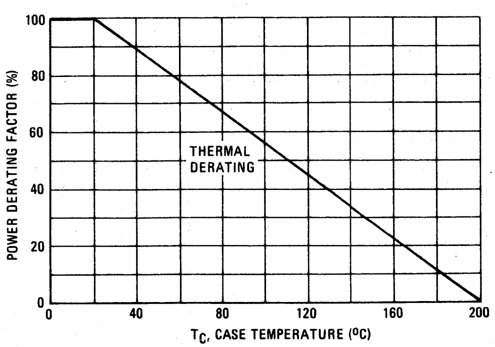
FIGURE 7 — FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 — POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N3789 thru 2N3792

SILICON PNP POWER TRANSISTORS

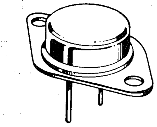
. . . designed for medium-speed switching and amplifier applications. These devices feature:

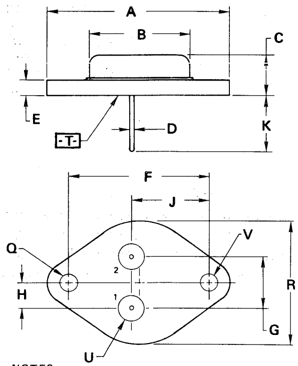
- Total Switching Time @ 3 A ≈ 1 μs (typ)
- Two Gain Ranges:
  h_{FE} (min) = 15 and 30 @ 3 A (2N3789, 2N3790)
  25 and 50 @ 1 A (2N3791, 2N3792)
- Low $V_{CE(sat)}$ = 0.5 V (typ) @ I_C = 4.0 A, I_B = 0.4 A
- Excellent Safe Area Limits
- Complementary NPN types available — 2N3713 thru 2N3716

10 AMPERE

POWER TRANSISTORS
PNP SILICON

60-80 VOLTS
150 WATTS





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   | ⌖ | ϕ.13 (0.005) Ⓜ | T | V Ⓜ |
   FOR LEADS:
   | ⌖ | ϕ.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

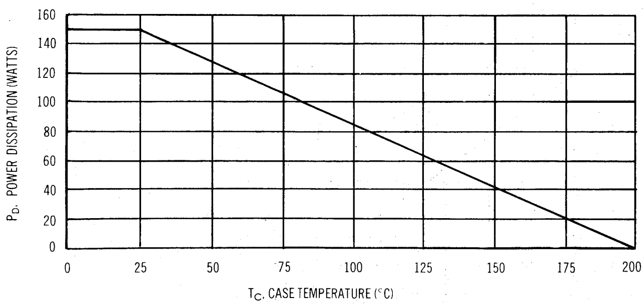
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Characteristic	Symbol	2N3789 2N3791	2N3790 2N3792	Unit
Collector-Base Voltage	V_{CB}	60	80	Volts
Collector-Emitter Voltage	V_{CEO}	60	80	Volts
Emitter-Base Voltage	V_{EB}	7.0	7.0	Volts
Collector Current (Continuous)	I_C	10	10	Amps
Base Current (Continuous)	I_B	4.0	4.0	Amps
Power Dissipation	P_D	150	150	Watts
Thermal Resitance	θ_{JC}	1.17	1.17	°C/W
Junction Operating and Storage Temperature Range	T_J, T_{stg}	-65 to +200		°C

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Limits are indicated by Figures 15, 16. Both limits are applicable and must be observed.

3

ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 200 mAdc, I_B = 0)	2N3789, 2N3791	$V_{CEO(sus)}$*	60	–	Vdc
	2N3790, 2N3792		80	–	
Collector-Emmiter Cutoff Current (V_{CE} = 60 Vdc, V_{BE} = -1.5 Vdc)	2N3789, 2N3791	I_{CEX}	–	1	mAdc
(V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc)	2N3790, 2N3792		–	1	
(V_{CE} = 60 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3789, 2N3791		–	5	
(V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3790, 2N3792		–	5	
Emitter-Base Cutoff Current (V_{EB} = 7 Vdc)	All Types	I_{EBO}	–	5	mAdc
DC Current Gain* (I_C = 1 Adc, V_{CE} = 2 Vdc)	2N3789, 2N3790	h_{FE}*	25	90	–
	2N3791, 2N3792		50	180	
(I_C = 3 Adc, V_{CE} = 2 Vdc)	2N3789, 2N3790		15	–	
	2N3791, 2N3792		30	–	
Collector-Emitter Saturation Voltage* (I_C = 4 Adc, I_B = 0.4 Adc)	2N3789, 2N3790	$V_{CE(sat)}$*	–	1.0	Vdc
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3791, 2N3792		–	1.0	
Base-Emitter On Voltage* (I_C = 5 A, V_{CE} = 2 Vdc)	2N3789, 2N3790	$V_{BE(on)}$*	–	2.0	Vdc
	2N3791, 2N3792		–	1.8	
(I_C = 10 Adc, V_{CE} = 4 Vdc)	All Types		–	4.0	
Current Gain – Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1 MHz)	All Types	f_T	4	–	MHz

*Sweep Test: 1/2 sine wave cycle @ 60 cps.

FIGURE 2 – TYPICAL SWITCHING TIMES AND TEST CIRCUIT

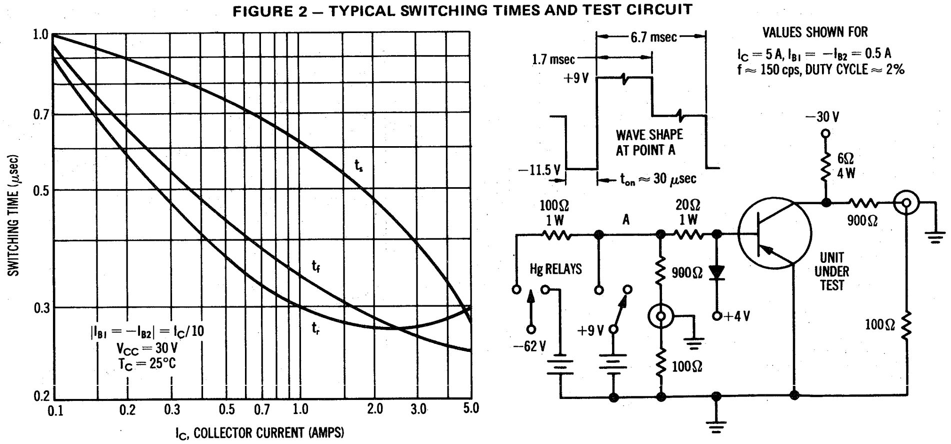


FIGURE 3 – CURRENT GAIN VARIATIONS

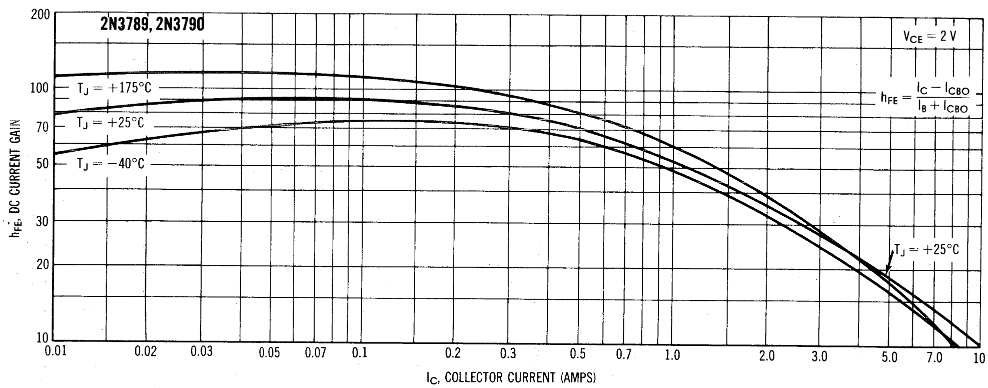


FIGURE 4 – CURRENT GAIN VARIATIONS

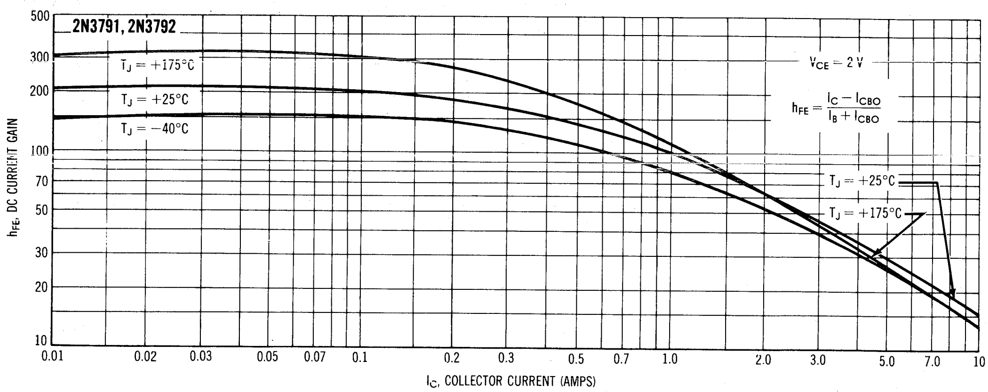


FIGURE 5 – SATURATION VOLTAGES

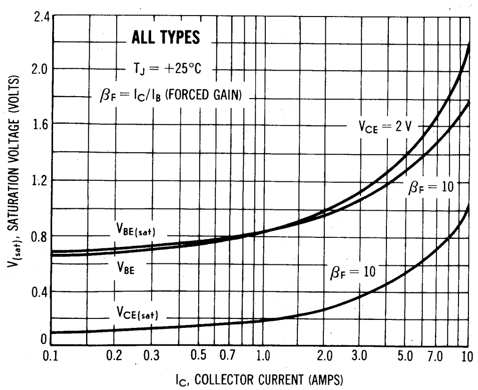
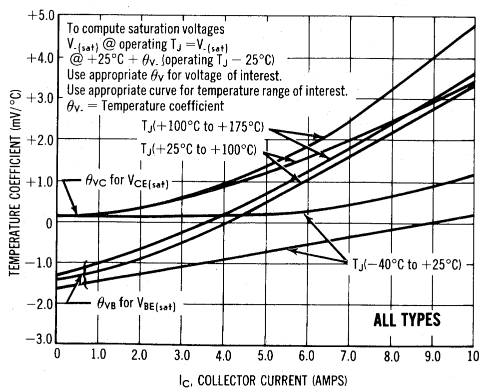


FIGURE 6 – TEMPERATURE COEFFICIENTS



SAFE OPERATING AREAS

FIGURE 7 — 2N3789, 2N3791

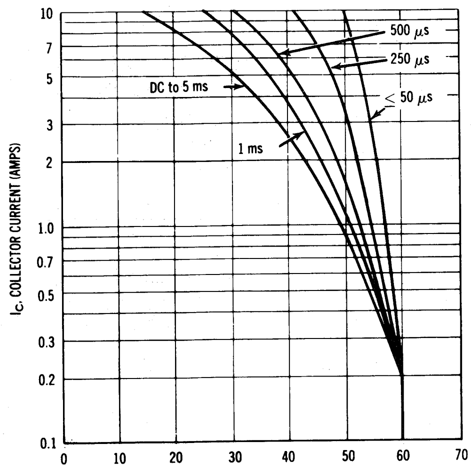
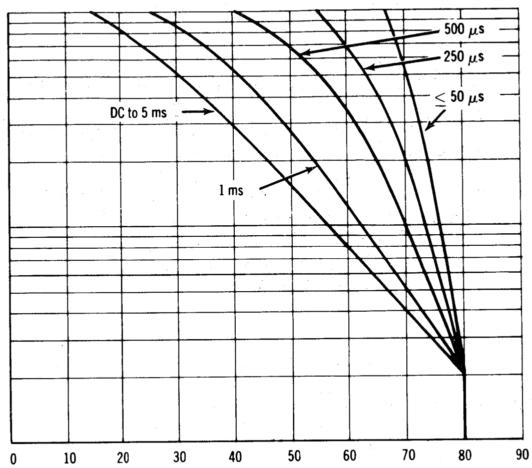


FIGURE 8 — 2N3790, 2N3792



V_{CE}, COLLECTOR-EMITTER VOLTAGE (VOLTS)

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

FIGURE 9 — CUT-OFF REGION TRANSCONDUCTANCE

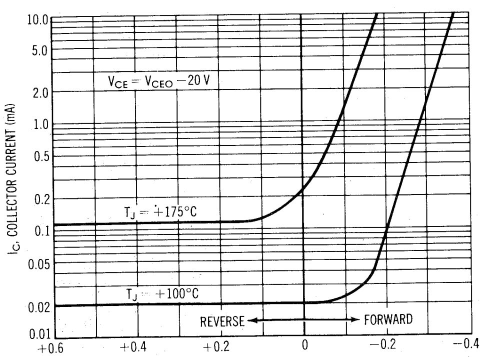
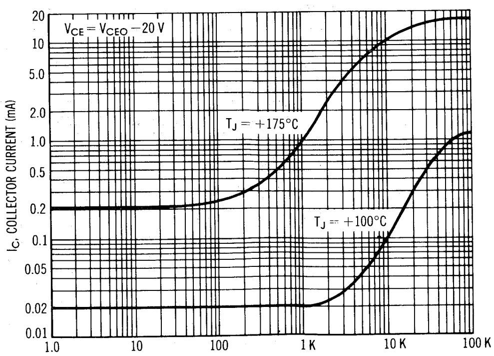


FIGURE 10 — COLLECTOR CUT-OFF CURRENT versus BASE-EMITTER RESISTANCE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N3867, 2N3868
See Page 3-32

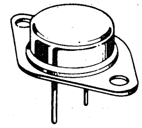
NPN
2N3902

HIGH VOLTAGE NPN SILICON TRANSISTORS

. . . designed for use in high-voltage inverters, converters, switching regulators and line operated amplifiers.

- High Collector-Emitter Voltage — V_{CEX} = 700 Vdc
- Excellent DC Current Gain — h_{FE} = 10 (Min) @ I_C = 2.5 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.8 Vdc (Max) @ I_C = 1.0 Adc

3.5 AMPERE
POWER TRANSISTORS
NPN SILICON
400 VOLTS
100 WATTS



*MAXIMUM RATINGS

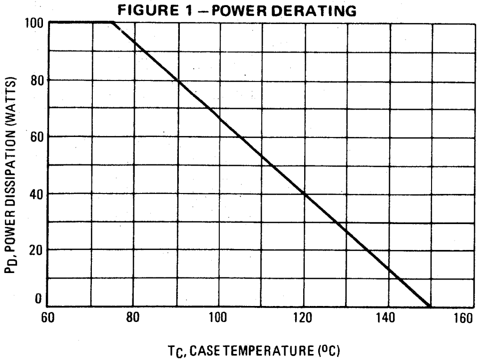
Rating	Symbol	2N3902	Unit
Collector-Emitter Voltage	V_{CEO}	400	Vdc
Collector-Emitter Voltage	V_{CEX}	700	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	3.5	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	100 1.33	Watts W/°C
Operating Junction Temperature Range	T_J	-65 to +150	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

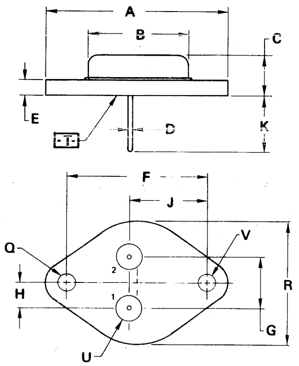
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.75	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	⌀.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	⌀.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0) (See Figure 12)	$V_{CEO(sus)}$	325	–	Vdc
Collector Cutoff Current (V_{CE} = 400 Vdc, I_B = 0)	I_{CEO}	–	0.25	mAdc
Collector Cutoff Current (V_{CE} = 700 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	– –	2.5 0.5	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	30 10	90 –	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc) (I_C = 2.5 Adc, I_B - 0.5 Adc)	$V_{CE(sat)}$	– –	0.8 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B - 0.1 Adc) (I_C 2.5 Adc, I_B 0.5 Adc)	$V_{BE(sat)}$	– –	1.5 2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc)	f_T	2.8	–	MHz

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2.0%.

3

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT

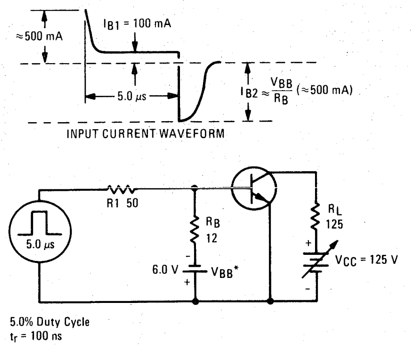


FIGURE 3 — TURN-ON TIME

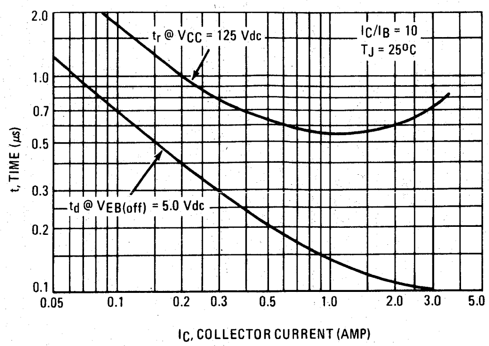


FIGURE 4 – THERMAL RESPONSE

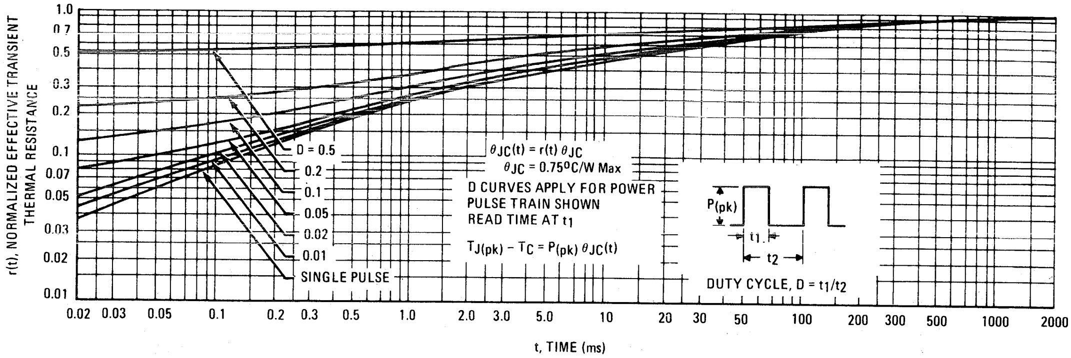
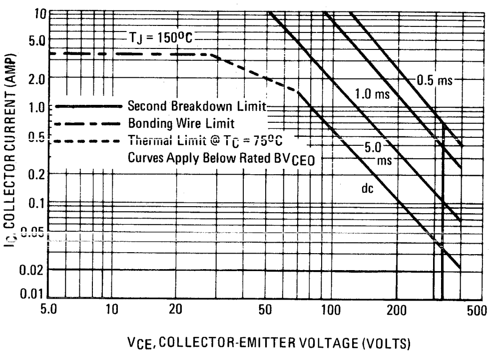


FIGURE 5 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 150^{\circ}C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

3

FIGURE 6 – TURN-OFF TIME

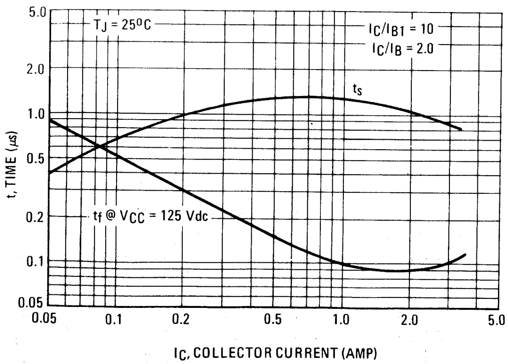


FIGURE 7 – CAPACITANCE

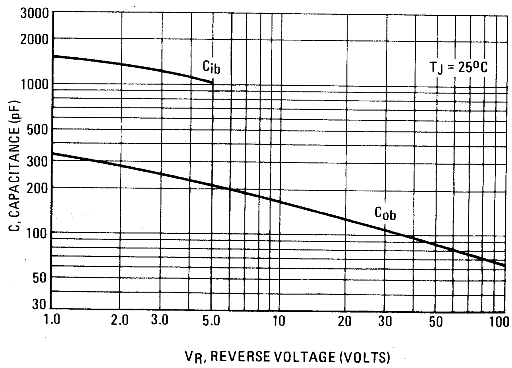


FIGURE 8 — DC CURRENT GAIN

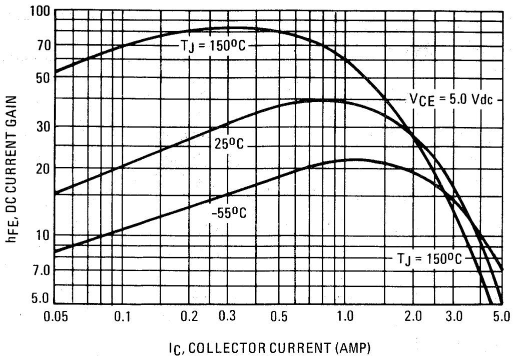


FIGURE 9 — "ON" VOLTAGES

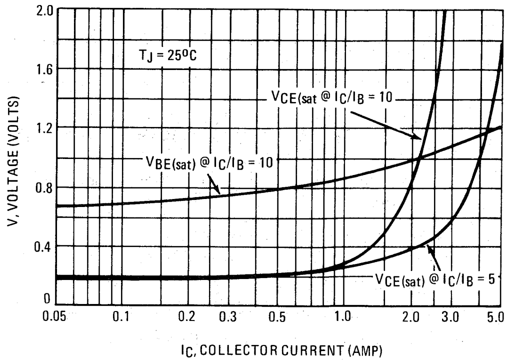


FIGURE 10 — COLLECTOR CUT-OFF REGION

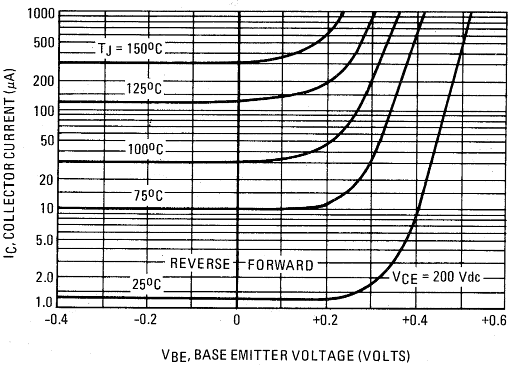


FIGURE 11 — TEMPERATURE COEFFICIENTS

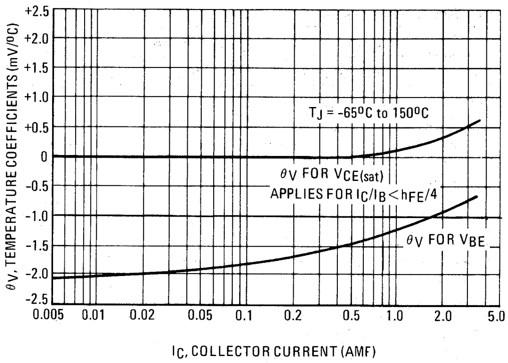
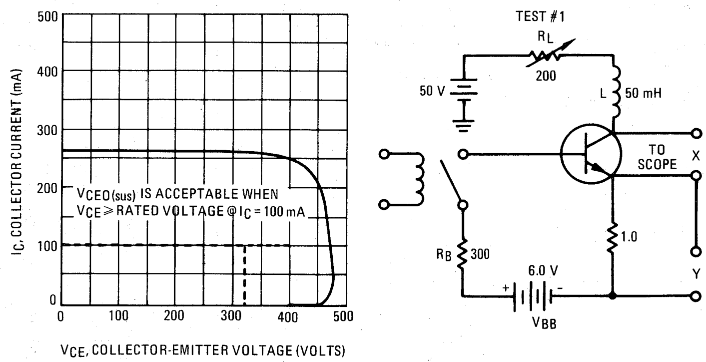


FIGURE 12 — COLLECTOR-EMITTER SUSTAINING VOLTAGE TEST CIRCUITS AND LOAD LINES



3

2N4233A

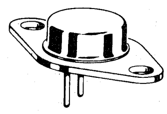
MEDIUM-POWER SILICON TRANSISTOR

. . . designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 1.5 Adc
- Low Leakage Current — I_{CEX} = 0.1 mAdc (Max)
- Excellent DC Current Gain — h_{FE} = 25-100 @ I_C = 1.5 Adc
- High Current Gain — Bandwidth Product — f_T = 4.0 MHz @ I_C = 0.25 Adc

**5.0 AMPERE
SILICON
POWER TRANSISTOR**

**80 VOLTS
75 WATTS**



*MAXIMUM RATINGS

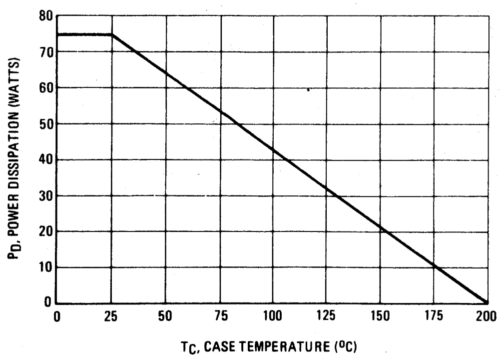
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak	I_C	5.0 10	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

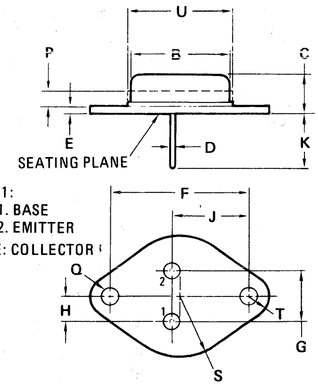
* THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.32	°C/W

*Indicates JEDEC registered data. (All values meet or exceed JEDEC registered data).

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

**CASE 80-02
TO-213AA**

3

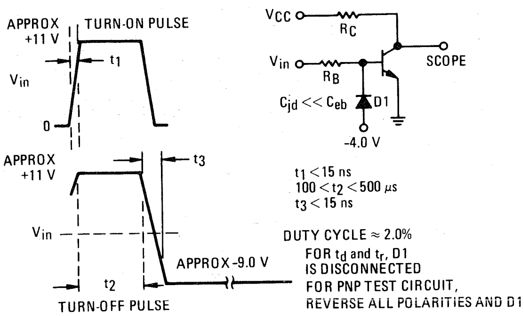
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	80	—	Vdc
Collector Cutoff Current (V_{CE} = 70 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current	I_{CEX}			mAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		—	0.1	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		—	1.0	
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	0.05	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain (1)	h_{FE}			—
*(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)		40	—	
*(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)		25	100	
*(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)		10	—	
*(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)		4.0	—	
*Collector-Emitter Saturation Voltage (1)	$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)		—	0.7	
(I_C = 3.0 Adc, I_B = 0.3 Adc)		—	2.0	
(I_C = 5.0 Adc, I_B = 1.25 Adc)		—	4.0	
*Base-Emitter On Voltage (1) (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.4	Vdc
***DYNAMIC CHARACTERISTICS**				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	300	pF
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	20	—	—

*Indicates JEDEC registered data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



FOR CURVES OF FIGURES 3 AND 6, R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

FIGURE 3 — TURN "ON" TIME

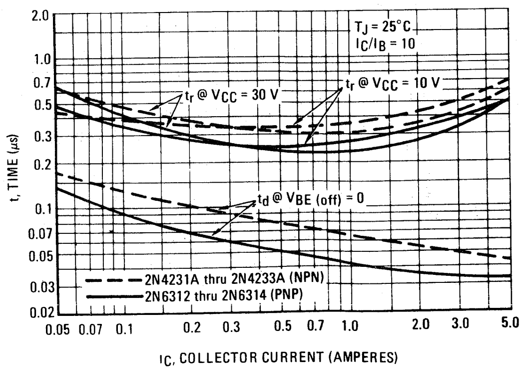


FIGURE 4 – THERMAL RESPONSE

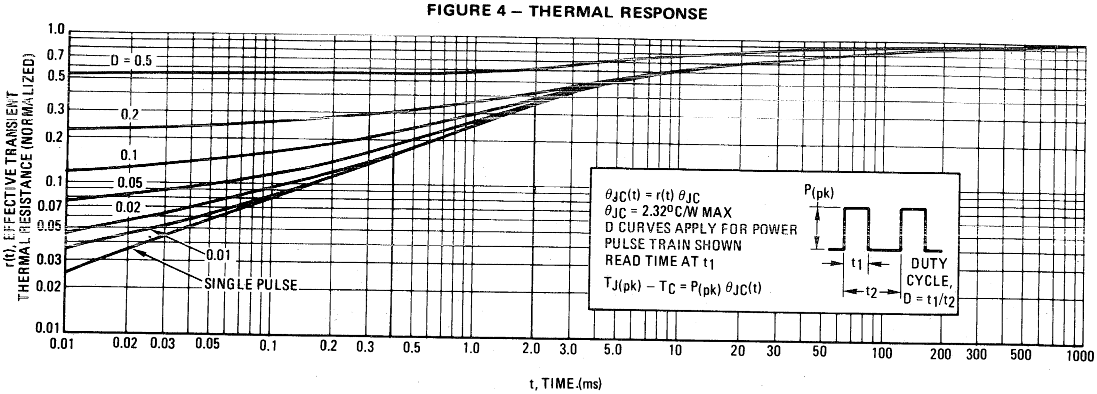
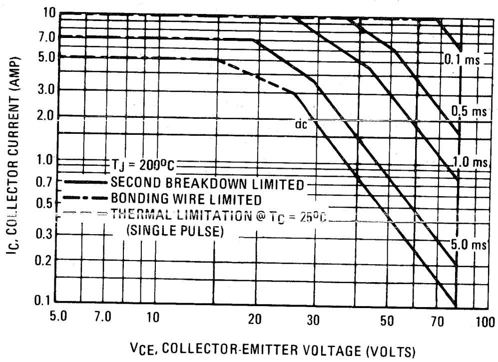


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN "OFF" TIME

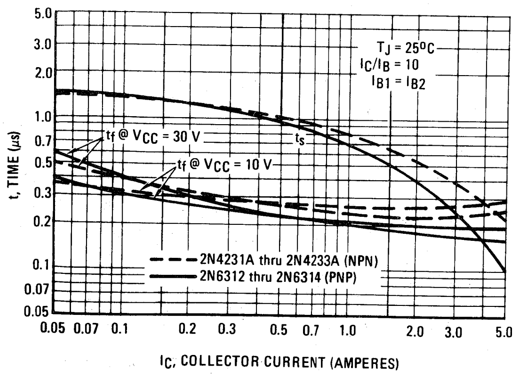


FIGURE 7 – CAPACITANCE

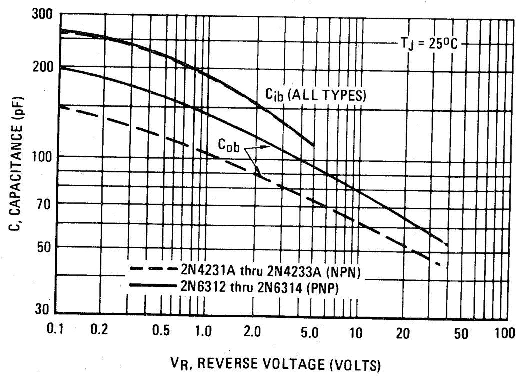


FIGURE 8 – DC CURRENT GAIN

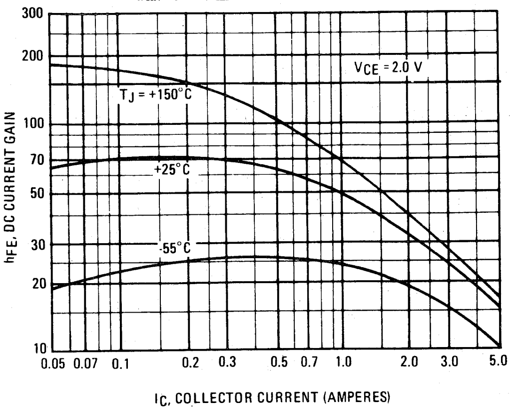


FIGURE 9 – COLLECTOR SATURATION REGION

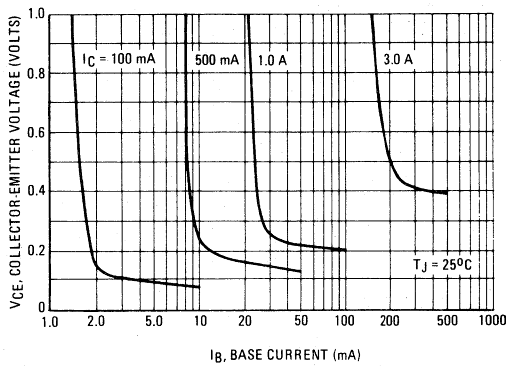
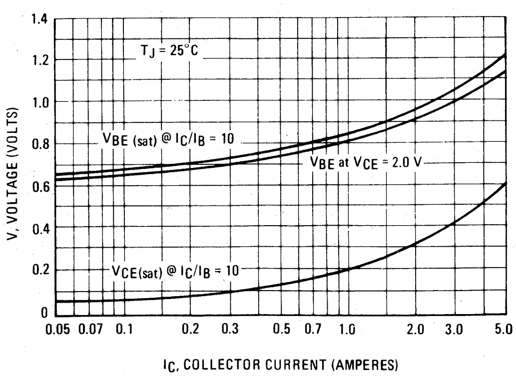


FIGURE 10 – "ON" VOLTAGES



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N4347
See Page 3-15

2N4398, 2N4399 2N5745

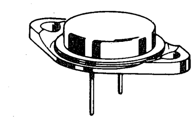
PNP SILICON HIGH-POWER TRANSISTORS

. . . designed for use in power amplifier and switching circuits.

- Low Collector-Emitter Saturation Voltage — I_C = 15 Adc, $V_{CE(sat)}$ = 1.0 Vdc (Max) 2N4398,99
  = 1.5 Vdc (Max) 2N5745
- DC Current Gain Specified — 1.0 to 30 Adc
- Complements to NPN 2N5301, 2N5302, 2N5303

20, 30 AMPERE
POWER TRANSISTORS
PNP SILICON

40–60–180 VOLTS
200 WATTS



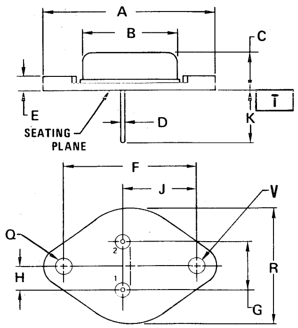
*MAXIMUM RATINGS

Rating	Symbol	2N4398	2N4399	2N5745	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	30 50	30 50	20 50	Adc
Base Current — Continuous Peak	I_B	← 7.5 → ← 15 →			Adc
Total Device Dissipation @ T_A = 25°C** Derate above 25°C	P_D	← 5.0 → ← 28.6 →			Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 200 → ← 1.15 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	35	°C/W

*Indicates JEDEC Registered Data
**Motorola guarantees this data in addition to JEDEC Registered Data.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

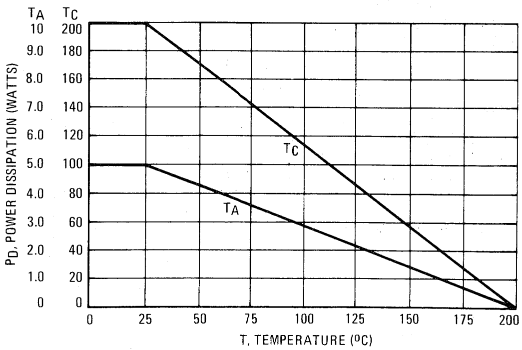
STYLE 3:
PIN 1. ANODE
2. CATHODE

NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⊕ ϕ 0.25 (0.010) Ⓜ T V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⊕ ϕ 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 13. All limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N4398	$V_{CEO(sus)}$	40	—	Vdc
	2N4399		60	—	
	2N5745		80	—	
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	2N4398	I_{CEO}	—	5.0	mAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N4399		—	5.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5745		—	5.0	
Collector Cutoff Current (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4398	I_{CEX}	—	5.0	mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4399		—	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5745		—	5.0	
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N4398, 2N4399		—	10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5745		—	10	
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	2N4398	I_{CBO}	—	1.0	mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N4399		—	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5745		—	1.0	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	All Types	h_{FE}	40	—	—
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5745		15	60	
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4398, 2N4399		15	60	
(I_C = 20 Adc, V_{CE} = 2.0 Vdc)	2N5745		5.0	—	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N4398, 2N4399		5.0	—	
Collector-Emitter Saturation Voltage (1) (I_C = 10 Adc, I_B = 1.0 Adc)	2N4398, 2N4399	$V_{CE(sat)}$	—	0.75	Vdc
	2N5745		—	1.0	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N4398, 2N4399		—	1.0	
	2N5745		—	1.5	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N4398, 2N4399		—	2.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5745		—	2.0	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N4398, 2N4399		—	4.0	
Base Emitter Saturation Voltage (1) (I_C = 10 Adc, I_B = 1.0 Adc)**	2N4398, 2N4399	$V_{BE(sat)}$	—	1.6	Vdc
	2N5745		—	1.7	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N4398, 2N4399		—	1.85	
	2N5745		—	2.0	
(I_C = 20 Adc, I_B = 2.0 Adc)**	2N4398, 2N4399		—	2.5	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5745		—	2.5	
Base-Emitter On Voltage (1) (I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5745	$V_{BE(on)}$	—	1.5	Vdc
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4398, 2N4399		—	1.7	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5745		—	2.5	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N4398, 2N4399		—	3.0	
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	2N4398, 2N4399	f_T	4.0	—	MHz
	2N5745		2.0	—	
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	40	—	—
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	2N4398, 2N4399	t_r	—	0.4	μs
	2N5745		—	1.0	
Storage Time	2N4398, 2N4399	t_s	—	1.5	μs
	2N5745		—	2.0	
Fall Time	2N4398, 2N4399	t_f	—	0.6	μs
	2N5745		—	1.0	

*Indicates JEDEC Registered Data.
**Motorola Guarantees this Data in Addition to JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

FIGURE 2 — TURN-ON TIME

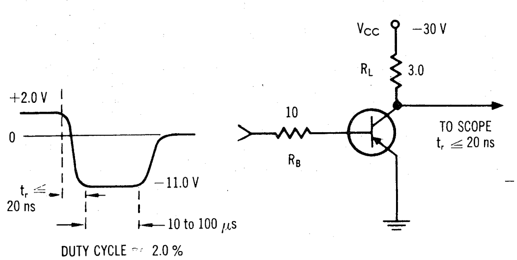
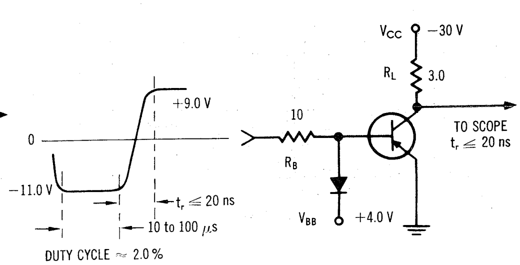


FIGURE 3 — TURN-OFF TIME



3

TYPICAL "ON" REGION CHARACTERISTICS

FIGURE 4 – DC CURRENT GAIN

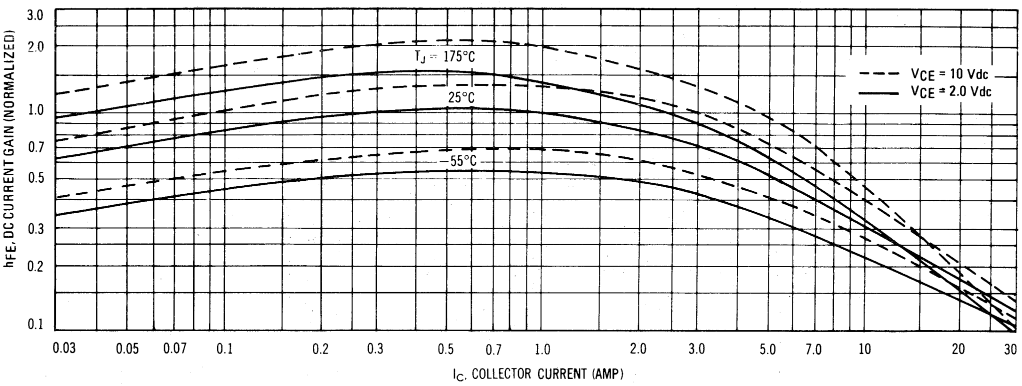


FIGURE 5 – COLLECTOR SATURATION REGION

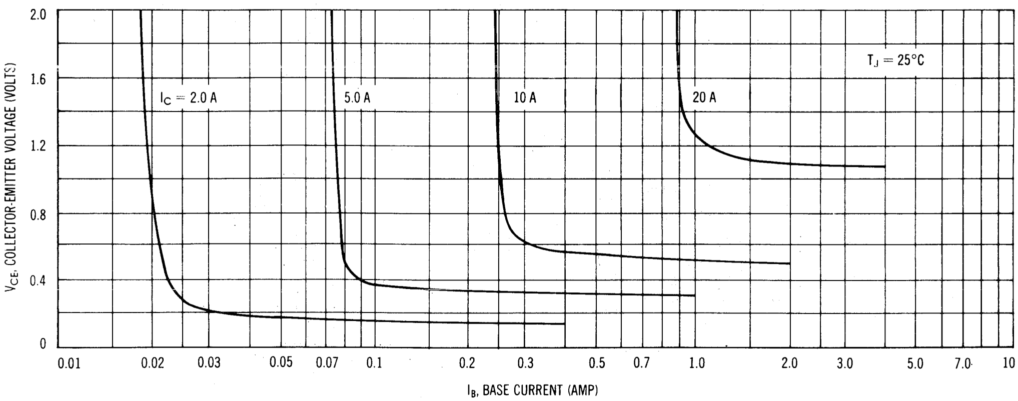


FIGURE 6 – "ON" VOLTAGES

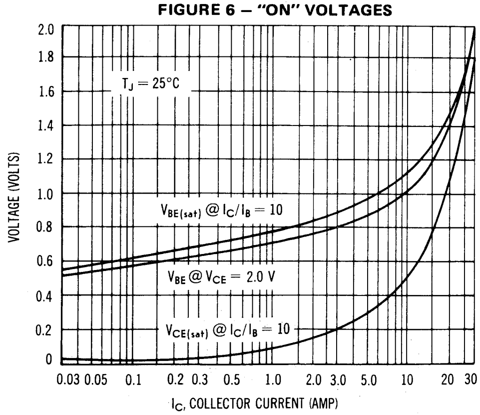
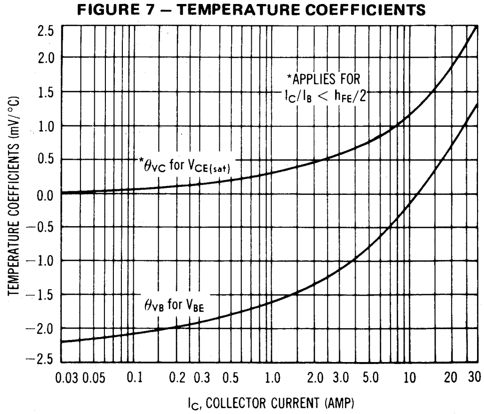


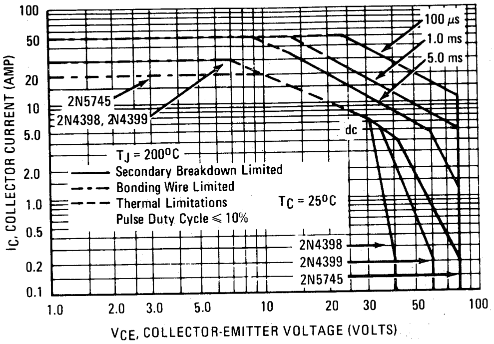
FIGURE 7 – TEMPERATURE COEFFICIENTS



3

RATINGS AND THERMAL DATA

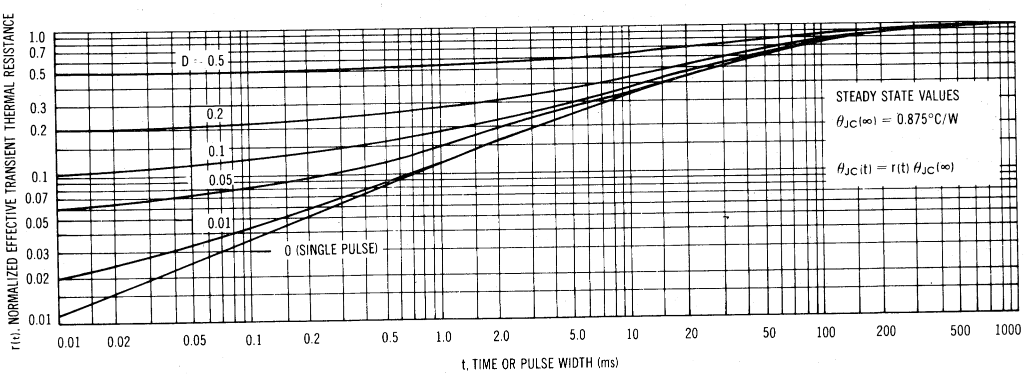
FIGURE 8 — ACTIVE REGION SAFE OPERATING AREA



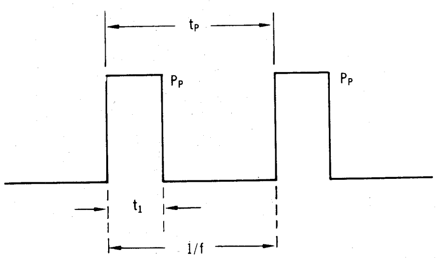
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 8 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 9 — THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



DUTY CYCLE $D = t_1 f = \frac{t_1}{t_P}$

PEAK PULSE POWER = P_P

A train of periodical power pulses can be represented by the model as shown in Figure A. Using the model and the device thermal reponse, the normalized effective transient thermal resistance of Figure 9 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 9 by the steady state value $\theta_{JC}(\infty)$.

Example:
The 2N4398 is dissipating 100 watts under the following conditions: t_1 = 1.0 ms, t_P = 5.0 ms. (D = 0.2)

Using Figure 9, at a pulse width of 1.0 ms and D = 0.2, the reading of r (t) is 0.28.

The peak rise in junction temperature is therefore
$\Delta T = r(t) \times P_P \times \theta_{JC}(\infty) = 0.28 \times 100 \times 0.875 = 24.5°C$

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N4898 thru 2N4900

MEDIUM-POWER PNP SILICON TRANSISTORS

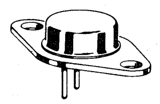
. . . designed for driver circuits, switching, and amplifier applications. These high-performance devices feature:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 V max @ I_C = 1.0 Amp
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Ampere
- 2N4900 Complementary to NPN 2N4912

4 AMPERE

GENERAL PURPOSE POWER TRANSISTORS

40-80 VOLTS
25 WATTS



MAXIMUM RATINGS

Rating	Symbol	2N4898	2N4899	2N4900	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous*	I_C*	← 1.0 → ← 4.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	← 25 → ← 0.143 →			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

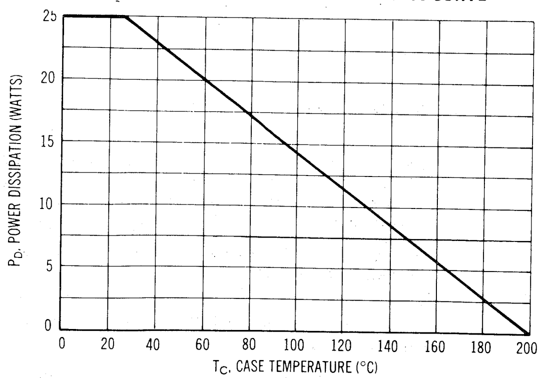
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Reistance, Junction to Case	θ_{JC}	7.0	°C/W

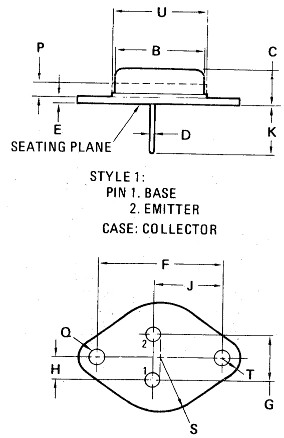
*The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements.
The 4.0 Amp maximum value is based upon actual current-handling capability of the device (see Figure 5).

3

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.
CASE 80-02
TO-213AA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) 2N4898		$V_{CEO(sus)}$*	40	-	Vdc
2N4899			60	-	
2N4900			80	-	
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) 2N4898		I_{CEO}	-	0.5	mAdc
(V_{CE} = 30 Vdc, I_B = 0) 2N4899			-	0.5	
(V_{CE} = 40 Vdc, I_B = 0) 2N4900			-	0.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEX}	-	0.1	mAdc
(V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			-	1.0	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	-	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	-	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)		h_{FE}*	40	-	-
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			20	100	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			10	-	
Collector-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$*	-	0.6	Vdc
Base-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$*	-	1.3	Vdc
Base-Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$*	-	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C - 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	-	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	-	-

* Pulse Test: PW ≈300 μs, Duty Cycle ≈ 2.0%

3

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

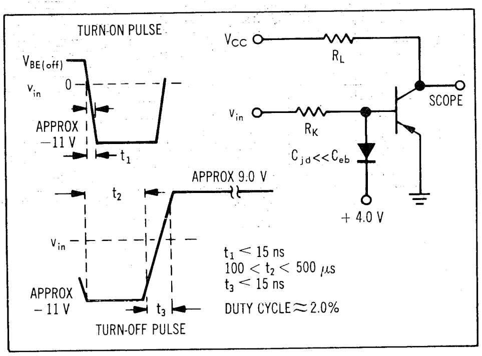


FIGURE 3 – TURN-ON TIME

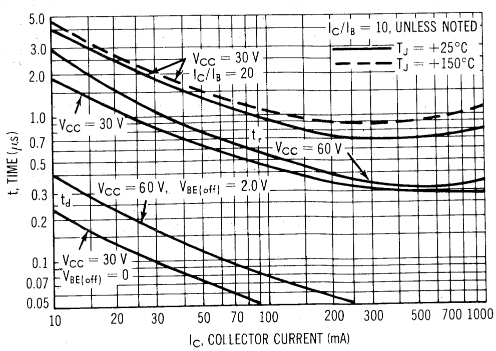


FIGURE 4 – THERMAL RESPONSE

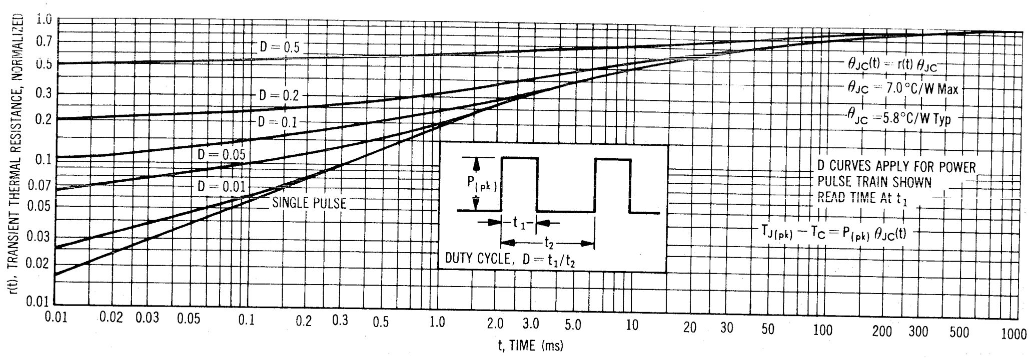
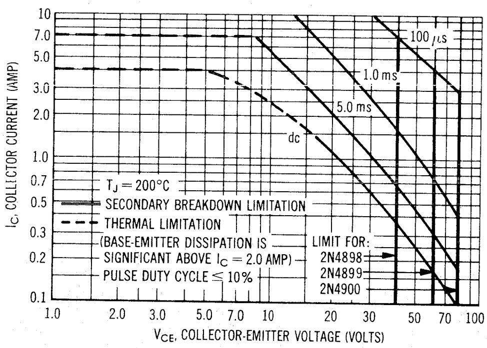


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



The safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor which must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 5 is based upon $T_{J(pk)} = 200°C$; T_C is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power which can be handled to values less than the limitations imposed by secondary breakdown.

3

FIGURE 6 – STORAGE TIME

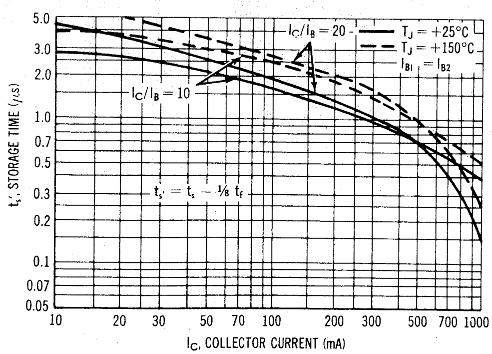
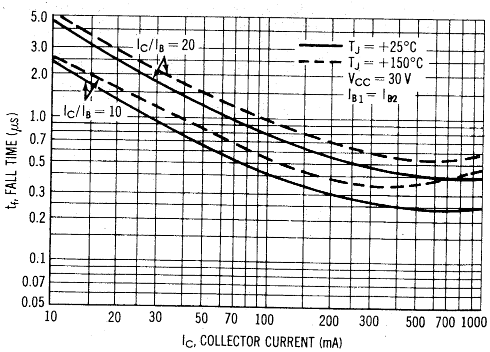


FIGURE 7 – FALL TIME



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N4912

NPN SILICON TRANSISTOR

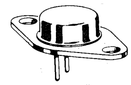
. . . designed for driver circuits, switching, and amplifier applications. This high-performance device features:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 V max @ I_C = 1.0 Amp
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to PNP 2N4900

1 AMPERE

NPN SILICON POWER TRANSISTOR

80 VOLTS
25 WATTS



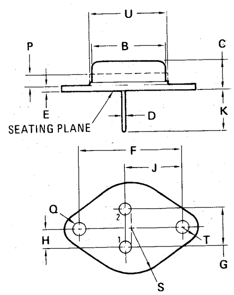
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous*	I_C*	1.0	Adc
Base Current — Continuous	I_B	1.0	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	25 0.143	Watts mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.0	°C/W

*The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements.



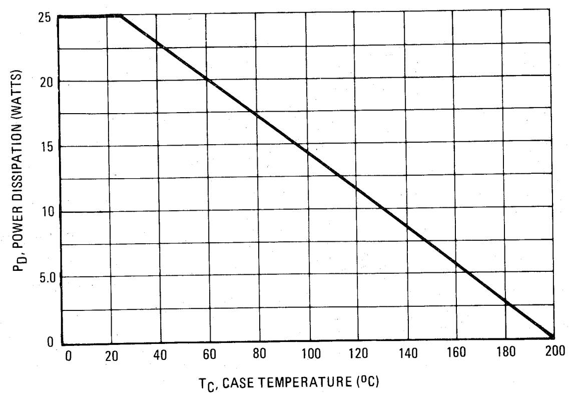
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	$V_{CEO(sus)}$	80	—	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	—	0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	- —	0.1 1.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40 20 10	— 100 —	—
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.6	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	—	1.3	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} - 1.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	—	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	25	—	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

3

FIGURE 2 — SWITCHING TIME EQUIVALENT CIRCUIT

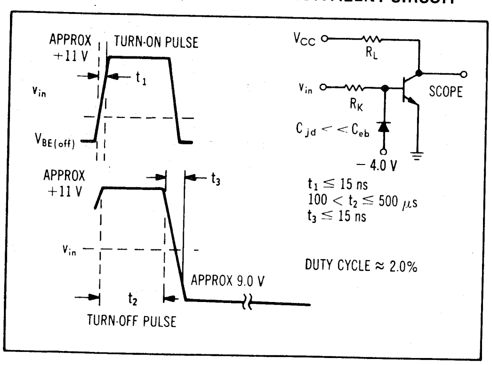


FIGURE 3 — TURN-ON TIME

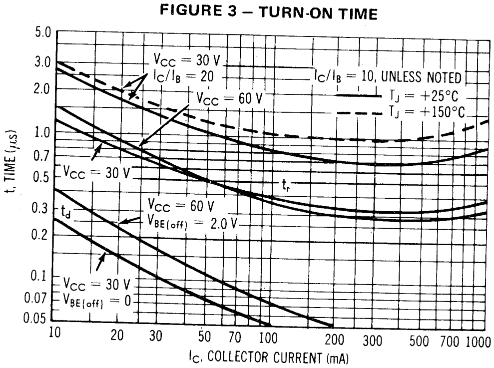


FIGURE 4 — THERMAL RESPONSE

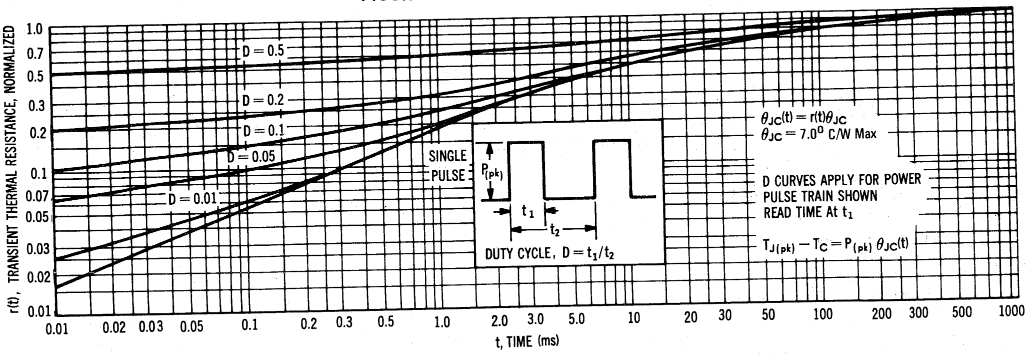
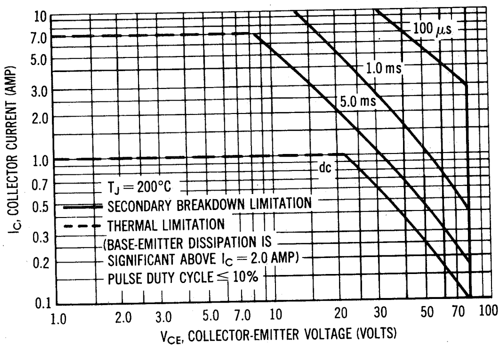


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 — STORAGE TIME

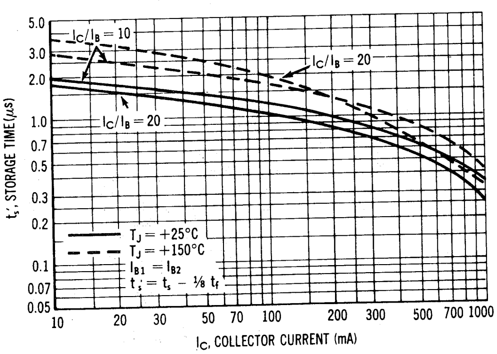
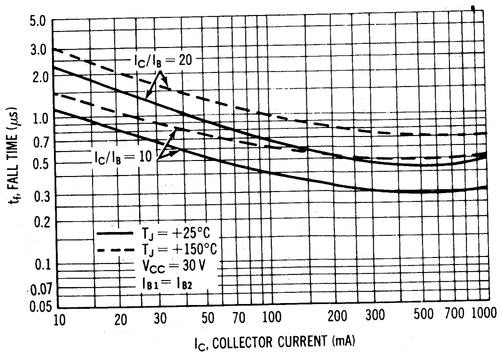


FIGURE 7 — FALL TIME



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N4918 thru 2N4920

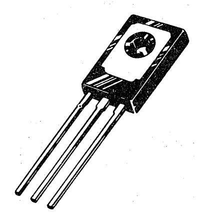
MEDIUM-POWER PLASTIC PNP SILICON TRANSISTORS

. . . designed for driver circuits, switching, and amplifier applications. These high-performance plastic devices feature:

- Low Saturation Voltage – $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction – P_D = 30 W @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to NPN 2N4921, 2N4922, 2N4923

3 AMPERE GENERAL-PURPOSE POWER TRANSISTORS

40-80 VOLTS
30 WATTS



*MAXIMUM RATINGS

Ratings	Symbol	2N4918	2N4919	2N4920	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current – Continuous (1)	I_C*		1.0 3.0		Adc
Base Current	I_B		1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		30 0.24		Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}		–65 to +150		°C

THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

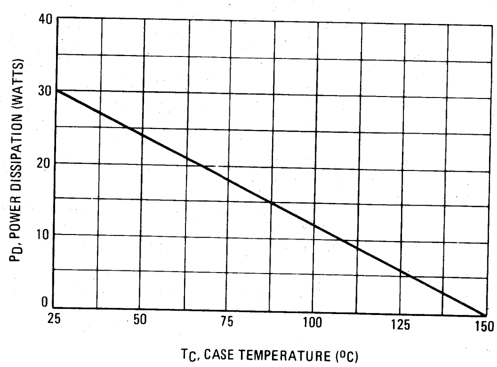
*Indicates JEDEC Registered Data for 2N4918 Series

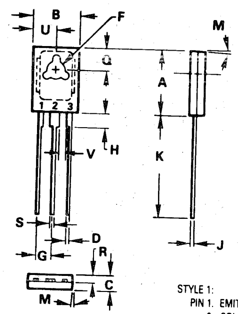
(1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current-handling capability of the device (See Figure 5).

(2) Recommend use of thermal compound for lowest thermal resistance.

3

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-225AA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0) 2N4918		$V_{CEO(sus)}$	40	–	Vdc
2N4919			60	–	
2N4920			80	–	
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) 2N4918		I_{CEO}	–	0.5	mAdc
(V_{CE} = 30 Vdc, I_B = 0) 2N4919			–	0.5	
(V_{CE} = 40 Vdc, I_B = 0) 2N4920			–	0.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEX}	–	0.1	mAdc
(V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)			–	0.5	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)		h_{FE}	40	–	–
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			30	150	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	–	0.6	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	–	1.3	Vdc
Base-Emitter On Voltage (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.3	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

*Indicates JEDEC Registered Data
(1) Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%

3

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

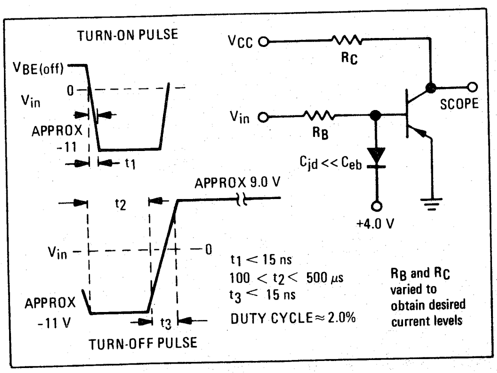


FIGURE 3 – TURN-ON TIME

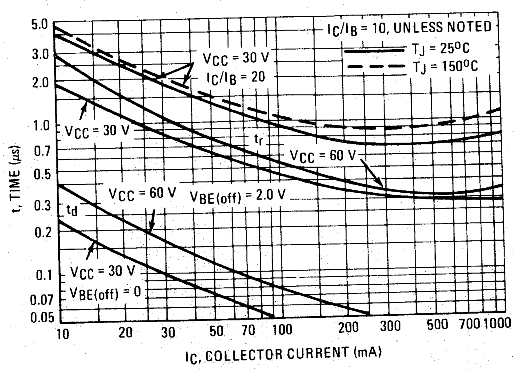


FIGURE 4 – THERMAL RESPONSE

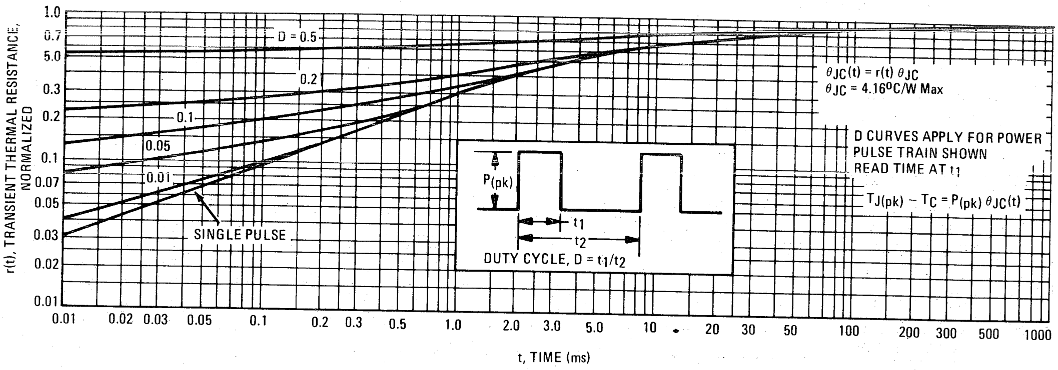
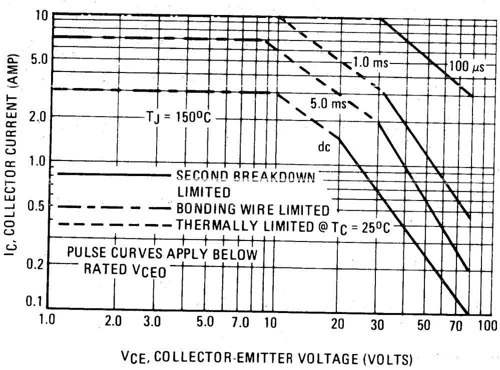


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – STORAGE TIME

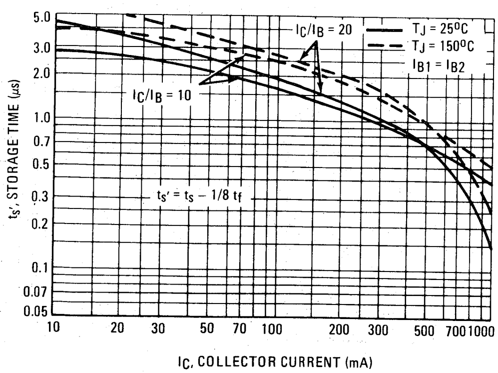
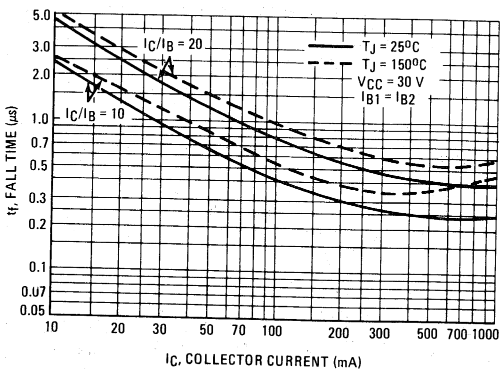


FIGURE 7 – FALL TIME



TYPICAL DC CHARACTERISTICS

FIGURE 8 – CURRENT GAIN

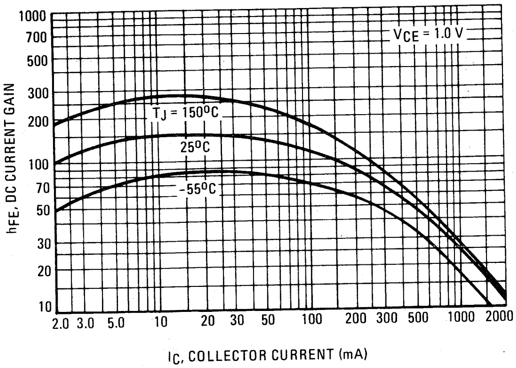


FIGURE 9 – COLLECTOR SATURATION REGION

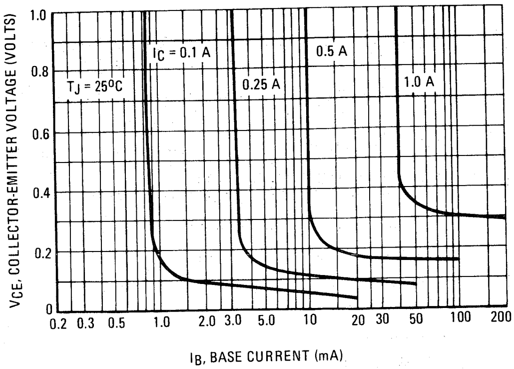


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

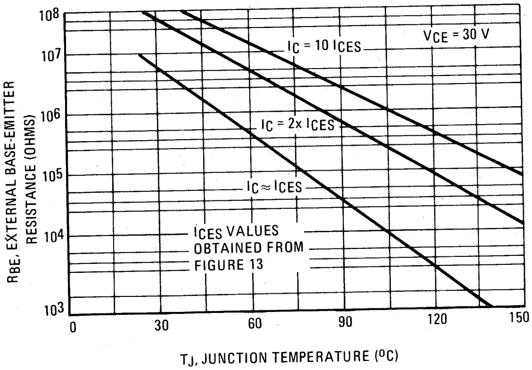


FIGURE 11 – "ON" VOLTAGE

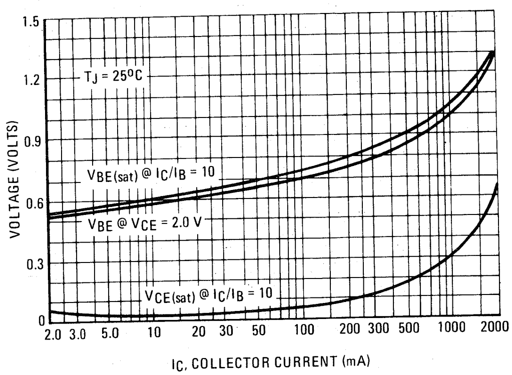


FIGURE 12 – COLLECTOR CUTOFF REGION

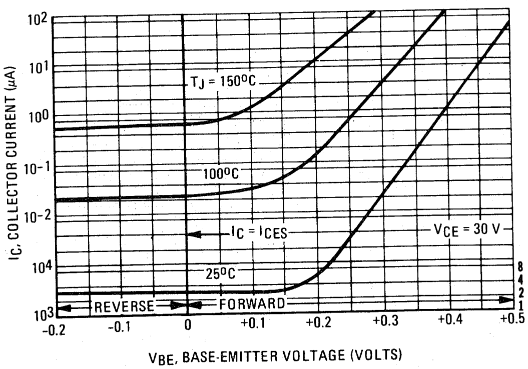
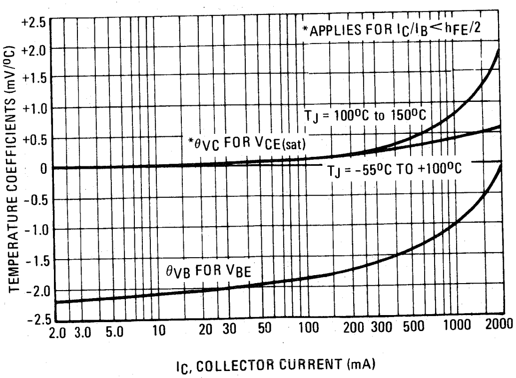


FIGURE 13 – TEMPERATURE COEFFICIENTS



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N4921 thru 2N4923

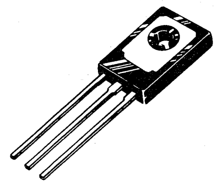
MEDIUM-POWER PLASTIC NPN SILICON TRANSISTORS

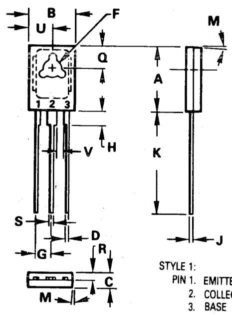
. . . designed for driver circuits, switching, and amplifier applications. These high-performance plastic devices feature:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction — P_D = 30 W @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to PNP 2N4918, 2N4919, 2N4920

3 AMPERE GENERAL-PURPOSE POWER TRANSISTORS

40-80 VOLTS
30 WATTS





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-225AA

*MAXIMUM RATINGS

Rating	Symbol	2N4921	2N4922	2N4923	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current - Continuous (1)	I_C	← 1.0 → ← 3.0 →			Adc
Base Current — Continuous	I_B	← 1.0 →			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

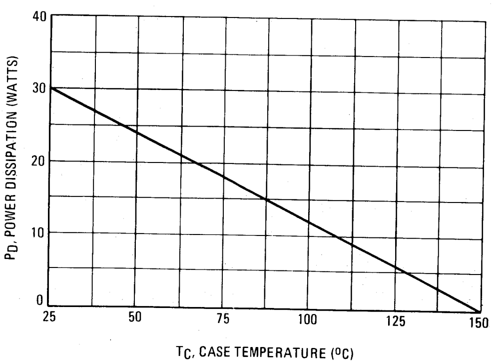
THERMAL CHARACTERISTICS (2)

Characteristic	Symbol		Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

(1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current-handling capability of the device (see Figures 5 and 6).
(2) Recommend use of thermal compound for lowest thermal resistance.
*Indicates JEDEC Registered Data.

3

FIGURE 1 — POWER DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0) 2N4921 2N4922 2N4923	$V_{CEO(sus)}$	 40 60 80	 – – –	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) 2N4921 (V_{CE} = 30 Vdc, I_B = 0) 2N4922 (V_{CE} = 40 Vdc, I_B = 0) 2N4923	I_{CEO}	 – – –	 0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	 – –	 0.1 0.5	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	–	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	 40 30 10	 – 150 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	–	0.6	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	–	1.3	Vdc
Base-Emitter On Voltage (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	–	1.3	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	25	–	–

(1) Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%.
*Indicates JEDEC Registered Data

3

FIGURE 2 — SWITCHING TIME EQUIVALENT CIRCUIT

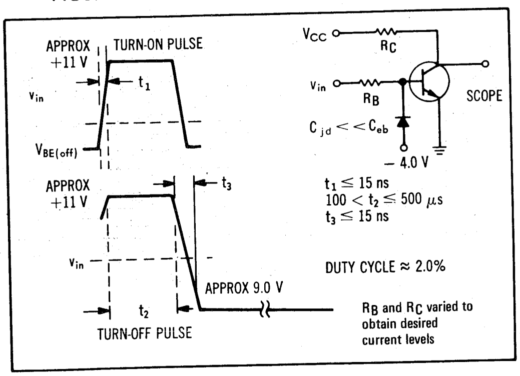


FIGURE 3 — TURN-ON TIME

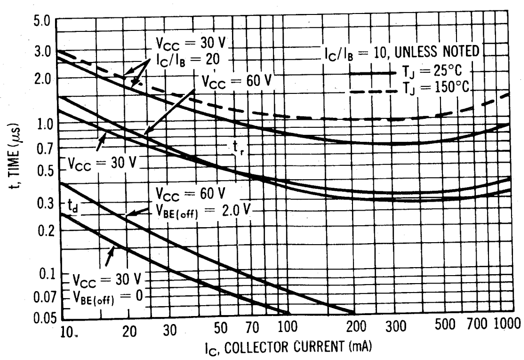


FIGURE 4 – THERMAL RESPONSE

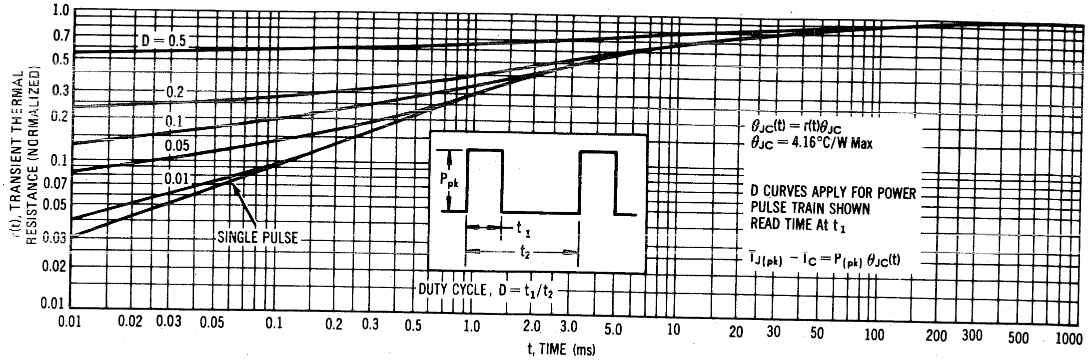
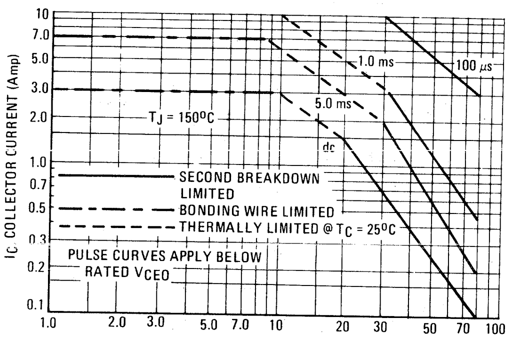


FIGURE 5 – ACTIVE – REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – STORAGE TIME

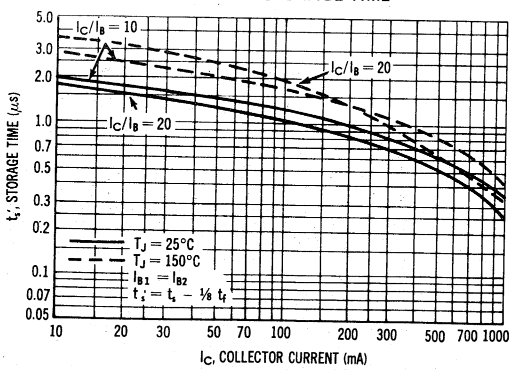


FIGURE 7 – FALL TIME

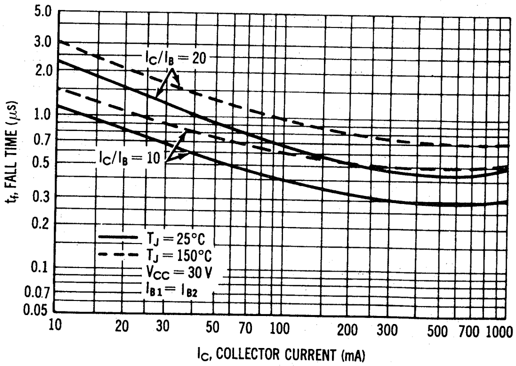


FIGURE 8 – CURRENT GAIN

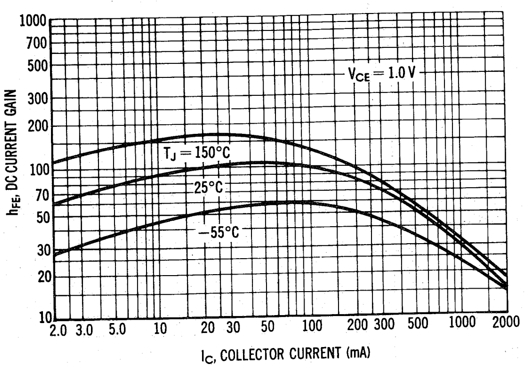


FIGURE 9 – COLLECTOR SATURATION REGION

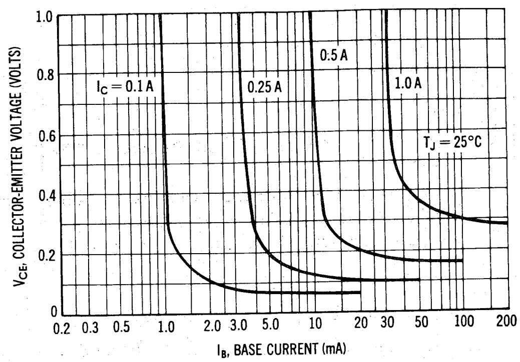


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

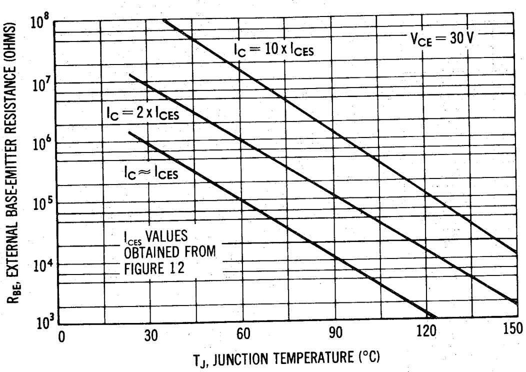


FIGURE 11 – "ON" VOLTAGE

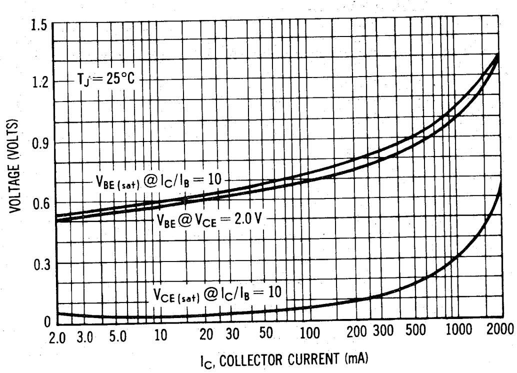


FIGURE 12 – COLLECTOR CUTOFF REGION

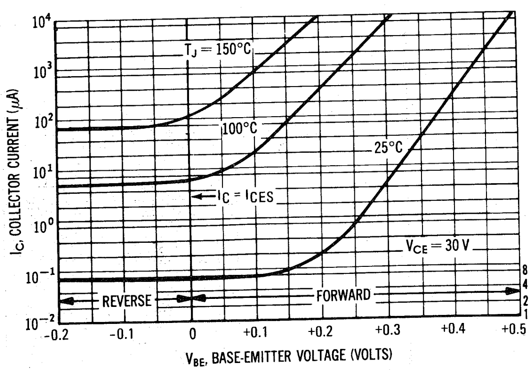
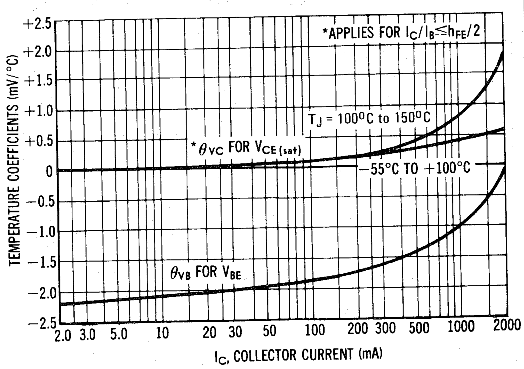


FIGURE 13 – TEMPERATURE COEFFICIENTS



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N5038
2N5039

NPN SILICON TRANSISTORS

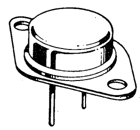
. . . fast switching speeds and high current capacity ideally suit these parts for use in switching regulators, inverters, wide-band amplifiers and power oscillators in industrial and commercial applications.

- High Speed — t_f = 0.5 μs (Max)
- High Current — $I_{C(max)}$ = 30 Amps
- Low Saturation — $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 20 Amps

20 AMPERE

NPN SILICON POWER TRANSISTORS

75 and 90 VOLTS
140 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N5038	2N5039	Unit
Collector-Base Voltage	V_{CBO}	150	120	Vdc
Collector-Emitter Voltage	V_{CEV}	150	120	Vdc
Emitter-Base Voltage	V_{EBO}	7		Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	140 0.8		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

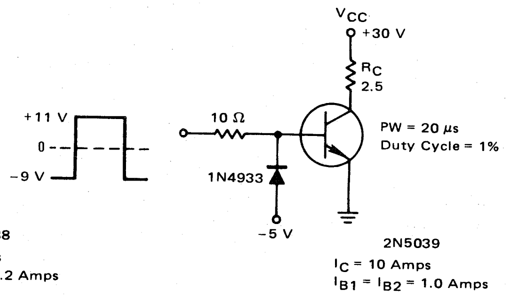
THERMAL CHARACTERISTICS

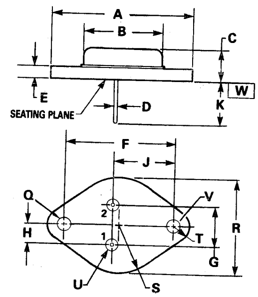
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 10 ms, Duty Cycle ≤ 50%.

3

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

CASE 1-04
TO-204AA

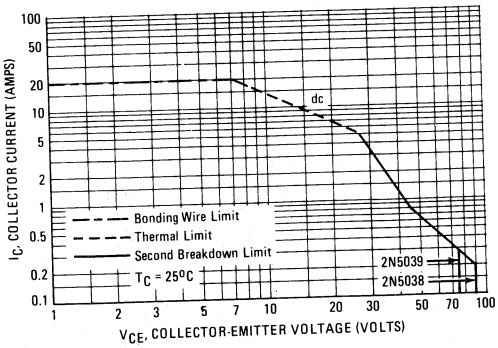
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5038	$V_{CEO(sus)}$	90	–	Vdc
	2N5039		75	–	
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 V)	2N5038	I_{CEX}	–	50	mAdc
(V_{CE} = 110 Vdc, $V_{BE(off)}$ = 1.5 V)	2N5039		–	50	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5038		–	10	
(V_{CE} = 85 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5039		–	10	
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	2N5038	I_{EBO}	–	5	mAdc
	2N5039		–	15	
(V_{EB} = 7 Vdc, I_C = 0)	Both		–	50	
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 12 Adc, V_{CE} = 5 Vdc)	2N5038	h_{FE}	20	100	–
(I_C = 10 Adc, V_{CE} = 5 Vdc)	2N5039		20	100	
Collector-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 5 Adc)		$V_{CE(sat)}$	–	2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 5 Adc)		$V_{BE(sat)}$	–	3.3	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common-Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 2 Adc, V_{CE} = 10 Vdc, f = 5 MHz)		$\|h_{fe}\|$	12	–	–
SWITCHING CHARACTERISTICS					
RESISTIVE LOAD					
Rise Time	(V_{CC} = 30 Vdc)	t_r	–	0.5	µs
Storage Time	(I_C = 12 Adc, I_{B1} = I_{B2} = 1.2 Adc) 2N5038	t_s	–	1.5	µs
Fall Time	(I_C = 10 Adc, I_{B1} = I_{B2} = 1 Adc) 2N5039	t_f	–	0.5	µs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

FIGURE 2 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Second breakdown pulse limits are valid for duty cycles to 10%. At high case temperatures, thermal limitations may reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

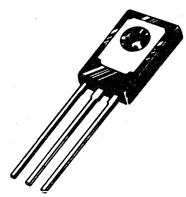
2N5190 thru 2N5192

SILICON NPN POWER TRANSISTORS

. . . for use in power amplifier and switching circuits, — excellent safe area limits. Complement to PNP 2N5193, 2N5194, 2N5195

4 AMPERE
POWER TRANSISTORS
SILICON NPN

40-80 VOLTS
40 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N5190	2N5191	2N5192	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current	I_C	← 4.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	40 320			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

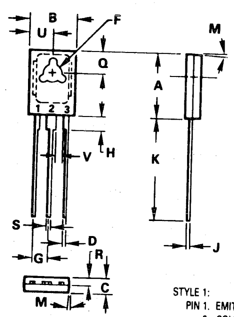
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	2N5190 2N5191 2N5192	$V_{CEO(sus)}$	40 60 80	– – –	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	2N5190 2N5191 2N5192	I_{CEO}	– – –	1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5190 2N5191 2N5192 2N5190 2N5191 2N5192	I_{CEX}	– – – – – –	0.1 0.1 0.1 2.0 2.0 2.0	mAdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	2N5190 2N5191 2N5192	I_{CBO}	– – –	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N5190 2N5191 2N5192	h_{FE}	25 25 20	100 100 80	–
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	2N5190 2N5191 2N5192		10 10 7.0	– –	
Collector-Emitter Saturation Voltage (1) (I_C = 1.5 Adc, I_B = 0.15 Adc) (I_C = 4.0 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	– –	0.6 1.4	Vdc
Base-Emitter On Voltage (1) (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
*Indicates JEDEC Registered Data



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-225AA

3

FIGURE 1 – DC CURRENT GAIN

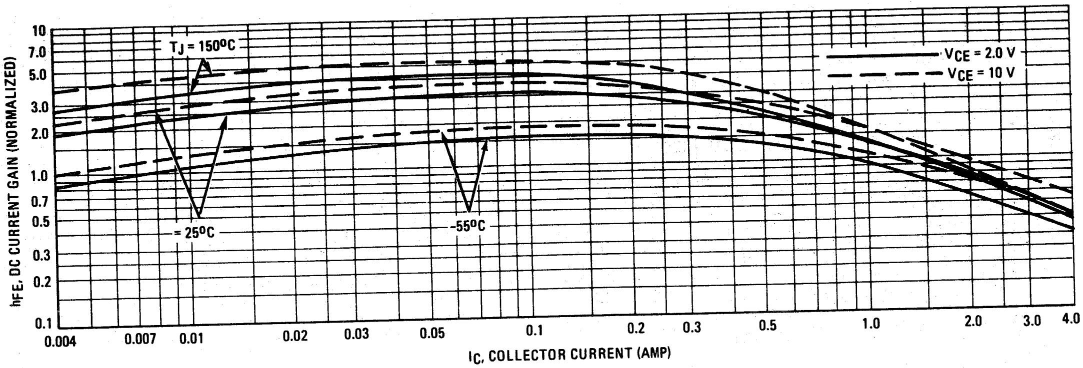


FIGURE 2 – COLLECTOR SATURATION REGION

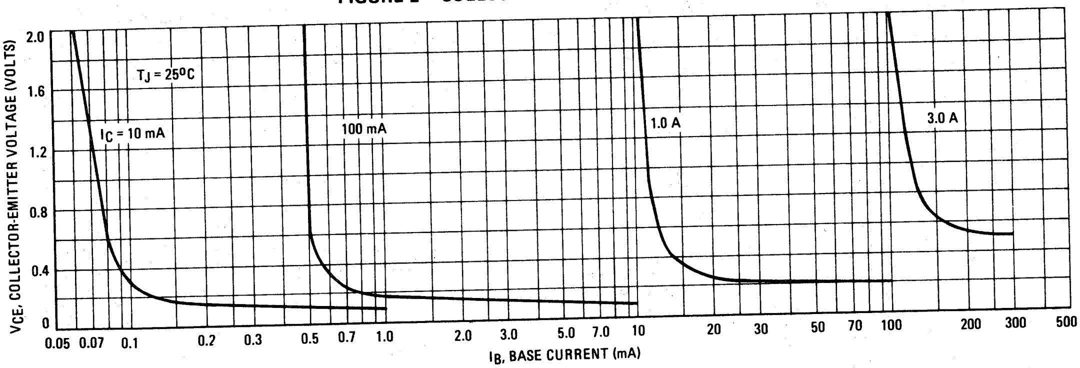


FIGURE 3 – "ON" VOLTAGES

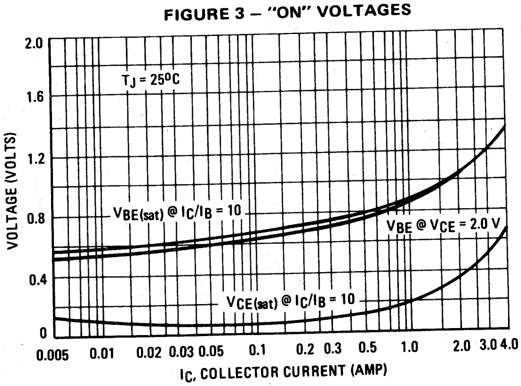


FIGURE 4 – TEMPERATURE COEFFICIENTS

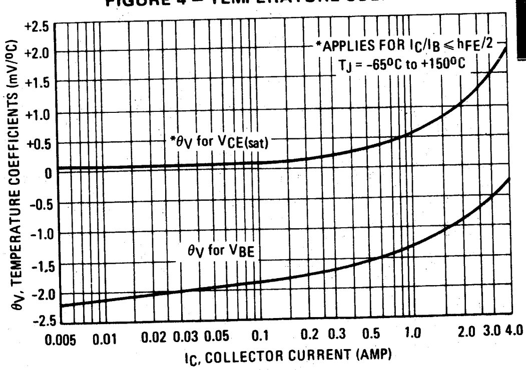


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FIGURE 5 – COLLECTOR CUT-OFF REGION

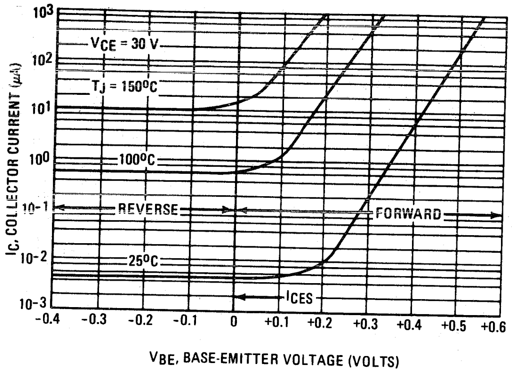

FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

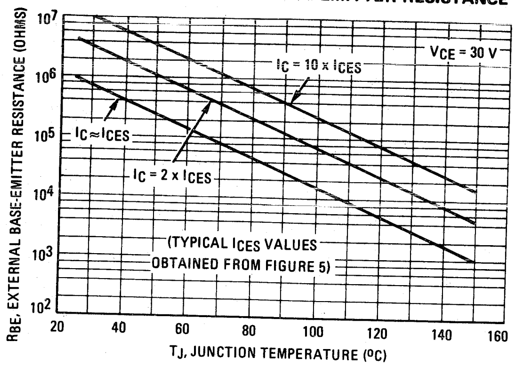

FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT

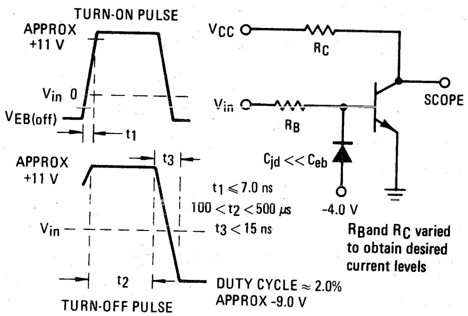

FIGURE 8 – CAPACITANCE

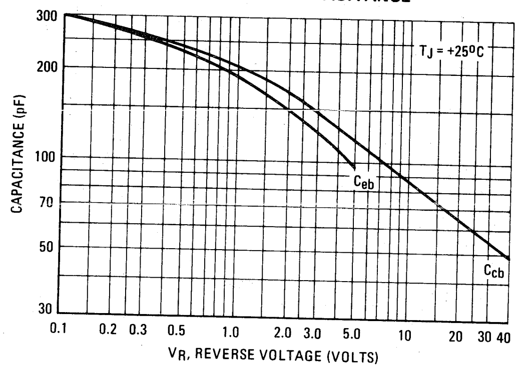

FIGURE 9 – TURN-ON TIME

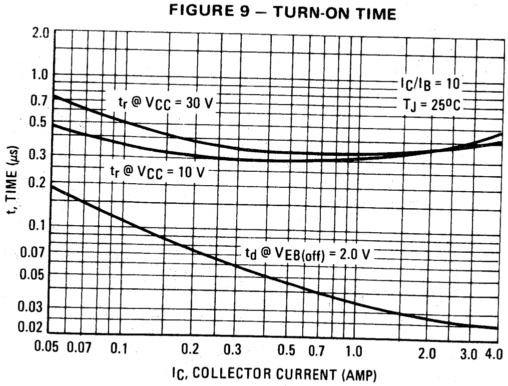

FIGURE 10 – TURN-OFF TIME

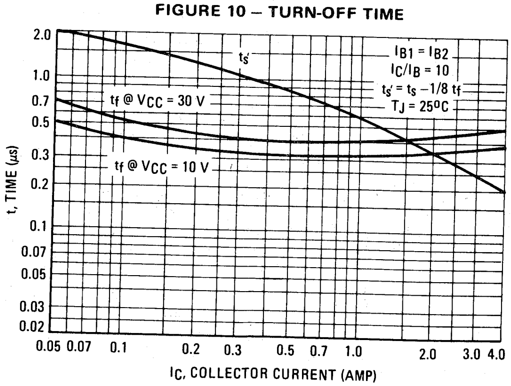

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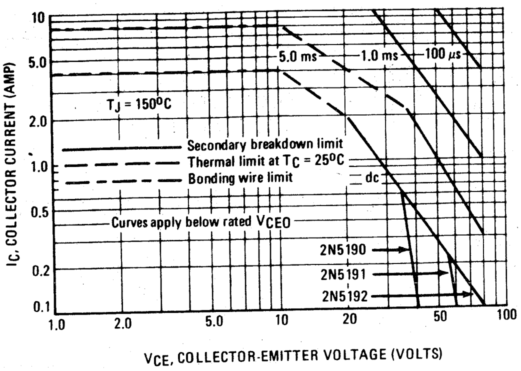
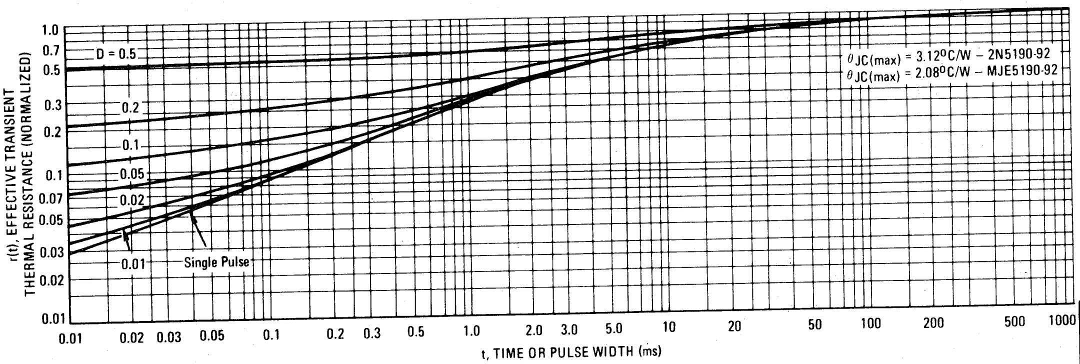
FIGURE 11 RATING AND THERMAL DATA
ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 12 – THERMAL RESPONSE



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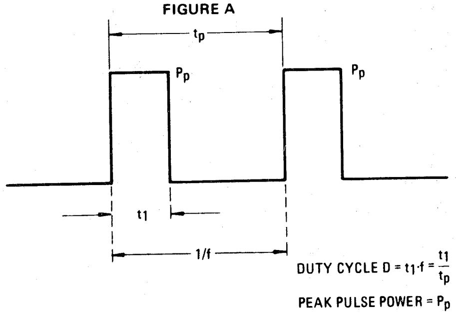
DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N5190 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, tp = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of r (t_1, D) is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2°C$$

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

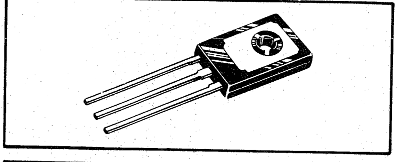
2N5193 thru 2N5195

SILICON PNP POWER TRANSISTORS

. . . for use in power amplifier and switching circuits, – excellent safe area limits. Complement to NPN 2N5190, 2N5191, 2N5192

4 AMPERE POWER TRANSISTORS SILICON PNP

40-80 VOLTS



*MAXIMUM RATINGS

Rating	Symbol	2N5193	2N5194	2N5195	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current	I_C	← 4.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ $T_C = 25^oC$	P_D	← 40 →			Watts
Derate above 25^oC		← 320 →			$mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +150 →			$^oC/W$

THERMAL CHARACTERISTICS

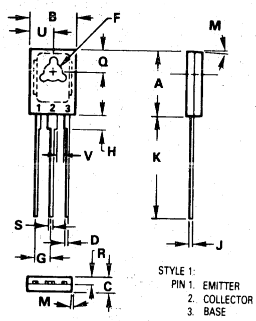
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	$^oC/W$

*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0) 2N5193	$V_{CEO(sus)}$	40	–	Vdc
2N5194		60	–	
2N5195		80	–	
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) 2N5193	I_{CEO}	–	1.0	mAdc
(V_{CE} = 60 Vdc, I_B = 0) 2N5194		–	1.0	
(V_{CE} = 80 Vdc, I_B = 0) 2N5195		–	1.0	
Collector Cutoff Current (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5193	I_{CEX}	–	0.1	mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5194		–	0.1	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5195		–	0.1	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, 2N5193 $T_C = 125^oC$)		–	2.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, 2N5194 $T_C = 125^oC$)		–	2.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, 2N5195 $T_C = 125^oC$)		–	2.0	
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) 2N5193	I_{CBO}	–	0.1	mAdc
(V_{CB} = 60 Vdc, I_E = 0) 2N5194		–	0.1	
(V_{CB} = 80 Vdc, I_E = 0) 2N5195		–	0.1	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc) 2N5193	h_{FE}	25	100	–
2N5194		25	100	
2N5195		20	80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc) 2N5193		10	–	
2N5194		10	–	
2N5195		7.0	–	
Collector-Emitter Saturation Voltage (1) (I_C = 1.5 Adc, I_B = 0.15 Adc)	$V_{CE(sat)}$	–	0.6	Vdc
(I_C = 4.0 Adc, I_B = 1.0 Adc)		–	1.4	
Base-Emitter On Voltage (1) (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	–	MHz

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	–	0.040	–

CASE 77-05
TO-225AA

3

FIGURE 1 – DC CURRENT GAIN

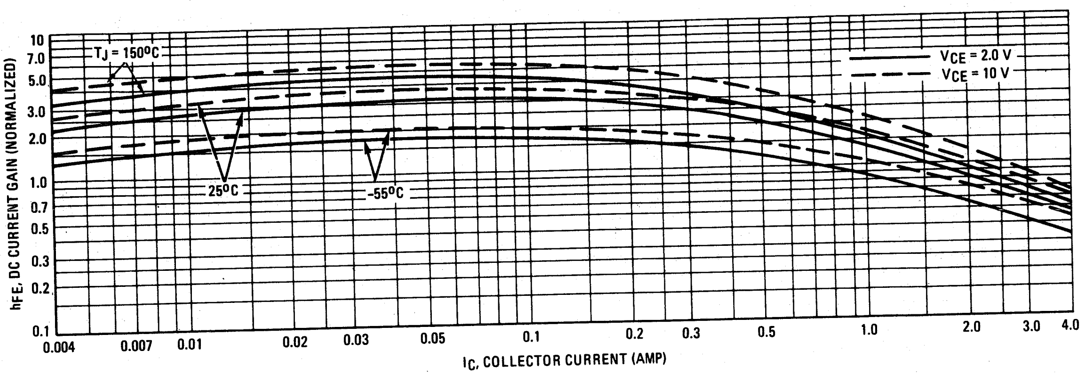


FIGURE 2 – COLLECTOR SATURATION REGION

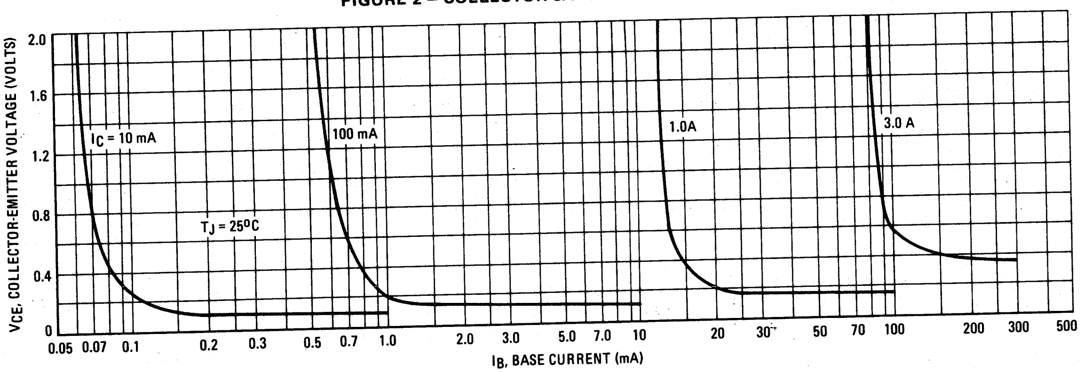


FIGURE 3 – "ON" VOLTAGE

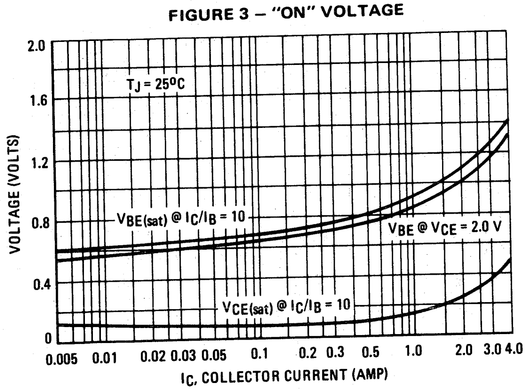


FIGURE 4 – TEMPERATURE COEFFICIENTS

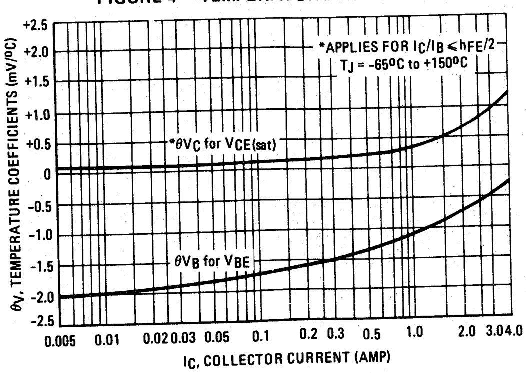


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FIGURE 5 – COLLECTOR CUT-OFF REGION

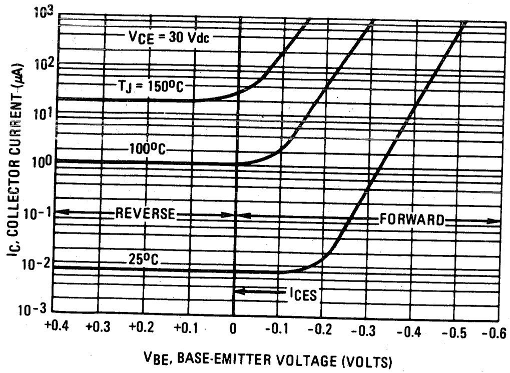


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

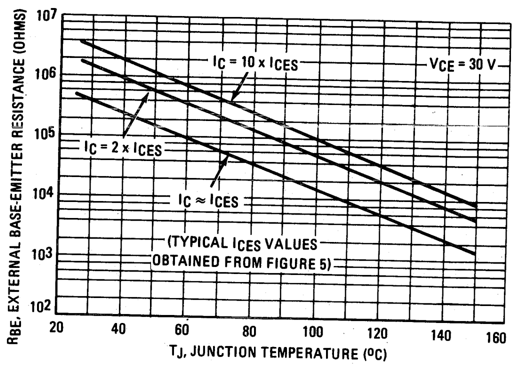


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT

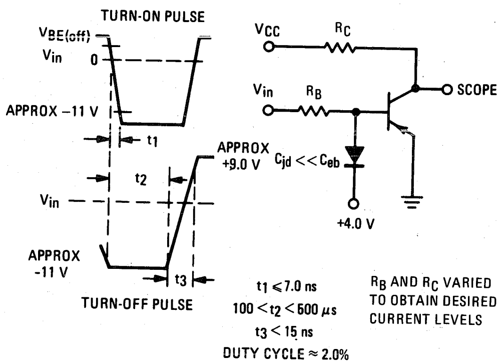


FIGURE 8 – CAPACITANCE

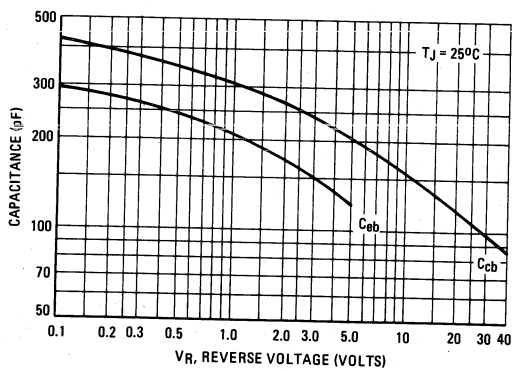


FIGURE 9 – TURN-ON TIME

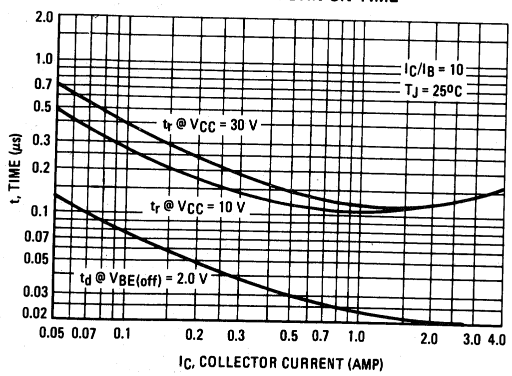


FIGURE 10 – TURN-OFF TIME

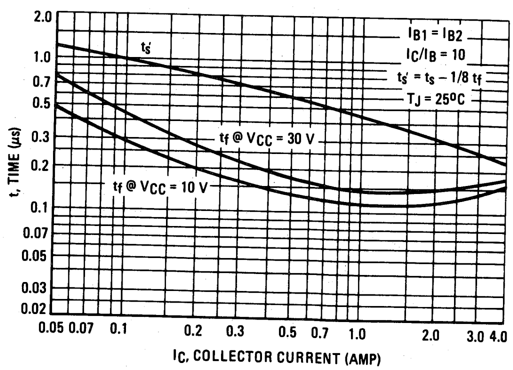
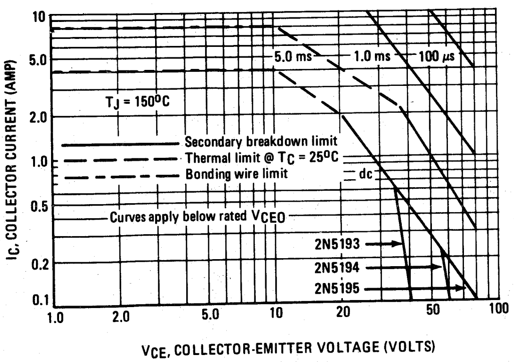


FIGURE 11

RATING AND THERMAL DATA
ACTIVE-REGION SAFE OPERATING AREA

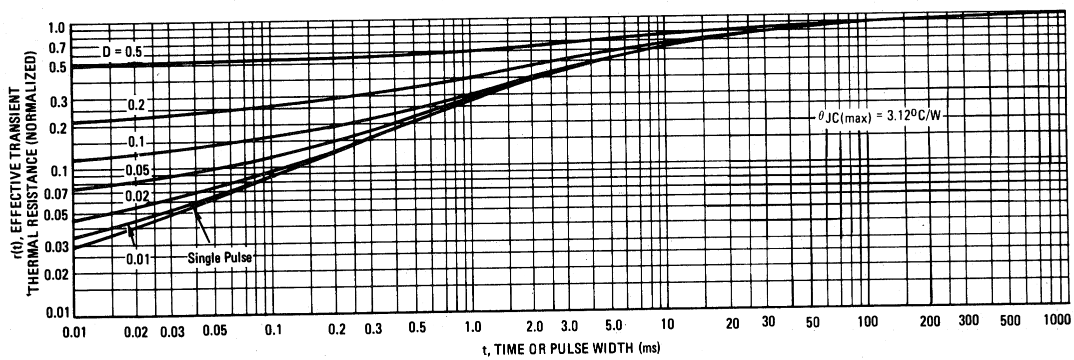


Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

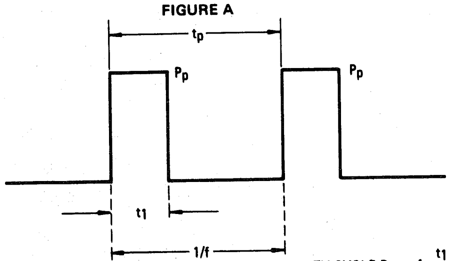
The data of Figure 11 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant$ 150°C. At high-case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 12 – THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



DUTY CYCLE $D = t_1 \cdot f = \frac{t_1}{t_p}$

PEAK PULSE POWER = P_p

A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N5193 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, tp = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of r(t_1, D) is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ C$$

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N5301
2N5302
2N5303

3

HIGH-POWER NPN SILICON TRANSISTORS

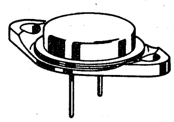
. . . for use in power amplifier and switching circuits applications.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) @ I_C = 200 mAdc (2N5303)
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.75 Vdc (Max) @ I_C = 10 Adc (2N5301, 2N5302)
  1.0 Vdc (Max) @ I_C = 10 Adc (2N5303)
- Excellent Safe Operating Area —
  200 Watt dc Power Rating to 30 Vdc (2N5303)
- Complements to PNP 2N4398, 2N4399 and 2N5745

**20 AND 30 AMPERE
POWER TRANSISTORS**

NPN SILICON

**40-60-80 VOLTS
200 WATTS**



*MAXIMUM RATINGS

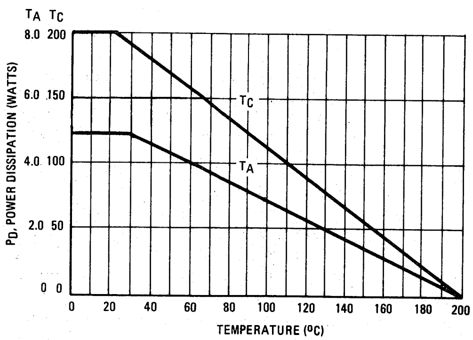
Rating	Symbol	2N5301	2N5302	2N5303	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Collector Current — Continuous	I_C	30	30	20	Adc
Base Current	I_B	← 7.5 →			Adc
Total Device Dissipation @ T_C=25°C Derate above 25°C	P_D	← 200 → ← 1.14 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

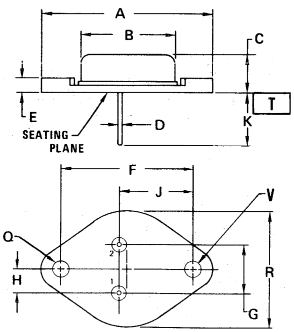
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Case to Ambient	θ_{CA}	34	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 3:
PIN 1. ANODE
2. CATHODE

NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⊕ Ø 0.25 (0.010) Ⓜ T V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⊕ Ø 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

**CASE 11-01
TO-204AA**

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	2N5301	$V_{CEO(sus)}$	40	–	Vdc
	2N5302		60	–	
	2N5303		80	–	
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	2N5301	I_{CEO}	–	5.0	mAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N5302		–	5.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5303		–	5.0	
Collector Cutoff Current (V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5301	I_{CEX}	–	1.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5302		–	1.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5303		–	1.0	
Collector Cutoff Current (V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5301	I_{CEX}	–	10	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5302		–	10	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5303		–	10	
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	2N5301	I_{CBO}	–	1.0	mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5302		–	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5303		–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1) *(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	ALL TYPES	h_{FE}	40	–	–
*(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5303		15	60	
*(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N5301,2N5302		15	60	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5303		5.0	–	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N5301,2N5302		5.0	–	
*Collector-Emitter Saturation Voltage (Note 1) (I_C = 10 Adc, I_B = 1.0 Adc)	2N5301,2N5302	$V_{CE(sat)}$	–	0.75	Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	2N5303		–	1.0	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5303		–	1.5	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N5301,2N5302		–	2.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5303		–	2.0	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N5301,2N5302		–	3.0	
*Base-Emitter Saturation Voltage (Note 1) (I_C = 10 Adc, I_B = 1.0 Adc)	ALL TYPES	$V_{BE(sat)}$	–	1.7	Vdc
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5301,2N5302		–	1.8	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5303		–	2.0	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N5301,2N5302		–	2.5	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5303		–	2.5	
*Base-Emitter On Voltage (Note 1) (I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5303	$V_{BE(on)}$	–	1.5	Vdc
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N5301,2N5302		–	1.7	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5303		–	2.5	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N5301,2N5302		–	3.0	
***DYNAMIC CHARACTERISTICS**					
Current-Gain—Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.0	–	MHz
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	40	–	–
***SWITCHING CHARACTERISTICS**					
Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	–	1.0	µs
Storage Time		t_s	–	2.0	µs
Fall Time		t_f	–	1.0	µs

*Indicates JEDEC Registered Data.
Note 1: Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

FIGURE 2 – TURN-ON TIME

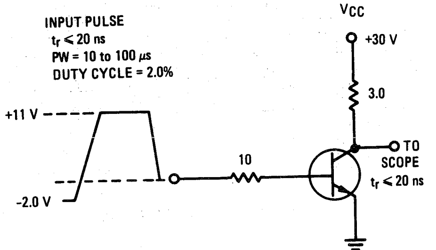


FIGURE 3 – TURN-OFF TIME

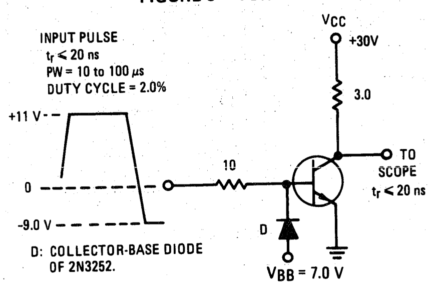


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FIGURE 4 — THERMAL RESPONSE

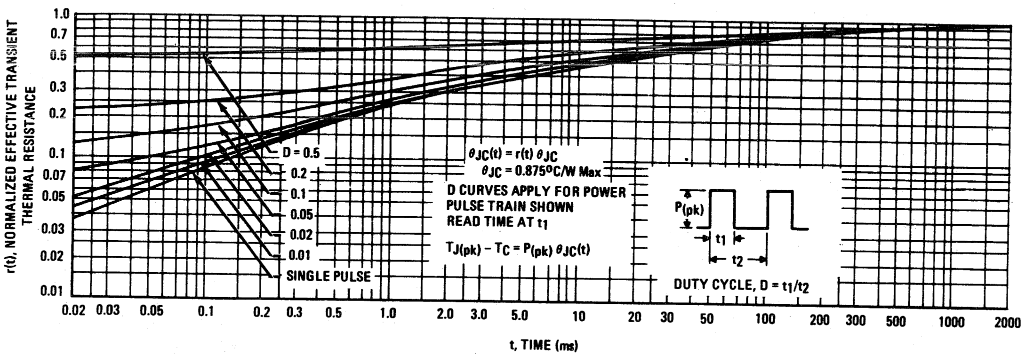

FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA

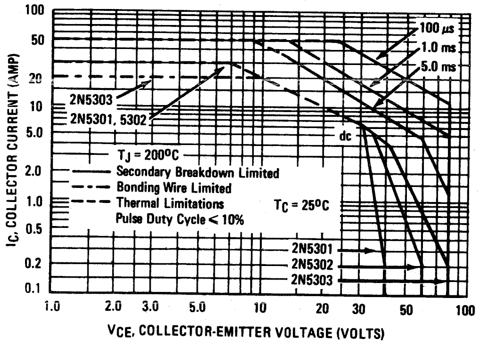

FIGURE 6 — CAPACITANCE versus VOLTAGE

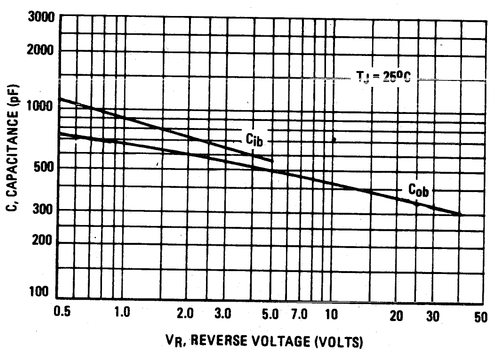

FIGURE 7 — TURN-ON TIME

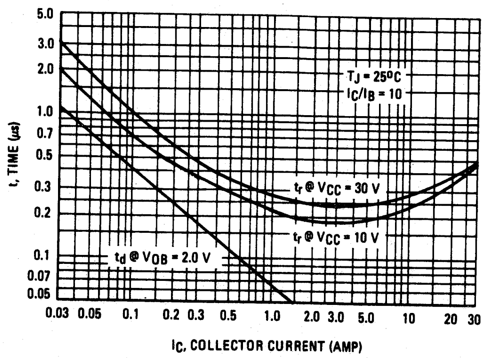

FIGURE 8 — TURN-OFF TIME

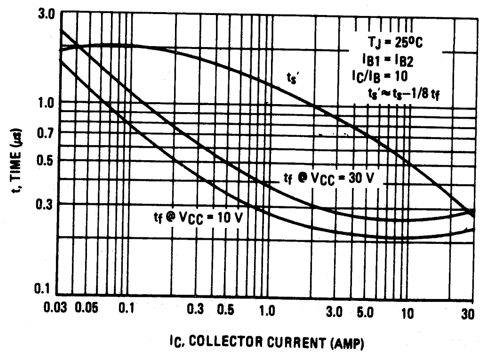

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FIGURE 9 – DC CURRENT GAIN

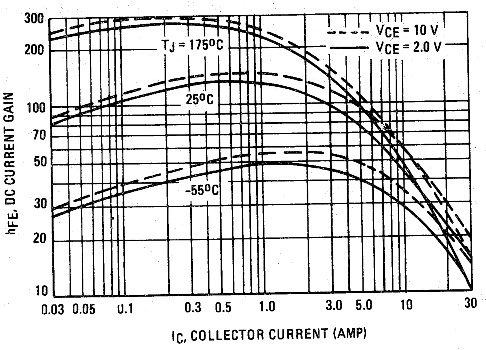


FIGURE 10 – COLLECTOR SATURATION REGION

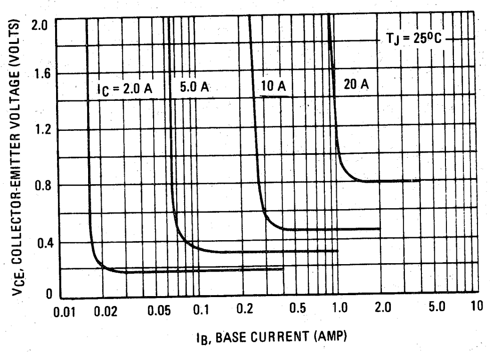


FIGURE 11 – EFFECTS OF BASE-EMITTER RESISTANCE

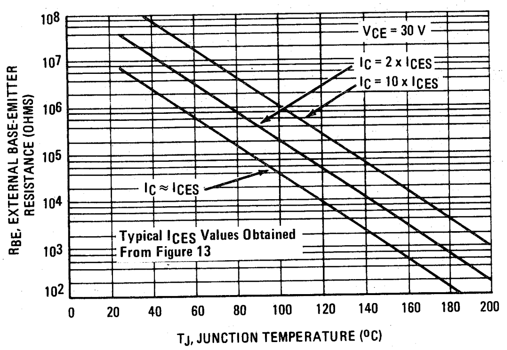


FIGURE 12 – "ON" VOLTAGES

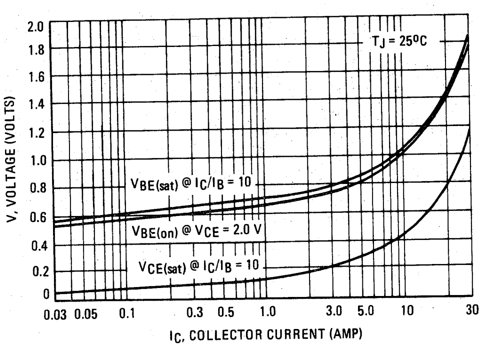


FIGURE 13 – COLLECTOR CUT-OFF REGION

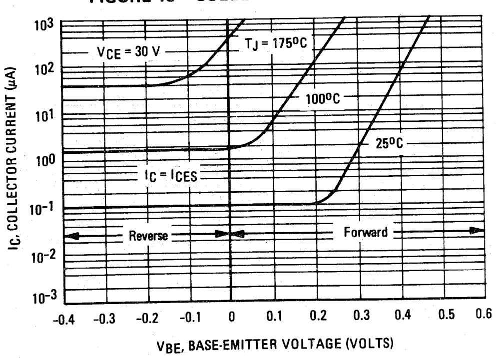
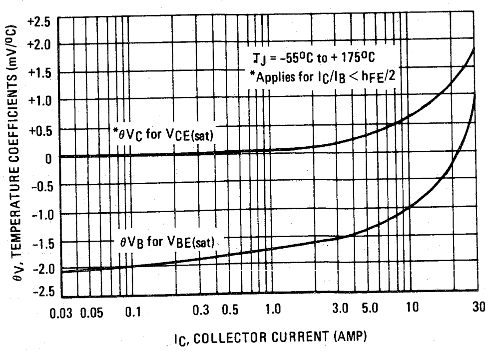


FIGURE 14 – TEMPERATURE COEFFICIENTS



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N5336 thru 2N5339

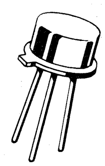
MEDIUM-POWER NPN SILICON TRANSISTORS

. . . designed for switching and wide band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)} = 1.2$ Vdc (Max) @ $I_C = 5.0$ Amp
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-205AD Case for Critical Space-Limited Applications
- Complement to 2N6190 thru 2N6193

5 AMPERE
POWER TRANSISTORS
NPN SILICON

80–100 VOLTS
6 WATTS



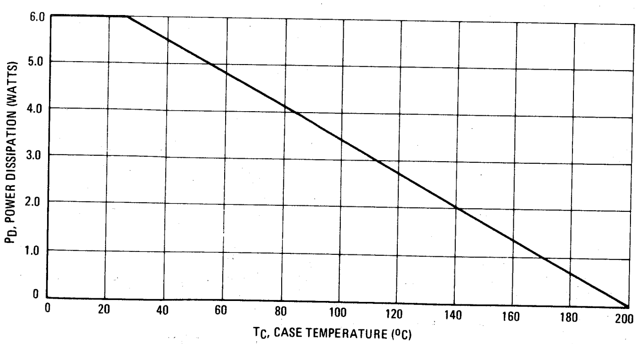
MAXIMUM RATINGS

Rating	Symbol	2N5336 2N5337	2N5338 2N5339	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	6.0 34.3		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

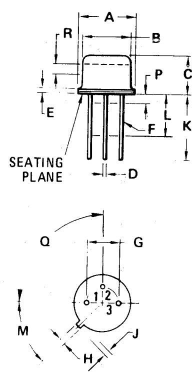
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	29.2	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-205AD

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage*		—	$V_{CEO(sus)}$*			Vdc
(I_C = 50 mAdc, I_B = 0)	2N5336, 2N5337			80	—	
	2N5338, 2N5339			100	—	
Collector Cutoff Current		—	I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N5336, 2N5337			—	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N5338, 2N5339			—	100	
Collector Cutoff Current		12	I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5336, 2N5337			—	10	
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5338, 2N5339			—	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5336, 2N5337			—	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5338, 2N5339			—	1.0	
Collector Cutoff Current		—	I_{CBO}			μAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N5336, 2N5337			—	10	
(V_{CB} = 100 Vdc, I_E = 0)	2N5338, 2N5339			—	10	
Emitter Cutoff Current		—	I_{EBO}			μAdc
(V_{BE} = 6.0 Vdc, I_C = 0)				—	100	
ON CHARACTERISTICS						
DC Current Gain*		8	h_{FE}*			—
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N5336, 2N5338			30	—	
	2N5337, 2N5339			60	—	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N5336, 2N5338			30	120	
	2N5337, 2N5339			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N5336, 2N5338			20	—	
	2N5337, 2N5339			40	—	
Collector-Emitter Saturation Voltage*		9, 11, 13	$V_{CE(sat)}$*			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				—	0.7	
(I_C = 5.0 Adc, I_B = 0.5 Adc)				—	1.2	
Base-Emitter Saturation Voltage*		11, 13	$V_{BE(sat)}$*			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				—	1.2	
(I_C = 5.0 Adc, I_B = 0.5 Adc)				—	1.8	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 10 MHz)		—	f_T	30	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		7	C_{ob}	—	250	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		7	C_{ib}	—	1,000	pF
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc,	2, 3	t_d	—	100	ns
Rise Time	I_C = 2.0 Adc, I_{B1} = 0.2 Adc)		t_r	—	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	2, 6	t_s	—	2.0	μs
Fall Time	I_{B1} = I_{B2} = 0.2 Adc)		t_f	—	200	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

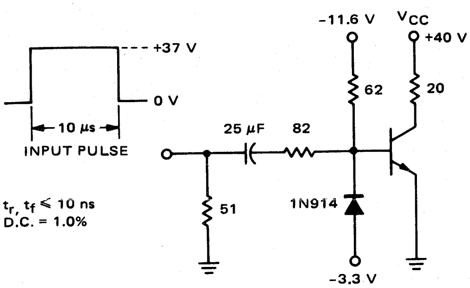


FIGURE 3 — TURN-ON TIME

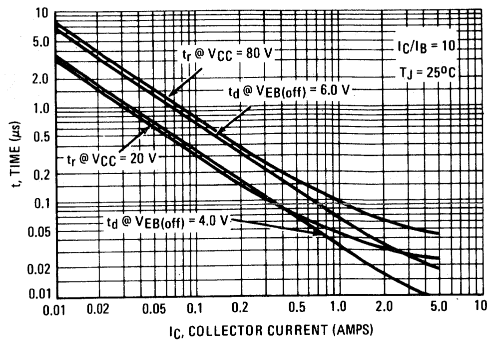


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FIGURE 4 – THERMAL RESPONSE

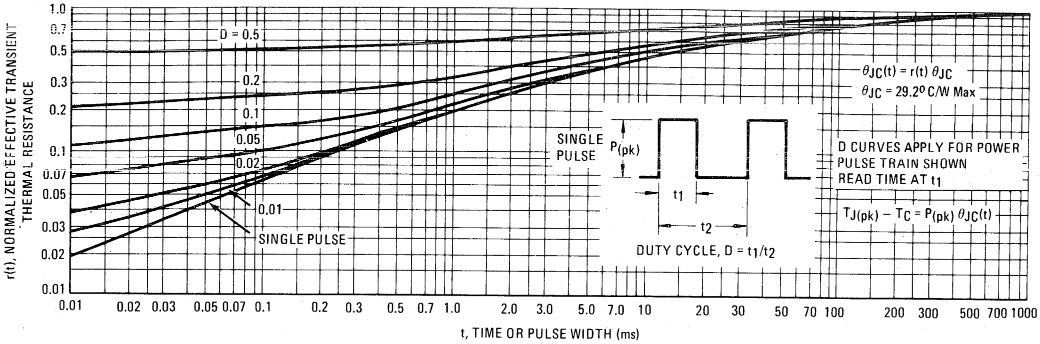
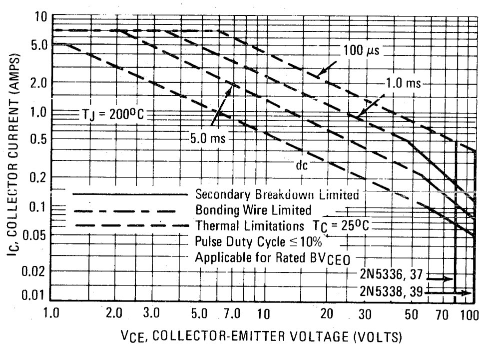


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

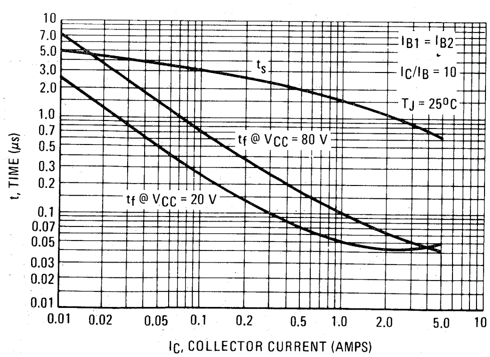


FIGURE 7 – CAPACITANCE versus VOLTAGE

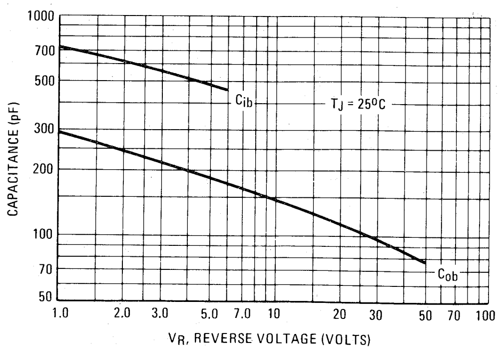


FIGURE 8 — DC CURRENT GAIN

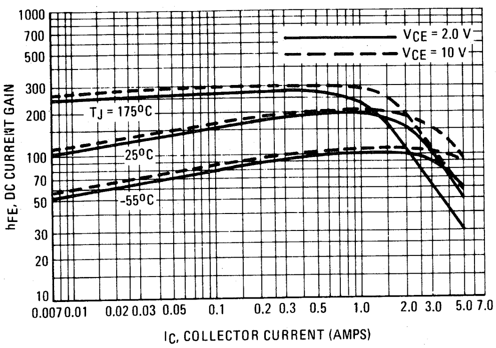


FIGURE 9 — COLLECTOR SATURATION REGION

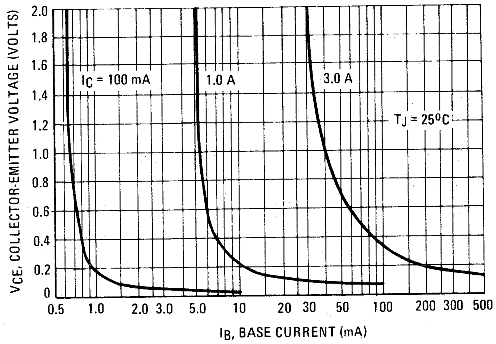


FIGURE 10 — EFFECTS OF BASE-EMITTER RESISTANCE

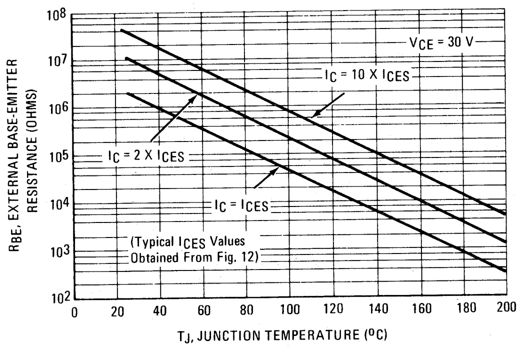


FIGURE 11 — ON VOLTAGES

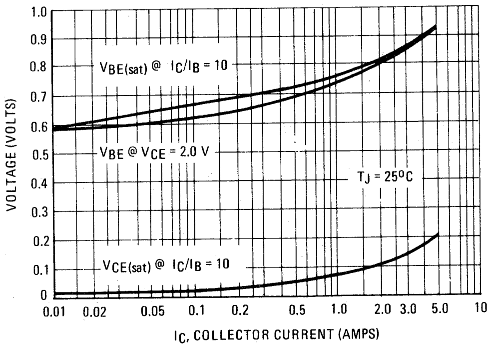


FIGURE 12 — COLLECTOR CUT-OFF REGION

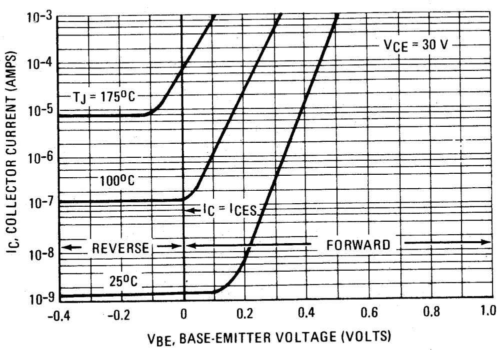
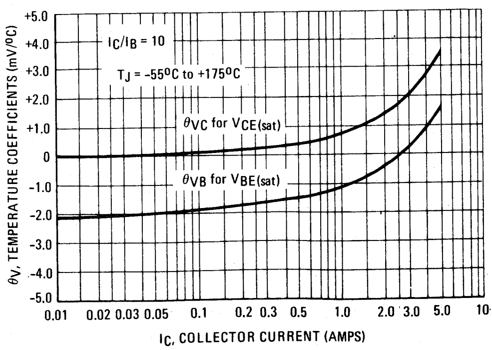


FIGURE 13 — TEMPERATURE COEFFICIENTS



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N5344

HIGH VOLTAGE POWER PNP SILICON TRANSISTOR

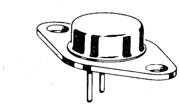
. . . designed for high-voltage switching and amplifier applications.

- High Voltage Rating — V_{CEO} = 250 Vdc
- Fast Switching Time — Typically Less Than 550 ns Total @ V_{CC} = 100 Vdc
- High Current-Gain-Bandwidth Product — f_T = 60 MHz (Min) @ I_C = 100 mAdc
- Packaged in the Compact, High-Efficiency TO-213AA Case

1 AMPERE

POWER TRANSISTOR
PNP SILICON

250-300 VOLTS
40 WATTS

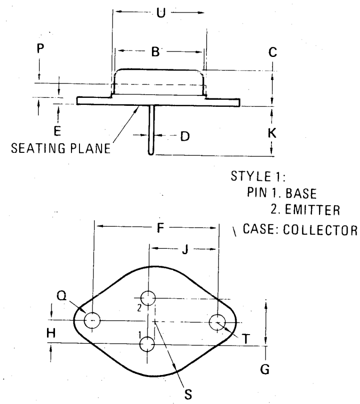


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	250	Vdc
Collector-Base Voltage	V_{CB}	250	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	1.0	Adc
Base Current — Continuous	I_B	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 228	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.38	°C/W



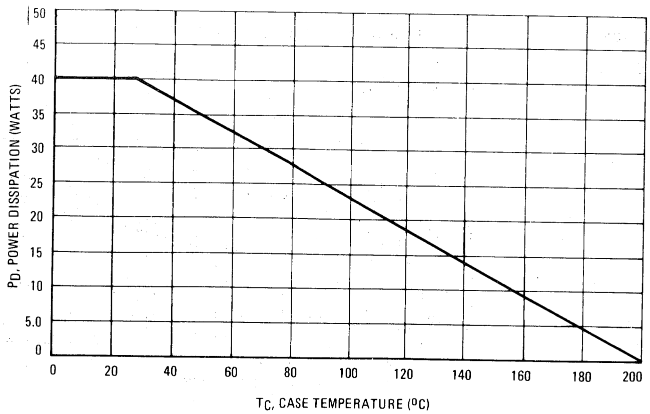
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves Are Indicated By Figure 5.
All Limits Are Applicable And Must Be Observed

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	2N5344	5	$V_{CEO(sus)}$	250	—	Vdc
Collector Cutoff Current (V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5344	10, 12	I_{CEX}	—	100	μAdc
(V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5344			—	1.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		—	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		—	I_{EBO}	—	0.1	mAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)		8	h_{FE}	25	150	—
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)				7.0	—	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		9, 11, 13	$V_{CE(sat)}$	—	3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		11, 13	$V_{BE(sat)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 100 mAdc, V_{CE} = 20 Vdc, f = 10 MHz)		—	f_T	60	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0)		7	C_{ob}	—	200	pF
SWITCHING CHARACTERISTICS						
Turn-On	(V_{CC} = 100 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc)	2, 3	t_{on}	—	200	ns
Turn-Off	(V_{CC} = 100 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc)	2, 6	t_{off}	—	700	ns

(1) Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

3

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

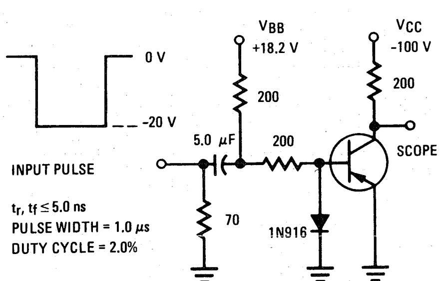


FIGURE 3 — TURN-ON TIME

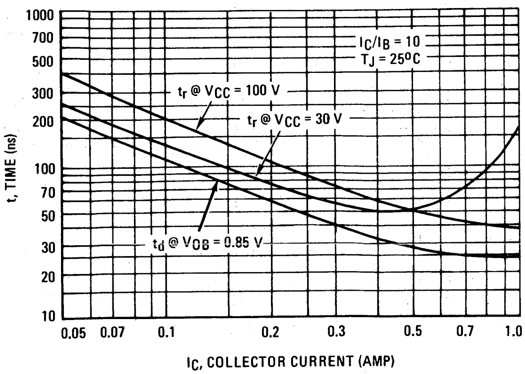


FIGURE 4 — THERMAL RESPONSE

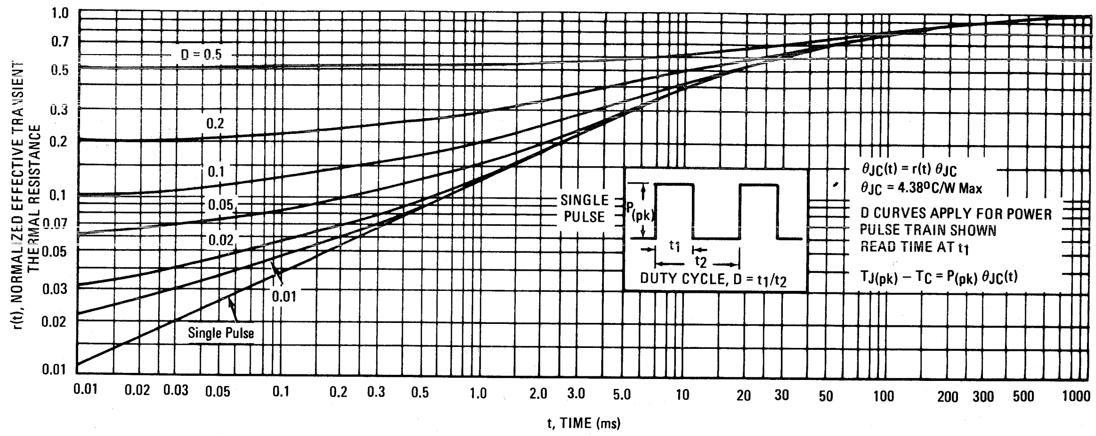
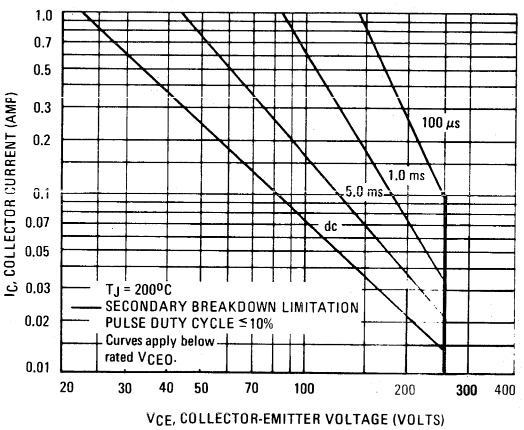


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \le 200^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

3

FIGURE 6 — TURN-OFF TIME

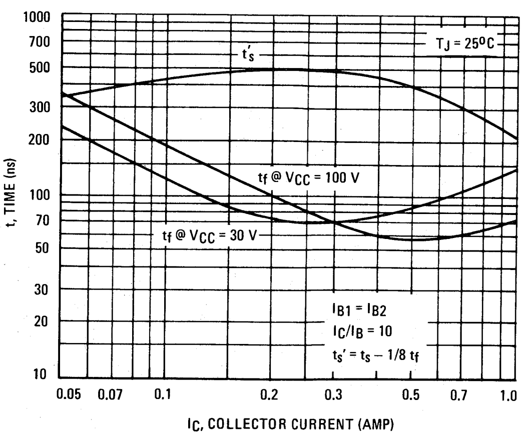
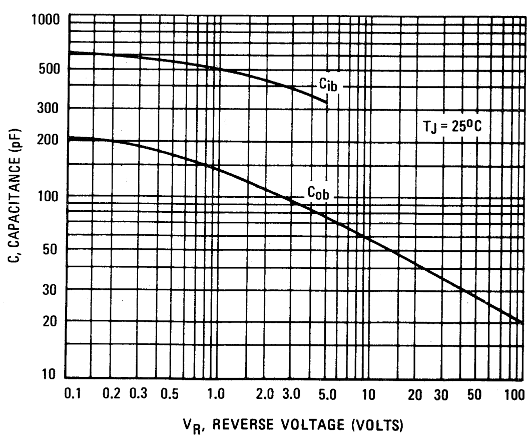


FIGURE 7 — CAPACITANCES



TYPICAL DC CHARACTERISTICS

FIGURE 8 — DC CURRENT GAIN

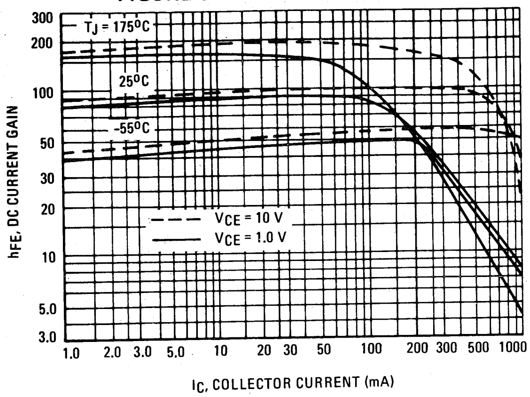


FIGURE 9 — COLLECTOR SATURATION REGION

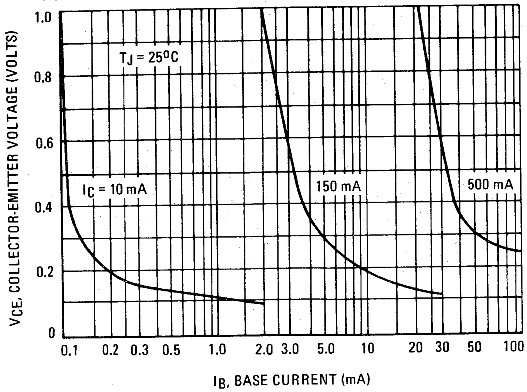


FIGURE 10 — EFFECTS OF BASE-EMITTER RESISTANCE

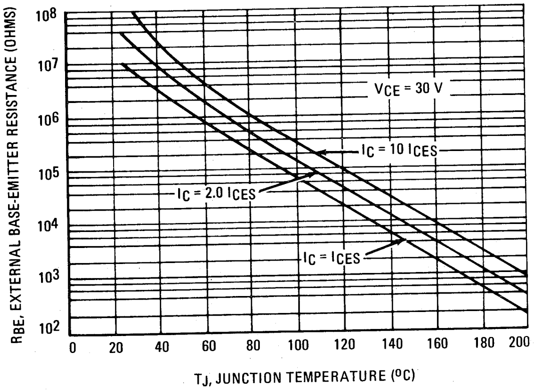


FIGURE 11 — "ON" VOLTAGES

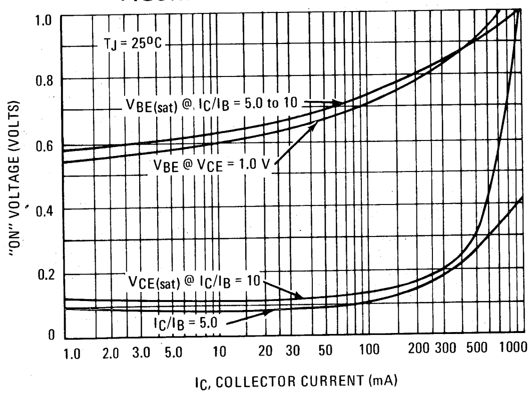


FIGURE 12 — COLLECTOR CUT-OFF REGION

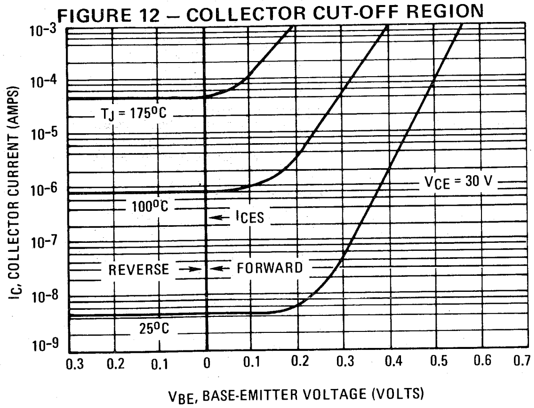
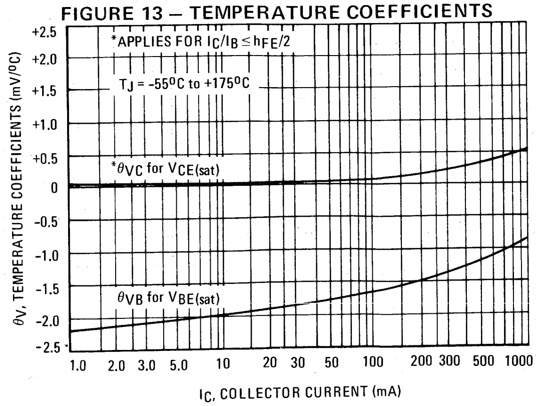


FIGURE 13 — TEMPERATURE COEFFICIENTS



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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N5428 thru 2N5430

MEDIUM-POWER NPN SILICON TRANSISTORS

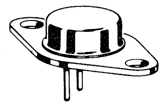
. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 7.0 Adc
- DC Current Gain Specified to 7 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-213AA Case

7 AMPERE

POWER TRANSISTORS
NPN SILICON

80–100 VOLTS
40 WATTS



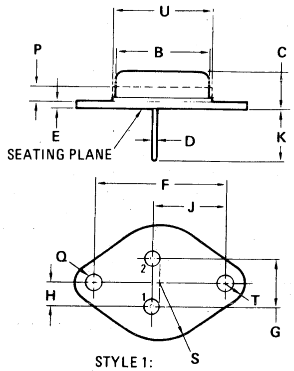
*MAXIMUM RATINGS

Rating	Symbol	2N5428	2N5429 2N5430	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	7.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 228		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.37	°C/W

* Indicates JEDEC Registered Data



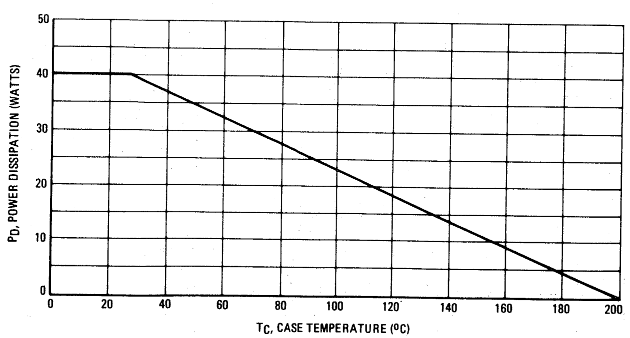
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



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***ELECTRICAL CHARACTERISTICS** (T_C = 25°C, unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		–	$V_{CEO(sus)}$*			Vdc
(I_C = 50 mAdc, I_B = 0)	2N5428			80	–	
	2N5429, 2N5430			100	–	
Collector Cutoff Current		–	I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N5428			–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N5429, 2N5430			–	100	
Collector Cutoff Current		12	I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5428			–	10	
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5429, 2N5430			–	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5428			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5429, 2N5430			–	1.0	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		–	I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		–	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)						
DC Current Gain		8	h_{FE}*			–
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N5429			30	–	
	2N5428, 2N5430			60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N5429			30	120	
	2N5428, 2N5430			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N5429			20	–	
	2N5428, 2N5430			40	–	
Collector-Emitter Saturation Voltage		9, 11, 13	$V_{CE(sat)}$*			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	0.7	
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	1.2	
Base-Emitter Saturation Voltage		11, 13	$V_{BE(sat)}$*			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	1.2	
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	2.0	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		–	f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		7	C_{ob}	–	250	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		7	C_{ib}	–	1,000	pF
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc,	2, 3	t_d	–	100	ns
Rise Time	I_C = 2.0 Adc, I_{B1} = 200 mAdc)		t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	2, 6	t_s	–	2.0	μs
Fall Time	I_{B1} = I_{B2} = 200 mAdc)		t_f	–	200	ns

*Indicates JEDEC Registered Data. (1)Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

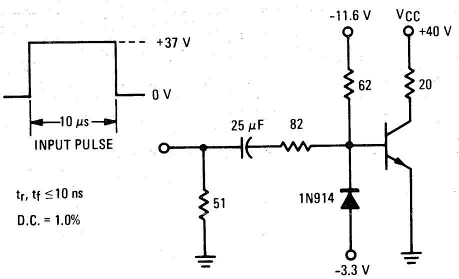

FIGURE 3 – TURN-ON TIME

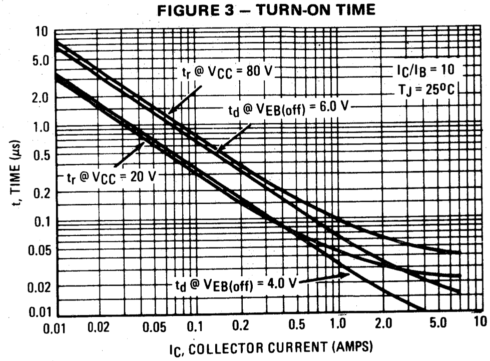

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FIGURE 4 — THERMAL RESPONSE

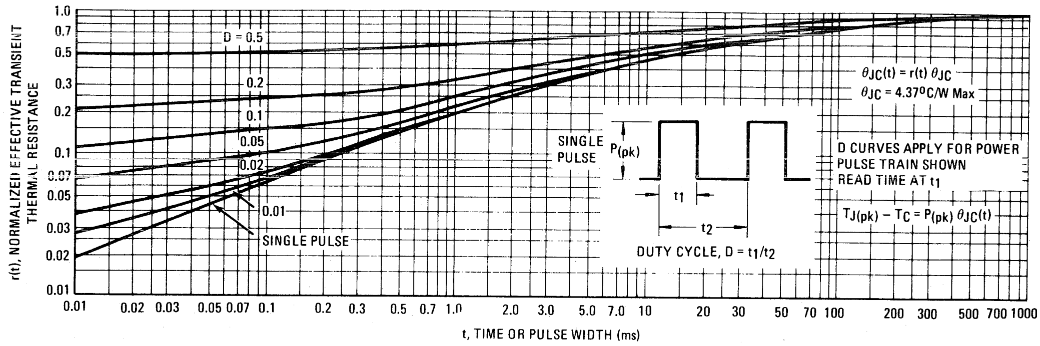
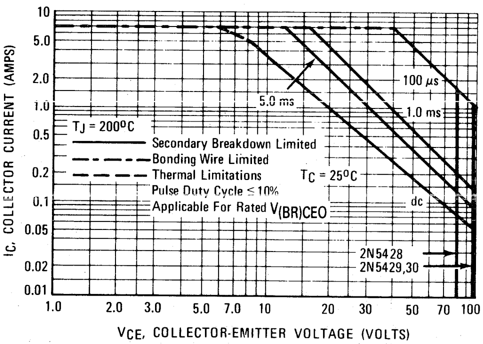


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

3

FIGURE 6 — TURN-OFF TIME

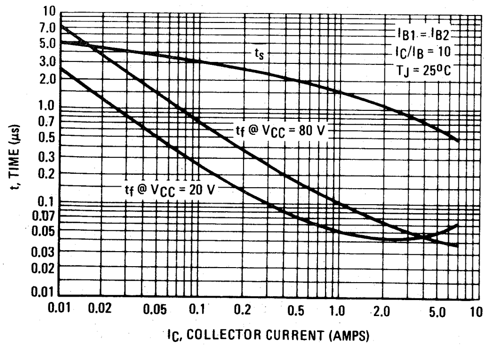


FIGURE 7 — CAPACITANCE versus VOLTAGE

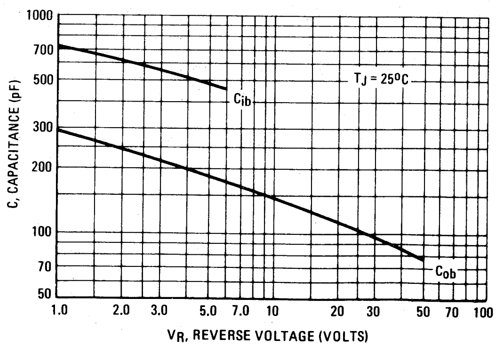


FIGURE 8 – DC CURRENT GAIN

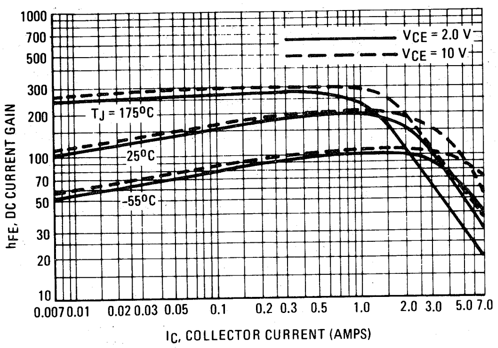


FIGURE 9 – COLLECTOR SATURATION REGION

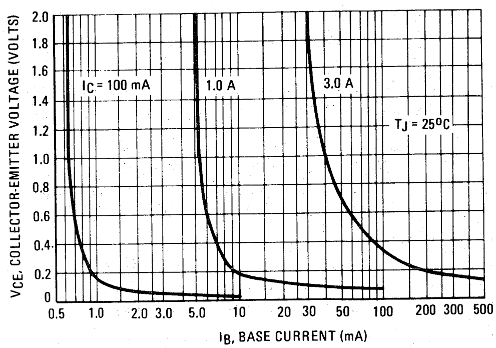


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

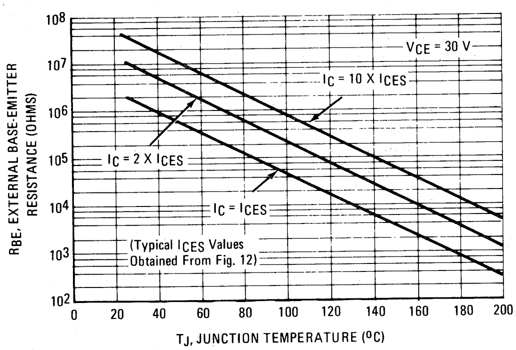


FIGURE 11 – "ON" VOLTAGES

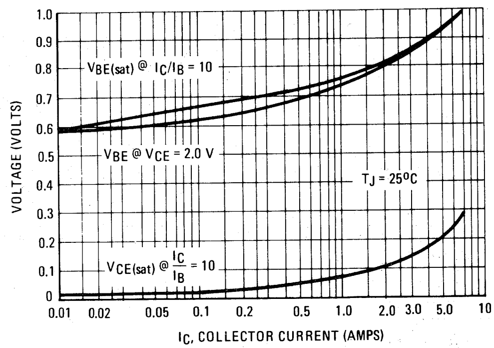


FIGURE 12 – COLLECTOR CUT-OFF REGION

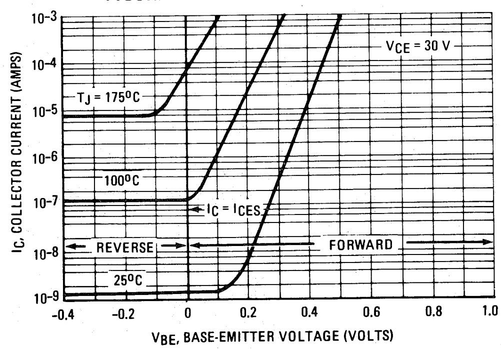
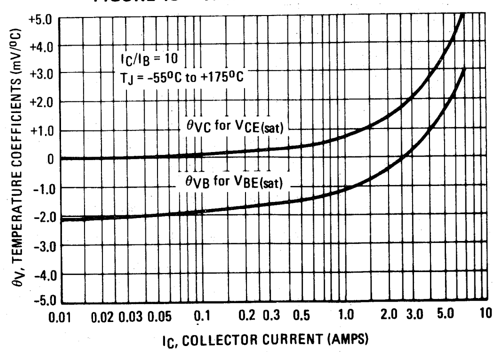


FIGURE 13 – TEMPERATURE COEFFICIENTS



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
2N5629	2N6029
2N5630	2N6030
2N5631	2N6031

HIGH-VOLTAGE – HIGH POWER TRANSISTORS

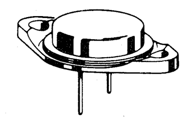
. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc – 2N5629, 2N6029
  = 120 Vdc – 2N5630, 2N6030
  = 140 Vdc – 2N5631, 2N6031
- High DC Current Gain – @ I_C = 8.0 Adc
  h_{FE} = 25 (Min) – 2N5629, 2N6029
  = 20 (Min) – 2N5630, 2N6030
  = 15 (Min) – 2N5631, 2N6031
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc

16 AMPERE

**POWER TRANSISTORS
COMPLEMENTARY SILICON**

**100-120-140 VOLTS
200 WATTS**



*MAXIMUM RATINGS

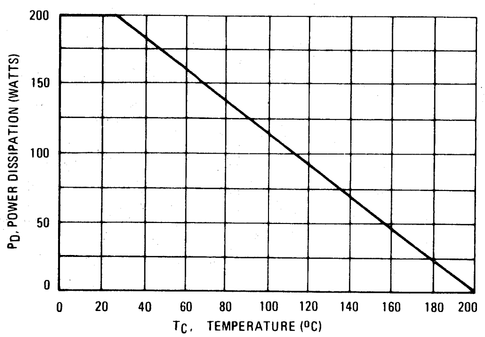
Rating	Symbol	2N5629 2N6029	2N5630 2N6030	2N5631 2N6031	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}		← 7.0 →		Vdc
Collector Current Continuous Peak	I_C		← 16 → ← 20 →		Adc
Base Current Continuous	I_B		← 5.0 →		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		← 200 → ← 1.14 →		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +200		°C

*THERMAL CHARACTERISTICS

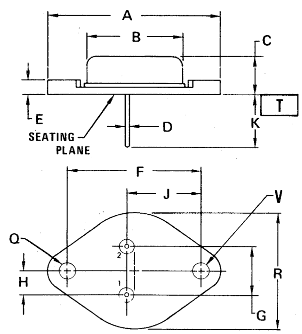
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



Safe Area Curves are indicated by Figure 5 All Limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 3:
PIN 1. ANODE
2. CATHODE

NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⊕ ∅ 0.25 (0.010) Ⓜ T V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⊕ ∅ 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

**CASE 11-01
TO-204AA**

3

2N5629, 2N5630, 2N5631 NPN
2N6029, 2N6030, 2N6031 PNP

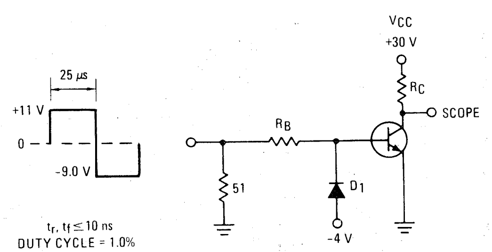
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5629, 2N6029 2N5630, 2N6030 2N5631, 2N6031	$V_{CEO(sus)}$	100 120 140	— —	Vdc
Collector-Emitter Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 70 Vdc, I_B = 0)	2N5629, 2N6029 2N5630, 2N6030 2N5631, 2N6031	I_{CEO}	— — —	2.0 2.0 2.0	mAdc
Collector-Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	— —	2.0 7.0	mAdc
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	2.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 16 Adc, V_{CE} = 2.0 Vdc)	2N5629, 2N6029 2N5630, 2N6030 2N5631, 2N6031 All Types	h_{FE}	25 20 15 4.0	100 80 60 —	—
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 16 Adc, I_B = 4.0 Adc)	All Types	$V_{CE(sat)}$	— —	1.0 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	—	1.8	Vdc
Base-Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5629, 30, 31 2N6029, 30, 31	C_{ob}	—	500 1000	pF
Small-Signal Current Gain (I_C = 4.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15	—	—

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≥2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

3

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE IB ~100 mA
MSD6100 USED BELOW IB ~100 mA

For PNP test circuit, reverse all polarities and D1.

FIGURE 3 — TURN-ON TIME

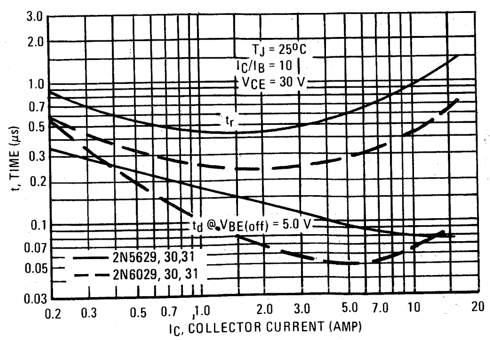


FIGURE 4 – THERMAL RESPONSE

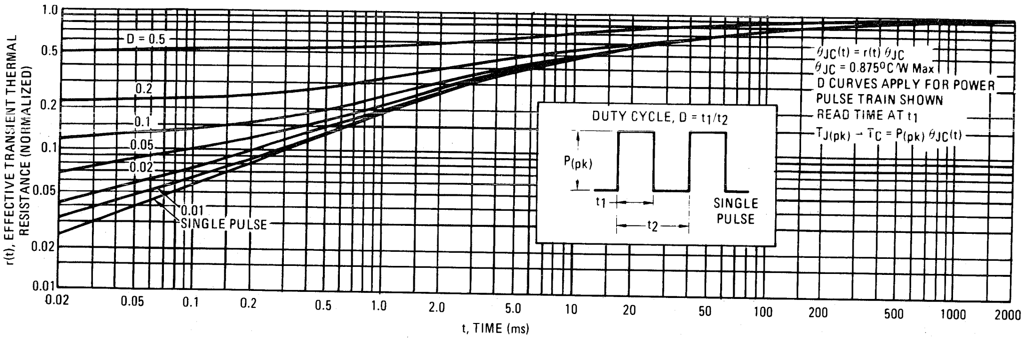
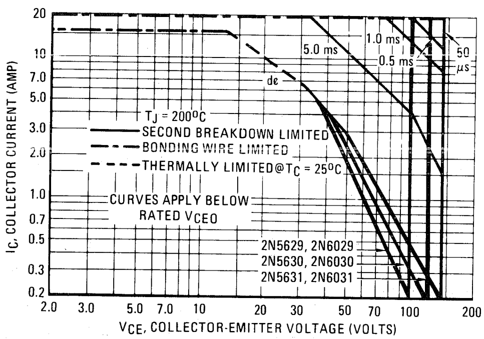


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



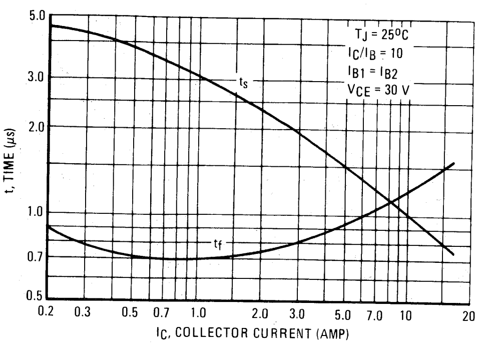
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

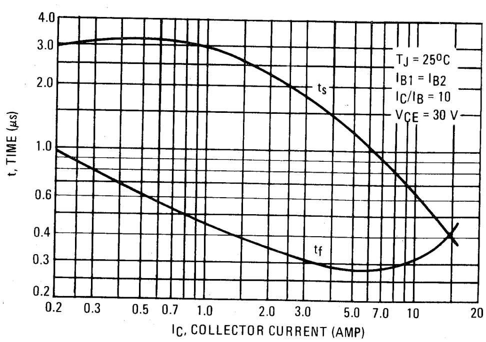
The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN
2N5629, 2N5630, 2N5631

PNP
2N6029, 2N6030, 2N6031

FIGURE 6 – TURN-OFF TIME

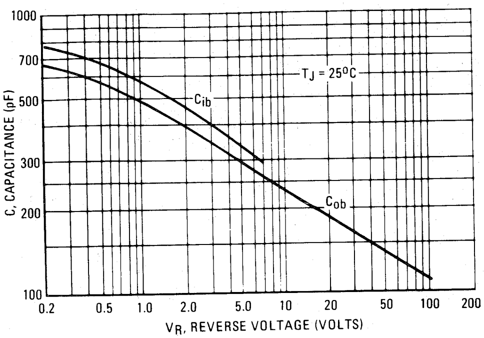




NPN
2N5629, 2N5630, 2N5631

PNP
2N6029, 2N6030, 2N6031

FIGURE 7 – CAPACITANCE



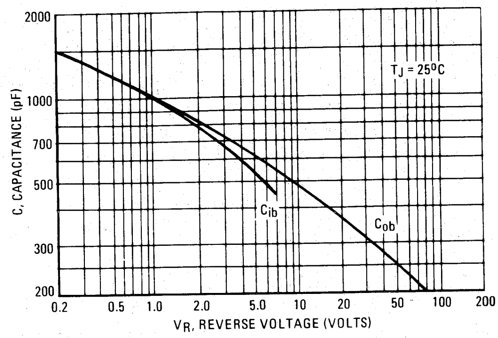
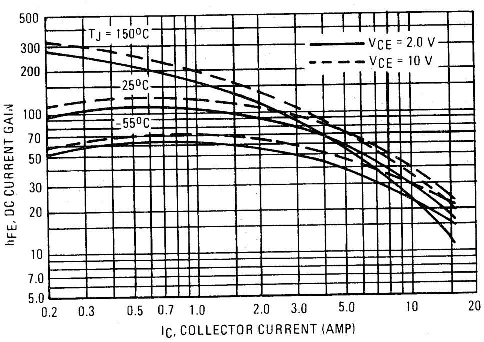


FIGURE 8 – DC CURRENT GAIN



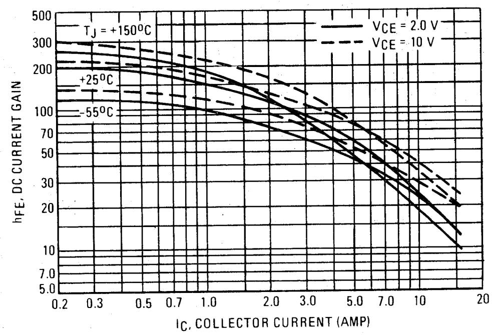
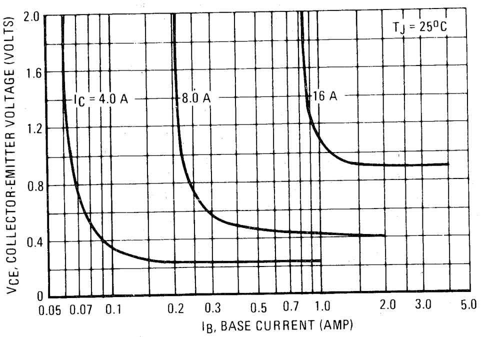
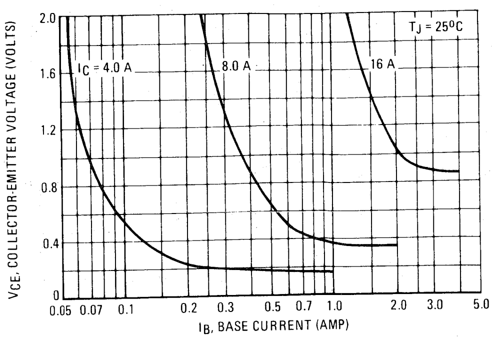


FIGURE 9 – COLLECTOR SATURATION REGION





3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N5655
2N5656
2N5657

PLASTIC NPN SILICON HIGH-VOLTAGE POWER TRANSISTOR

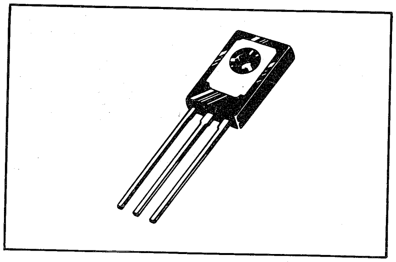
. . . designed for use in line-operated equipment such as audio output amplifiers; low-current, high-voltage converters; and AC line relays

- Excellent DC Current Gain — h_{FE} = 30-250 @ I_C = 100 mAdc
- Current-Gain — Bandwidth Product — f_T = 10 MHz (Min) @ I_C = 50 mAdc
- Packaged in Thermopad Case for Low Cost

0.5 AMPERE

POWER TRANSISTORS NPN SILICON

250–300–350 VOLTS
20 WATTS



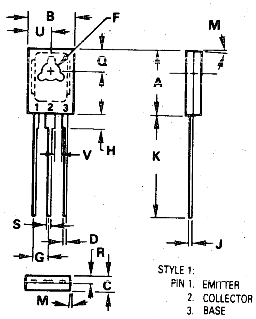
*MAXIMUM RATINGS

Rating	Symbol	2N5655	2N5656	2N5657	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector-Base Voltage	V_{CB}	275	325	375	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 0.5 → ← 1.0 →			Adc
Base Current	I_B	← 0.25 →			Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	20 0.16			Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^oC/W$

*Indicates JEDEC Registered Data



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-225AA

FIGURE 1 — POWER DERATING

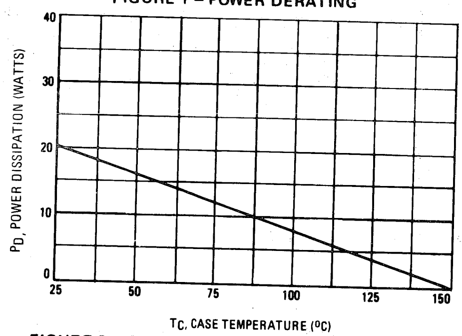
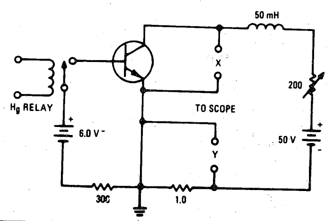


FIGURE 2 — SUSTAINING VOLTAGE TEST CIRCUIT



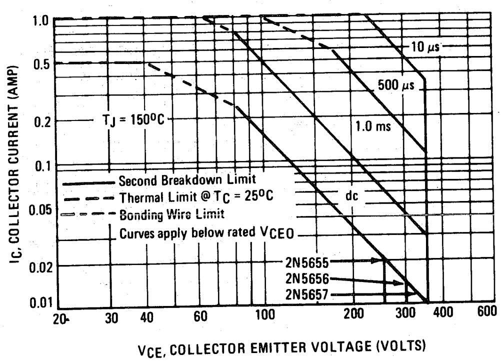
Safe Area Limits are indicated by Figures 3 and 4. Both limits are applicable and must be observed.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc (inductive), L = 50 mH)	2N5655	$V_{CEO(sus)}$	250	–	Vdc
	2N5656		300	–	
	2N5657		350	–	
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	2N5655	$V_{(BR)CEO}$	250	–	Vdc
	2N5656		300	–	
	2N5657		350	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 150 Vdc, I_B = 0)	2N5655		–	0.1	
(V_{CE} = 200 Vdc, I_B = 0)	2N5656		–	0.1	
(V_{CE} = 250 Vdc, I_B = 0)	2N5657		–	0.1	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5655		–	0.1	
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5656		–	0.1	
(V_{CE} = 350 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5657		–	0.1	
(V_{CE} = 150 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5655		–	1.0	
(V_{CE} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5656		–	1.0	
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5657		–	1.0	
Collector Cutoff Current		I_{CBO}			µAdc
(V_{CB} = 275 Vdc, I_E = 0)	2N5655		–	10	
(V_{CB} = 325 Vdc, I_E = 0)	2N5656		–	10	
(V_{CB} = 375 Vdc, I_E = 0)	2N5657		–	10	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	10	µAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 50 mAdc, V_{CE} = 10 Vdc)			25	–	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)			30	250	
(I_C = 250 mAdc, V_{CE} = 10 Vdc)			15	–	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 100 mAdc, I_B = 10 mAdc)			–	1.0	
(I_C = 250 mAdc, I_B = 25 mAdc)			–	2.5	
(I_C = 500 mAdc, I_B = 100 mAdc)			–	10	
Base-Emitter Voltage (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc)		V_{BE}	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	10	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	25	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–

*Indicates JEDEC Registered Data for 2N5655 Series.
(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.
(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 3 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 – CURRENT GAIN

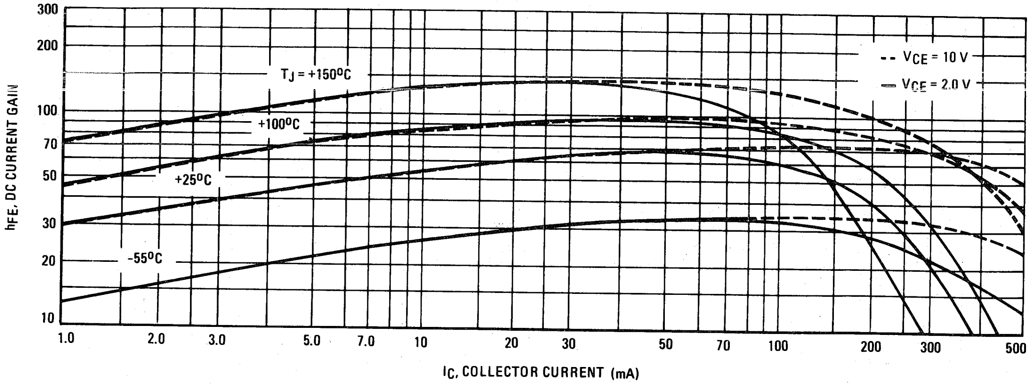


FIGURE 5 – "ON" VOLTAGES

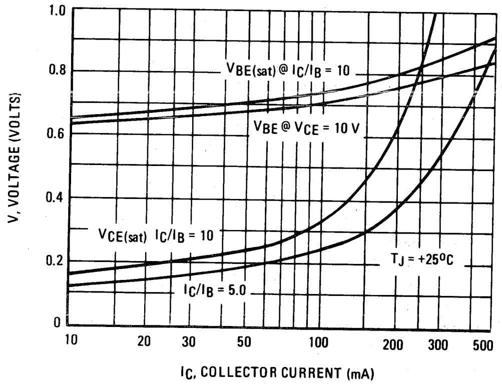


FIGURE 6 – CAPACITANCE

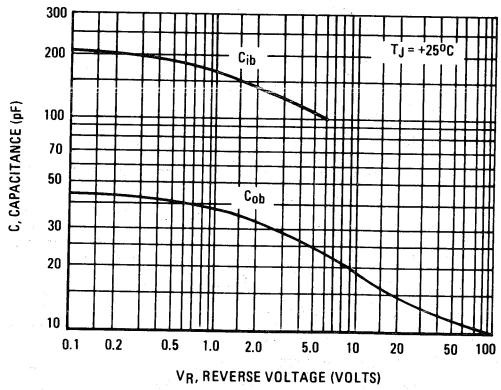


FIGURE 7 – TURN-ON TIME

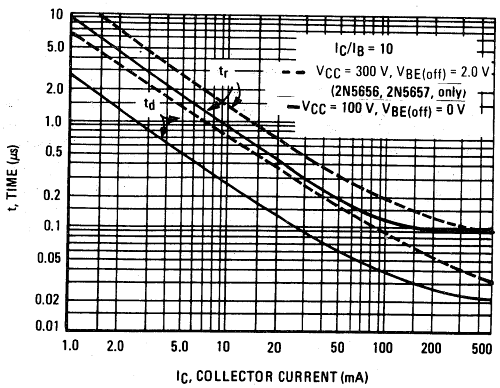
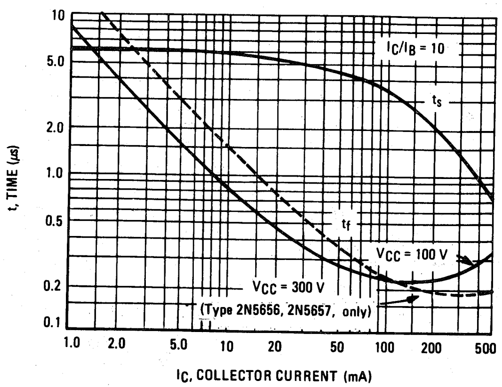


FIGURE 8 – TURN-OFF TIME



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
2N5683, 2N5684
NPN
2N5685, 2N5686

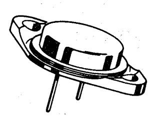
HIGH-CURRENT COMPLEMENTARY SILICON POWER TRANSISTORS

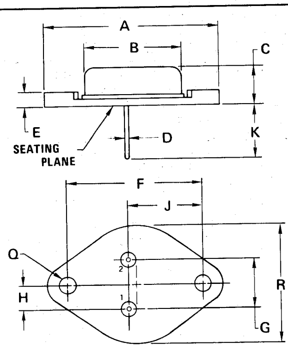
. . . designed for use in high-power amplifier and switching circuit applications.

- High Current Capability — I_C Continuous = 50 Amperes.
- DC Current Gain — h_{FE} = 15 - 60 @ I_C = 25 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 25 Adc

50 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60–80 VOLTS
300 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

*MAXIMUM RATINGS

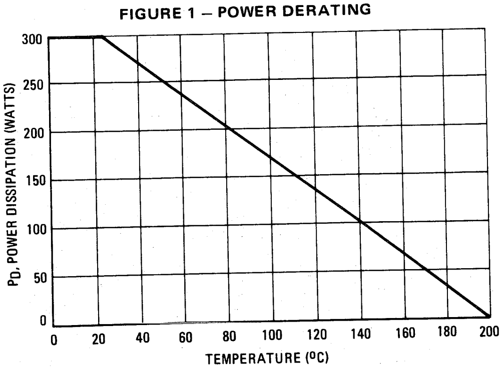
Rating	Symbol	2N5683 2N5685	2N5684 2N5686	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	50		Adc
Base Current	I_B	15		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.715		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.584	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

3

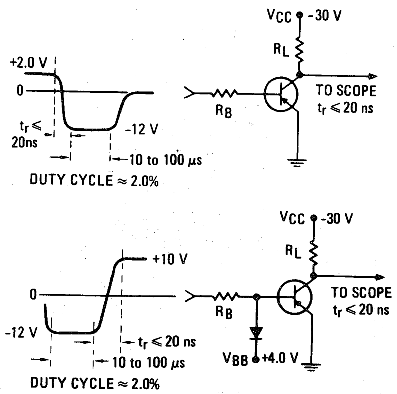
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Note 1) (I_C = 0.2 Adc, I_B = 0)	2N5683, 2N5685 2N5684, 2N5686	$V_{CEO(sus)}$	60 80	– –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	2N5683, 2N5685 2N5684, 2N5686	I_{CEO}	– –	1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5683, 2N5685 2N5684, 2N5686 2N5683, 2N5685 2N5684, 2N5686	I_{CEX}	– – – –	2.0 2.0 10 10	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	2N5683, 2N5685 2N5684, 2N5686	I_{CBO}	– –	2.0 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1) (I_C = 25 Adc, V_{CE} = 2.0 Vdc) (I_C = 50 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	15 5.0	60 –	–
Collector-Emitter Saturation Voltage (Note 1) (I_C = 25 Adc, I_B = 2.5 Adc) (I_C = 50 Adc, I_B = 10 Adc)		$V_{CE(sat)}$	– –	1.0 5.0	Vdc
Base-Emitter Saturation Voltage (Note 1) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter On Voltage (Note 1) (I_C = 25 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 5.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5683, 2N5684 2N5685, 2N5686	C_{ob}	– –	2000 1200	pF
Small-Signal Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	15	–	

*Indicates JEDEC Registered Data

Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

FIGURE 3 – TURN-ON TIME

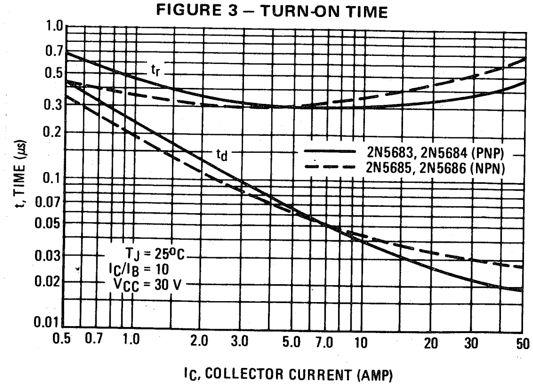


FIGURE 4 – THERMAL RESPONSE

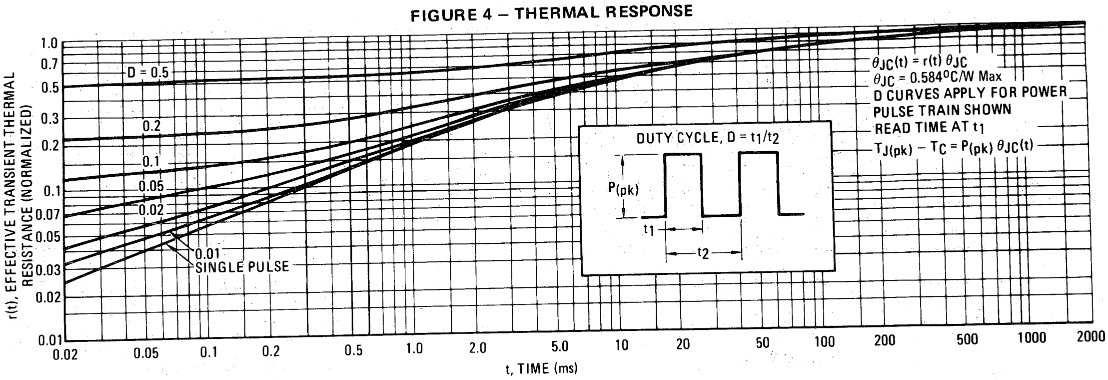
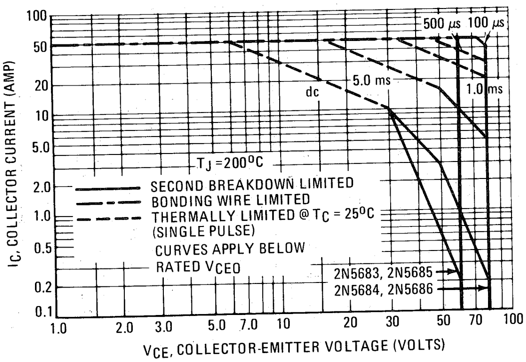


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

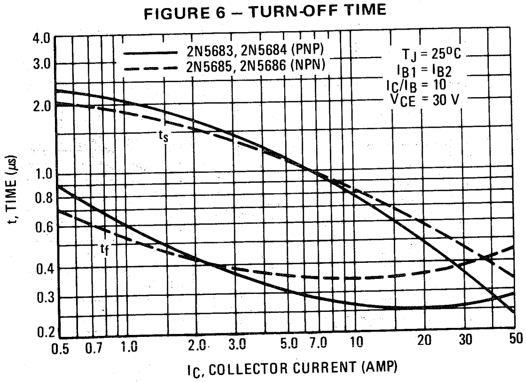
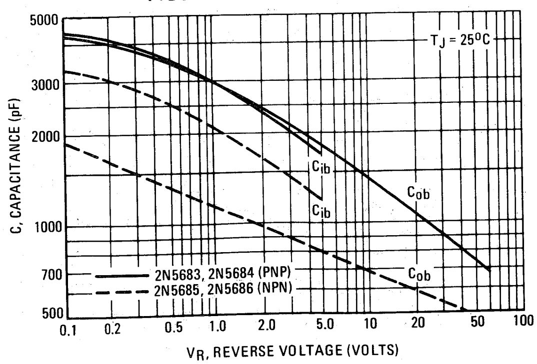


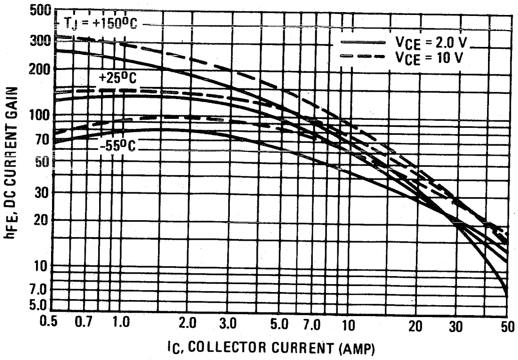
FIGURE 7 – CAPACITANCE



PNP
2N5683, 2N5684

NPN
2N5685, 2N5686

FIGURE 8 — DC CURRENT GAIN



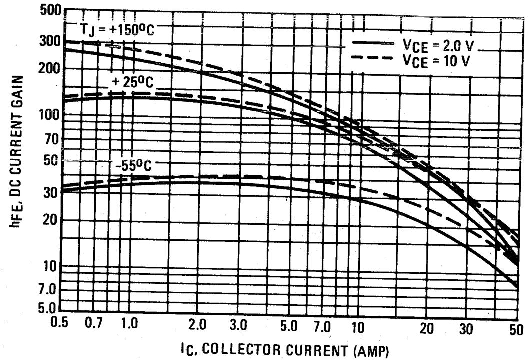
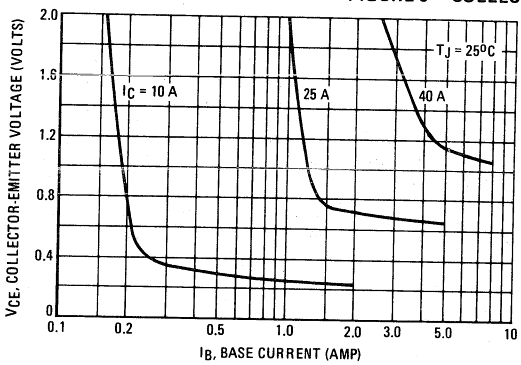


FIGURE 9 — COLLECTOR SATURATION REGION



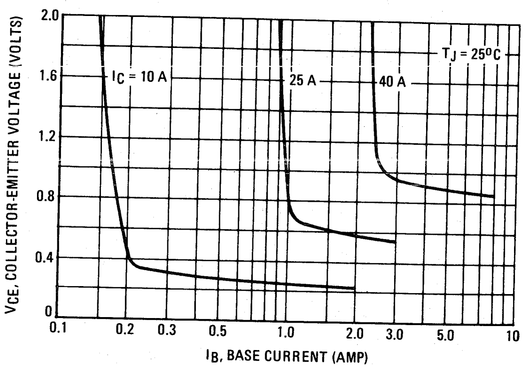
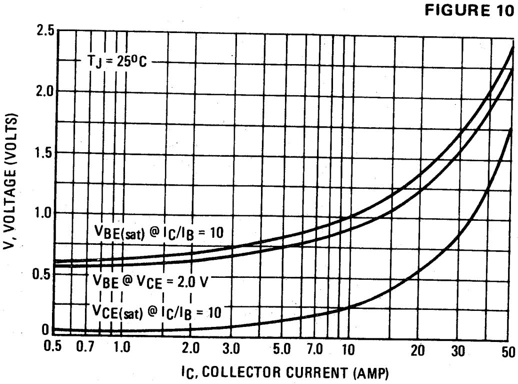
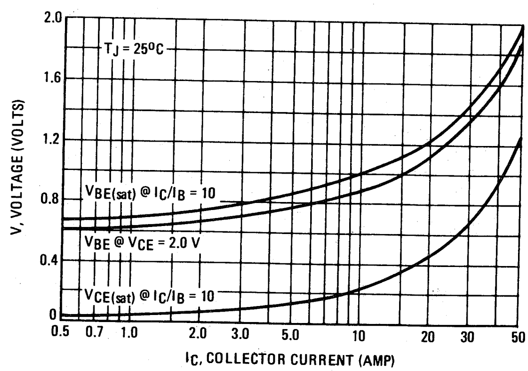


FIGURE 10 — "ON" VOLTAGES





3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

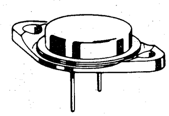
2N5758
2N5760

HIGH-VOLTAGE HIGH-POWER SILICON TRANSISTORS

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min) — 2N5758
  = 140 Vdc (Min) — 2N5760
- DC Current Gain @ I_C = 3.0 Adc —
  h_{FE} = 25 (Min) — 2N5758
  = 15 (Min) — 2N5760
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 3.0 Adc

6 AMPERE
POWER TRANSISTORS
NPN SILICON
100–140 VOLTS
150 WATTS



***MAXIMUM RATINGS**

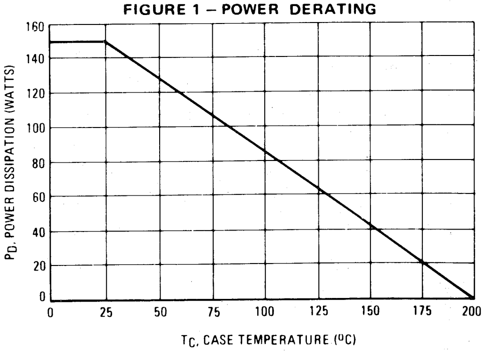
Rating	Symbol	2N5758	2N5760	Unit
Collector-Emitter Voltage	V_{CEO}	100	140	Vdc
Collector-Base Voltage	V_{CB}	100	140	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	6.0 10		Adc
Base Current	I_B	4.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857		Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

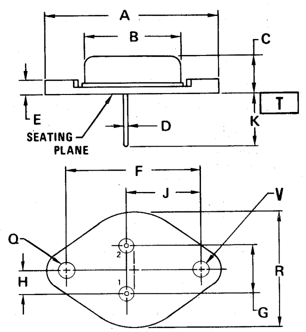
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING



Safe area limits are indicated by Figure 5.
Both limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
⊕ ∅ 0.25 (0.010) Ⓜ T V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
⊕ ∅ 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

3

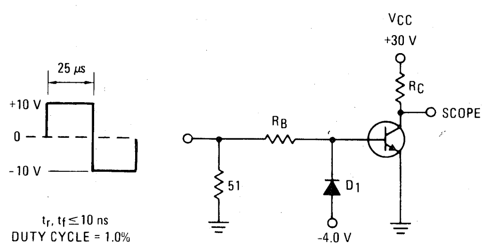
***ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)**

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5758 2N5760	$V_{CEO(sus)}$	100 120 140	– –	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 70 Vdc, I_B = 0)	2N5758 2N5760	I_{CEO}	– – –	1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	– –	1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)	2N5758 2N5760 All Types	h_{FE}	25 — 15 5.0	100 — 60 —	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc) (I_C = 6.0 Adc, I_B = 1.2 Adc)		$V_{CE(sat)}$	– –	1.0 2.0	Vdc
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	300	pF
Small-Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15	–	–

*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
(2) $f_T = |h_{fe}| \bullet f_{test}$

3

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

***For PNP test circuit, reverse all polarities and D1.**

FIGURE 3 – TURN-ON TIME

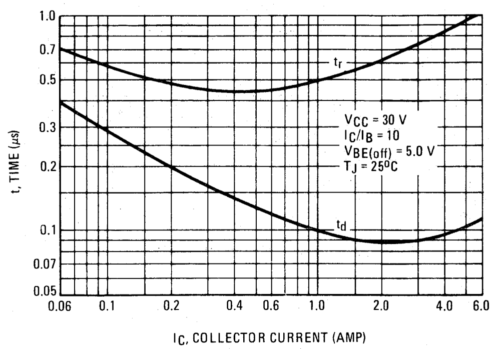


FIGURE 4 – THERMAL RESPONSE

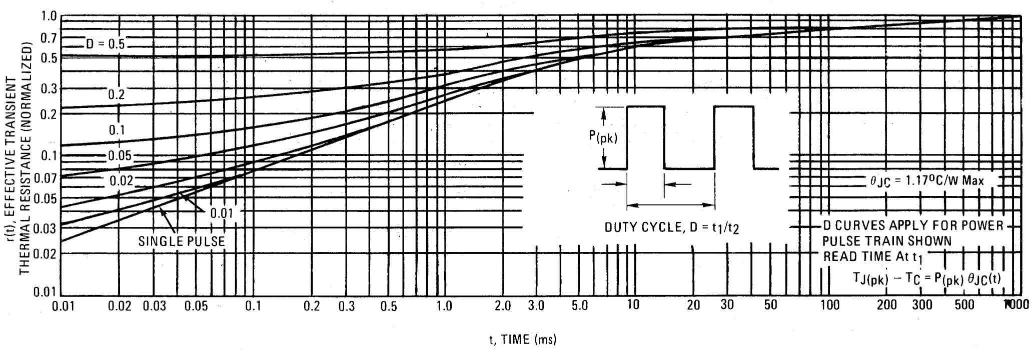
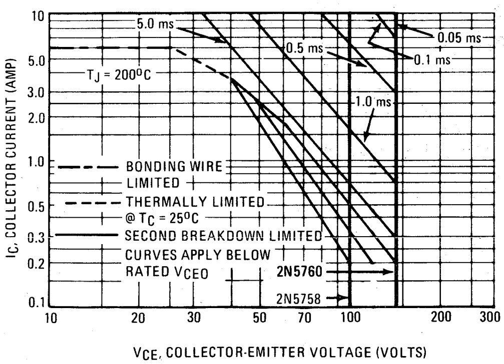


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 — TURN-OFF TIME

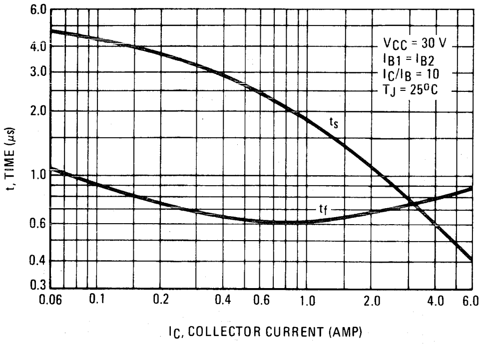


FIGURE 7 — CAPACITANCE

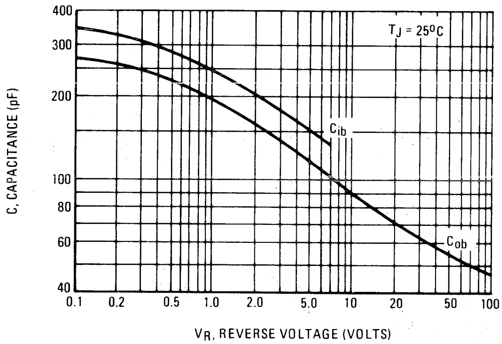
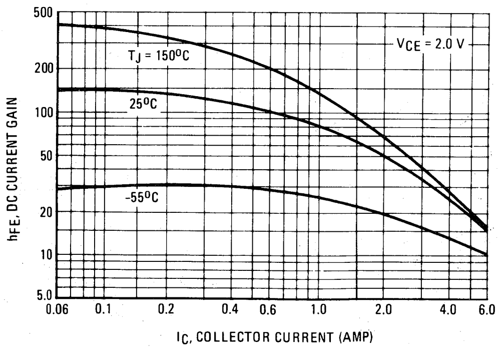


FIGURE 8 — DC CURRENT GAIN



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
2N5875, 2N5876
NPN
2N5877, 2N5878

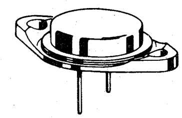
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 5.0 Adc
- Low Leakage Current — I_{CEX} = 0.5 mAdc (Max) @ Rated Voltage
- Excellent DC Current Gain — h_{FE} = 20 (Min) @ I_C = 4.0 Adc
- High Current Gain — Bandwidth Product — f_T = 4.0 MHz (Min) @ I_C = 0.5 A

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
150 WATTS



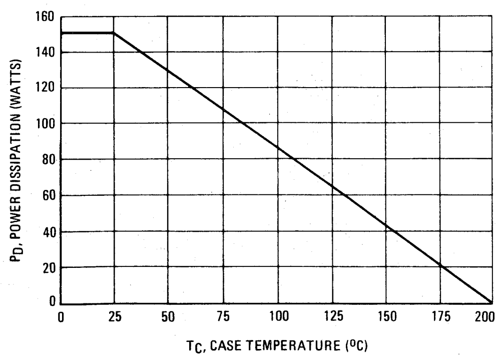
*MAXIMUM RATINGS

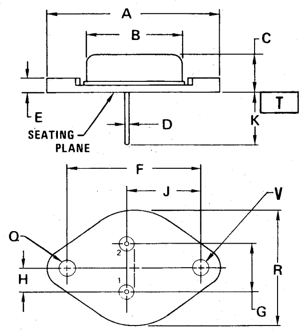
Rating	Symbol	2N5875 2N5877	2N5876 2N5878	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous / Peak	I_C	10 / 20		Adc
Base Current	I_B	4.0		Adc
Total Device Dissipation @ T_C = 25°C / Derate above 25°C	P_D	150 / 0.857		Watts / W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 3:
PIN 1. ANODE
2. CATHODE

NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⊕ | ∅ 0.25 (0.010) Ⓜ | T | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⊕ | ∅ 0.30 (0.012) Ⓜ | T | V Ⓜ | Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

3

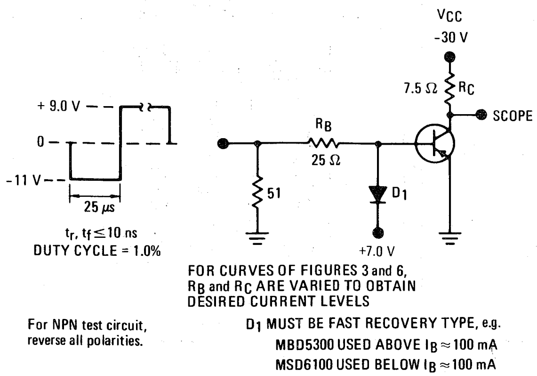
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5875, 2N5877	$V_{CEO(sus)}$	60	–	Vdc
	2N5876, 2N5878		80	–	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	2N5875, 2N5877	I_{CEO}	–	1.0	mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N5876, 2N5878		–	1.0	
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5875, 2N5877	I_{CEX}	–	0.5	mAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5876, 2N5878		–	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5875, 2N5877		–	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5876, 2N5878		–	5.0	
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)	2N5875, 2N5877	I_{CBO}	–	0.5	mAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N5876, 2N5878		–	0.5	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_E = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	35	–	–
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
Collector-Emitter Saturation Voltage (1) (I_C = 5.0 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	–	1.0	Vdc
(I_C = 10 Adc, I_B = 2.5 Adc)			–	3.0	
Base-Emitter Saturation Voltage (1) (I_C = 10 Adc, I_B = 2.5 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2) (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5875, 2N5876	C_{ob}	–	500	pF
	2N5877, 2N5878		–	300	
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 4.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, See Figure 2)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

3

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



For NPN test circuit, reverse all polarities.

FIGURE 3 – TURN-ON TIME

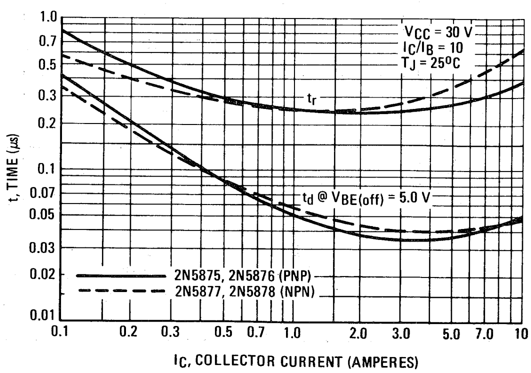


FIGURE 4 — THERMAL RESPONSE

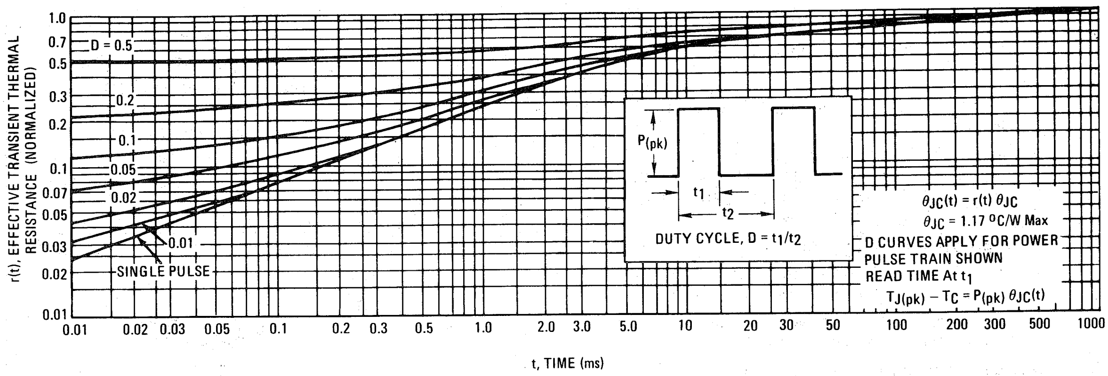
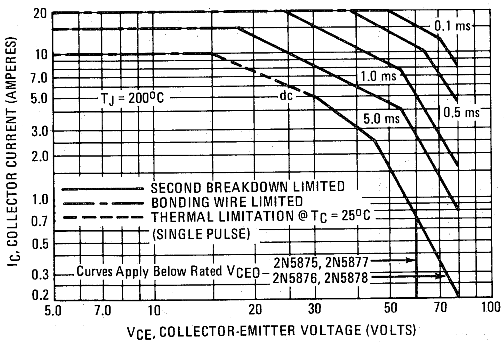


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 — TURN-OFF TIME

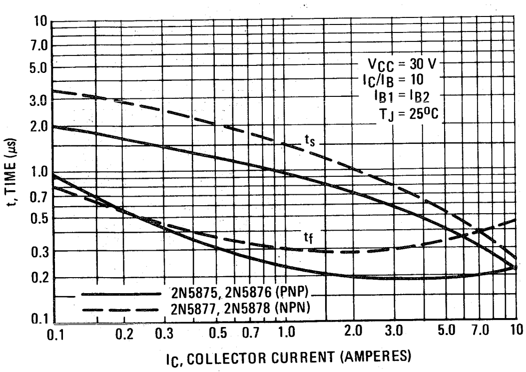
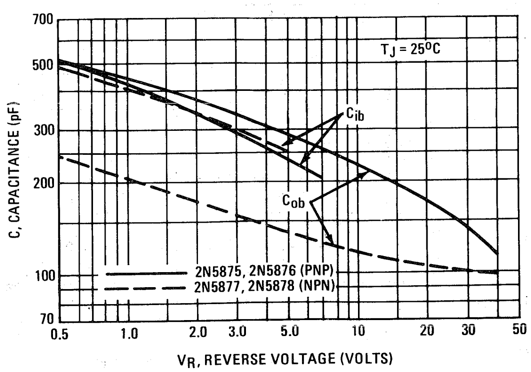


FIGURE 7 — CAPACITANCE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
2N5879, 2N5880
NPN
2N5881, 2N5882

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

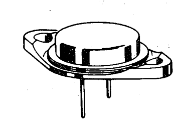
. . . designed for general-purpose power amplifier and switching applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N5879, 2N5881
  = 80 Vdc (Min) – 2N5880, 2N5882
- DC Current Gain —
  h_{FE} = 20 (Min) @ I_C = 6.0 Adc
- Low Collector — Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 7.0 Adc
- High Current — Gain-Bandwidth Product —
  f_T = 4.0 MHz (Min) @ I_C = 1.0 Adc
- Recommended for New Circuit Designs

15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60–80 VOLTS
160 WATTS



*MAXIMUM RATINGS

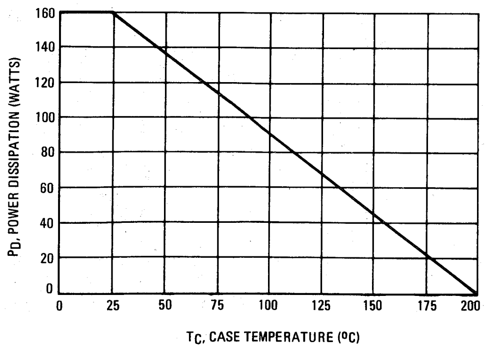
Rating	Symbol	2N5879 2N5881	2N5880 2N5882	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	15 30		Adc
Base Current	I_B	5.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	160 0.915		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

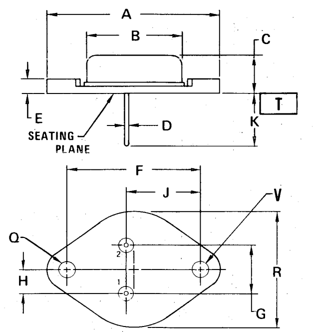
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.1	°C/W

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
⊕ ϕ 0.25 (0.010) Ⓜ T V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
⊕ ϕ 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5879, 2N5881		60	–	
	2N5880, 2N5882		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5879, 2N5881		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5880, 2N5882		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5879, 2N5881		–	0.5	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5880, 2N5882		–	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5879, 2N5881		–	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5880, 2N5882		–	5.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5879, 2N5881		–	0.5	
(V_{CB} = 80 Vdc, I_E = 0)	2N5880, 2N5882		–	0.5	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)			35	–	
(I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 7.0 Adc, I_B = 0.7 Adc)			–	1.0	
(I_C = 15 Adc, I_B = 3.75 Adc)			–	4.0	
Base-Emitter Saturation Voltage (1) (I_C = 15 Adc, I_B = 3.75 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	2N5879, 2N5880		–	600	
	2N5881, 2N5882		–	400	
Small-Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 6.0 Adc, I_{B1} = I_{B2} = 0.6 Adc See Figure 2)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
(2) $f_T = |h_{fe}| \bullet f_{test}$

3

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT

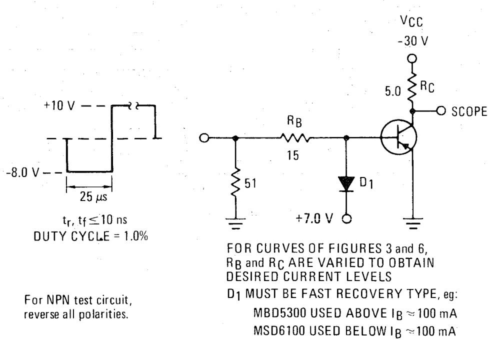


FIGURE 3 — TURN-ON TIME

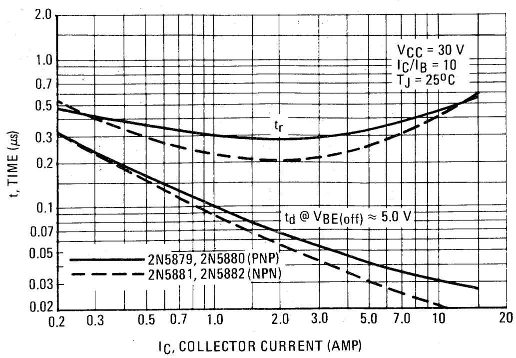


FIGURE 4 – THERMAL RESPONSE

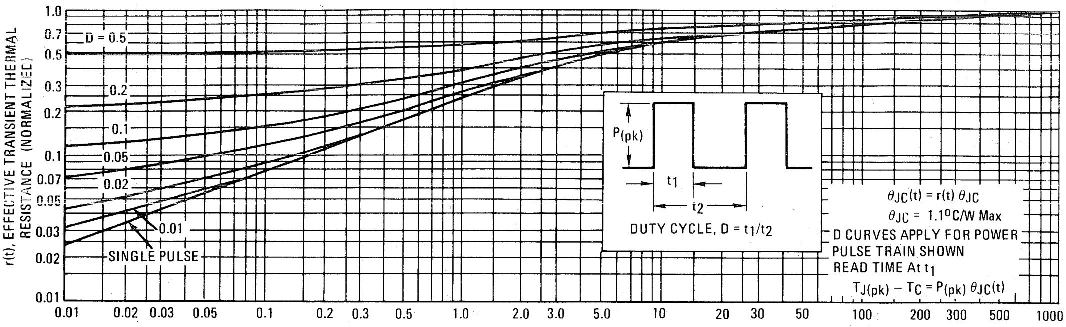
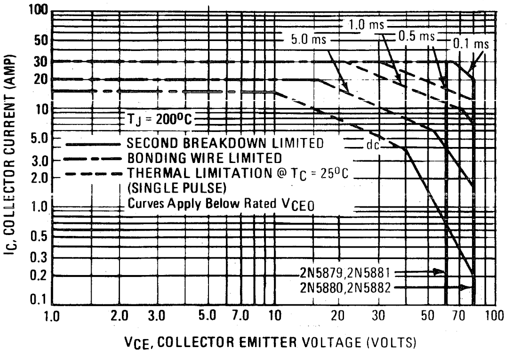


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

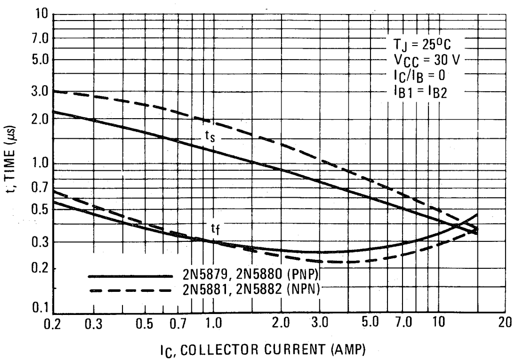
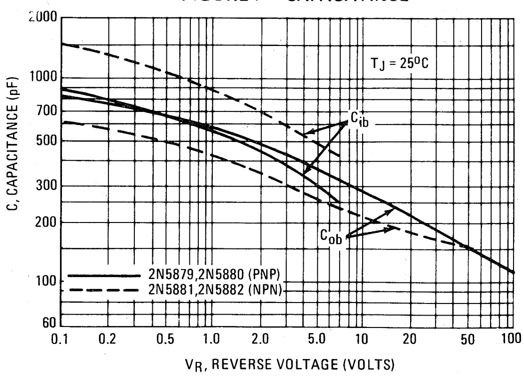


FIGURE 7 – CAPACITANCE



3

PNP
2N5879, 2N5880

NPN
2N5881, 2N5882

FIGURE 8 — DC CURRENT GAIN

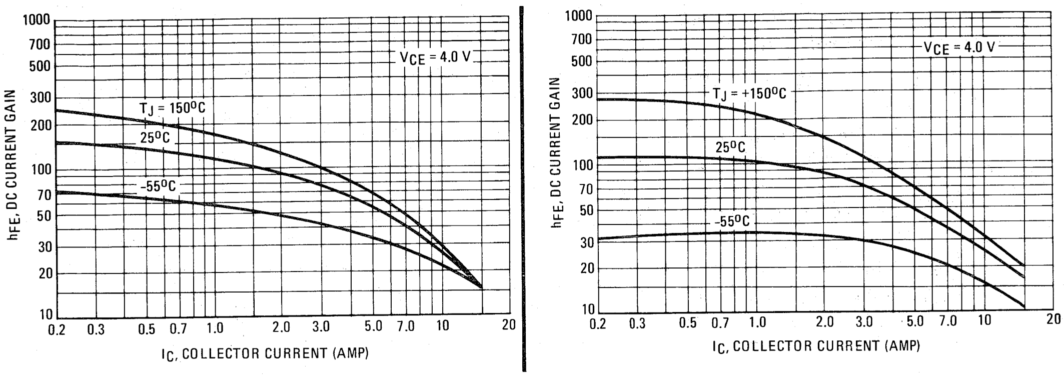


FIGURE 9 — COLLECTOR SATURATION REGION

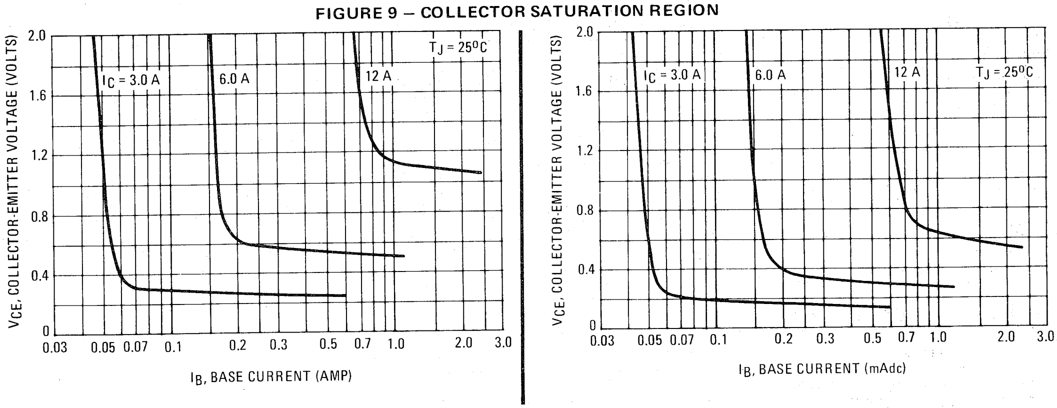
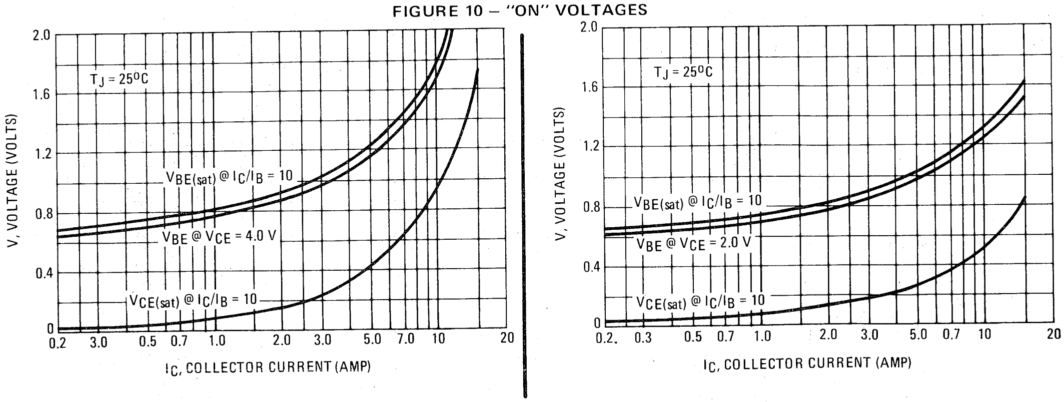


FIGURE 10 — "ON" VOLTAGES



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
2N5883, 2N5884
NPN
2N5885, 2N5886

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for general-purpose power amplifier and switching applications.

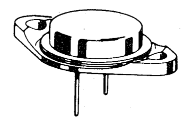
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc, (max) at I_C = 15 Adc
- Low Leakage Current I_{CEX} = 1.0 mAdc (max) at Rated Voltage
- Excellent DC Current Gain — h_{FE} = 20 (min) at I_C = 10 Adc
- High Current Gain Bandwidth Product — f_T = 4.0 MHz (min) at I_C = 1.0 Adc

25 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60–80 VOLTS

200 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N5883 2N5885	2N5884 2N5886	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	25 50		Adc
Base Current	I_B	7.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.15		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

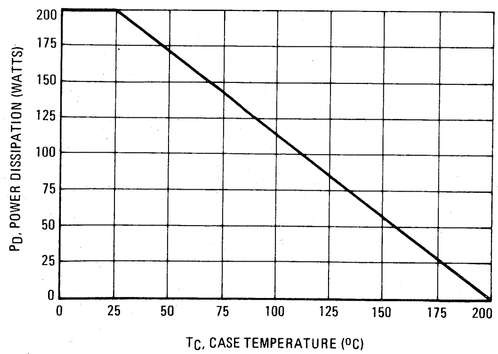
THERMAL CHARACTERISTICS

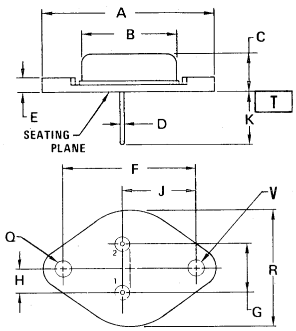
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

3

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⊕ | ∅ 0.25 (0.010) Ⓜ | T | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⊕ | ∅ 0.30 (0.012) Ⓜ | T | V Ⓜ | Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

2N5883, 2N5884 PNP, 2N5885, 2N5886 NPN

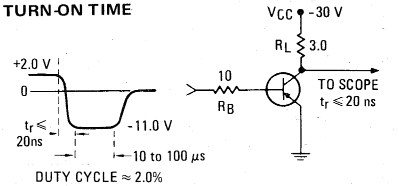
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5883, 2N5885 2N5884, 2N5886	$V_{CEO(sus)}$	60 80	– –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	2N5883, 2N5885 2N5884, 2N5886	I_{CEO}	– –	2.0 2.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5883, 2N5885 2N5884, 2N5886 2N5883, 2N5885 2N5884, 2N5886	I_{CEX}	– – – –	1.0 1.0 10 10	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	2N5883, 2N5885 2N5884, 2N5886	I_{CBO}	– –	1.0 1.0	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 25 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	35 20 4.0	– 100 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 25 Adc, I_B = 6.25 Adc)		$V_{CE(sat)}$	– –	1.0 4.0	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 25 Adc, I_B = 6.25 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5883, 2N5884 2N5885, 2N5886	C_{ob}	– –	1000 500	pF
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 kHz)		h_{fe}	20	–	–
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

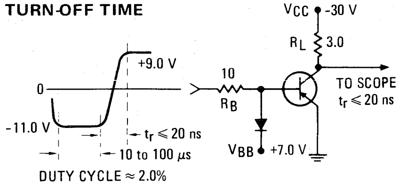
*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%. (2) $f_T = |h_{fe}| \bullet f_{test}$.

FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUITS

TURN-ON TIME

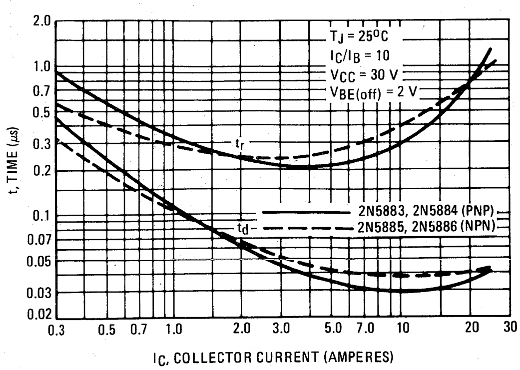


TURN-OFF TIME



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME



3

FIGURE 4 – THERMAL RESPONSE

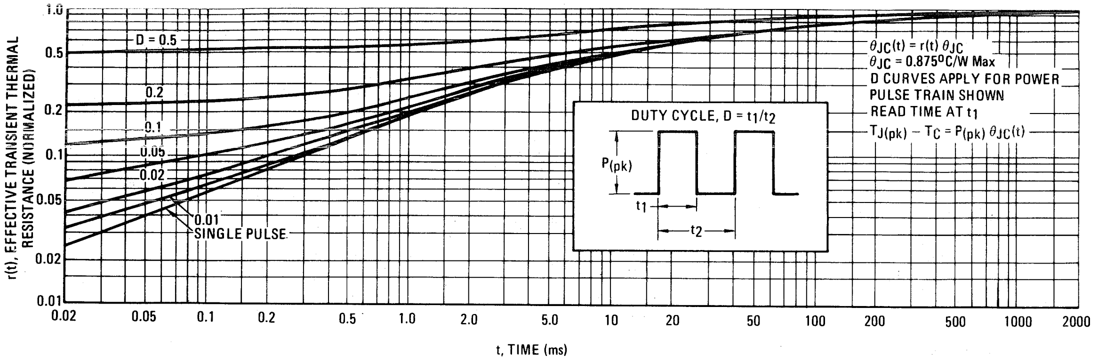
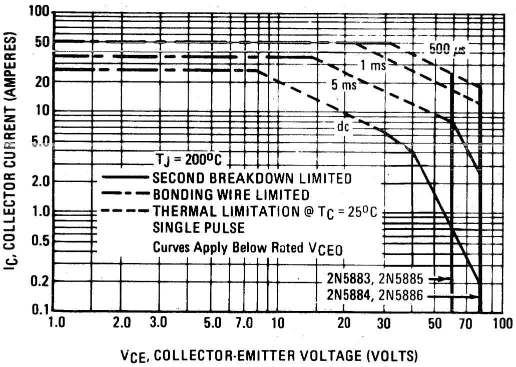


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

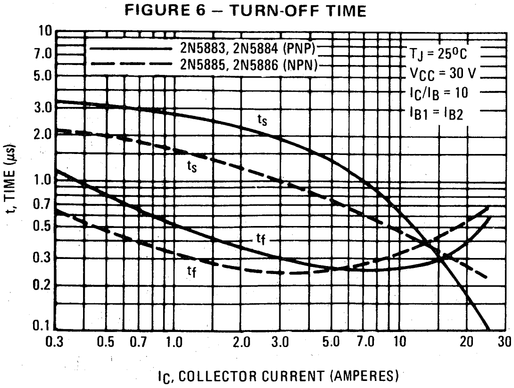
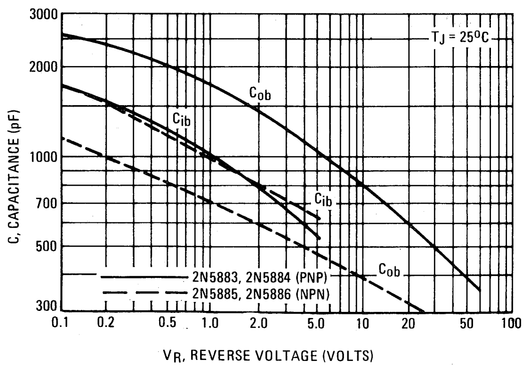


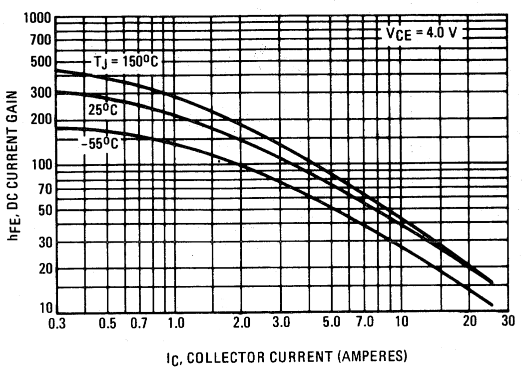
FIGURE 7 – CAPACITANCE



PNP DEVICES
2N5883 and 2N5884

NPN DEVICES
2N5885 and 2N5886

FIGURE 8 – DC CURRENT GAIN



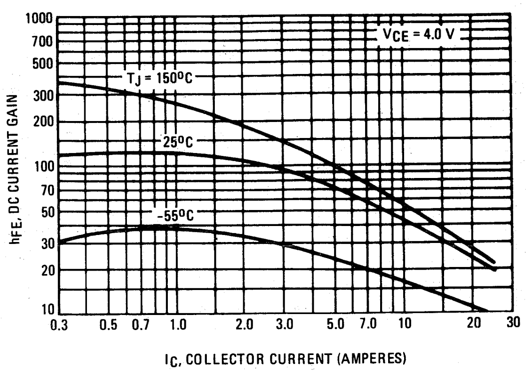
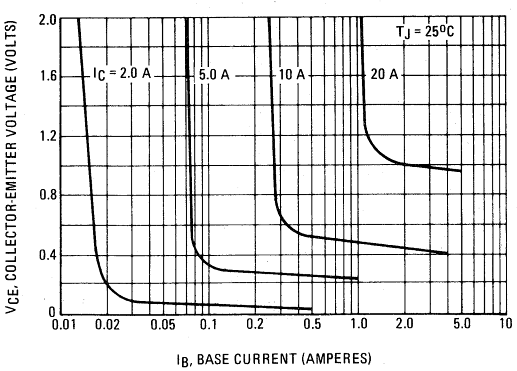


FIGURE 9 – COLLECTOR SATURATION REGION



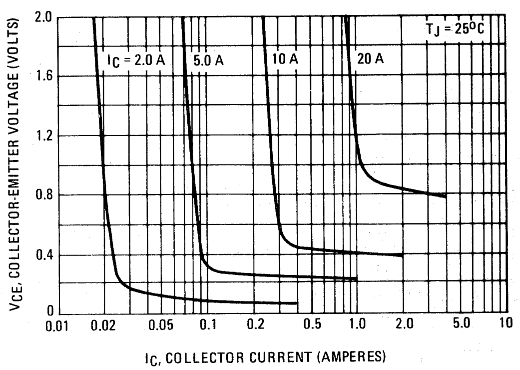
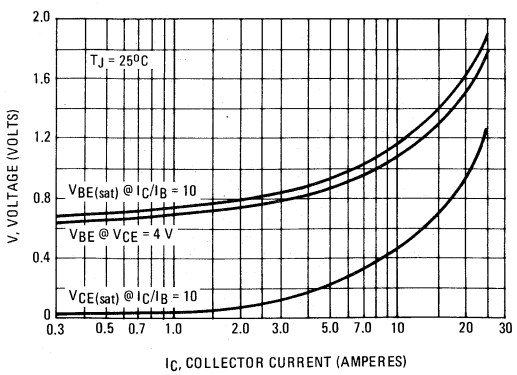
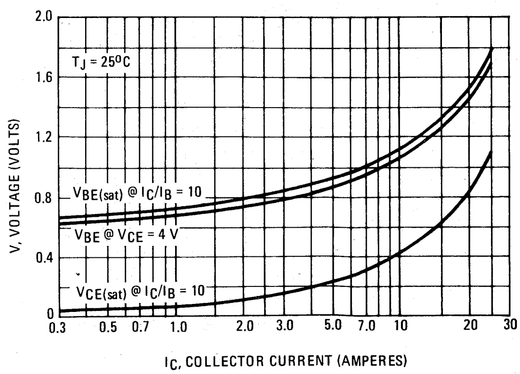


FIGURE 10 – "ON" VOLTAGES





MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
2N5986, 2N5987
2N5988
NPN
2N5989, 2N5991

HIGH POWER PLASTIC COMPLEMENTARY SILICON POWER TRANSISTORS

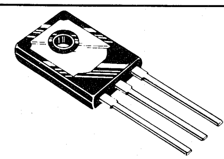
. . . designed for use in general-purpose amplifier and switching circuits.

- Collector-Base Voltage — V_{CBO} = 60 Vdc — 2N5986, 2N5989
  = 80 Vdc — 2N5987
  = 100 Vdc — 2N5988, 2N5991
- Collector-Emitter Voltage — V_{CEO} = 40 Vdc — 2N5986, 2N5989
  = 60 Vdc — 2N5987
  = 80 Vdc — 2N5988, 2N5991
- DC Current Gain —
  h_{FE} = 20-120 @ I_C = 6.0 Adc
  = 7.0 (Min) @ I_C = 12 Adc
- Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 6.0 Adc

12 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

40, 60, 80 VOLTS
100 WATTS



*MAXIMUM RATINGS

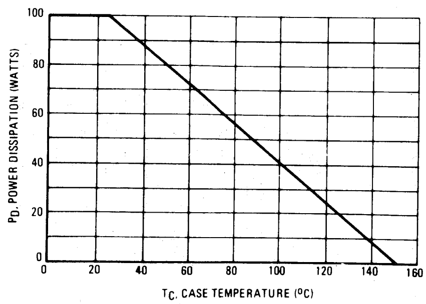
Rating	Symbol	2N5986 2N5989	2N5987	2N5988 2N5991	Unit
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous Peak	I_C		12 20		Adc
Base Current	I_B		4.0		Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25°C	P_D		100 0.8		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +150		°C

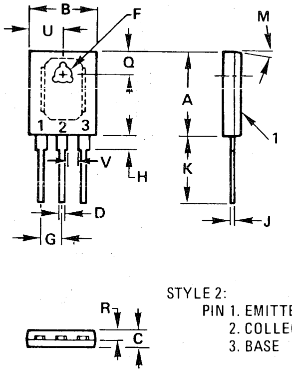
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.25	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	—	0.080	—

CASE 90-05
TO-225AB

3

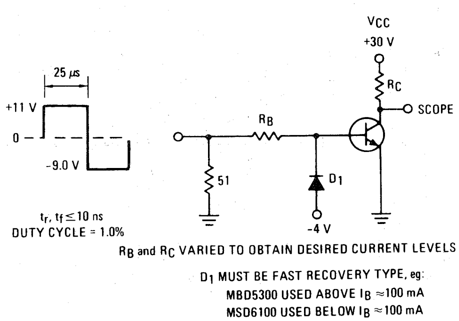
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 0.2 Adc, I_B = 0)	2N5986, 2N5989		40	–	
	2N5987		60	–	
	2N5988, 2N5991		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N5986, 2N5989		–	2.0	
(V_{CE} = 30 Vdc, I_B = 0)	2N5987		–	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5988, 2N5991		–	2.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5986, 2N5989		–	200	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5987		–	200	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5988, 2N5991		–	200	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5986, 2N5989		–	2.0	mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5987		–	2.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5988, 2N5991		–	2.0	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)			20	120	
(I_C = 12 Adc, V_{CE} = 2.0 Vdc)			7.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 6.0 Adc, I_B = 0.6 Adc)			–	0.6	
(I_C = 12 Adc, I_B = 1.8 Adc)			–	1.7	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 12 Adc, I_B = 1.8 Adc)			–	2.5	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)			–	1.4	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product		f_T			MHz
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)			2.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5986 thru 2N5988		–	500	
	2N5989, 2N5991		–	300	
Small-Signal Current Gain		h_{fe}			–
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)			20	–	

*Indicates JEDEC Registered Data.
(1) $f_T = |h_{fe}| \bullet f_{test}$

3

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



For PNP test circuit reverse diode and voltage polarities.

FIGURE 3 — TURN-ON TIME

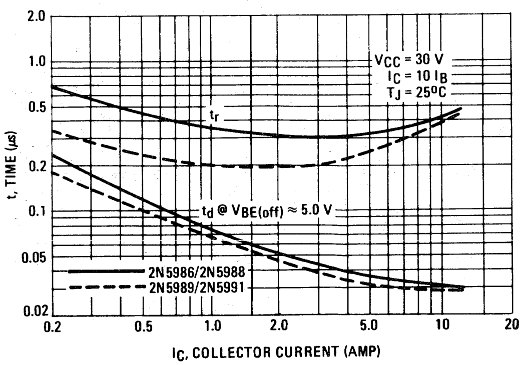


FIGURE 4 – THERMAL RESPONSE

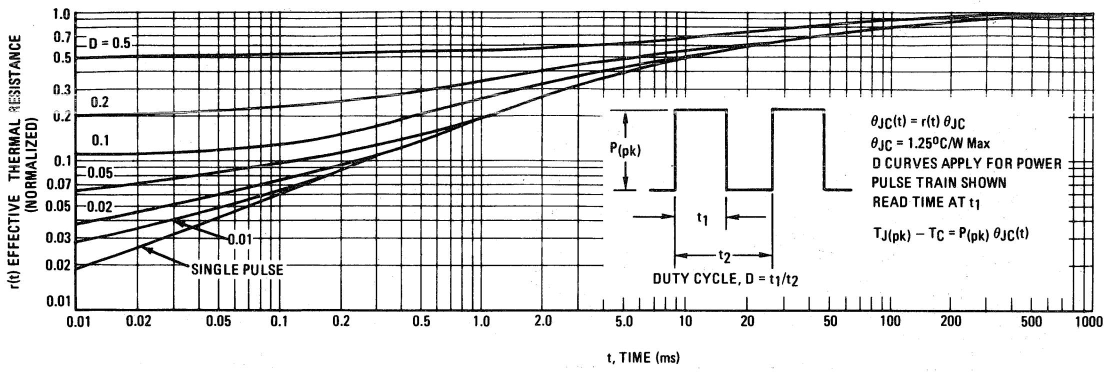
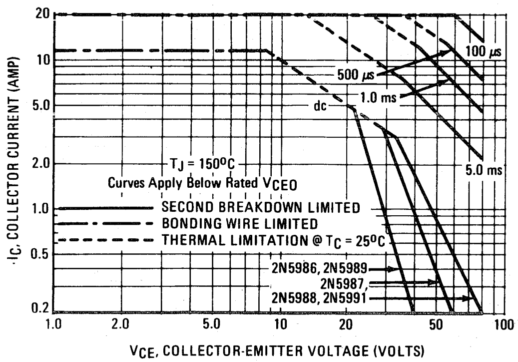


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$ $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

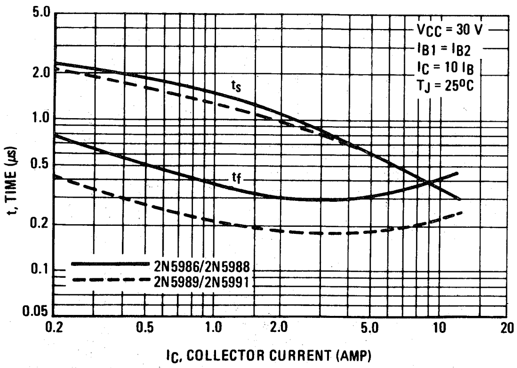
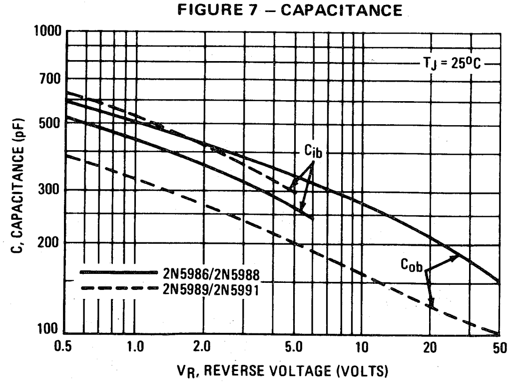


FIGURE 7 – CAPACITANCE



PNP 2N5986 thru 2N5988	NPN 2N5989, 2N5991

FIGURE 8 — DC CURRENT GAIN

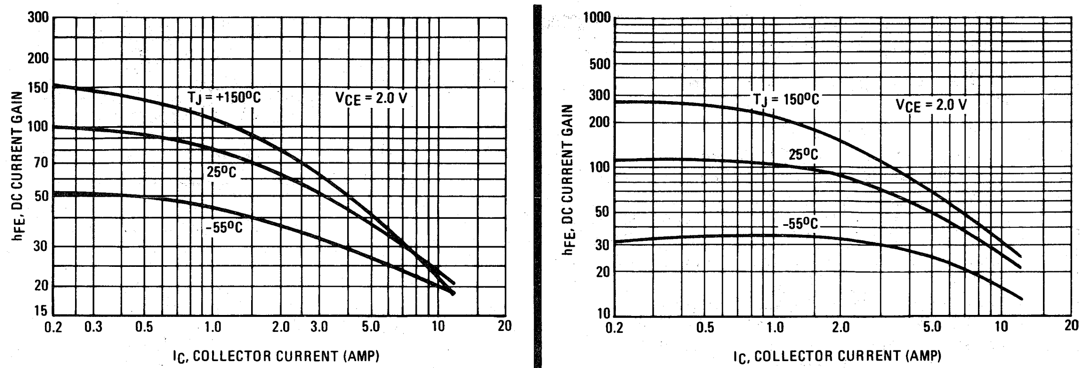


FIGURE 9 — COLLECTOR SATURATION REGION

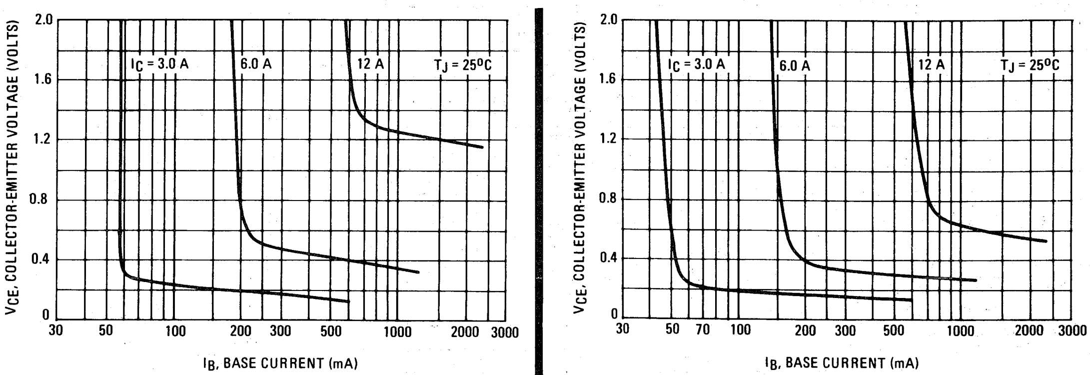
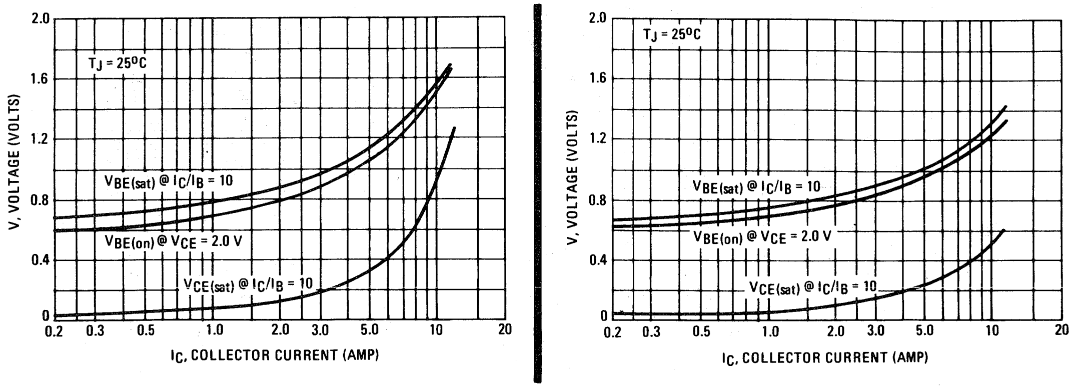


FIGURE 10 — "ON" VOLTAGES



3

2N6029 thru 2N6031
See Page 3-112

PNP	NPN
2N6034	2N6037
2N6035	2N6038
2N6036	2N6039

PLASTIC DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

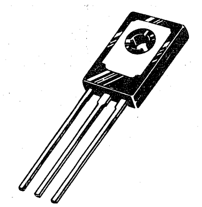
. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain — h_{FE} = 2000 (Typ) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 40 Vdc (Min) — 2N6034, 2N6037
  = 60 Vdc (Min) — 2N6035, 2N6038
  = 80 Vdc (Min) — 2N6036, 2N6039
- Forward Biased Second Breakdown Current Capability
  $I_{S/b}$ = 1.5 Adc @ 25 Vdc
- Monolithic Construction with Built-In Base-Emitter Resistors to Limit Leakage Multiplication
- Space-Saving High Performance-to-Cost Ratio TO-225AA Plastic Package

DARLINGTON
4-AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40, 60, 80 VOLTS
40 WATTS



*MAXIMUM RATINGS

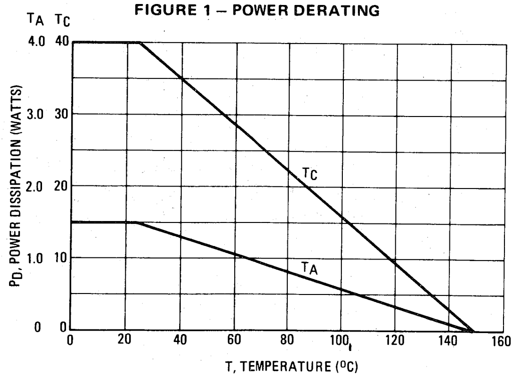
Rating	Symbol	2N6034 2N6037	2N6035 2N6038	2N6036 2N6039	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous	I_C	4.0			Adc
Peak		8.0			
Base Current	I_B	100			mAdc
Total Power Dissipation @ T_C = 25°C	P_D	40			Watts
Derate above 25°C		0.32			W/°C
Total Power Dissipation @ T_A = 25°C	P_D	1.5			Watts
Derate above 25°C		0.012			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

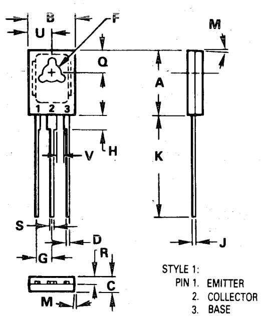
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.3	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-225AA

3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6034, 2N6037		40	–	
	2N6035, 2N6038		60	–	
	2N6036, 2N6039		80	–	
Collector-Cutoff Current		I_{CEO}			μA
(V_{CE} = 40 Vdc, I_B = 0)	2N6034, 2N6037		–	100	
(V_{CE} = 60 Vdc, I_B = 0)	2N6035, 2N6038		–	100	
(V_{CE} = 80 Vdc, I_B = 0)	2N6036, 2N6039		–	100	
Collector Cutoff Current		I_{CEX}			μA
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6034, 2N6037		–	100	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6035, 2N6038		–	100	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6036, 2N6039		–	100	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C)	2N6034, 2N6037		–	500	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C)	2N6035, 2N6038		–	500	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C)	2N6036, 2N6039		–	500	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N6034, 2N6037		–	0.5	
(V_{CB} = 60 Vdc, I_E = 0)	2N6035, 2N6038		–	0.5	
(V_{CB} = 80 Vdc, I_E = 0)	2N6036, 2N6039		–	0.5	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 3.0 Vdc)			500	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			750	15,000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 8.0 mAdc)			–	2.0	
(I_C = 4.0 Adc, I_B = 40 mAdc)			–	3.0	
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current-Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	25	–	–
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6034, 2N6035, 2N6036		–	200	
	2N6037, 2N6038, 2N6039		–	100	

*Indicates JEDEC Registered Data.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

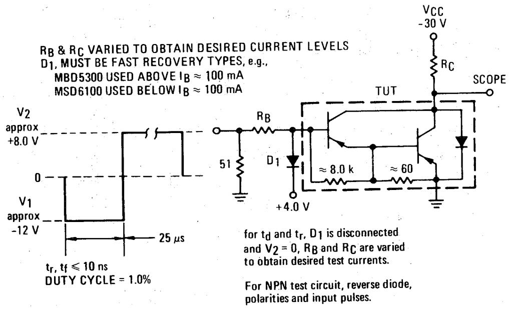
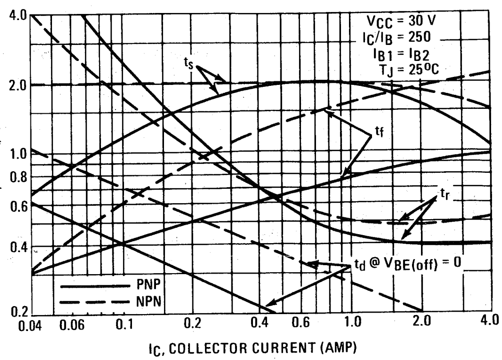
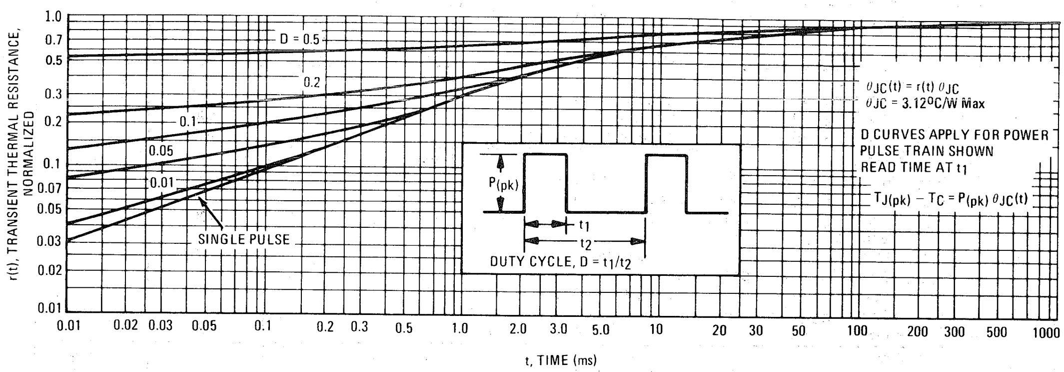


FIGURE 3 – SWITCHING TIMES



3

FIGURE 4 — THERMAL RESPONSE



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 5 — 2N6034, 2N6035, 2N6036

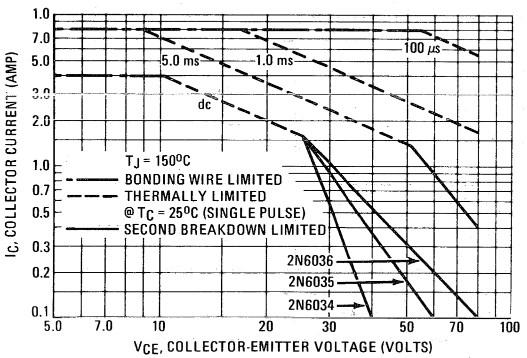
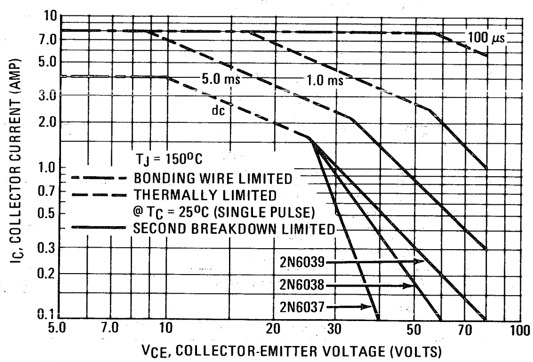


FIGURE 6 — 2N6037 2N6038, 2N6039

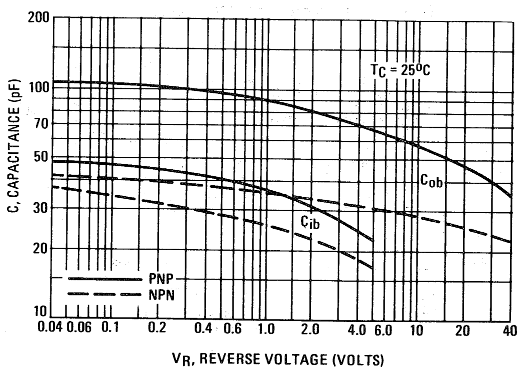


3

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

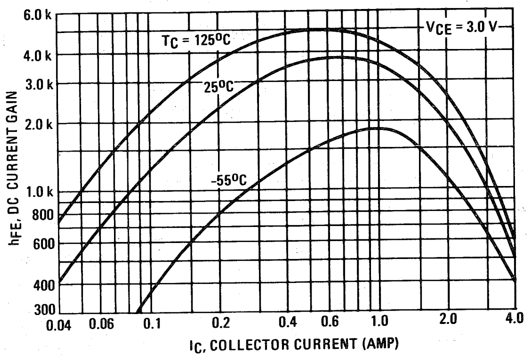
The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 — CAPACITANCE



PNP 2N6034, 2N6035, 2N6036	NPN 2N6037, 2N6038, 2N6039

FIGURE 8 – DC CURRENT GAIN



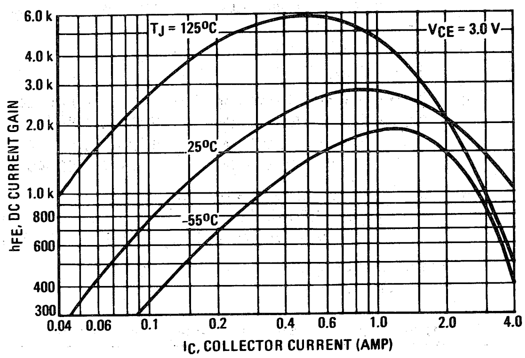
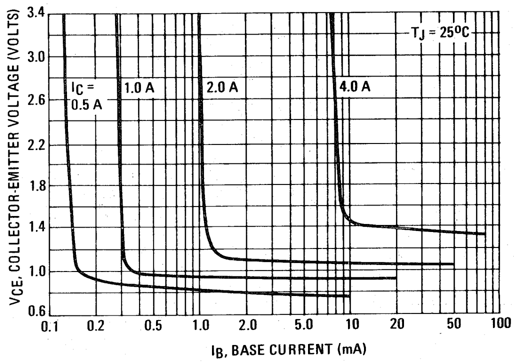


FIGURE 9 – COLLECTOR SATURATION REGION



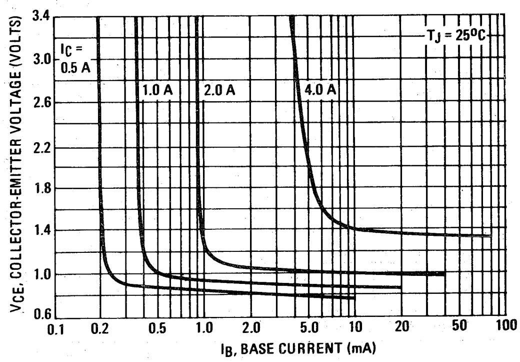
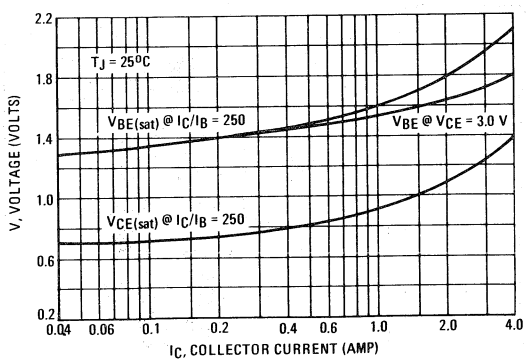
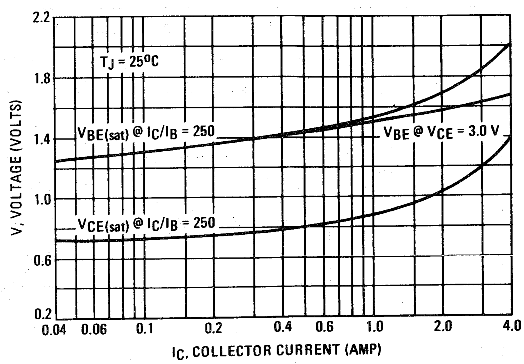


FIGURE 10 – "ON" VOLTAGES





3

2N6040 thru 2N6042 PNP
2N6043 thru 2N6045 NPN
MJE6040 thru MJE6041 PNP
MJE6043 thru MJE6045 NPN

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mAdc (1)
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6040, 2N6043
  = 80 Vdc (Min) — 2N6041, 2N6044
  = 100 Vdc (Min) — 2N6042, 2N6045
- Low Collector-Emitter Saturation Voltage — (1)
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc — 2N6040,41,2N6043,44
  = 2.0 Vdc (Max) @ I_C = 3.0 Adc — 2N6042, 2N6045
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

(1) Applies to corresponding in-house part numbers also.

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
75 WATTS

*MAXIMUM RATINGS

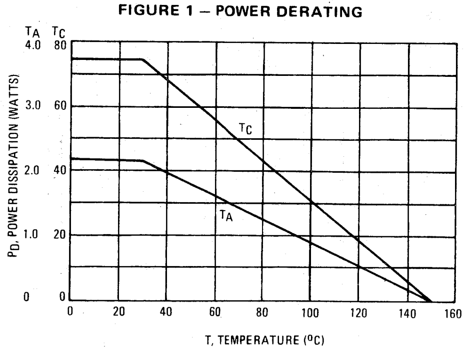
Rating	Symbol	2N6040 2N6043 MJE6040 MJE6043	2N6041 2N6044 MJE6041 MJE6044	2N6042 2N6045 MJE6045	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	8.0 16			Adc
Base Current	I_B	120			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.60			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.2 0.0175			Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

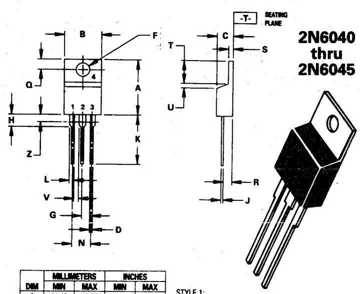
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	57	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING



2N6040 thru 2N6045



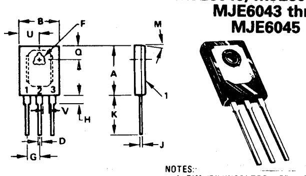
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

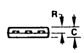
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MJE6040, MJE6041 and MJE6043 thru MJE6045





NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-225AB

3

2N6040 thru 2N6042 PNP
2N6043 thru 2N6045 NPN
MJE6040 thru MJE6041 PNP
MJE6043 thru MJE6045 NPN

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	2N6040, 2N6043, MJE6040, MJE6043 2N6041, 2N6044, MJE6041, MJE6044 2N6042, 2N6045, MJE6045	$V_{CEO(sus)}$	60 80 100	– – –	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0) (V_{CE} = 100 Vdc, I_B = 0)	2N6040, 2N6043, MJE6040, MJE6043 2N6041, 2N6044, MJE6041, MJE6044 2N6042, 2N6045, MJE6045	I_{CEO}	– – –	20 20 20	μA
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6040, 2N6043, MJE6040, MJE6043 2N6041, 2N6044, MJE6041, MJE6044 2N6042, 2N6045, MJE6045 2N6040, 2N6043, MJE6040, MJE6043 2N6041, 2N6044, MJE6041, MJE6044 2N6042, 2N6045, MJE6045	I_{CEX}	– – – – – –	20 20 20 200 200 200	μA
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	2N6040, 2N6043, MJE6040, MJE6043 2N6041, 2N6044, MJE6041, MJE6044 2N6042, 2N6045, MJE6045	I_{CBO}	– – –	20 20 20	μA
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	2N6040,41, 2N6043,44, MJE6040,41, MJE6043,44 2N6042, 2N6045, MJE6045 All Types	h_{FE}	1000 1000 100	20,000 20,000 –	–
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 16 mAdc) (I_C = 3.0 Adc, I_B = 12 mAdc) (I_C = 8.0 Adc, I_B = 80 mAdc)	2N6040,41,2N6043,44,MJE6040,41,MJE6043,44 2N6042,2N6045,MJE6045 All Types	$V_{CE(sat)}$	– – –	2.0 2.0 4.0	Vdc
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 80 mAdc)		$V_{BE(sat)}$	–	4.5	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6040/2N6042, MJE6040 2N6043/2N6045, MJE6043/MJE6045	C_{ob}	– –	300 200	pF
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data.

3

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

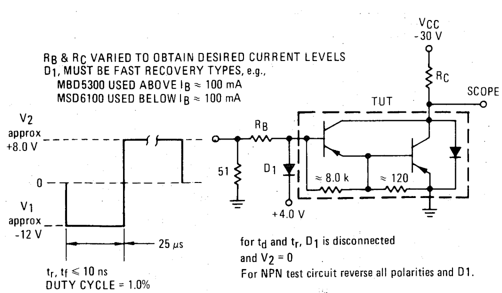


FIGURE 3 – SWITCHING TIMES

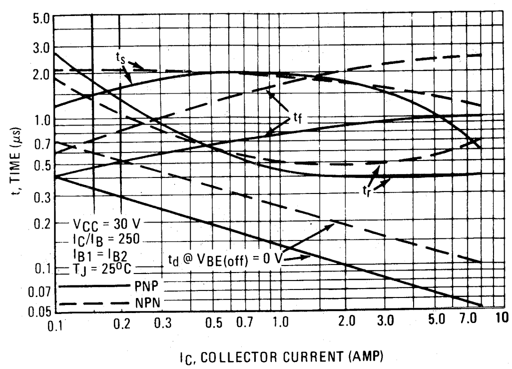


FIGURE 4 – THERMAL RESPONSE

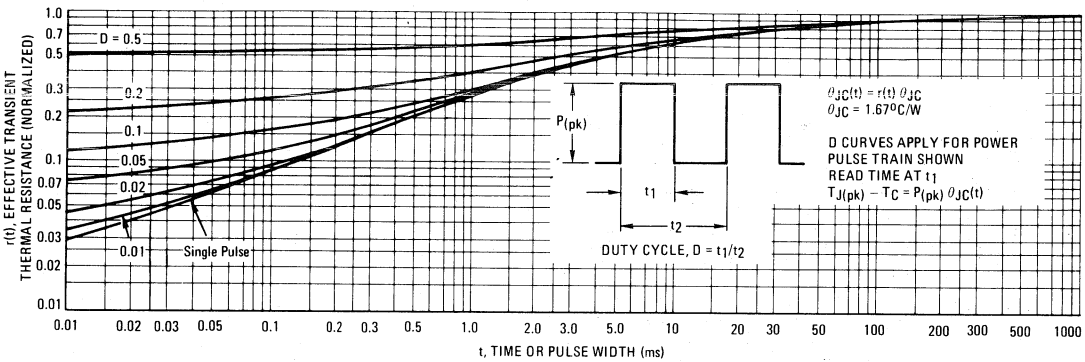
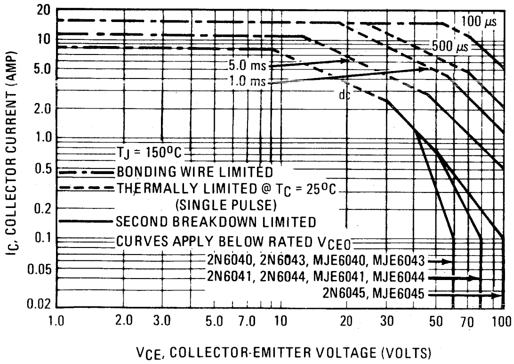


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

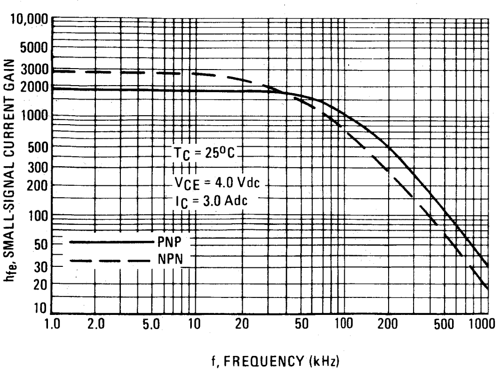
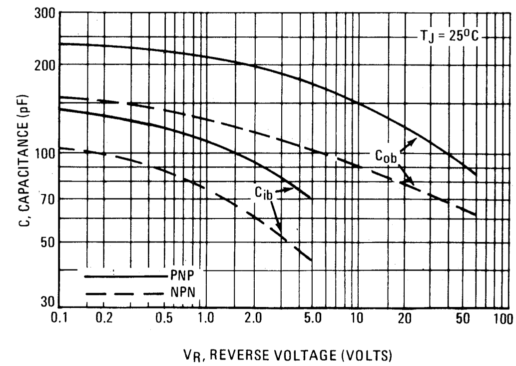


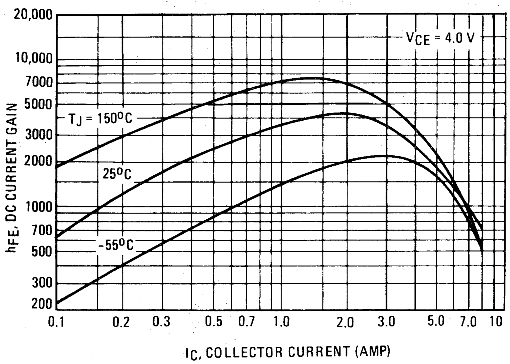
FIGURE 7 – CAPACITANCE



2N6040 thru 2N6042 PNP
2N6043 thru 2N6045 NPN
MJE6040 thru MJE6041 PNP
MJE6043 thru MJE6045 NPN

FIGURE 8 – DC CURRENT GAIN

PNP
2N6040, 2N6041, 2N6042
MJE6040, MJE6041



NPN
2N6043, 2N6044, 2N6045
MJE6043, MJE6044, MJE6045

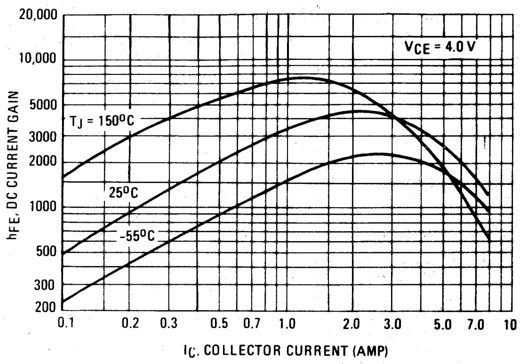
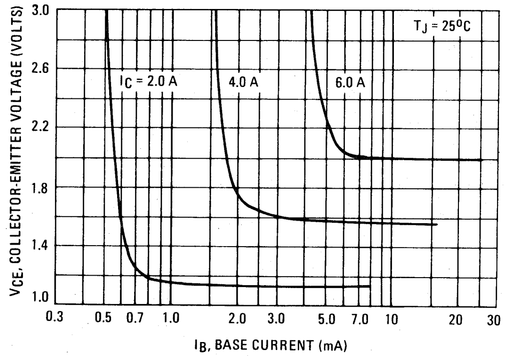


FIGURE 9 – COLLECTOR SATURATION REGION



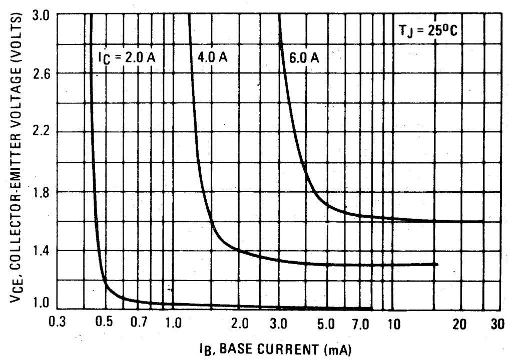
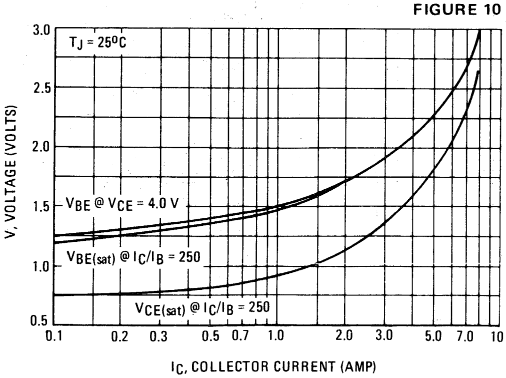
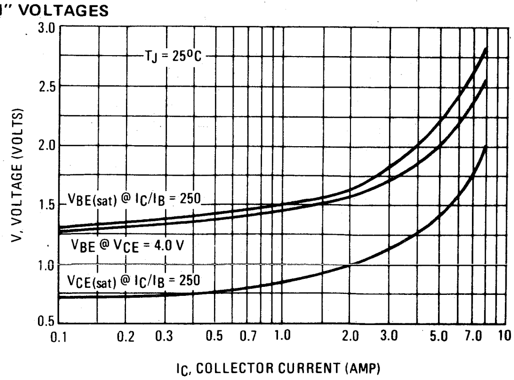


FIGURE 10 – "ON" VOLTAGES





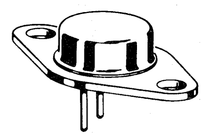
2N6049

MEDIUM-POWER PNP SILICON TRANSISTOR

. . . designed for general-purpose switching and amplifier applications

- Excellent Safe Operating Area
- DC Current Gain Specified to 4.0 Amperes
- Complement to NPN Type 2N3054A

4 AMPERE
POWER TRANSISTOR
PNP SILICON
55 VOLTS
75 WATTS



*MAXIMUM RATINGS

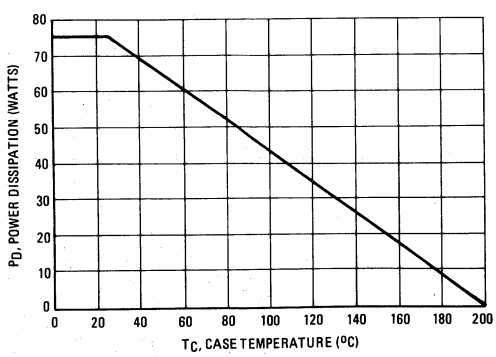
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	55	Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	60	Vdc
Collector-Base Voltage	V_{CB}	90	Vdc
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous	I_C	4.0	Adc
Peak		10	
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 25°C	P_D	75	Watts
Derate above 25°		0.43	W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200	°C

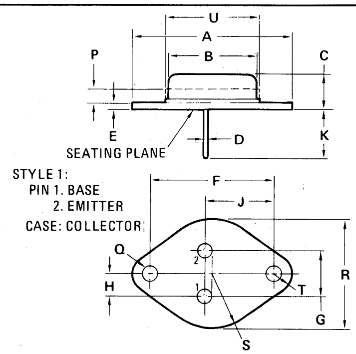
*Indicates JEDEC Registered Data

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.33	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	55	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, R_{BE} = 100 Ω)	$V_{CER(sus)}$	60	–	Vdc
Collector Cuttoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 6.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 500 mAdc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	25 6.0	100 –	–
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 4.0 Adc, I_B = 800 mAdc)	$V_{CE(sat)}$	– –	0.5 2.0	Vdc
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc)	f_T	3.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	200	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	25	180	

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width ≲ 300 μs, Duty Cycle ≲ 2.0%

3

FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUIT

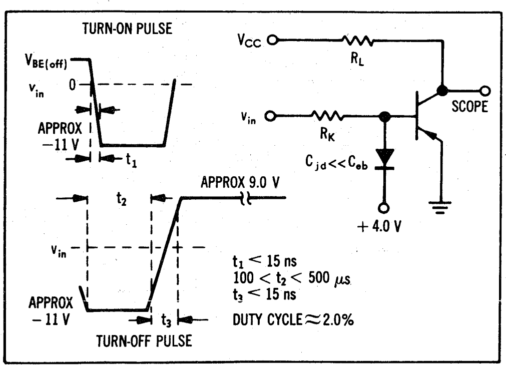


FIGURE 3 – TURN-ON TIME

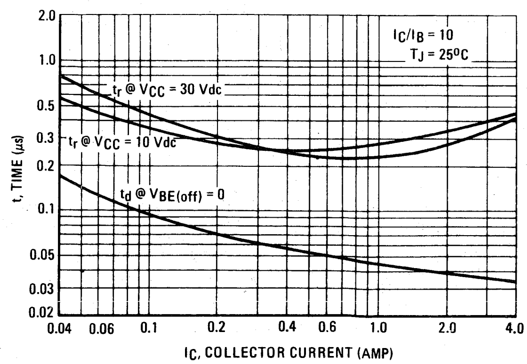


FIGURE 4 – THERMAL RESPONSE

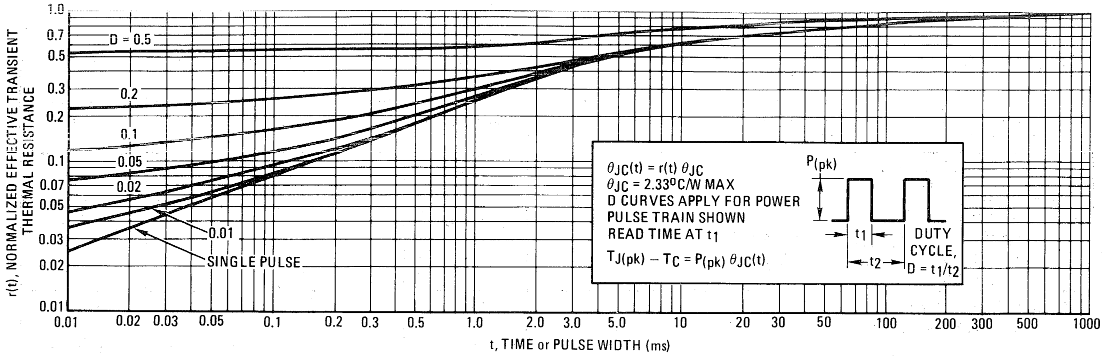
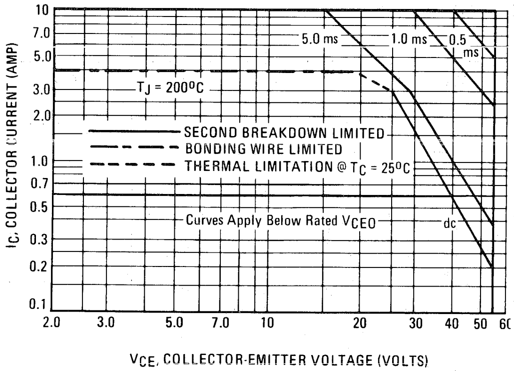


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

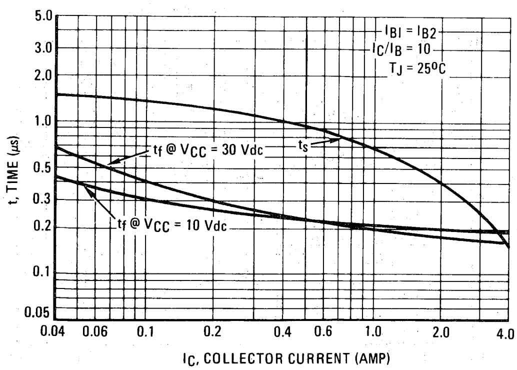
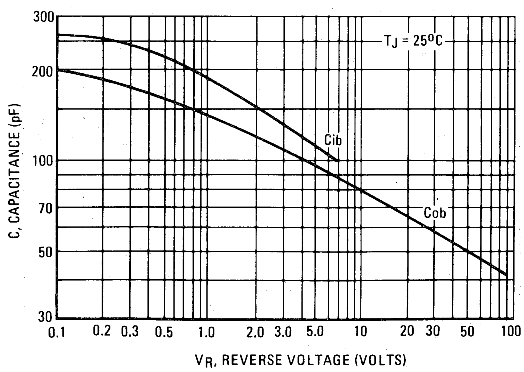


FIGURE 7 – CAPACITANCE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

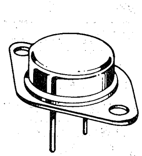
PNP
2N6050 thru 2N6052
NPN
2N6057 thru 2N6059

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain —
  h_{FE} = 3500 (Typ) @ I_C = 5.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6050, 2N6057
  80 Vdc (Min) — 2N6051, 2N6058
  100 Vdc (Min) — 2N6052, 2N6059
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON
12 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
150 WATTS



*MAXIMUM RATINGS

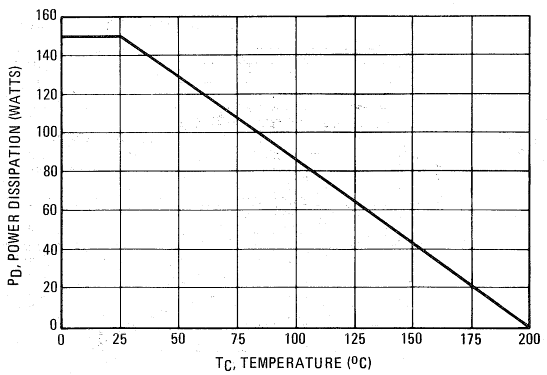
Rating	Symbol	2N6050 2N6057	2N6051 2N6058	2N6052 2N6059	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 12 → ← 20 →			Adc
Base Current	I_B	← 0.2 →			Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C	P_D	← 150 → ← 0.857 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200°C →			°C

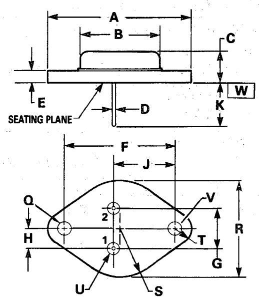
THERMAL CHARACTERISTICS

Characteristic	Symbol	Rating	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

3

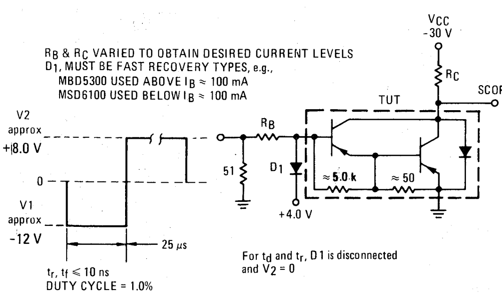
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0) 2N6050, 2N6057 2N6051, 2N6058 2N6052, 2N6059	$V_{CEO(sus)}$	 60 80 100	 – – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) 2N6050, 2N6057 (V_{CE} = 40 Vdc, I_B = 0) 2N6051, 2N6058 (V_{CE} = 50 Vdc, I_B = 0) 2N6052, 2N6059	I_{CEO}	 – – –	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 –	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 12 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	 750 100	 18,000 –	–
Collector-Emitter Saturation Volatage (I_C = 6.0 Adc, I_B = 24 mAdc) (I_C = 12 Adc, I_B = 120 mAdc)	$V_{CE(sat)}$	 – –	 2.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 12 Adc, I_B = 120 mAdc)	$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc)	$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$\|h_{fe}\|$	4.0	–	MHz
Output Capacitance 2N6050/2N6052 (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) 2N6057/2N6059	C_{ob}	– –	500 300	pF
Small-Signal Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)	h_{fe}	300	–	–

*Indicates JEDEC Registered Data
(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

3

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 – SWITCHING TIMES

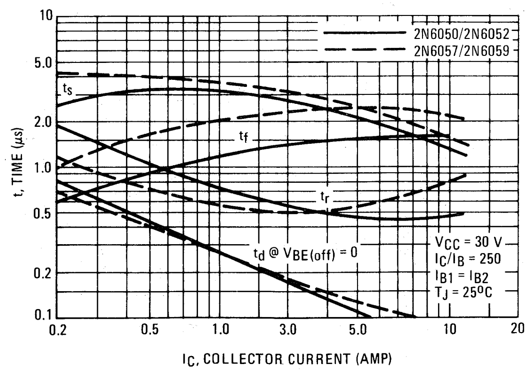
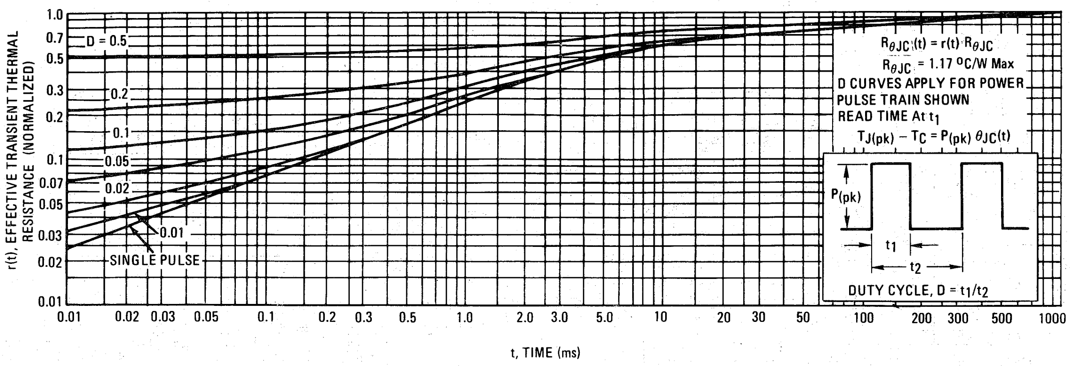


FIGURE 4 — THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 — 2N6050, 2N6057

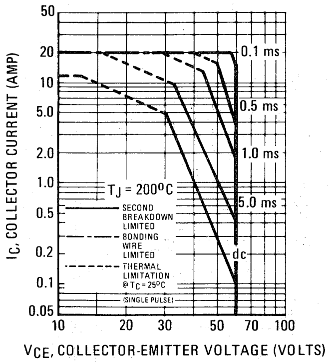


FIGURE 6 — 2N6051, 2N6058

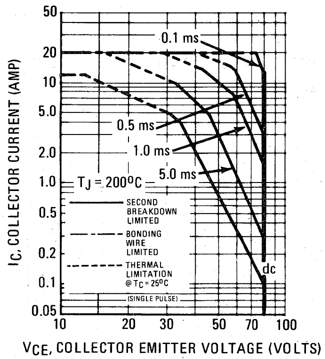
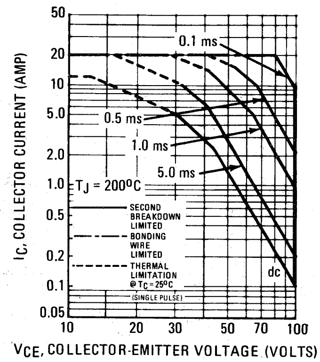


FIGURE 7 — 2N6052, 2N6059



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6 and 7 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant$ 200°C $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 8 — SMALL-SIGNAL CURRENT GAIN

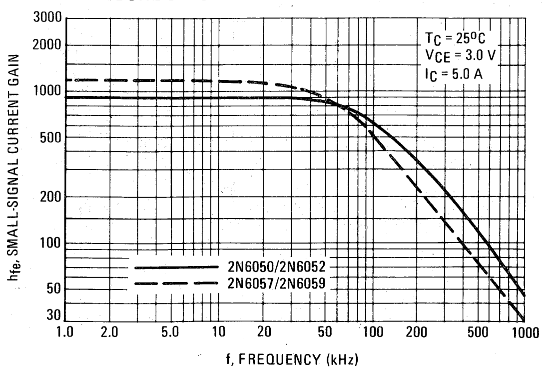
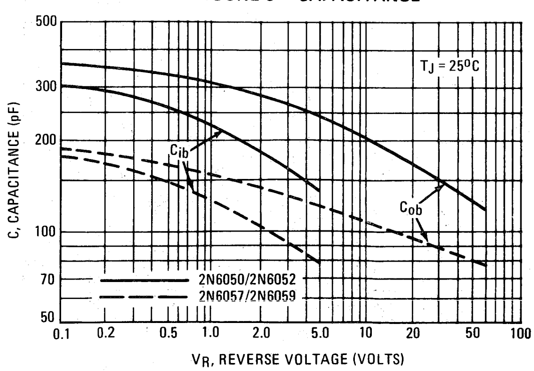


FIGURE 9 — CAPACITANCE



PNP
2N6050, 2N6051, 2N6052

NPN
2N6057, 2N6058, 2N6059

FIGURE 10 – DC CURRENT GAIN

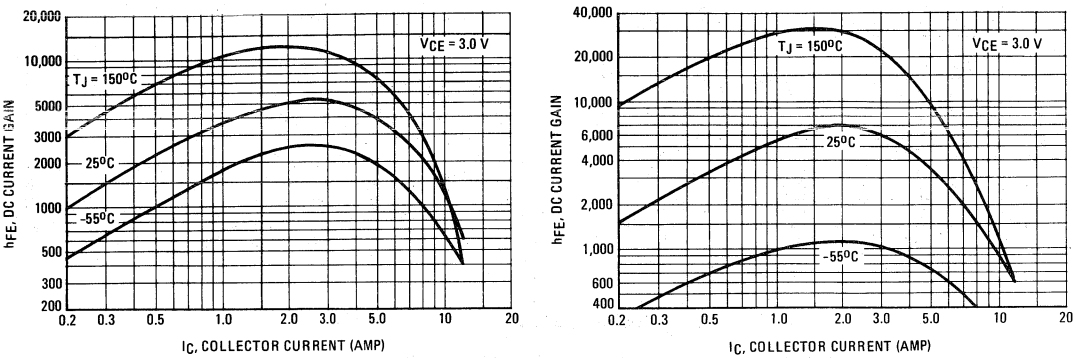


FIGURE 11 – COLLECTOR SATURATION REGION

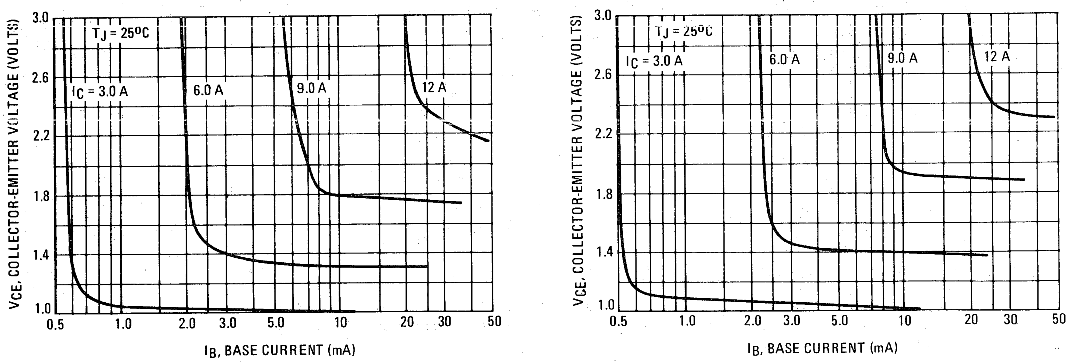
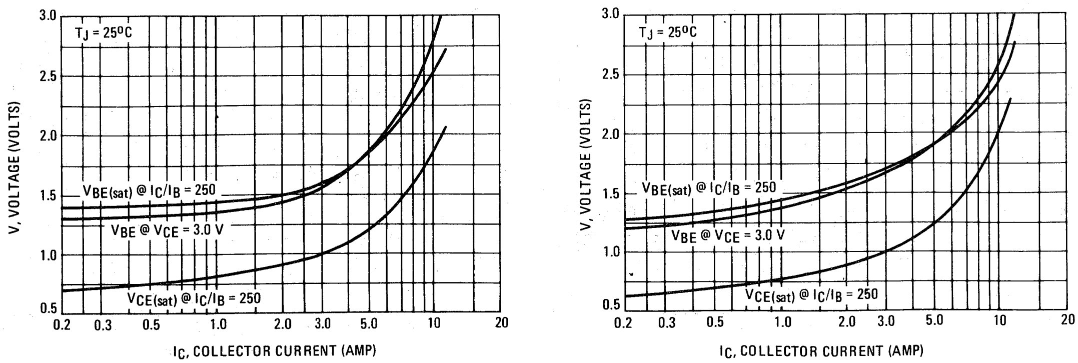


FIGURE 12 – "ON" VOLTAGES



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6053, 2N6054
2N6298, 2N6299 PNP
2N6055, 2N6056
2N6300, 2N6301 NPN

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain —
  h_{FE} = 3000 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6053, 2N6055, 2N6298, 2N6300
  = 80 Vdc (Min) — 2N6054, 2N6056, 2N6299, 2N6301
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc
  = 3.0 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON 8 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
75,100 WATTS

*MAXIMUM RATINGS

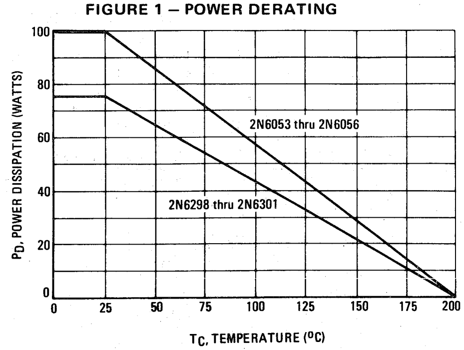
Rating	Symbol	2N6053 2N6055 2N6298 2N6300	2N6054 2N6056 2N6299 2N6301	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	8.0 16		Adc
Base Current	I_B	120		mAdc
		2N6053 2N6054 2N6055 2N6056	2N6298 2N6299 2N6300 2N6301	
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.571	75 0.428	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

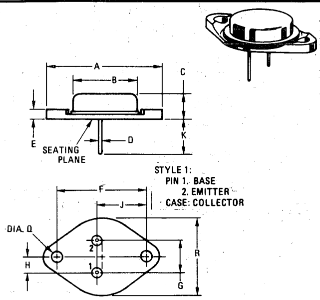
Characteristic	Symbol	2N6053 2N6054 2N6055 2N6056	2N6298 2N6299 2N6300 2N6301	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	2.33	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING



2N6053
2N6054
2N6055
2N6056



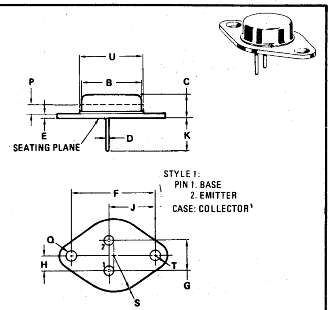
NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.

CASE 11-01
TO-204AA

2N6298
2N6299
2N6300
2N6301



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

3

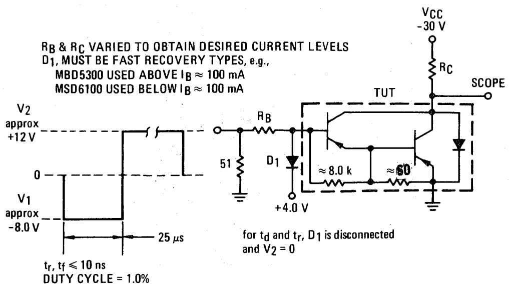
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	2N6053, 2N6055, 2N6298, 2N6300	$V_{CEO(sus)}$	60	–	Vdc
	2N6054, 2N6056, 2N6299, 2N6301		80	–	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	2N6053, 2N6055, 2N6298, 2N6300	I_{CEO}	–	0.5	mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6054, 2N6056, 2N6299, 2N6301		–	0.5	
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEX}	–	0.5	mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	750	18000	–
(I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 16 mAdc)		$V_{CE(sat)}$	–	2.0	Vdc
(I_C = 8.0 Adc, I_B = 80 mAdc)			–	3.0	
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 80 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short Circuit Current Transfer Ratio (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6053, 2N6054, 2N6298, 2N6299	C_{ob}	–	300	pF
	2N6055, 2N6056, 2N6300, 2N6301		–	200	
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0 %.

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode, polarities and input pulses.

FIGURE 3 — SWITCHING TIMES

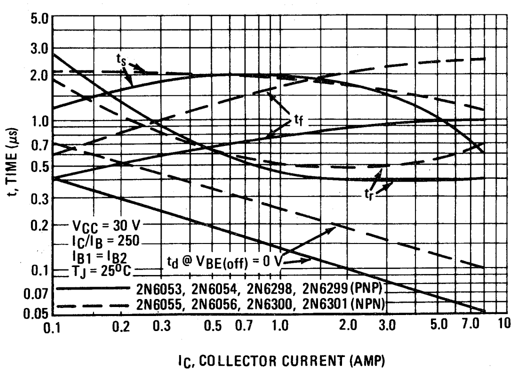
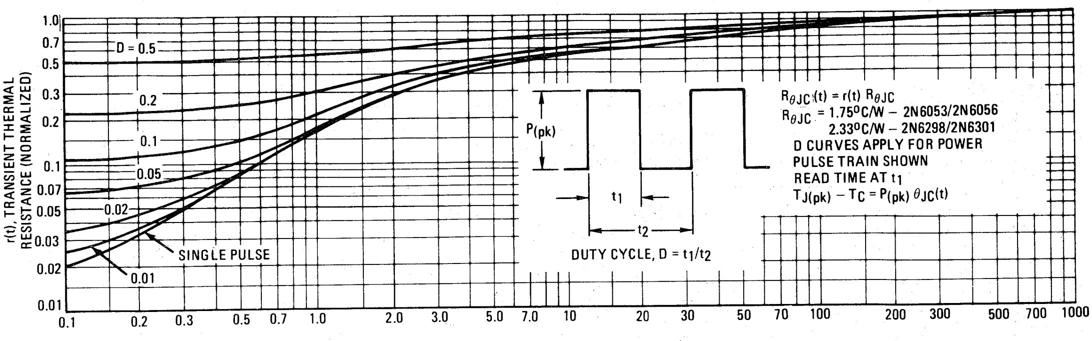


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6053 thru 2N6056

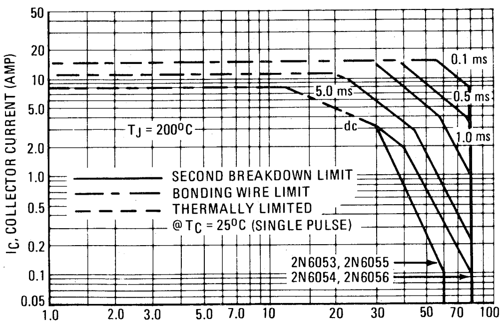
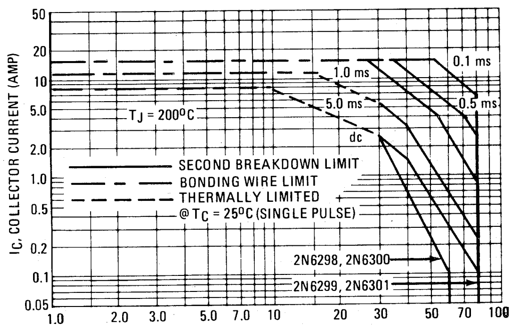


FIGURE 6 – 2N6298 thru 2N6301



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 200^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 – SMALL-SIGNAL CURRENT GAIN

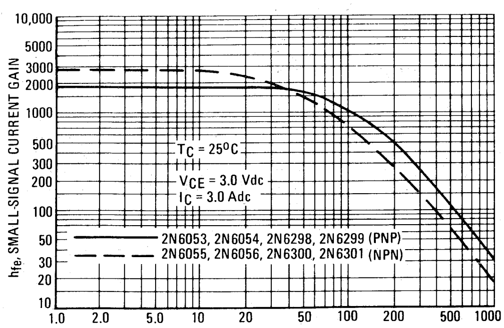
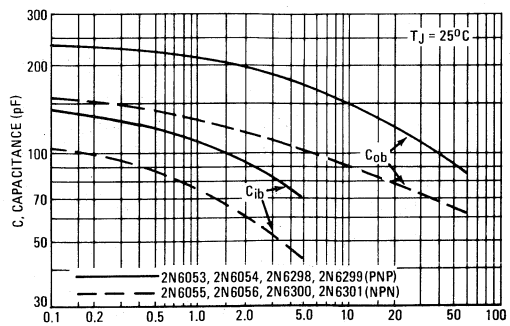


FIGURE 8 – CAPACITANCE



3

PNP — 2N6053, 2N6054, 2N6298, 2N6299

NPN — 2N6055, 2N6056, 2N6300, 2N6301

FIGURE 9 – DC CURRENT GAIN

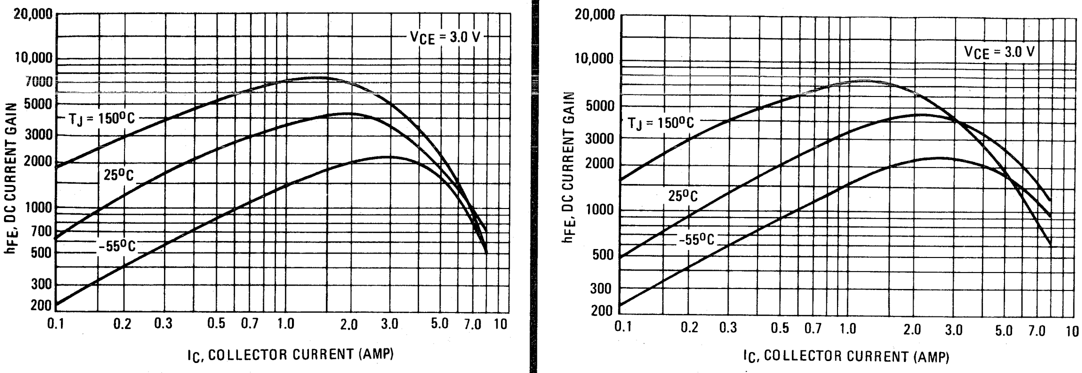


FIGURE 10 – COLLECTOR SATURATION REGION

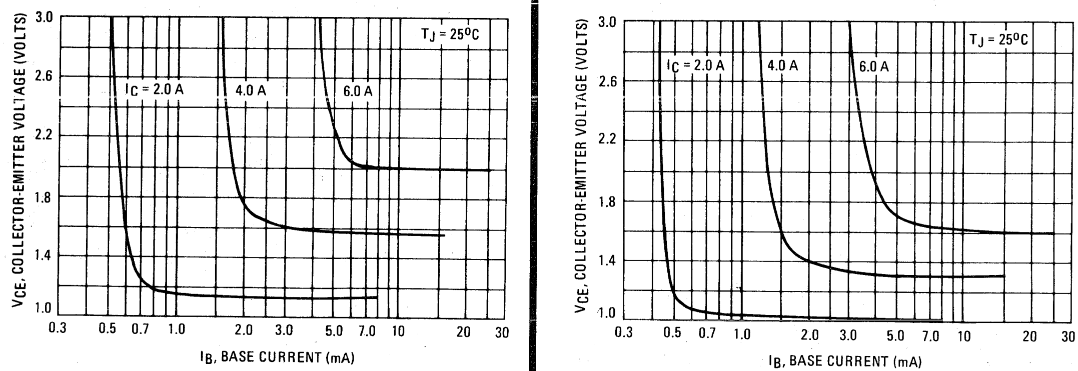
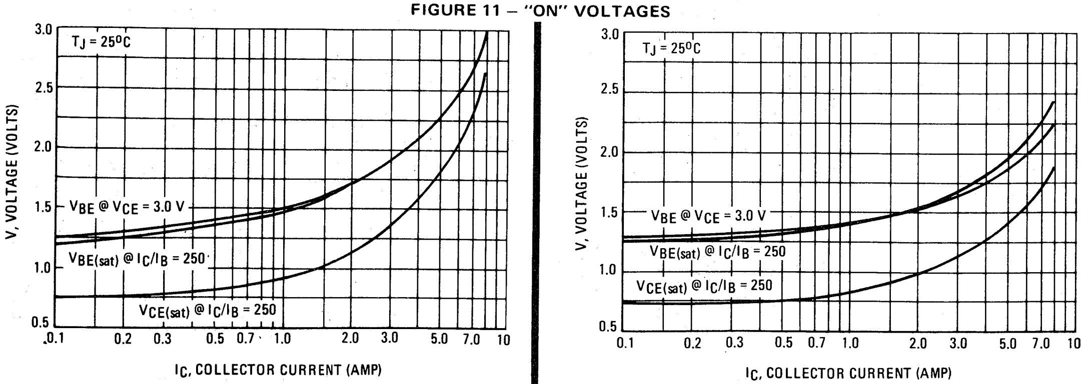


FIGURE 11 – "ON" VOLTAGES



3

2N6057 thru 2N6059
See Page 3-153

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
2N6107, 2N6109 2N6111
NPN
2N6288, 2N6292

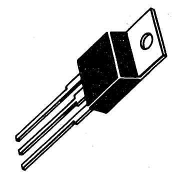
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 7.0 Amperes
  h_{FE} = 30–150 @ I_C = 3.0 Adc – 2N6111, 2N6288
  = 2.3 (Min) @ I_C = 7.0 Adc – All Devices
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 30 Vdc (Min) – 2N6111, 2N6288
  = 50 Vdc (Min) – 2N6109
  = 70 Vdc (Min) – 2N6107, 2N6292
- High Current Gain – Bandwidth Product
  f_T = 4.0 MHz (Min) @ I_C = 500 mAdc – 2N6288, 90, 92
  = 10 MHz (Min) @ I_C = 500 mAdc – 2N6107, 09, 11
- TO-220AB Compact Package
- TO-213AA Leadform Also Available

7 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

30–50–70 VOLTS
40 WATTS



*MAXIMUM RATINGS

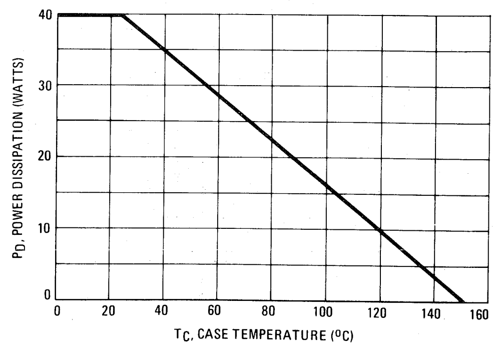
Rating	Symbol	2N6111 2N6288	2N6109	2N6107 2N6292	Unit
Collector-Emitter Voltage	V_{CEO}	30	50	70	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current – Continuous Peak	I_C		7.0 10		Adc
Base Current	I_B		3.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		40 0.32		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +150		°C

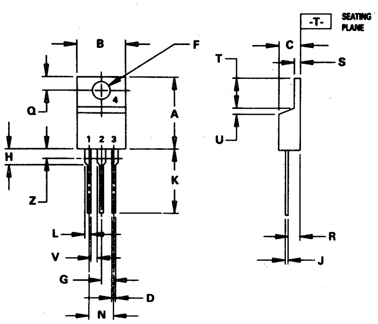
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

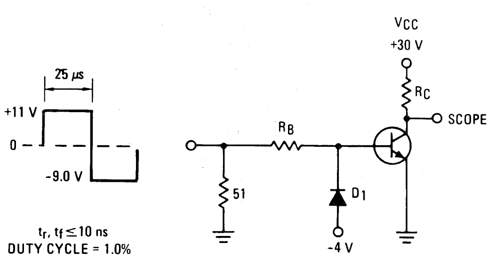
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	2N6111, 2N6288	$V_{CEO(sus)}$	30	–	Vdc
	2N6109		50	–	
	2N6107, 2N6292		70	–	
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	2N6111, 2N6288	I_{CEO}	–	1.0	mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6109		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6107, 2N6292		–	1.0	
Collector Cutoff Current (V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6111, 2N6288	I_{CEX}	–	100	μAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6109		–	100	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6107, 2N6292		–	100	
(V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6111, 2N6288		–	2.0	mAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6109		–	2.0	
(V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6107, 2N6292		–	2.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)	2N6107, 2N6292	h_{FE}	30	150	–
(I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)	2N6109		30	150	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N6111, 2N6288		30	150	
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)	All Devices		2.3	–	
Collector-Emitter Saturation Voltage (I_C = 7.0 Adc, I_B = 3.0 Adc)		$V_{CE(sat)}$	–	3.5	Vdc
Base-Emitter On Voltage (I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	3.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)	2N6288, 92	f_T	4.0	–	MHz
	2N6107, 09, 11		10	–	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	250	pF
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 50 kHz)		h_{fe}	20	–	–

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

3

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE IB ≈ 100 mA
MSD6100 USED BELOW IB ≈ 100 mA

FIGURE 3 – TURN-ON TIME

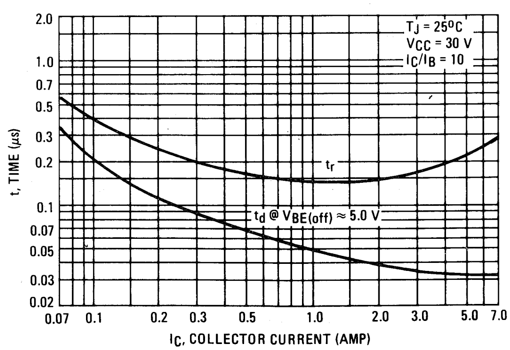


FIGURE 4 — THERMAL RESPONSE

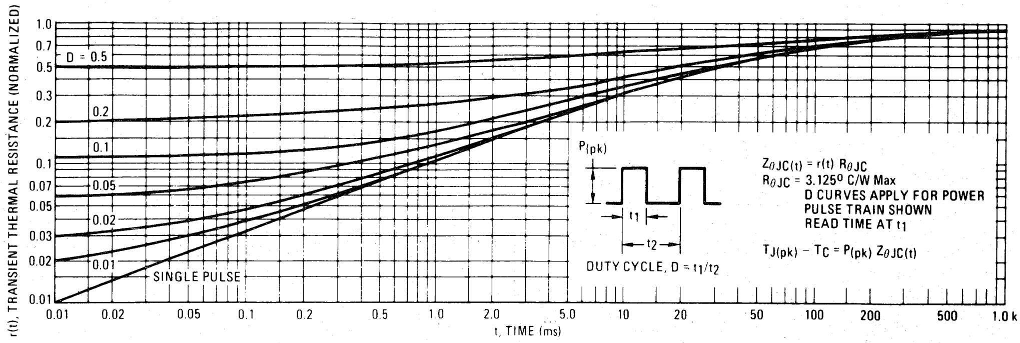
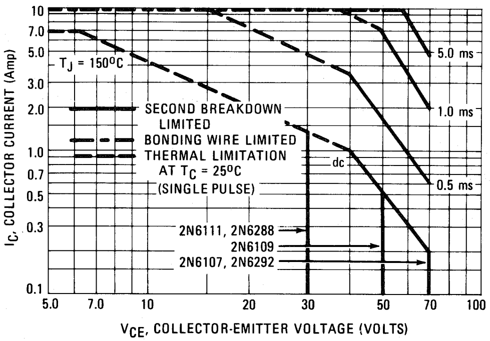


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 — TURN-OFF TIME

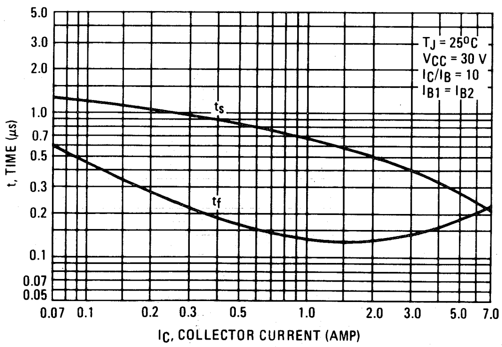
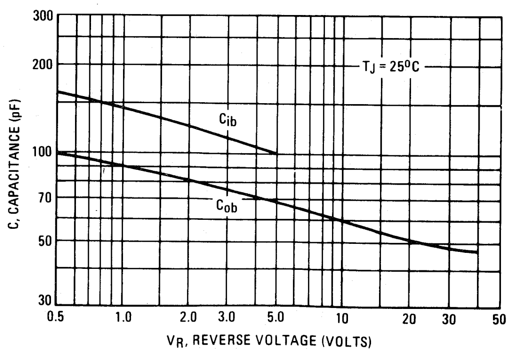


FIGURE 7 — CAPACITANCE



3

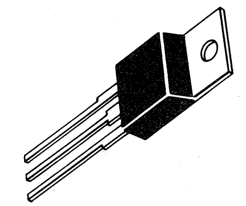
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
2N6121, 2N6122
2N6123
PNP
2N6124, 2N6125

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in power amplifier and switching circuits, — packaged in the compact TO-220AB outline. TO-66 leadform also available.

4 AMPERE
POWER TRANSISTORS COMPLEMENTARY SILICON
45-80 VOLTS
40 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N6121 2N6124	2N6122 2N6125	2N6123	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current	I_C	← 4.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	← 40 → ← 320 →			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← –65 to +150 →			°C

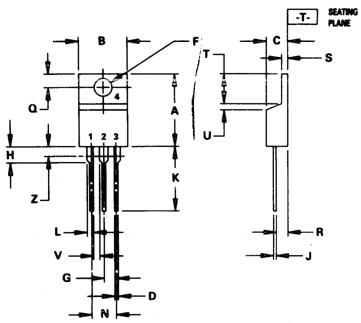
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	°C/W

*ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0)	2N6121, 2N6124		45	—	
	2N6122, 2N6125		60	—	
	2N6123		80	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 45 Vdc, I_B = 0)	2N6121, 2N6124		—	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6122, 2N6125		—	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N6123		—	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6121, 2N6124		—	0.1	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6122, 2N6125		—	0.1	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6123		—	0.1	
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6121, 2N6124		—	2.0	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6122, 2N6125		—	2.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6123, 2N6126		—	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 45 Vdc, I_E = 0)	2N6121, 2N6124		—	0.1	
(V_{CB} = 60 Vdc, I_E = 0)	2N6122, 2N6125		—	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	2N6123		—	0.1	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N6126, 2N6124		25	100	
	2N6122, 2N6125		25	100	
	2N6123		20	80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	2N6121, 2N6124		10	—	
	2N6122, 2N6125		10		
	2N6123		7.0	—	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			—	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)			—	1.4	
Base-Emitter On Voltage (1) (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 0.1 Adc, V_{CE} = 2.0 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		f_T	2.5	—	MHz

(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.
*Indicates JEDEC Registered Data.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

FIGURE 1 – DC CURRENT GAIN

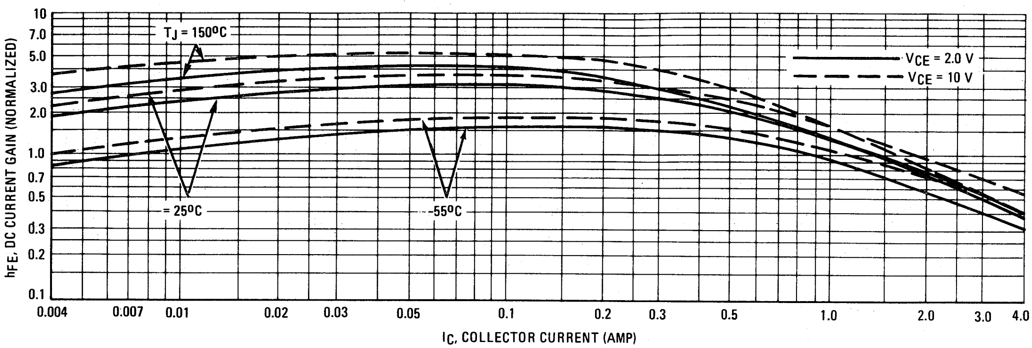


FIGURE 2 – COLLECTOR SATURATION REGION

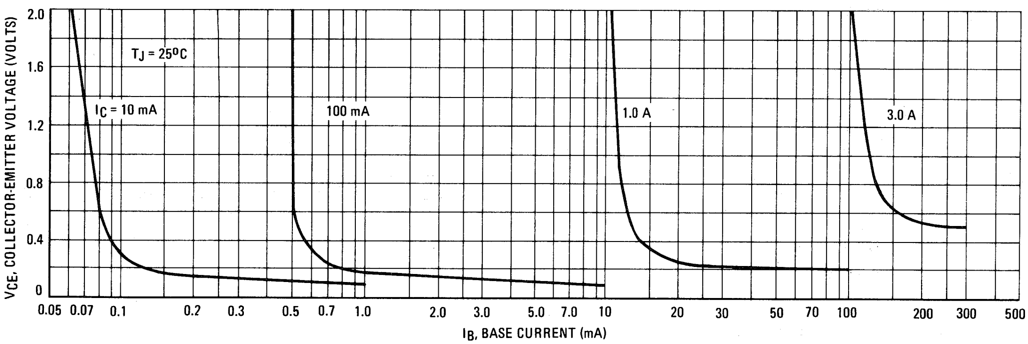


FIGURE 3 – "ON" VOLTAGES

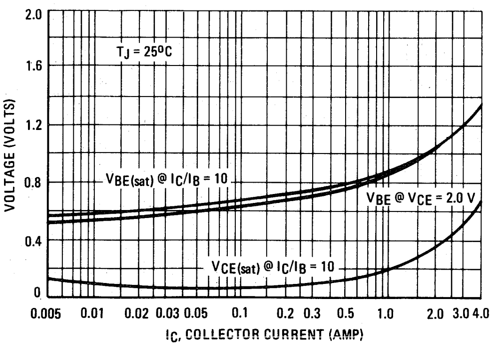
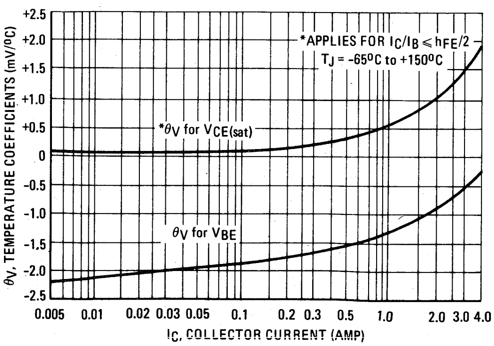


FIGURE 4 – TEMPERATURE COEFFICIENTS



3

FIGURE 5 — COLLECTOR CUT-OFF REGION

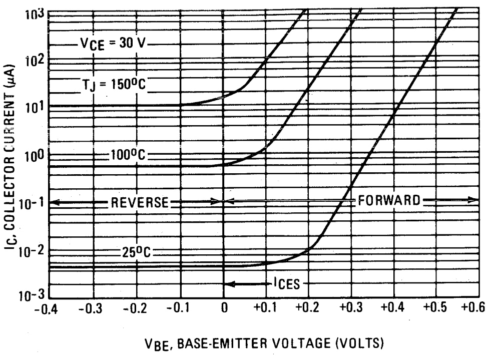


FIGURE 6 — EFFECTS OF BASE-EMITTER RESISTANCE

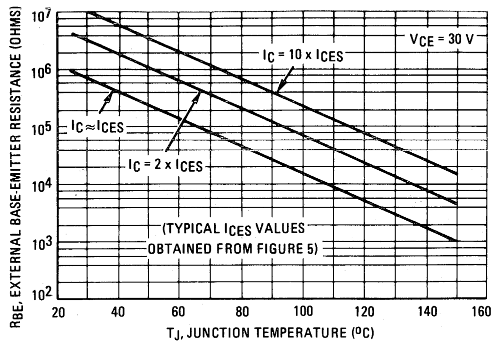
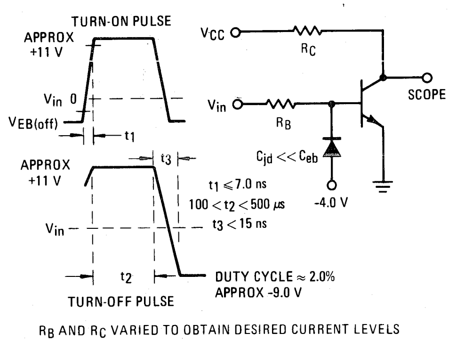


FIGURE 7 — SWITCHING TIME EQUIVALENT CIRCUIT



Reverse all polarities and diode for PNP transistors.

FIGURE 8 — CAPACITANCE

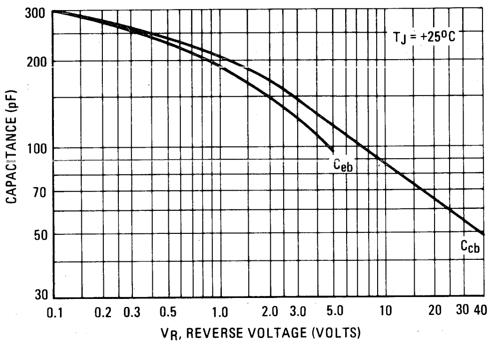


FIGURE 9 — TURN-ON TIME

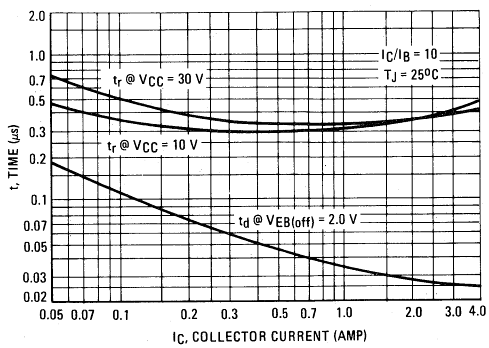
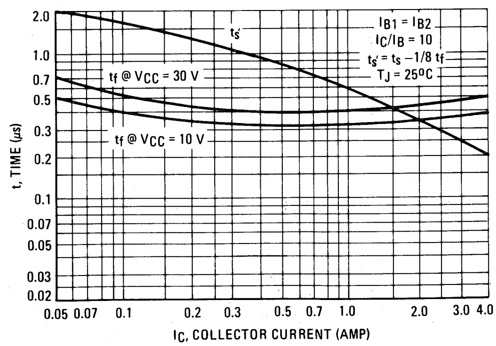
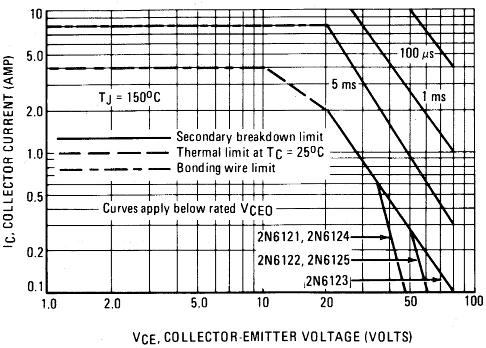


FIGURE 10 — TURN-OFF TIME



RATING AND THERMAL DATA

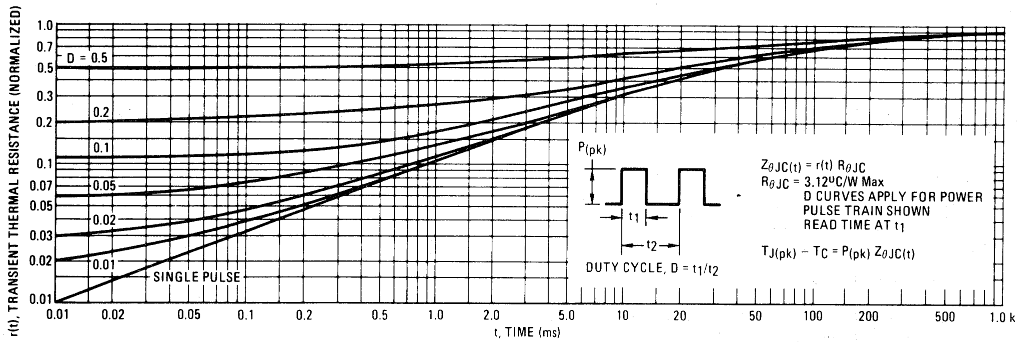
FIGURE 11 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: peak junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

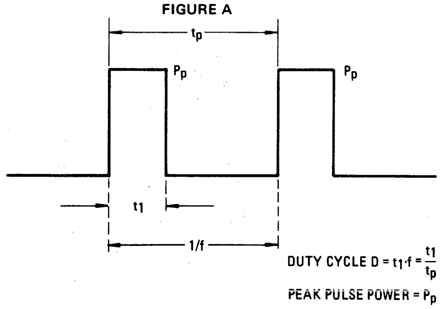
The data of Figure 11 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 12 — THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:
The 2N6121 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, t_p = 0.5 ms. (D = 0.2).
Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.
The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2°C$$

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6190
2N6191
2N6193

MEDIUM-POWER PNP SILICON TRANSISTORS

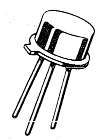
. . . designed for switching and wide band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)} = 1.2$ Vdc (Max) @ $I_C = 5.0$ Amp
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-205AD Case for Critical Space Limited Applications
- Complement to NPN 2N5336 thru 2N5339

5 AMPERE

POWER TRANSISTORS
PNP SILICON

80-100 VOLTS
10 WATTS



*MAXIMUM RATINGS

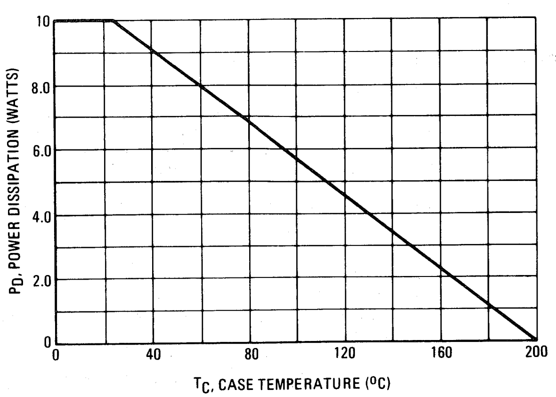
Rating	Symbol	2N6190 2N6191	2N6193	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25^oC$	P_D	10		Watts
Derate above 25^oC		57.1		$mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

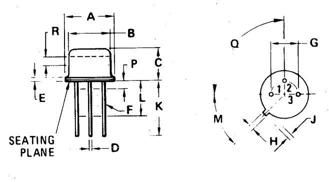
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	17.5	$^oC/W$

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER-TEMPERATURE DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-205AD

* ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	2N6190, 2N6191	$V_{CEO(sus)}$	80	–	Vdc
	2N6193		100	–	
Collector Cutoff Current (V_{CE} = 75 Vdc, I_B = 0)	2N6190, 2N6191	I_{CEO}	–	100	μAdc
(V_{CE} = 90 Vdc, I_B = 0)	2N6193		–	100	
Collector Cutoff Current (V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6190, 2N6191	I_{CEX}	–	10	μAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6193		–	10	
(V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6190, 2N6191		–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6193		–	1.0	
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	2N6190, 2N6191	I_{CBO}	–	10	μAdc
(V_{CB} = 100 Vdc, I_E = 0)	2N6193		–	10	
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N6190	h_{FE}	30	–	–
	2N6191, 2N6193		60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N6190		30	120	
	2N6191, 2N6193		60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N6190		20	–	
	2N6191, 2N6193		40	–	
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	–	0.7	Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)			–	1.2	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)		$V_{BE(sat)}$	–	1.2	Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)			–	1.8	
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (2) (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{Test} = 10 MHz)		f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	300	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		C_{ib}	–	1250	pF
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 40 Vdc, $V_{BE(off)}$ = 3.0 Vdc, I_C = 2.0 Adc, I_{B1} = 0.2 Adc)	t_d	–	100	ns
Rise Time		t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc, I_{B1} = I_{B2} = 0.2 Adc)	t_s	–	2.0	μs
Fall Time		t_f	–	200	ns

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
(2) $f_T = |h_{fe}| \cdot f_{Test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

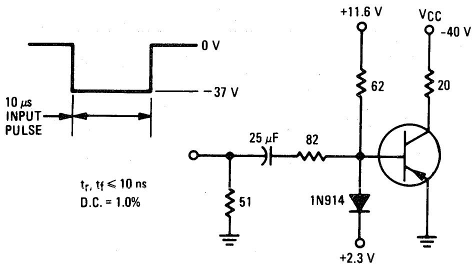
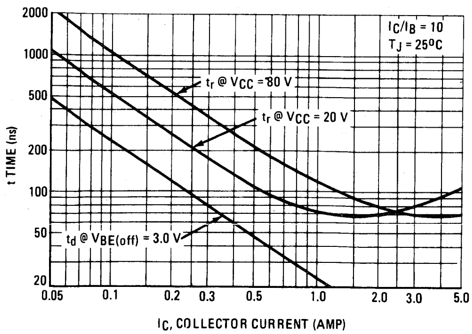


FIGURE 3 – TURN ON TIME



3

FIGURE 4 — THERMAL RESPONSE

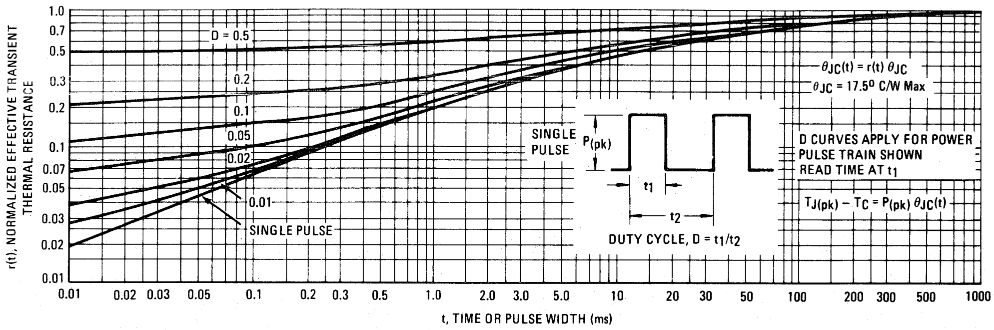
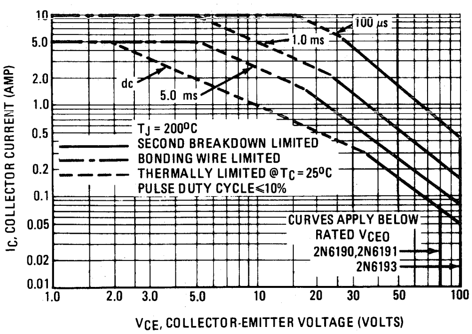


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitaitons imposed by second breakdown.

3

FIGURE 6 — TURN-OFF TIME

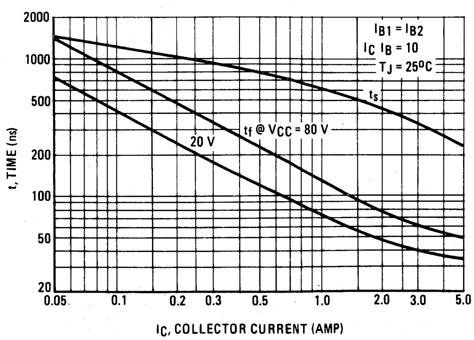
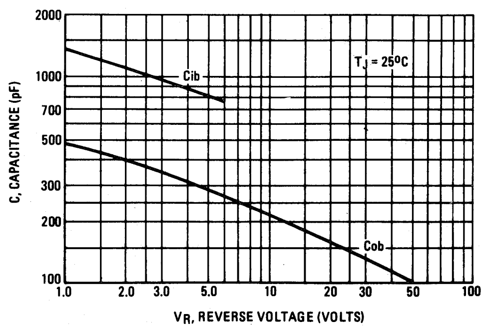


FIGURE 7 — CAPACITANCE versus VOLTAGE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6211 2N6212 2N6213

MEDIUM-POWER HIGH-VOLTAGE PNP POWER TRANSISTORS

. . . designed for high-speed switching and linear amplifier applications for high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

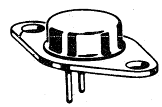
- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 225 to 350 Vdc @ I_C = 200 mAdc
- Second Breakdown Collector Current — $I_{s/b}$ = 875 mAdc @ V_{CE} = 40 Vdc
- t_f = 0.6 μs Resistive Fall Time
- Usable DC Current Gain to 2.0 Adc

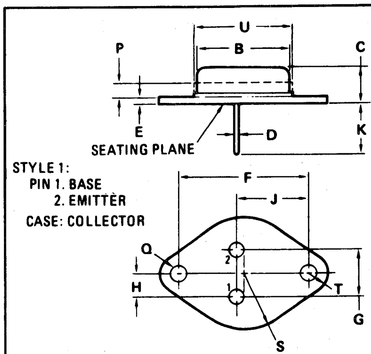
2 AMPERE

POWER TRANSISTORS

PNP SILICON

225–350 VOLTS
35 WATTS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

*MAXIMUM RATINGS

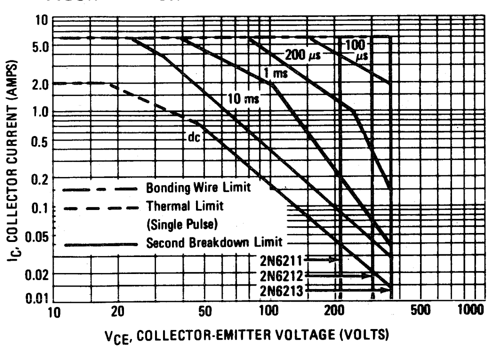
Rating	Symbol	2N6211	2N6212	2N6213	Unit
Collector-Emitter Voltage	V_{CEO}	225	300	350	Vdc
Collector-Base Voltage	V_{CB}	275	350	400	Vdc
Emitter-Base Voltage	V_{EB}		6		Vdc
Collector Current — Continuous Peak	I_C		2 5		Adc
Base Current	I_B		1		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		35 0.2		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See Figure 8).

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6211		225	–	
	2N6212		300	–	
	2N6213		350	–	
*Collector-Emitter Sustaining Voltage		$V_{CEX(sus)}$			Vdc
(I_C = 200 mA, V_{BE} = −1.5 V, L = 10 mH)	2N6211		275	–	
	2N6212		350	–	
	2N6213		400	–	
*Collector-Emitter Sustaining Voltage (1)		$V_{CER(sus)}$			Vdc
(I_C = 200 mA, I_B = 0, R_{BE} = 50 Ω)	2N6211		250	–	
	2N6212		325	–	
	2N6213		375	–	
*Emitter-Base Breakdown Voltage (1)		V_{EBO}			Vdc
(I_E = 0.5 mAdc, I_C = 0)	2N6212/13		6.0	–	
(I_E = 1.0 mAdc, I_C = 0)	2N6211		6.0	–	
*Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 25°C)			–	0.5	
(T_C = 100°C)			–	5.0	
(V_{CE} = 315 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 25°C)			–	0.5	
(T_C = 100°C)			–	5.0	
(V_{CE} = 360 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 25°C)			–	0.5	
(T_C = 100°C)			–	5.0	
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	All Types	I_{CEO}	–	5.0	mAdc
*Emitter Cutoff Current		I_{EBO}			mAdc
(V_{EB} = 6.0 Vdc, I_C = 0)	2N6211		–	1.0	
	2N6212		–	0.5	
	2N6213		–	0.5	
***ON CHARACTERISTICS (1)**					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 2.8 Vdc)	2N6211		10	100	
(I_C = 1.0 Adc, V_{CE} = 3.2 Vdc)	2N6212		10	100	
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)	2N6213		10	100	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 125 mAdc)	2N6211		–	1.4	
	2N6212		–	1.6	
	2N6213		–	2.0	
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 125 mAdc)	All Types	$V_{BE(sat)}$	–	1.4	Vdc
DYNAMIC CHARACTERISTICS					
*Current Gain—Bandwidth Product (2) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 5.0 MHz)		f_T	20	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	220	pF
***SECOND BREAKDOWN**					
*Second Breakdown Collector Current with Base Forward Biased t = 1.0 s (non-repetitive) (V_{CE} = 40 Vdc)		$I_{S/b}$	0.875	–	Adc
***SWITCHING CHARACTERISTICS**					
Rise Time	(V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.125 Adc)	t_r	–	0.6	µs
Storage Time		t_s	–	2.5	µs
Fall Time		t_f	–	0.6	µs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

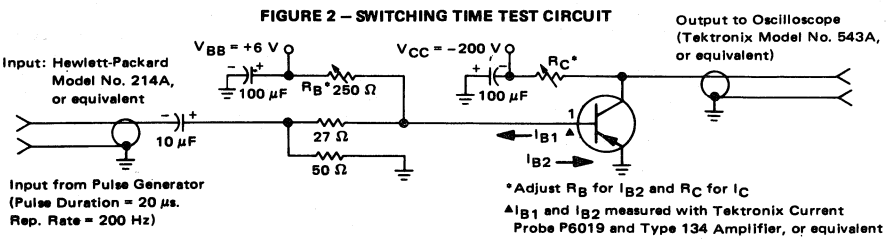


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FIGURE 3 — DC CURRENT GAIN

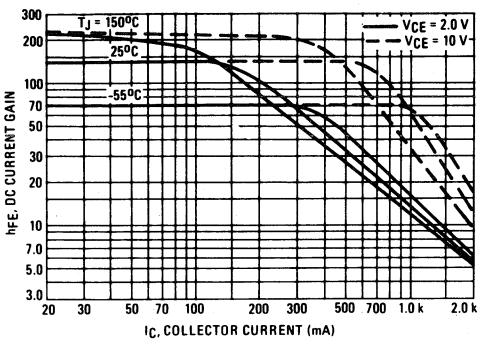


FIGURE 4 — COLLECTOR SATURATION REGION

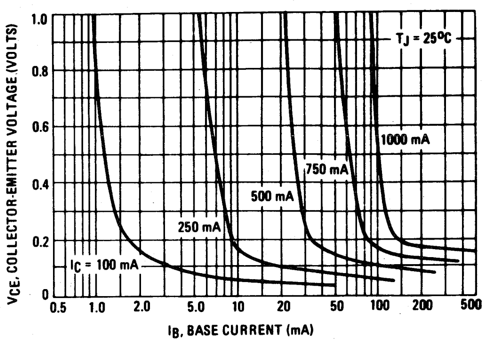


FIGURE 5 — COLLECTOR CUTOFF REGION

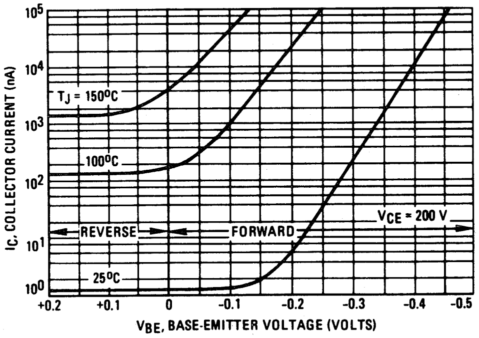


FIGURE 6 — TEMPERATURE COEFFICIENTS

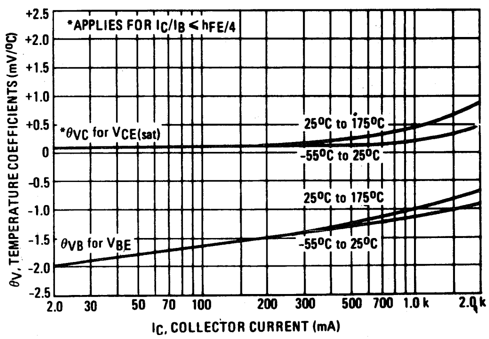


FIGURE 7 — BASE CUTOFF REGION

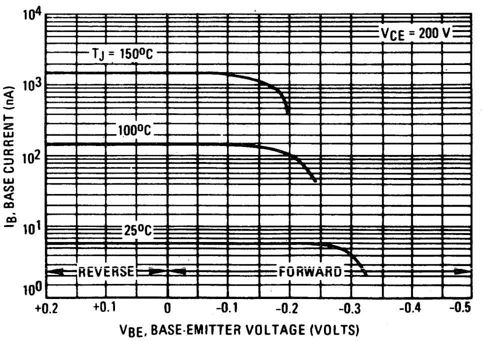
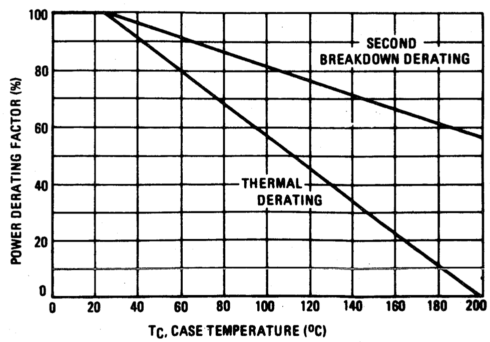


FIGURE 8 — POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6233
2N6235

HIGH VOLTAGE NPN SILICON TRANSISTORS

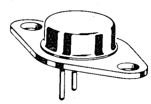
. . . useful for high-voltage medium power applications such as switching regulators.

- High Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 225 Vdc — 2N6233
  325 Vdc — 2N6235
- DC Current Gain — h_{FE} = 25 to 125 — I_C = 1.0 Adc
- Low Collector-Emitter Saturation Voltage $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 1.0 Adc
- High Frequency Response — f_T = 20 MHz (Min)
- Fast Switching Times @ 1.0 Adc —
  t_r = 0.5 μs (Max)
  t_s = 3.5 μs (Max)
  t_f = 0.5 μs (Max)

5 AMPERE

POWER TRANSISTORS
NPN SILICON

225,275,325 VOLTS
50 WATTS



*MAXIMUM RATINGS

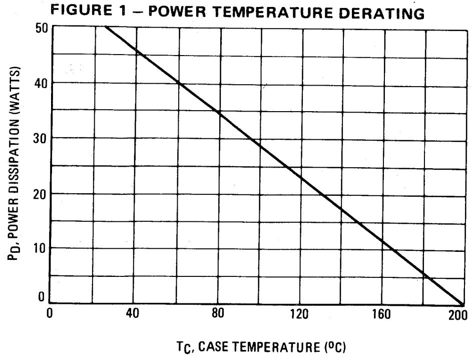
Rating	Symbol	2N6233	2N6235	Unit
Collector-Emitter Voltage	V_{CEO}	225	325	Vdc
Collector-Base Voltage	V_{CB}	250	350	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous Peak	I_C	5.0 10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.286		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

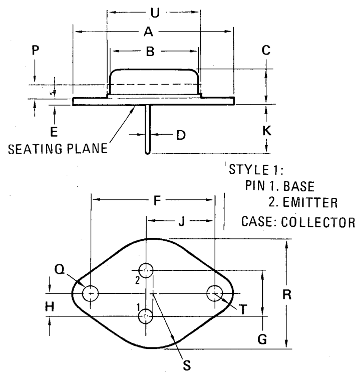
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.5	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER TEMPERATURE DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

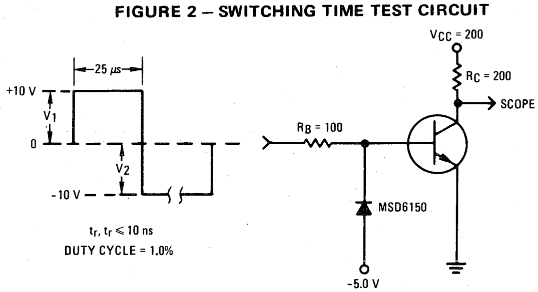
3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 20 mAdc, I_B = 0)	2N6233 2N6235	$V_{CEO(sus)}$	225 325	— —	Vdc
Collector Cutoff Current (V_{CE} = 225, I_B = 0) (V_{CE} = 325, I_B = 0)	2N6233 2N6235	I_{CEO}	— —	1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 350 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6233 2N6235	I_{CEX}	— —	1.0 1.0	mAdc
Collector Cutoff Current (V_{CB} = 250 Vdc, I_E = 0) (V_{CB} = 350 Vdc, I_E = 0)	2N6233 2N6235	I_{CBO}	— —	0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	0.1	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	25 25 10	— 125 —	—
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	— —	0.5 2.5	Vdc
Base Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	— —	1.0 2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (2) (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	20	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	250	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_B = 0.1 Adc)		t_r	—	0.5	μs
Storage Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)		t_s	—	3.5	μs
Fall Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)		t_f	—	0.5	μs

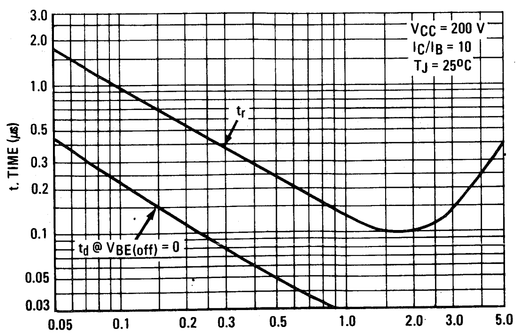
*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



FOR INFORMATION ON FIGURES 3 and 6 R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS; D_1 DISCONNECTED AND V_2 REDUCED TO 5 VOLTS FOR t_d MEASUREMENT.

FIGURE 3 — TURN-ON TIME



3

FIGURE 4 — THERMAL RESPONSE

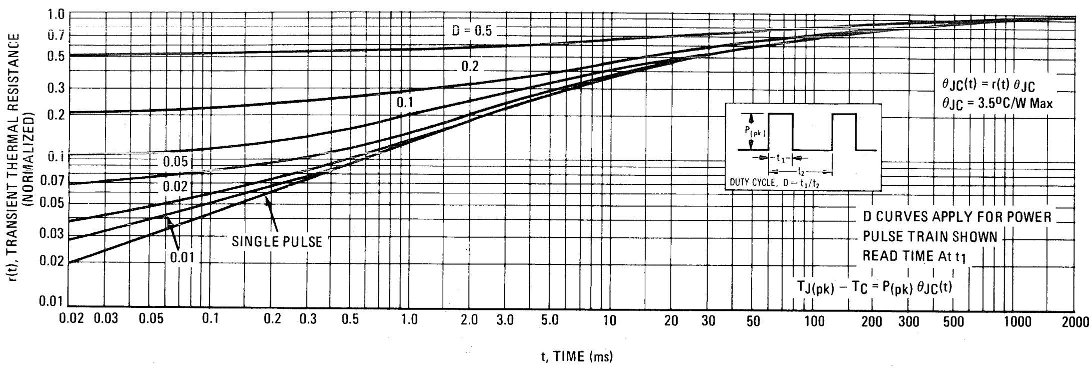
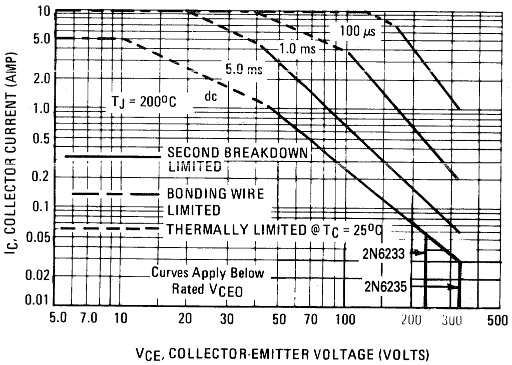


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 — TURN-OFF TIME

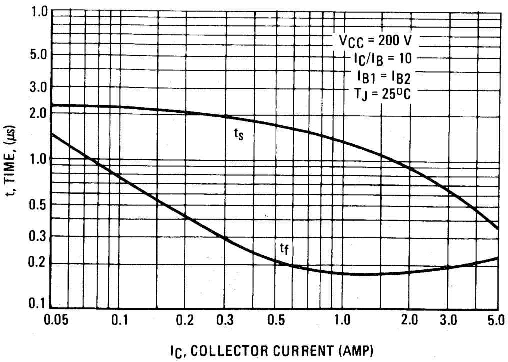
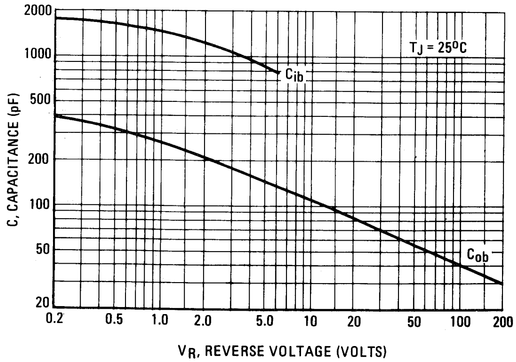


FIGURE 7 — CAPACITANCES



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6249
2N6250
2N6251

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

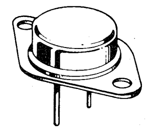
. . . designed for high voltage inverters, switching regulators and line operated amplifier applications. Especially well suited for switching power supply applications.

- High Voltage Breakdown Rating
- Low Saturation Voltages
- Fast Switching Capability
- High $E_{S/b}$ Energy Handling Capability

15 AMPERE

POWER TRANSISTORS NPN SILICON

200, 275, 350 VOLTS
175 WATTS



MAXIMUM RATINGS

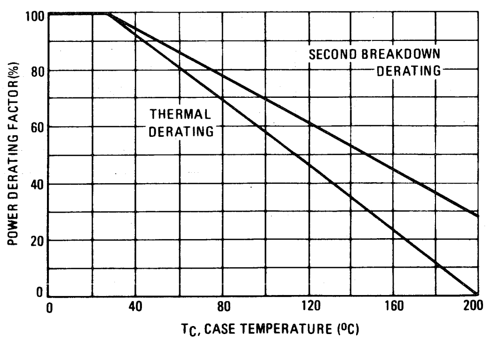
Rating	Symbol	2N6249	2N6250	2N6251	Unit
*Collector-Emitter Voltage	$V_{CEO(sus)}$	200	275	350	Vdc
*Collector-Emitter Voltage	$V_{CER(sus)}$	225	300	375	Vdc
*Collector-Base Voltage	V_{CB}	300	375	450	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current — Continuous** — Peak	I_C I_{CM}	← 15 → ← 30 →			Adc
Base Current — Continuous* — Peak	I_B I_{BM}	← 10 → ← 20 →			Adc
Emitter Current — Continuous — Peak	I_E I_{EM}	← 25 → ← 50 →			Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C*	P_D	← 175 → ← 100 → ← 1.0 →			Watts W/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

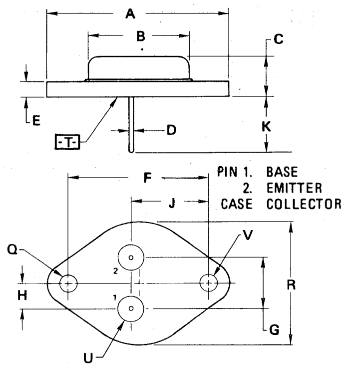
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

*Indicates JEDEC Registered Data.
**JEDEC Registered Value is 10 A, Motorola Guaranteed Value is 15 A.

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖ | ϕ0.13 (0.005) Ⓜ | T | V Ⓜ

FOR LEADS:

⌖ | ϕ0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 200 mA, I_B = 0)	2N6249	$V_{CEO(sus)}$	200	–	Vdc
	2N6250		275	–	
	2N6251		350	–	
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 200 mA)	2N6249	$V_{CER(sus)}$	225	–	Vdc
	2N6250		300	–	
	2N6251		375	–	
Collector Cutoff Current (V_{CE} = Rated V_{CER}, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	5.0	mAdc
(V_{CE} = Rated V_{CER}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)			–	10	
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	2N6249	I_{CEO}	–	5.0	mAdc
(V_{CE} = 225 Vdc, I_B = 0)	2N6250		–	5.0	
(V_{CE} = 300 Vdc, I_B = 0)	2N6251		–	5.0	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive)	(V_{CE} = 30 V)	$I_{S/b}$	5.8	–	Vdc
	(V_{CE} = 100 V)		0.3	–	
Second Breakdown Energy with base reverse biased (Table 1) (I_C = 10 A, $V_{BE(off)}$ = 4.0 Vdc, L = 50 μH)		$E_{S/b}$	2.5	–	mJ
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6249	h_{FE}	10	50	–
	2N6250		8.0	50	
	2N6251		6.0	50	
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)	2N6249	$V_{CE(sat)}$	–	1.5	Vdc
(I_C = 10 Adc, I_B = 1.25 Adc)	2N6250		–	1.5	
(I_C = 10 Adc, I_B = 1.67 Adc)	2N6251		–	1.5	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)	2N6249	$V_{BE(sat)}$	–	2.5	Vdc
(I_C = 10 Adc, I_B = 1.25 Adc)	2N6250		–	2.5	
(I_C = 10 Adc, I_B = 1.67 Adc)	2N6251		–	2.5	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	2.5	–	MHz
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Rise Time	(V_{CC} = 200 Vdc, I_C = 10 A, Duty Cycle ⩽ 2.0%, t_p = 100 μs)	t_r	–	2.0	μs
Storage Time	(I_{B1} = I_{B2} = 1.0 Adc) 2N6249; (I_{B1} = I_{B2} = 1.25 Adc) 2N6250; (I_{B1} = I_{B2} = 1.67 Adc) 2N6251	t_s	–	3.5	μs
Fall Time		t_f	–	1.0	μs

* Indicates JEDEC Registered Data.
(1) Measured on a curve tracer (60 Hz full-wave rectified sine wave).

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

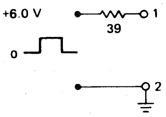
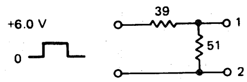
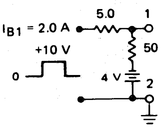
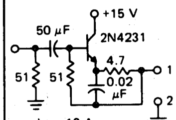
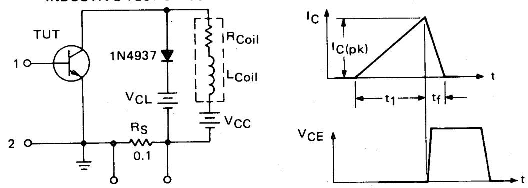
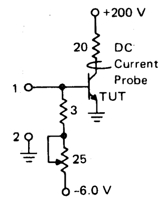
	$V_{CEO(sus)}$	$V_{CER(sus)}$	$E_{S/b}$	RESISTIVE SWITCHING
INPUT CONDITIONS				 I_C = 10 A PW ≈ 100 µs $t_r \leq$ 5 ns $t_f \leq$ 50 ns Duty Cycle ≤ 2%
CIRCUIT VALUES	L_{coil} = 42 mH R_{coil} = 0.7 Ω, f_o = 60 Hz V_{CC} = 0 to 50 V	L_{coil} = 14 mH R_{coil} = 0.05 Ω V_{CC} = 0 to 50 V f_o = 60 Hz	L_{coil} = 50 µH V_{CC} = 11.5 V R_{coil} = 0.2 Ω	V_{CC} = 200 V R_L = 20 Ω
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT / OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$ NOTE: Set $I_{C(pk)}$ to Obtain I_C = 200 mA at $V_{CEO(sus)}$ Equal to Rated Value. Adjust V_{Clamp} Voltage for $V_{CEO(sus)}$ Rated Value.			RESISTIVE TEST CIRCUIT 

FIGURE 2 – THERMAL RESPONSE

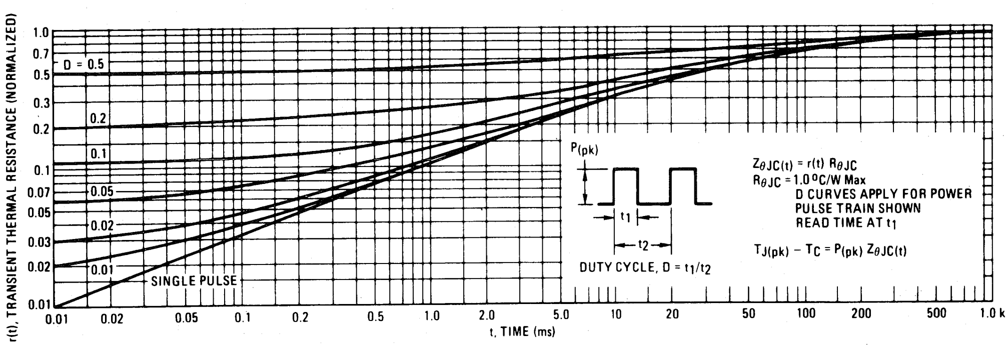
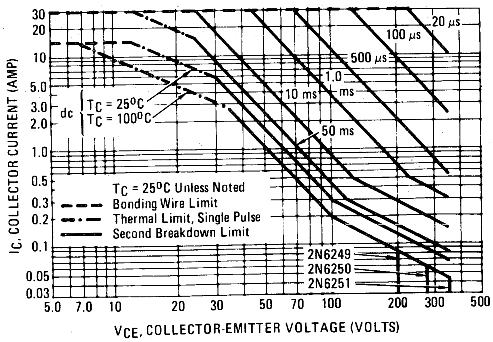


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on T_C = 25°C, $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 3 may be found at any case temperature by using the appropriate curve on Figure 1.

$T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

DC CHARACTERISTICS

FIGURE 4 — DC CURRENT GAIN

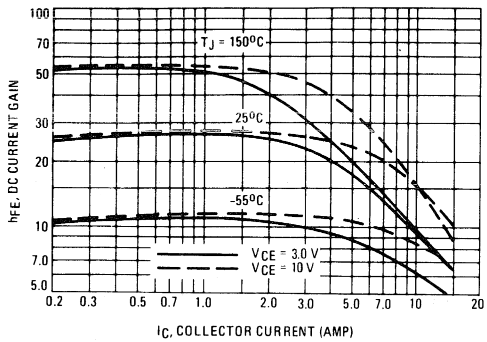


FIGURE 5 — COLLECTOR SATURATION REGION

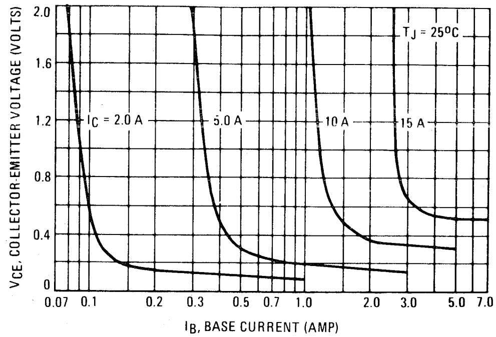


FIGURE 6 — "ON" VOLTAGE

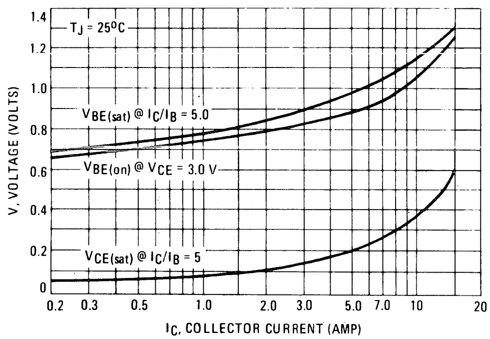
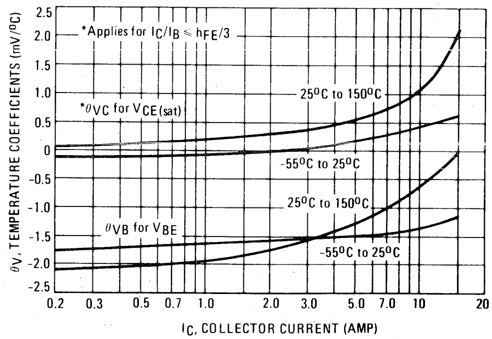


FIGURE 7 — TEMPERATURE COEFFICIENTS



RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

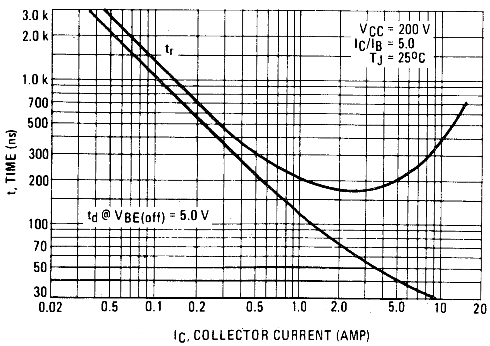
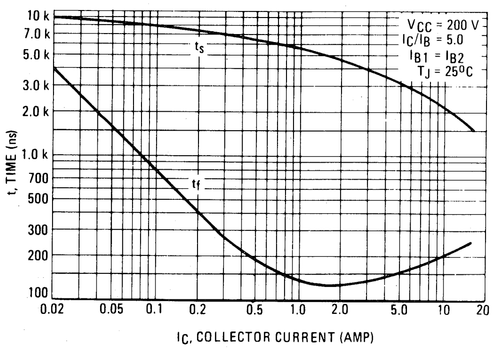


FIGURE 9 — TURN-OFF TIME



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

2N6274
2N6275
2N6277

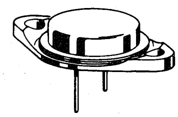
HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifer and switching circuit applications.

- High Collector Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min) — 2N6274
  = 120 Vdc (Min) — 2N6275
  = 150 Vdc (Min) — 2N6277
- High DC Current Gain —
  h_{FE} = 30-120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35 μs (Max)
  t_s = 0.8 μs (Max
  t_f = 0.25 μs (Max)
- Complement to 2N6377-79

50 AMPERE POWER TRANSISTORS NPN SILICON

100, 120, 140, 150 VOLTS 250 WATTS



*MAXIMUM RATINGS

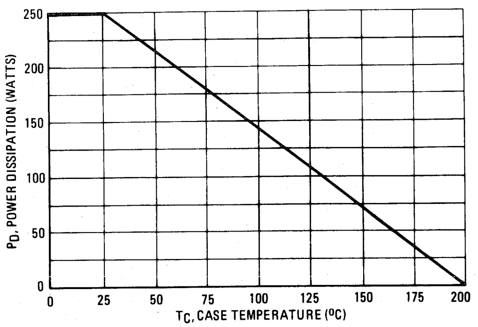
Rating	Symbol	2N6274	2N6275	2N6277	Unit
Collector-Base Voltage	V_{CB}	120	140	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	150	Vdc
Emitter-Base Voltage	V_{EB}		6.0		Vdc
Collector Current — Continuous Peak	I_C		50 100		Adc
Base Current	I_B		20		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		250 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +200		°C

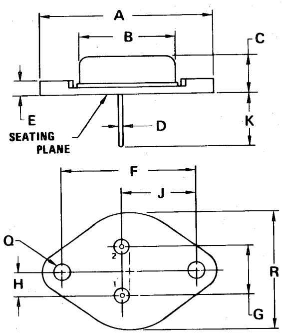
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01 TO-204AE

3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0) 2N6274	$V_{CEO(sus)}$	100	–	Vdc
2N6275		120	–	
2N6277		150	–	
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) 2N6274	I_{CEO}	–	50	μAdc
(V_{CE} = 60 Vdc, I_B = 0) 2N6275		–	50	
(V_{CE} = 75 Vdc, I_B = 0) 2N6277			50	
		–		
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	–	10	μAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	50	–	–
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)		30	120	
(I_C = 50 Adc, V_{CE} = 4.0 Vdc)		10	–	
Collector-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	–	1.0	Vdc
(I_C = 50 Adc, I_B = 10 Adc)		–	3.0	
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	–	1.8	Vdc
(I_C = 50 Adc, I_B = 10 Adc)		–	3.5	
Base-Emitter On Voltage (I_C = 20 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	600	pF
SWITCHING CHARACTERISTICS				
Rise Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = 2.0 Adc, $V_{BE(off)}$ = 5.0 Vdc)	t_r	–	0.35	μs
Storage Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)	t_s	–	0.80	μs
Fall Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)	t_f	–	0.25	μs

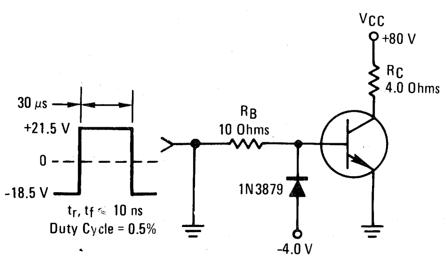
*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$.

3

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 — TURN-ON TIME

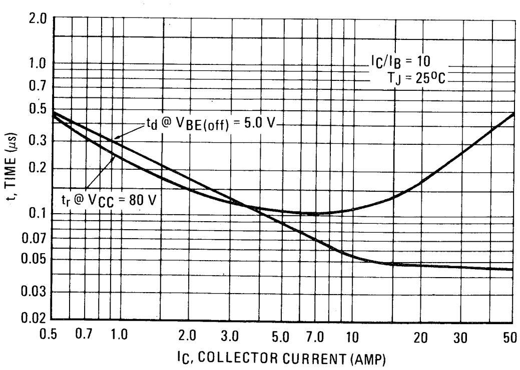


FIGURE 4 — THERMAL RESPONSE

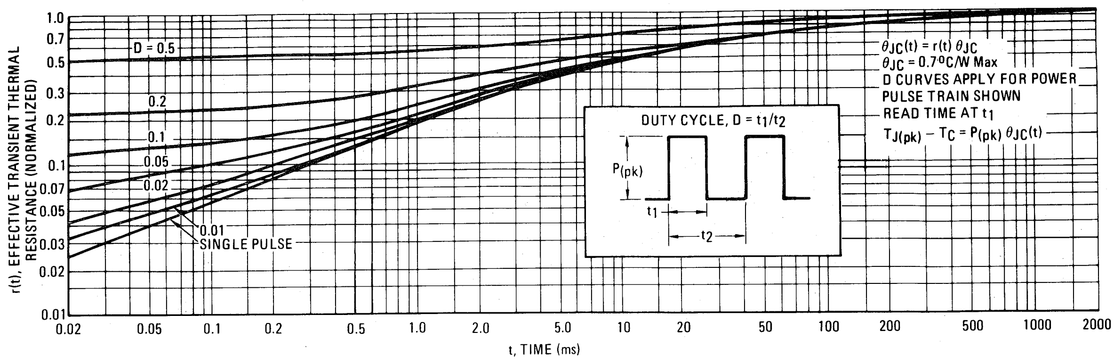
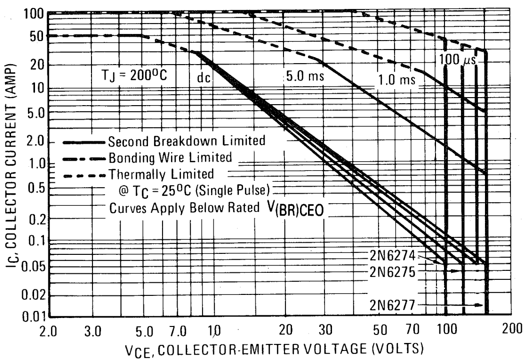


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 — TURN-OFF TIME

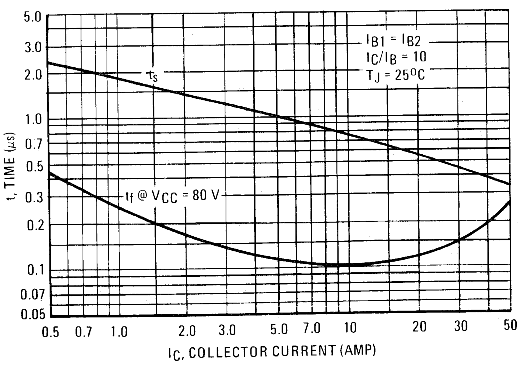


FIGURE 7 — CAPACITANCE

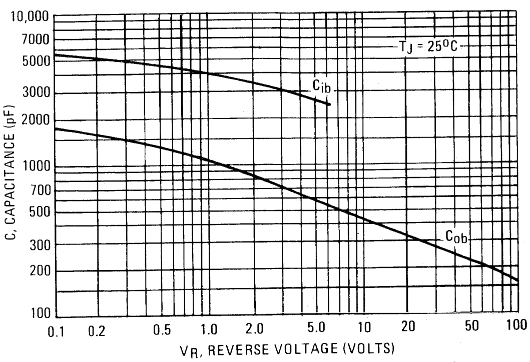


FIGURE 8 – DC CURRENT GAIN

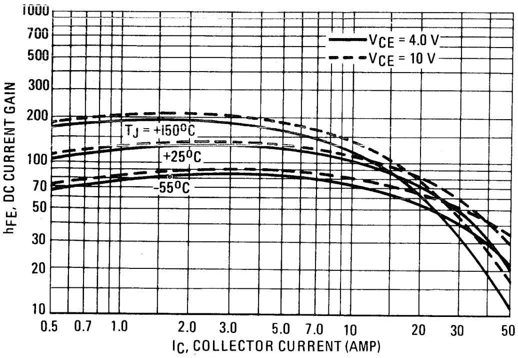


FIGURE 9 – COLLECTOR SATURATION REGION

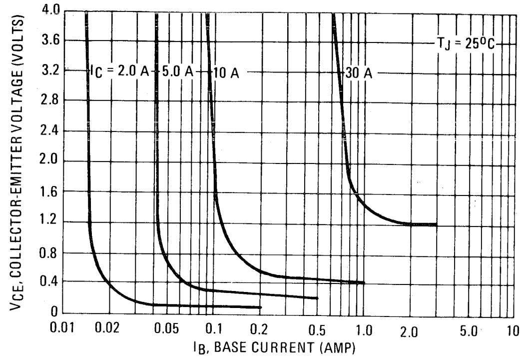


FIGURE 10 – "ON" VOLTAGES

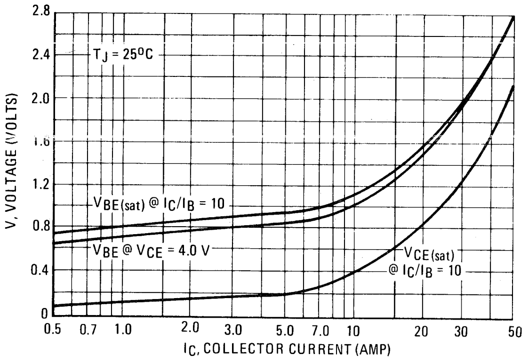


FIGURE 11 – TEMPERATURE COEFFICIENTS

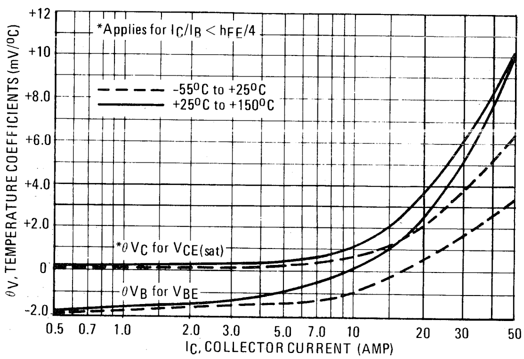


FIGURE 12 – COLLECTOR CUT-OFF REGION

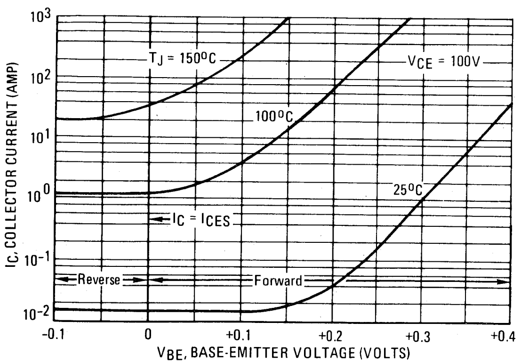
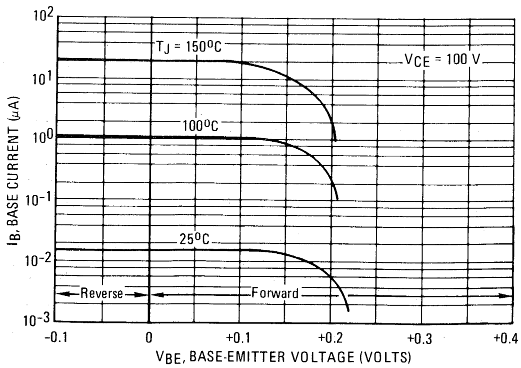


FIGURE 13 – BASE CUT-OFF REGION



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

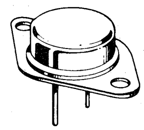
NPN
2N6282 thru 2N6284
PNP
2N6285 thru 2N6287

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low-frequency switching applications.

- High DC Current Gain @ I_C = 10 Adc —
  h_{FE} = 2400 (Typ) — 2N6282, 2N6283, 2N6284
  = 4000 (Typ) — 2N6285, 2N6286, 2N6287
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6282, 2N6285
  = 80 Vdc (Min) — 2N6283, 2N6286
  = 100 Vdc (Min) — 2N6284, 2N6287
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON
20 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60, 80, 100 VOLTS
160 WATTS



*MAXIMUM RATINGS

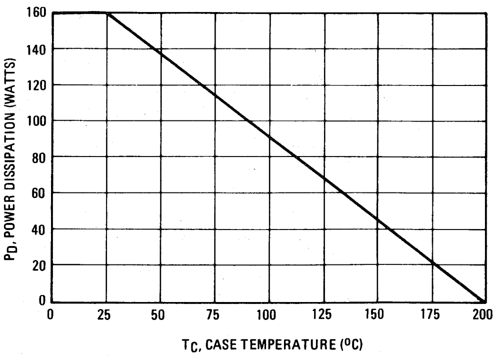
Rating	Symbol	2N6282 2N6285	2N6283 2N6286	2N6284 2N6287	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous Peak	I_C		20 40		Adc
Base Current	I_B		0.5		Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D		160 0.915		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +200		^oC

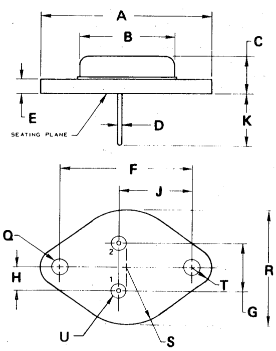
*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.09	$^oC/W$

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

CASE 1-04
TO-204AA

3

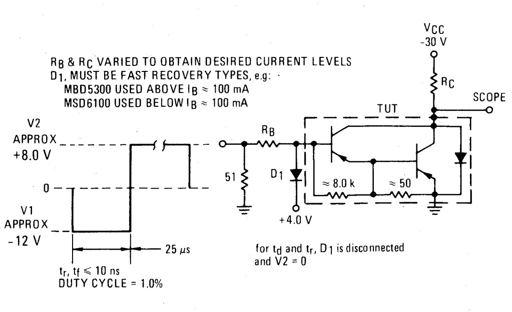
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 0.1 Adc, I_B = 0)	2N6282, 2N6285 2N6283, 2N6286 2N6284, 2N6287	$V_{CEO(sus)}$	60 80 100	– – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	2N6282, 2N6285 2N6283, 2N6286 2N6284, 2N6287	I_{CEO}	– – –	1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	– –	0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc) (I_C = 20 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	750 100	18,000 –	–
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 40 mAdc) (I_C = 20 Adc, I_B = 200 mAdc)		$V_{CE(sat)}$	– –	2.0 3.0	Vdc
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6282, 83, 84 2N6285, 86, 87	C_{ob}	– –	400 600	pF
Small-Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data.
(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2%

3

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 – SWITCHING TIMES

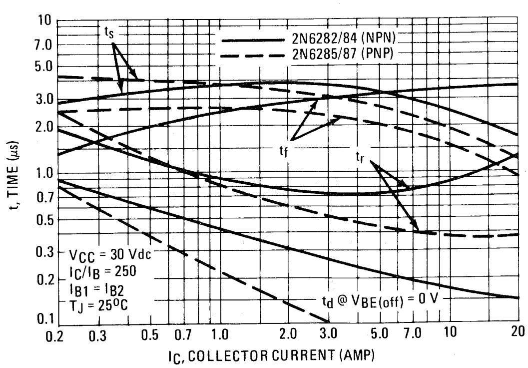
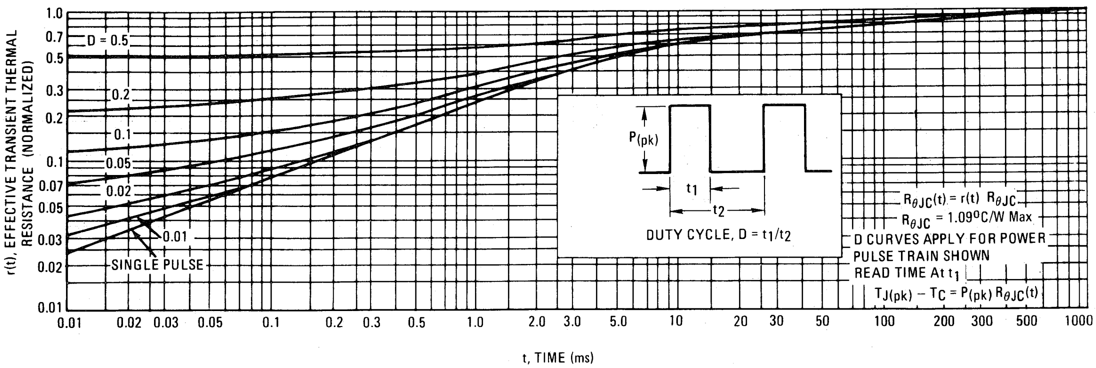


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6282, 2N6285

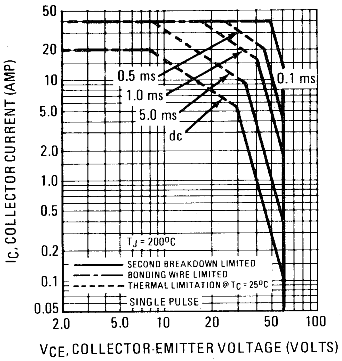


FIGURE 6 – 2N6283, 2N6286

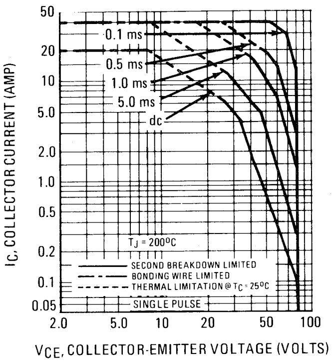
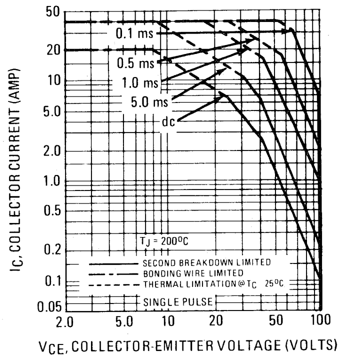


FIGURE 7 – 2N6284, 2N6287



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6 and 7 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 8 – SMALL-SIGNAL CURRENT GAIN

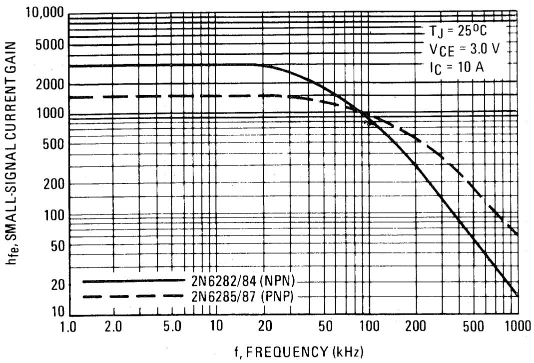
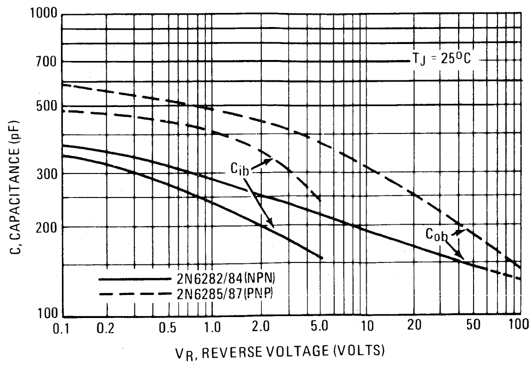
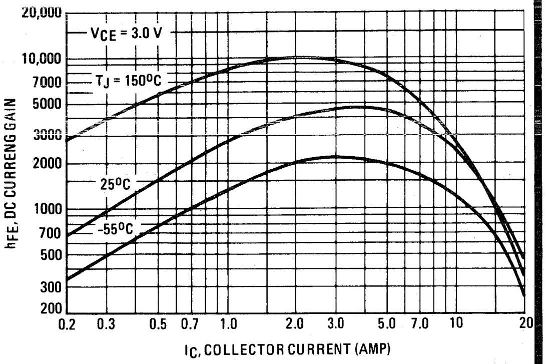


FIGURE 9 – CAPACITANCE



NPN	PNP
2N6282, 2N6283, 2N6284	2N6285, 2N6286, 2N6287

FIGURE 10 – DC CURRENT GAIN



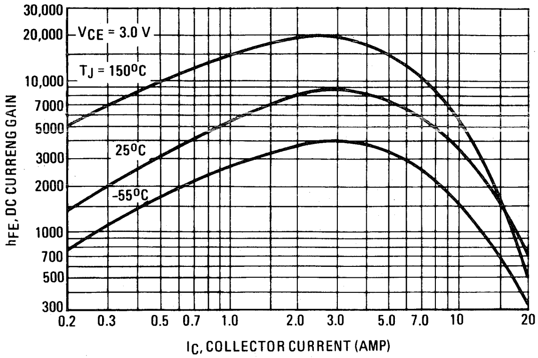
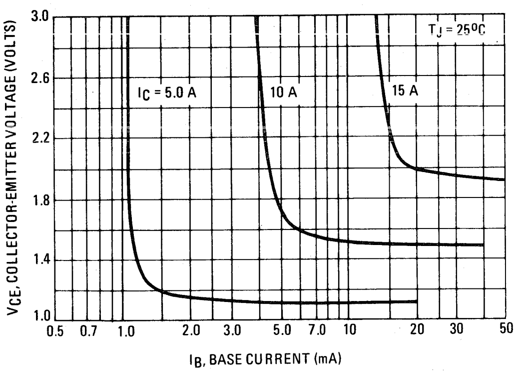


FIGURE 11 – COLLECTOR SATURATION REGION



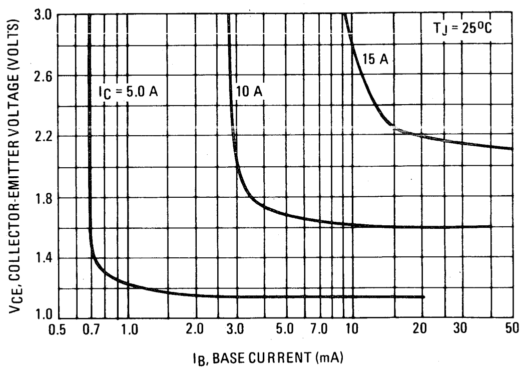
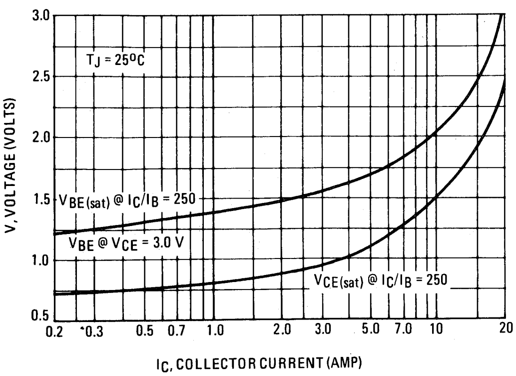
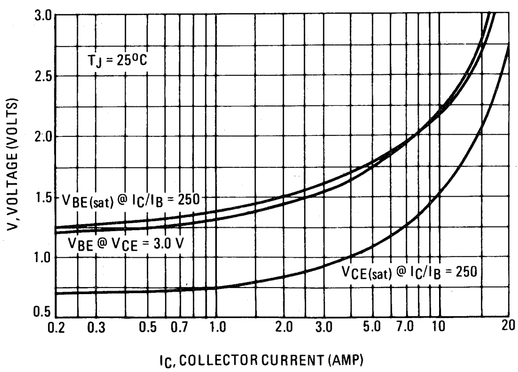


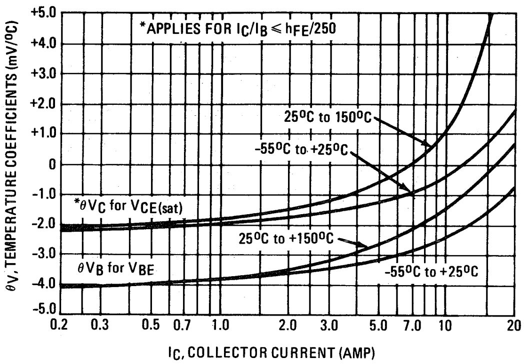
FIGURE 12 – "ON" VOLTAGES





NPN 2N6282, 2N6283, 2N6284	PNP 2N6285, 2N6286, 2N6287

FIGURE 13 – TEMPERATURE COEFFICIENTS



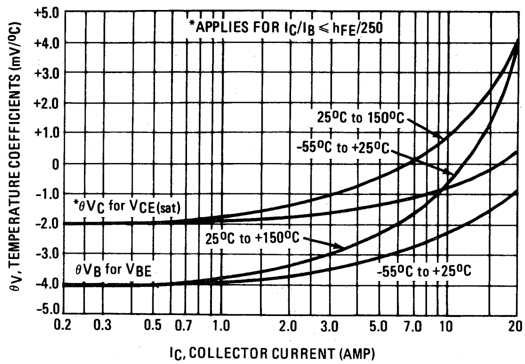
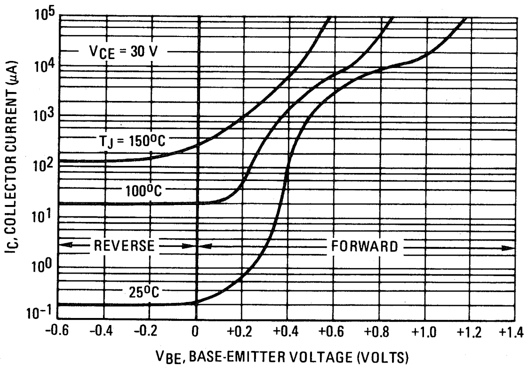


FIGURE 14 – COLLECTOR CUTOFF REGION



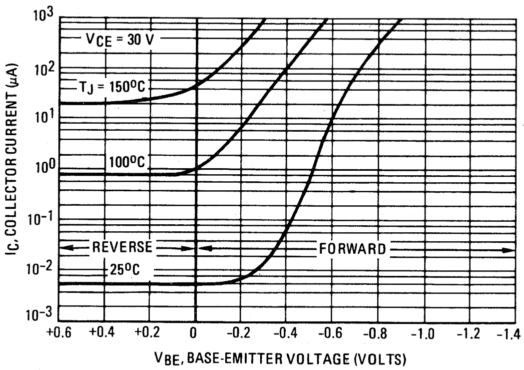
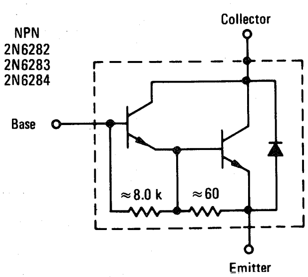
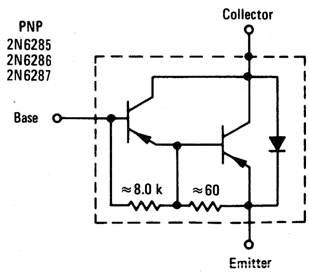


FIGURE 15 – DARLINGTON SCHEMATIC





3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

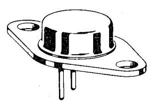
NPN 2N6294, 2N6295 PNP 2N6296, 2N6297

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier, low-frequency switching and hammer driver applications.

- High DC Current Gain — h_{FE} = 3000 (Typ) @ I_C = 2.0 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6294, 2N6296
  = 80 Vdc (Min) — 2N6295, 2N6297
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

4 AMPERES
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS
60, 80 VOLTS
50 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N6294 2N6296	2N6295 2N6297	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	4.0 8.0		Adc
Base Current	I_B	80		mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.286		Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200		°C

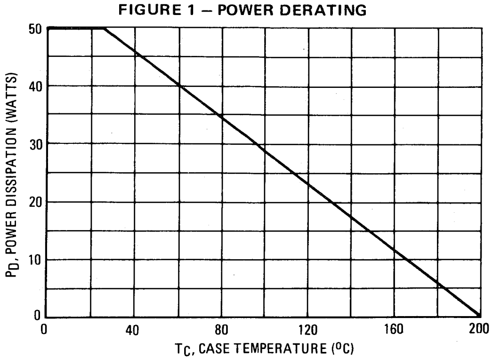
THERMAL CHARACTERISTICS

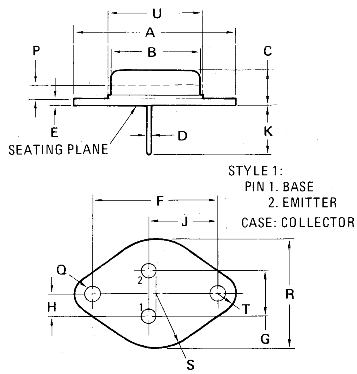
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W

*Indicates JEDEC Registered Data

3

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

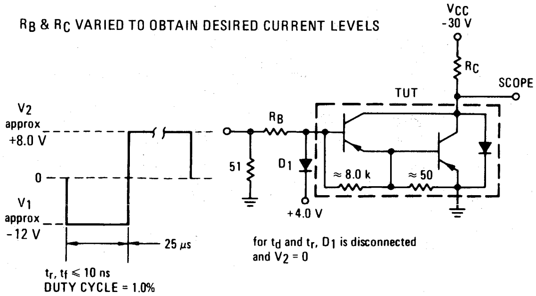
CASE 80-02
TO-213AA

*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($I_C = 50$ mAdc, $I_B = 0$)	2N6294, 2N6296 2N6295, 2N6297	$V_{CEO(sus)}$	60 80	– –	Vdc
Collector Cutoff Current ($V_{CE} = 30$ Vdc, $I_B = 0$) ($V_{CE} = 40$ Vdc, $I_B = 0$)	2N6294, 2N6296 2N6295, 2N6297	I_{CEO}	– –	0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)} = 1.5$ Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)} = 1.5$ Vdc) (V_{CE} = Rated V_{CB}, $V_{EB(off)} = 1.5$ Vdc, $T_C = 150^oC$) (V_{CE} = Rated V_{CB}, $V_{BE(off)} = 1.5$ Vdc, $T_C = 150^oC$)	2N6294, 2N6295 2N6296, 2N6297 2N6294, 2N6295 2N6296, 2N6297	I_{CEX}	– – – –	0.5 0.5 5.0 5.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain ($I_C = 2.0$ Adc, $V_{CE} = 3.0$ Vdc) ($I_C = 4.0$ Adc, $V_{CE} = 3.0$ Vdc)		h_{FE}	750 100	18000 –	–
Collector-Emitter Saturation Voltage ($I_C = 2.0$ Adc, $I_B = 8.0$ mAdc) ($I_C = 4.0$ Adc, $I_B = 40$ mAdc)		$V_{CE(sat)}$	– –	2.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 4.0$ Adc, $I_B = 40$ mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage ($I_C = 2.0$ Adc, $V_{CE} = 3.0$ Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio ($I_C = 1.5$ Adc, $V_{CE} = 3.0$ Vdc, f = 1.0 MHz)		$\lvert h_{fe} \rvert$	4.0	–	–
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, f = 0.1 MHz)	2N6294, 2N6295 2N6296, 2N6297	C_{ob}	– –	120 200	pF
Small-Signal Current Gain ($I_C = 1.5$ Adc, $V_{CE} = 3.0$ Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit, reverse all polarities.

FIGURE 3 – SWITCHING TIMES

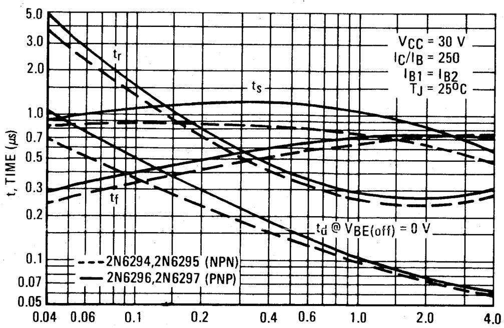


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FIGURE 4 — THERMAL RESPONSE

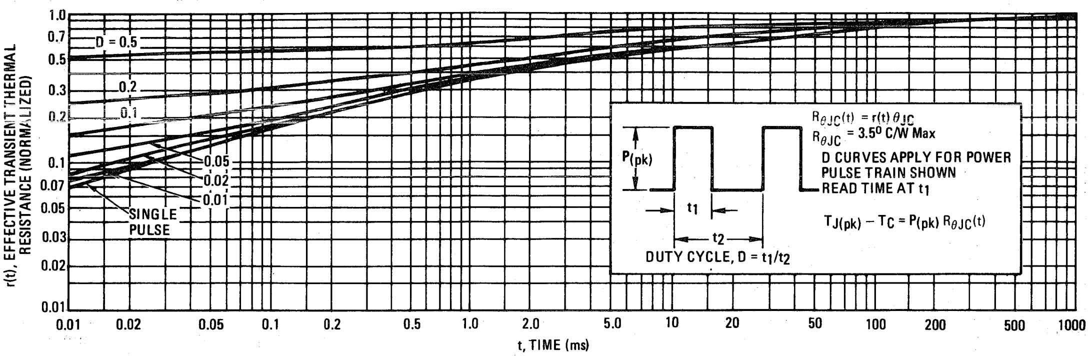
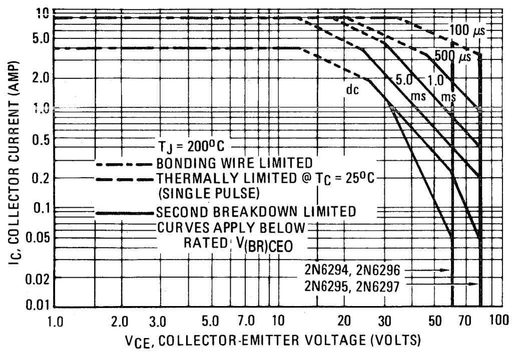


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — SMALL-SIGNAL CURRENT GAIN

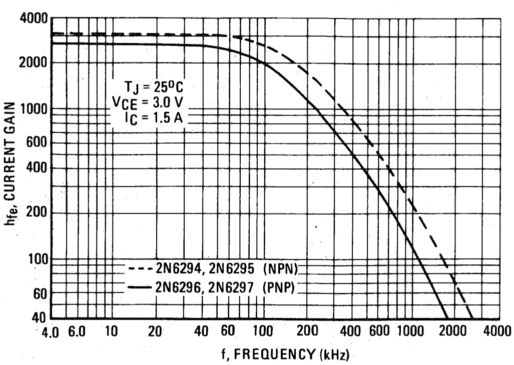
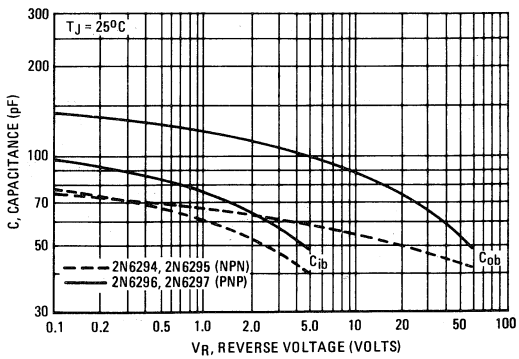


FIGURE 7 — CAPACITANCE



3

NPN
2N6294, 2N6295

PNP
2N6296, 2N6297

FIGURE 8 — DC CURRENT GAIN

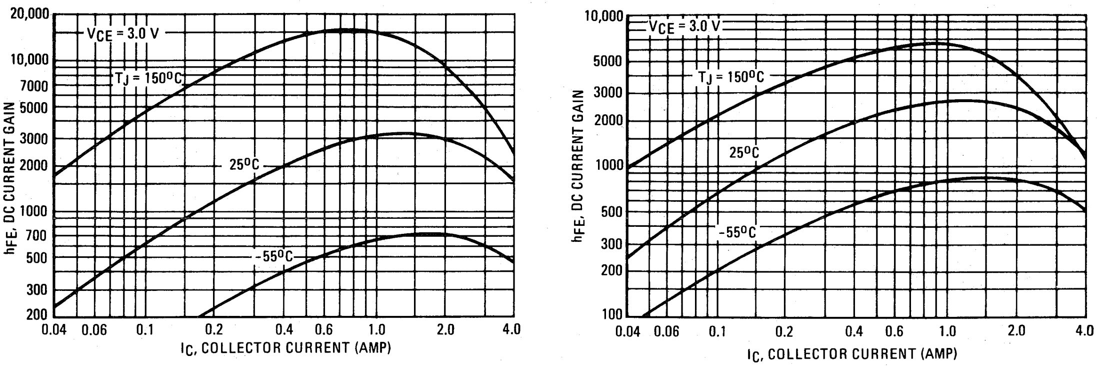


FIGURE 9 — COLLECTOR SATURATION REGION

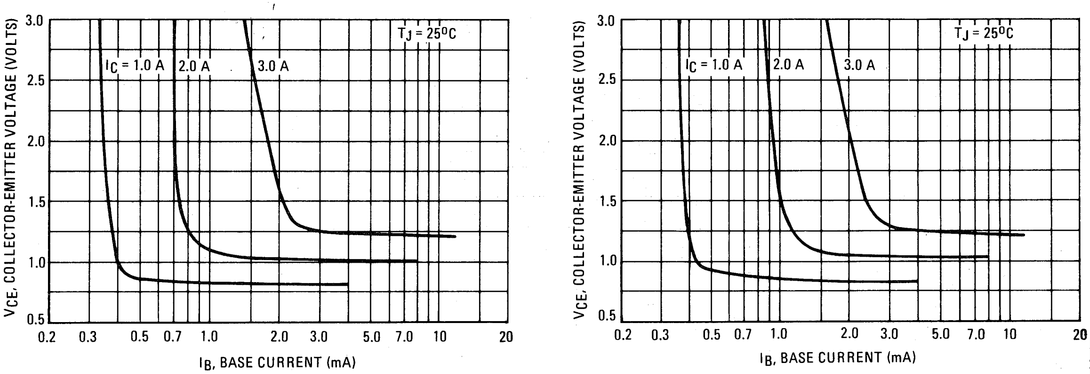
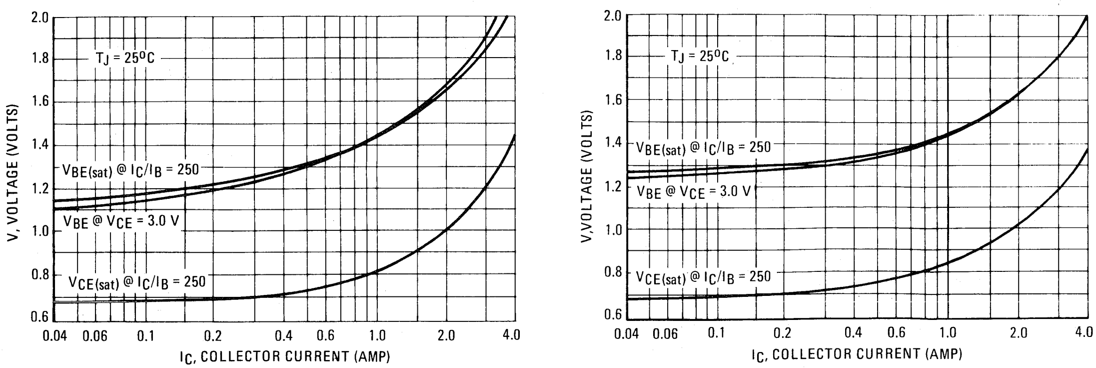


FIGURE 10 — "ON" VOLTAGES



3

2N6298 thru 2N6301
See Page 3-157
2N6303 — See Page 3-32

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6306
2N6307, 2N6308

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

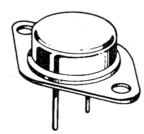
. . . designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications in associated consumer products.

- High Collector-Base Voltage —
  V_{CB} = 500 Vdc — 2N6306
  = 600 Vdc — 2N6307
  = 700 Vdc — 2N6308
- Excellent DC Current Gain @ I_C = 3.0 Adc
  h_{FE} = 15 - 75 — 2N6306, 2N6307
  = 12 - 60 — 2N6308
- Low Collector-Emitter Saturation Voltage @ I_C = 3.0 Adc
  $V_{CE(sat)}$ = 0.8 Vdc (Max) — 2N6306
  = 1.0 Vdc (Max) — 2N6307
  = 1.5 Vdc (Max) — 2N6308
- Current Gain Bandwidth Product —
  f_T = 5.0 MHz (Min) @ I_C = 0.3 Adc

8 AMPERE POWER TRANSISTORS

NPN SILICON

250-300-350 VOLTS
125 WATTS



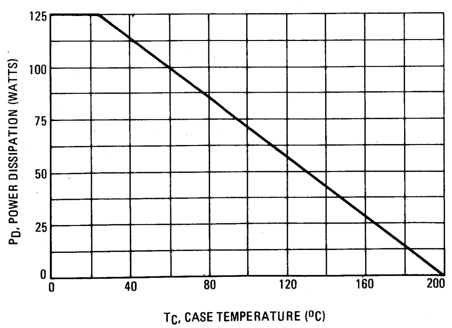
*MAXIMUM RATINGS

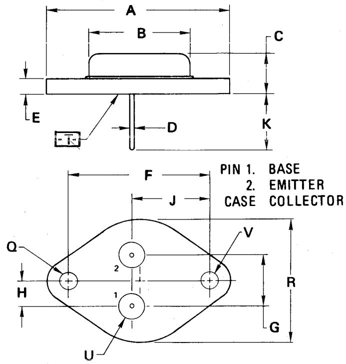
Rating	Symbol	2N6306	2N6307	2N6308	Unit
Collector-Base Voltage	V_{CB}	500	600	700	Vdc
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Emitter-Base Voltage	V_{EB}	8.0			Vdc
Collector Current — Continuous Peak	I_C	8.0 16			Adc
Base Current	I_B	4.0			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.714			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.4	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ϕ0.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ϕ0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6306		250	–	
	2N6307		300	–	
	2N6308		350	–	
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}	–	0.5	mAdc
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 500 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6306		–	0.5	
(V_{CE} = 600 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6307		–	0.5	
(V_{CE} = 700 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6308		–	0.5	
(V_{CE} = 450 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6306		–	2.5	
(V_{CE} = 550 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6307		–	2.5	
(V_{CE} = 650 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6308		–	2.5	
Emitter Cutoff Current (V_{BE} = 8.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	2N6306, 2N6307		15	75	
	2N6308		12	60	
(I_C = 8.0 Adc, V_{CE} = 5.0 Vdc)	2N6306, 2N6307		4.0	–	
	2N6308		3.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc)	2N6306		–	0.8	
	2N6307		–	1.0	
	2N6308		–	1.5	
(I_C = 8.0 Adc, I_B = 2.0 Adc)	2N6306, 2N6307		–	5.0	
(I_C = 8.0 Adc, I_B = 2.67 Adc)	2N6308		–	5.0	
Base-Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 8.0 Adc, I_B = 2.0 Adc)	2N6306, 2N6307		–	2.3	
(I_C = 8.0 Adc, I_B = 2.67 Adc)	2N6308		–	2.5	
Base-Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	2N6306, 2N6307		–	1.3	
	2N6308		–	1.5	
Second Breakdown Energy (Figure 2) ($I_{C(PK)}$ = 3.0 Adc, L = 40 mH, R_{BE} = 3 kΩ, V_{BB2} = 1.5 Vdc)		$E_{s/b}$	–	180	mJ
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 0.3 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	5.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	250	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 125 Vdc, I_C = 3.0 Adc, I_B = 0.6 Adc)		t_r	–	0.6	μs
Storage Time (3) (V_{CC} = 125 Vdc, I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc)		t_s			μs
	Pulse Width = 25 μs		–	1.6	
	Pulse Width = 5.0 μs		–	0.8	
Fall Time (V_{CC} = 125 Vdc, I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc)		t_f	–	0.4	μs

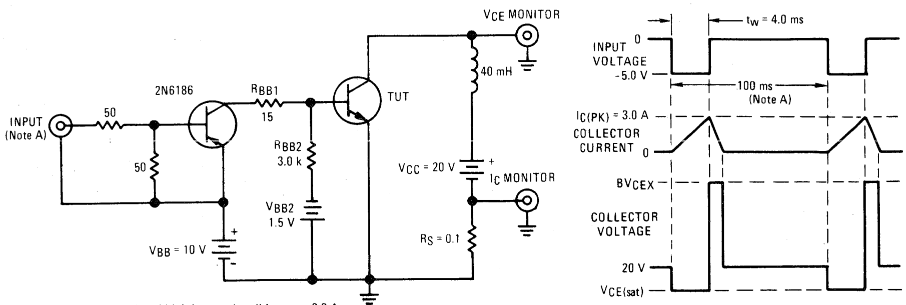
(1) Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle = 2.0%

(2) $f_T = |h_{fe}| \bullet f_{test}$

(3) "On" time is 25 μs. t_s decreases with shorter pulse widths, being approximately 50% of the values shown at a 5.0 μs pulse width.

*Indicates JEDEC Registered Data.

FIGURE 2 — SECOND BREAKDOWN ENERGY TEST CIRCUIT AND WAVEFORMS



Note A: Input pulse width is increased until $I_{C(PK)}$ = 3.0 A.

3

FIGURE 3 – THERMAL RESPONSE

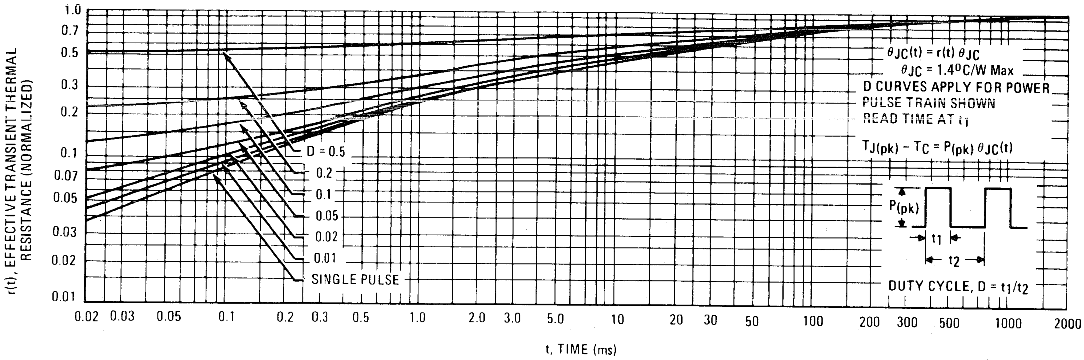
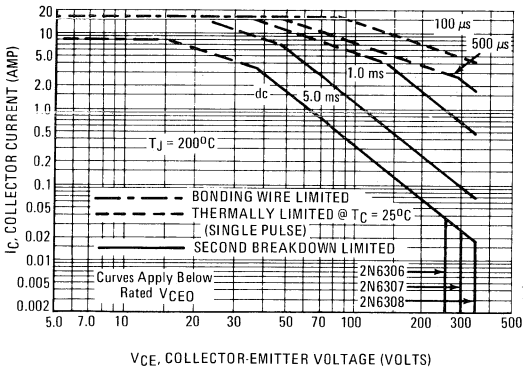


FIGURE 4 – ACTIVE-REGION SAFE OPERATING AREA

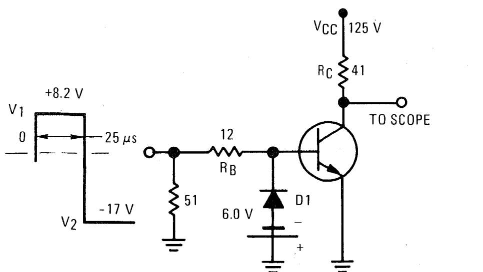


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 5 – SWITCHING TIMES TEST CIRCUIT



DUTY CYCLE 1%
t_r, $t_f \leq 10$ ns
D_1 – 1N3879
COLLECTOR-BASE JUNCTION

FOR DATA IN FIGURE 6, R_B & R_C ARE VARIED TO OBTAIN DESIRED TEST CONDITIONS. D_1 OMITTED AND V_2 REDUCED TO 5.0 V FOR t_d and t_r MEASUREMENTS

FIGURE 6 – TURN-ON AND TURN-OFF TIMES

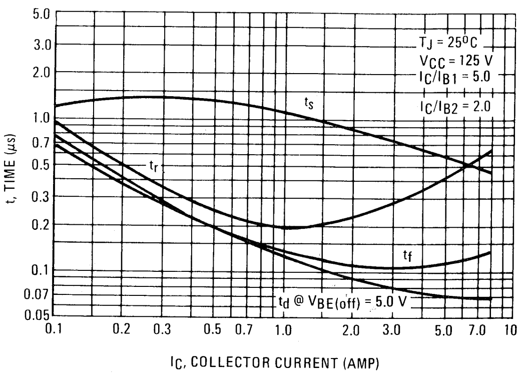


FIGURE 7 – DC CURRENT GAIN

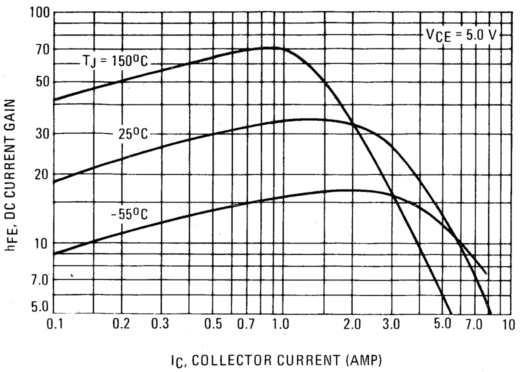


FIGURE 8 – COLLECTOR SATURATION REGION

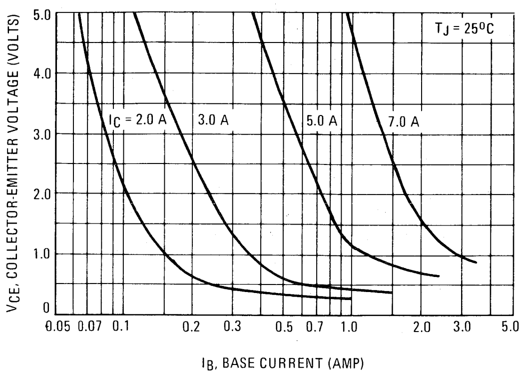


FIGURE 9 – "ON" VOLTAGES

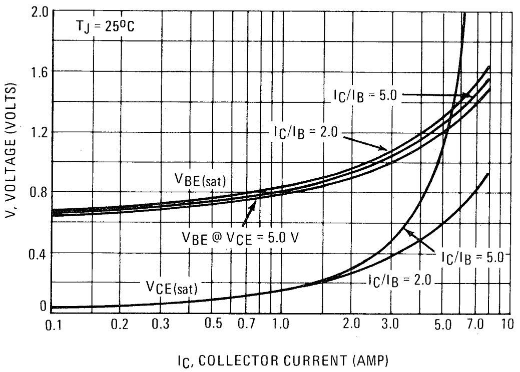


FIGURE 10 – TEMPERATURE COEFFICIENTS

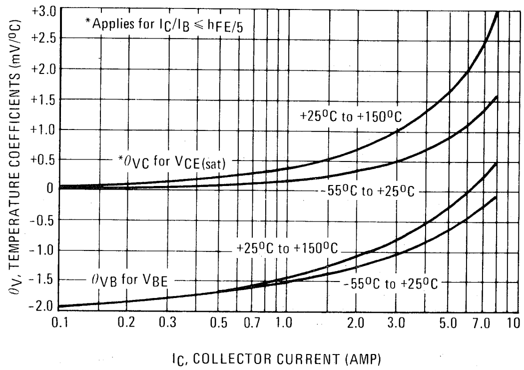


FIGURE 11 – COLLECTOR-CUTOFF REGION

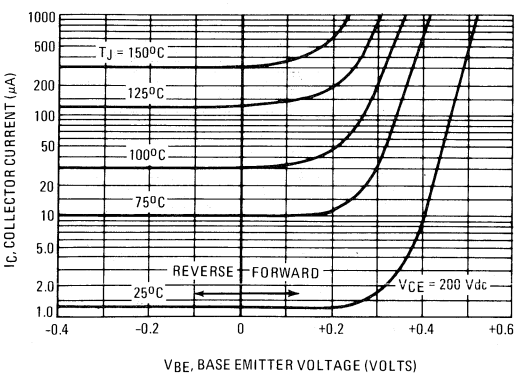
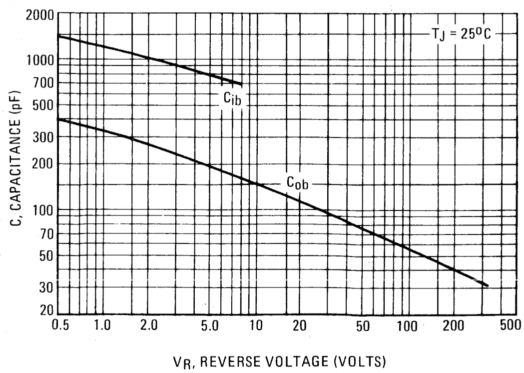


FIGURE 12 – CAPACITANCE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
2N6315, 2N6316
PNP
2N6317, 2N6318

COMPLEMENTARY SILICON MEDIUM-POWER TRANSISTORS

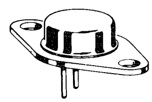
. . . designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 4.0 Adc
- Low Leakage Current — I_{CEX} = 0.25 mAdc (Max)
- Excellent DC Current Gain — h_{FE} = 20 (Min) @ I_C = 2.5 Adc
- High Current Gain — Bandwidth Product — f_T = 4.0 MHz @ I_C = 0.25 Adc

7.0 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
90 WATTS



*MAXIMUM RATINGS

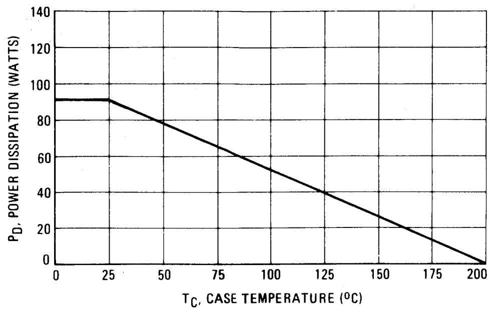
Rating	Symbol	2N6315 2N6317	2N6316 2N6318	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	7.0 15		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation — T_C = 25°C Derate above 25°C	P_D	90 0.515		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

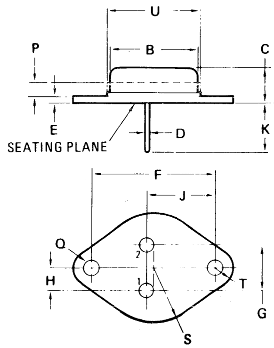
Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.94	°C/W

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

FIGURE 1 — POWER DERATING



Safe Area Limits are indicated by Figure 13.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	2N6315,2N6317	$V_{CEO(sus)}$	60	–	Vdc
	2N6316,2N6318		80	–	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	2N6315,2N6317	I_{CEO}	–	0.5	mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6316,2N6318		–	0.5	
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6315,2N6317	I_{CEX}	–	0.25	mAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6316,2N6318		–	0.25	
(V_{CE} = 60 Vdc $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6315,2N6317		–	2.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6316,2N6318		–	2.0	
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)	2N6315,2N6317	I_{CBO}	–	0.25	mAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N6316,2N6318		–	0.25	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	35	–	–
(I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
Collector-Emitter Saturation Voltage (1) (I_C = 4.0 Adc, I_B = 0.4 Adc)		$V_{CE(sat)}$	–	1.0	Vdc
(I_C = 7.0 Adc, I_B = 1.75 Adc)			–	2.0	
Base-Emitter Saturation Voltage (1) (I_C = 7.0 Adc, I_B = 1.75 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2) (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N6317,2N6318	C_{ob}	–	300	pF
	2N6315,2N6316		–	200	
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.25 Adc)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

3

NPN
2N6315 and 2N6316

PNP
2N6317 and 2N6318

FIGURE 2 — DC CURRENT GAIN

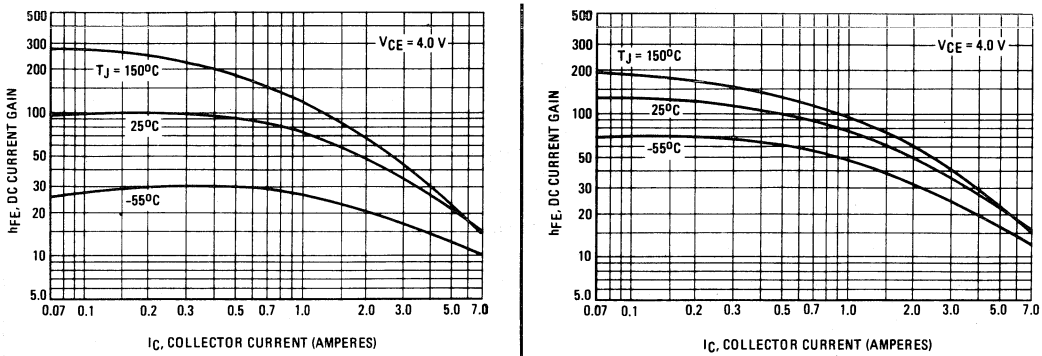


FIGURE 3 — COLLECTOR SATURATION REGION

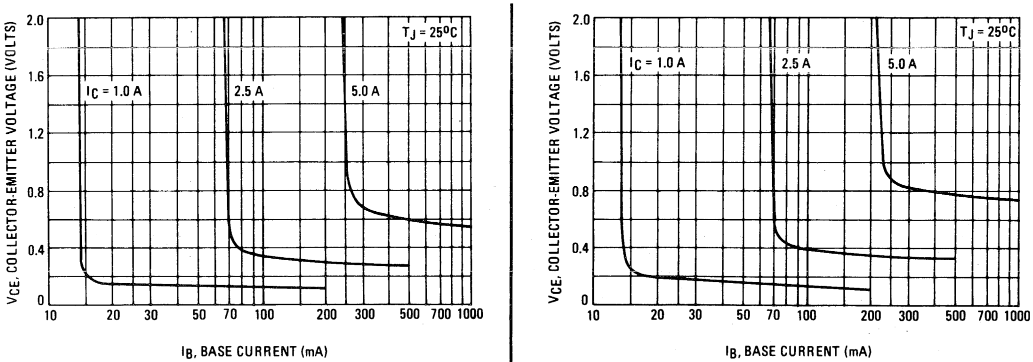


FIGURE 4 — "ON" VOLTAGES

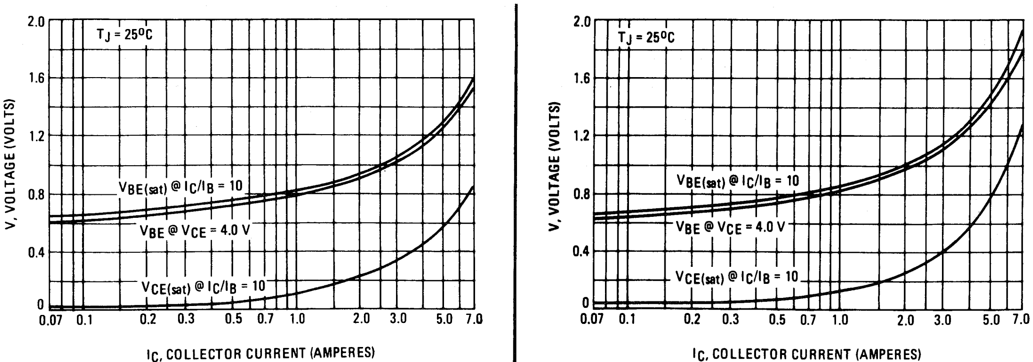
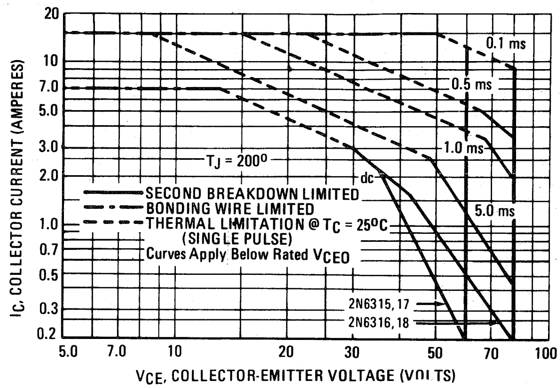


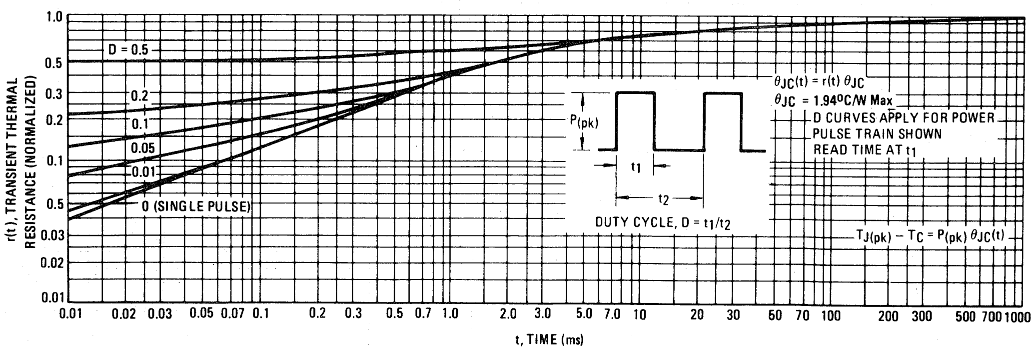
FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6338 thru 2N6341

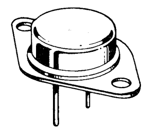
HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min) — 2N6338
  = 120 Vdc (Min) — 2N6339
  = 140 Vdc (Min) — 2N6340
  = 150 Vdc (Min) — 2N6341
- High DC Current Gain —
  h_{FE} = 30-120 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 μs (Max)
  t_s = 1.0 μs (Max)
  t_f = 0.25 μs (Max)
- Complement to 2N6436–38

25 AMPERE POWER TRANSISTORS NPN SILICON

100, 120, 140, 150 VOLTS 200 WATTS



*MAXIMUM RATINGS

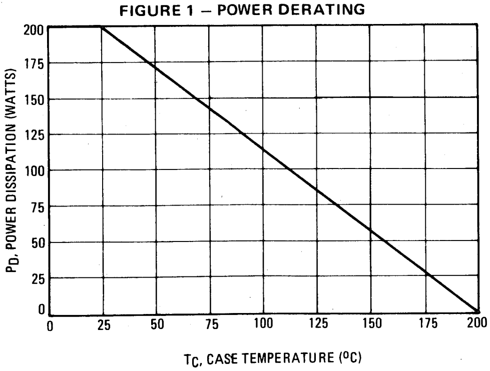
Rating	Symbol	2N6338	2N6339	2N6340	2N6341	Unit
Collector-Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →				Vdc
Collector Current — Continuous Peak	I_C	← 25 → ← 50 →				Adc
Base Current	I_B	← 10 →				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 200 → ← 1.14 →				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →				°C

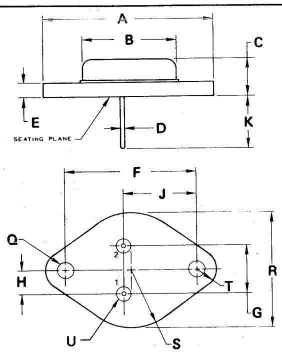
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1–04

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

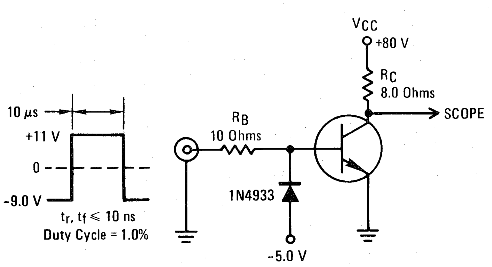
3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1)	$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0) 2N6338		100	–	
2N6339		120	–	
2N6340		140	–	
2N6341		150	–	
Collector Cutoff Current	I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0) 2N6338		–	50	
(V_{CE} = 60 Vdc, I_B = 0) 2N6339		–	50	
(V_{CE} = 70 Vdc, I_B = 0) 2N6340		–	50	
(V_{CE} = 75 Vdc, I_B = 0) 2N6341		–	50	
Collector Cutoff Current	I_{CEX}			
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc)		–	10	μAdc
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		–	1.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)		50	–	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)		30	120	
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)		12	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)		–	1.0	
(I_C = 25 Adc, I_B = 2.5 Adc)		–	1.8	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)		–	1.8	
(I_C = 25 Adc, I_B = 2.5 Adc)		–	2.5	
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	40	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	300	pF
SWITCHING CHARACTERISTICS				
Rise Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 6.0 Vdc)	t_r	–	0.3	μs
Storage Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_s	–	1.0	μs
Fall Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_f	–	0.25	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 — TURN-ON TIME

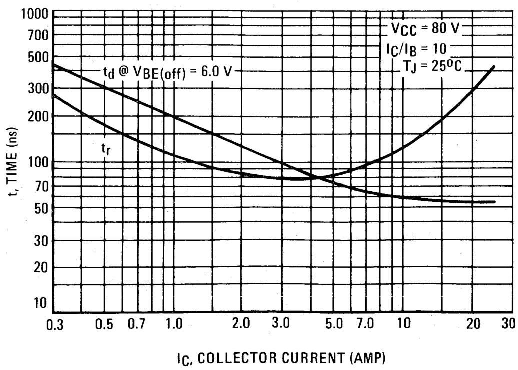


FIGURE 4 – THERMAL RESPONSE

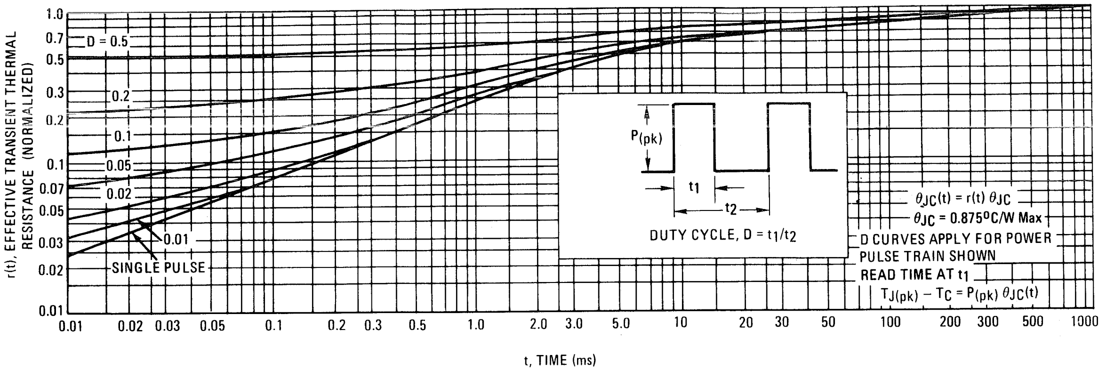
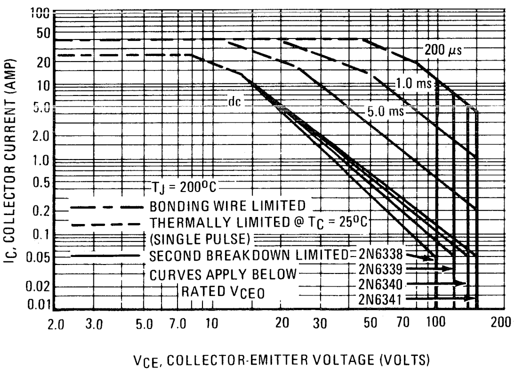


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

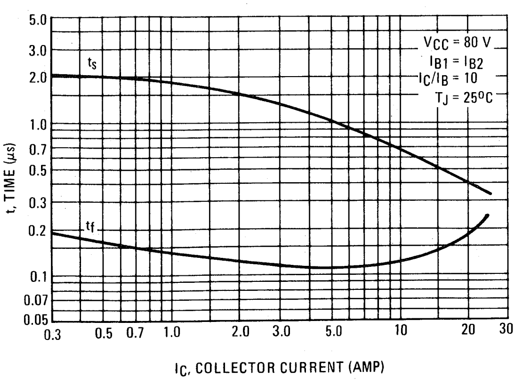
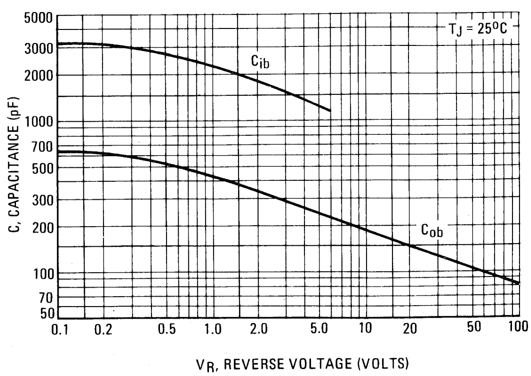


FIGURE 7 – CAPACITANCE



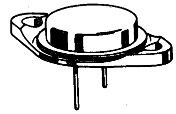
2N6377 thru 2N6379

HIGH-POWER PNP SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector Emitter Sustaining Voltage —
  $V_{CEO\ (sus)}$ = 80 Vdc (Min) — 2N6377
  = 100 Vdc (Min) — 2N6378
  = 120 Vdc (Min) — 2N6379
- High DC Current Gain —
  h_{FE} = 30-120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35 μs (Max)
  t_s = 0.8 μs (Max)
  t_f = 0.25 μs (Max)
- Complement to 2N6274—77

50 AMPERE
POWER TRANSISTORS
PNP SILICON
80, 100, 120 VOLTS
250 WATTS



* MAXIMUM RATINGS

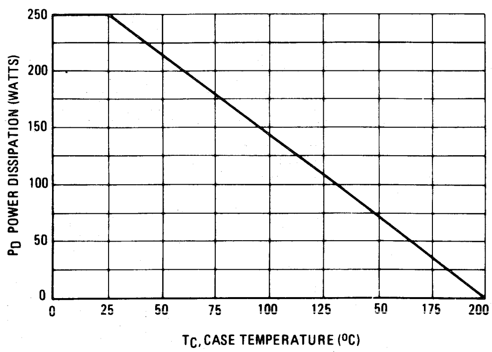
Rating	Symbol	2N6377	2N6378	2N6379	Unit
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Collector-Emitter Voltage	V_{CEO}	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 50 → ← 100 →			Adc
Base Current	I_B	← 20 →			Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	← 250 → ← 1.43 →			Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			^oC

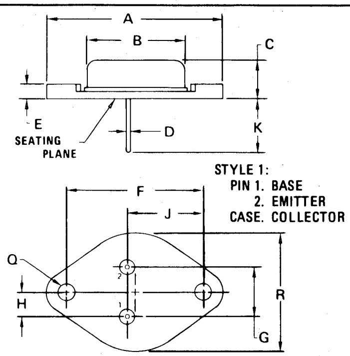
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^oC/W$

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

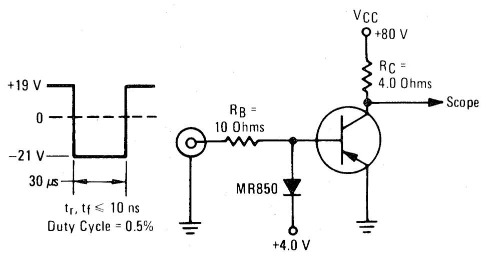
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0) 2N6377	$V_{CEO(sus)}$	80	–	Vdc
2N6378		100	–	
2N6379		120	–	
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) 2N6377	I_{CEO}	–	50	μAdc
(V_{CE} = 60 Vdc, I_B = 0) 2N6378		–	50	
(V_{CE} = 70 Vdc, I_B = 0) 2N6379		–	50	
Collector Cutoff Current (V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	10	μAdc
(V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
***ON CHARACTERISTICS** (1)				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	50	–	–
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)		30	120	
(I_C = 50 Adc, V_{CE} = 4.0 Vdc)		10	–	
Collector-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	–	1.2	Vdc
(I_C = 50 Adc, I_B = 10 Adc)		–	3.0	
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	–	1.8	Vdc
(I_C = 50 Adc, I_B = 10 Adc)		–	3.5	
DYNAMIC CHARACTERISTICS				
*Current-Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	30	–	MHz
*Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	1500	pF
***SWITCHING CHARACTERISTICS** (Figure 2)				
Rise Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)	t_r	–	0.35	μs
Storage Time	t_s	–	0.80	μs
Fall Time	t_f	–	0.25	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

3

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



Note: For information on Figures 3 & 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 — TURN ON TIME

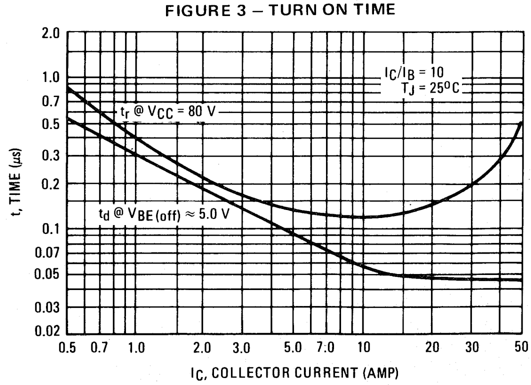


FIGURE 4 – THERMAL RESPONSE

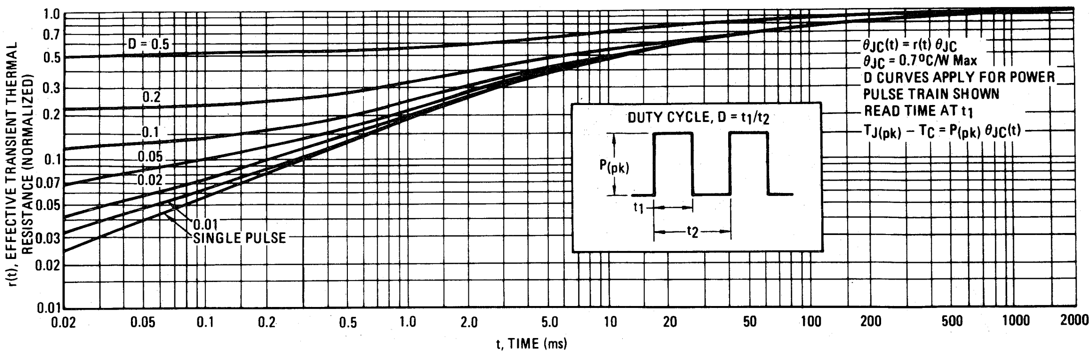
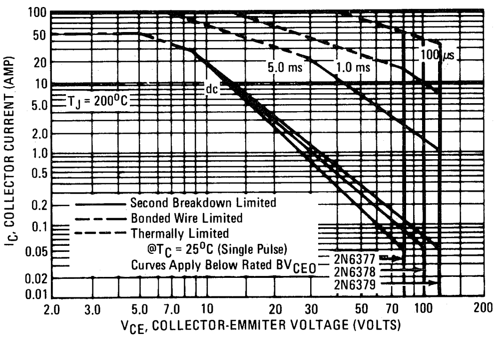


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

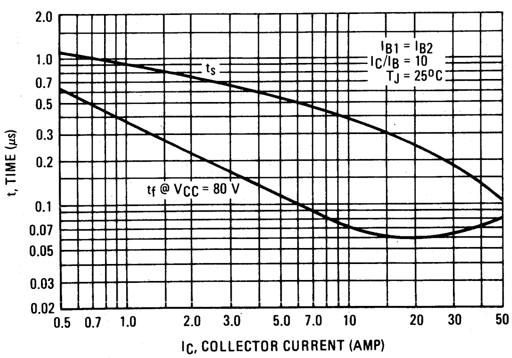


FIGURE 7 – CAPACITANCE

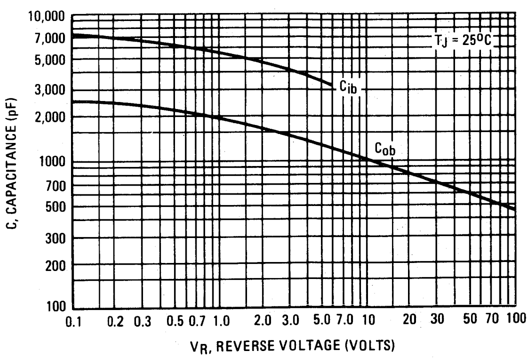


FIGURE 8 – DC CURRENT GAIN

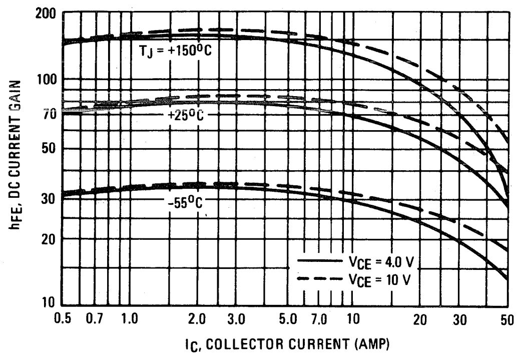


FIGURE 9 – COLLECTOR SATURATION REGION

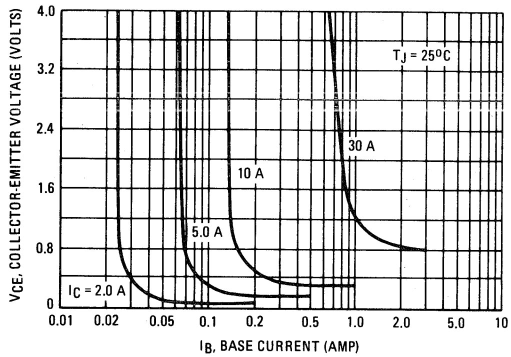


FIGURE 10 – "ON" VOLTAGES

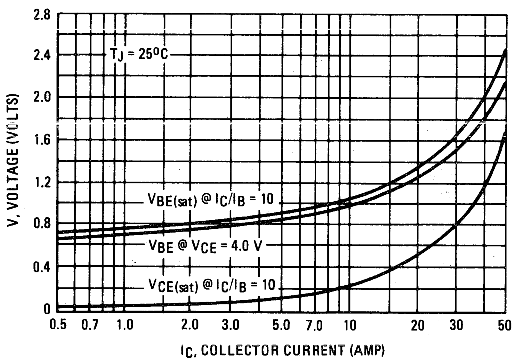
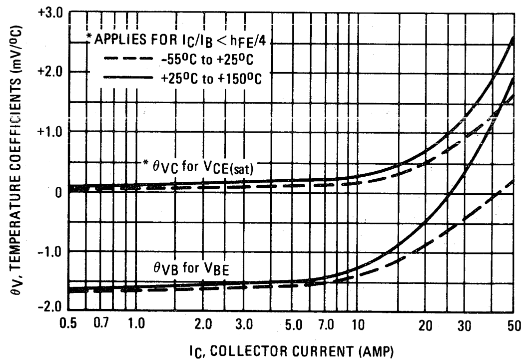


FIGURE 11 – TEMPERATURE COEFFICIENTS



3

FIGURE 12 – COLLECTOR CUT-OFF REGION

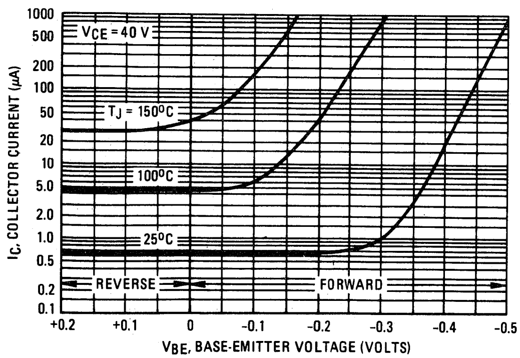
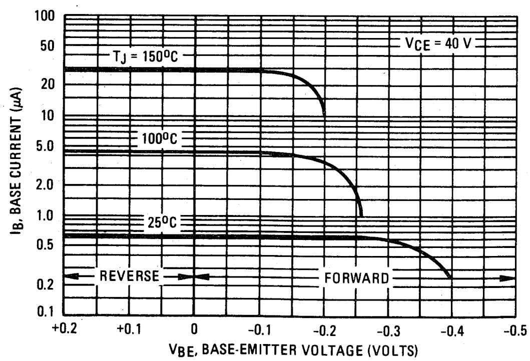


FIGURE 13 – BASE CUTOFF REGION



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

NPN
2N6383, 2N6384
2N6385
PNP
2N6648

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

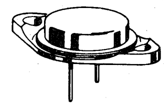
. . . monolithic complementary silicon Darlington transistors designed for low and medium frequency power applications such as power switching, audio amplifiers, hammer drivers, and shunt and series regulators.

- High Gain Darlington Performance
- True Complementary Specifications

15 AMPERE PEAK

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

40–60–80 VOLTS
100 WATTS



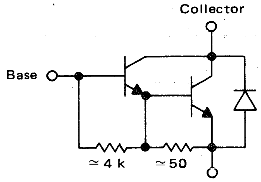
*MAXIMUM RATINGS

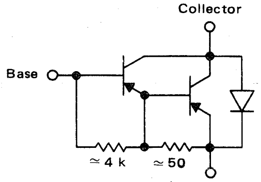
Rating	Symbol	2N6383 2N6648	2N6384	2N6385	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	40	60	80	Vdc
Collector-Emitter Voltage	V_{CEX}	40	60	80	Vdc
Collector-Emitter Voltage	V_{CBO}	40	60	80	Vdc
Emitter Base Voltage	V_{EBO}	← 5.0 →			Vdc
Collector Current — Continuous	I_C	← 10 →			Adc
Peak (1)**	I_{CM}	← 15 →			
Base Current — Continuous	I_B	← 0.25 →			Adc
Total Power Dissipation @ $T_C = 25°C$ (2)	P_D	← 100 →			Watts
Derate above 25°C		← 0.571 →			W/°C
Operating and Storage Junction Temperature Range (2)	T_J, T_{stg}	← −65 to +200 →			°C

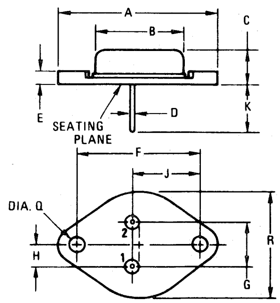
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/32″ from Case for 5 Seconds	T_L	235	°C

*Indicates JEDEC Registered Data.
**Not JEDEC Registered.
(1) Pulse Width = 50 ms, Duty Cycle ≤ 10%.
(2) Exceeds JEDEC Registration for 2N6648.
JEDEC Registration gives $P_D = 70$ W, $T_J = 150°C$.







STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
*Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0) 2N6383, 2N6648	$V_{CEO(sus)}$	40	–	Vdc
2N6384		60	–	
2N6385		80	–	
Collector Cutoff Current (V_{CE} = Rated Value)	I_{CEO}	–	1.0	mAdc
*Collector Cutoff Current (V_{CE} = Rated $V_{CEO(sus)}$ Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	0.3	mAdc
(V_{CE} = Rated $V_{CEO(sus)}$ Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	3.0	
*Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	10	mAdc
Collector-Emitter Sustaining Voltage (1) (R_{BE} = 100 Ω, I_C = 200 mA) 2N6383, 2N6648	$V_{CER(sus)}$	40	–	Vdc
2N6384		60	–	
2N6385		80	–	
Collector-Emitter Sustaining Voltage (1) ($V_{BE(off)}$ = 1.5 V, I_C = 200 mA) 2N6383, 2N6648	$V_{CEV(sus)}$	40	–	Vdc
2N6384		60	–	
2N6385		80	–	
ON CHARACTERISTICS (1)				
*DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	1000	20,000	–
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)		100	–	
*Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.01 Adc)	$V_{CE(sat)}$	–	2.0	Vdc
(I_C = 10 Adc, I_B = 0.1 Adc)		–	3.0	
*Base-Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	$V_{BE(on)}$	–	2.8	Vdc
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)		–	4.5	
Diode Forward Voltage (I_F = 10 Adc)	V_F	–	4.0	Vdc
***DYNAMIC CHARACTERISTICS**				
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)	C_{ob}	–	200	pF
*Magnitude of Common-Emitter Small-Signal Short-Circuit Current Transfer Ratio (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 MHz)	$\|h_{fe}\|$	20	–	–
Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	h_{fe}	1000	–	–
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base-Forward Biased	$I_{S/B}$	See Figures 8 and 9		
Second Breakdown Energy with Base Reverse-Biased (L = 12 mH, R_{BE} = 100 Ω, $V_{BE(off)}$ = 1.5 Vdc, I_C = 4.5 Adc)	$E_{s/b}$	120	–	mJ

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

* Indicates JEDEC Registered Data.

3

FIGURE 1 — DC CURRENT GAIN

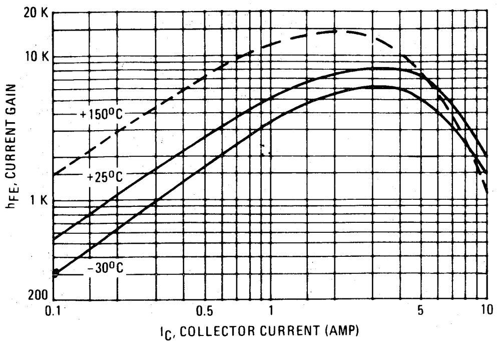


FIGURE 2 — COLLECTOR SATURATION REGION

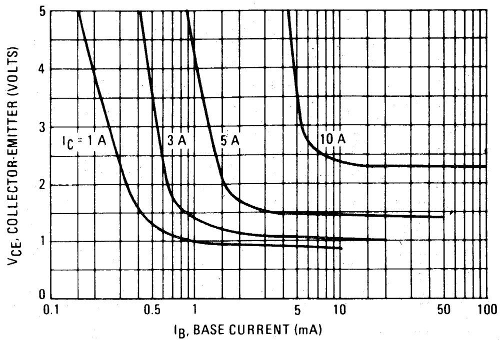


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

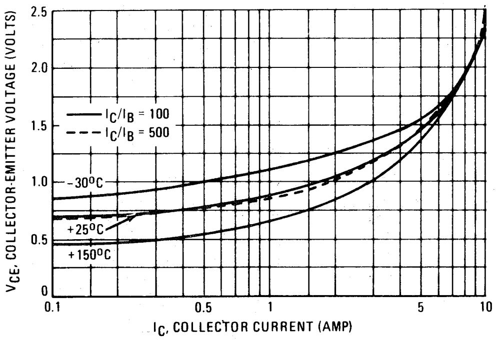


FIGURE 4 — BASE-EMITTER VOLTAGE

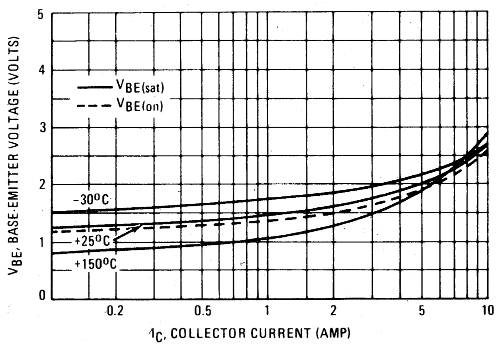


FIGURE 5 — SWITCHING TIME TEST CIRCUIT
(Shown for NPN)

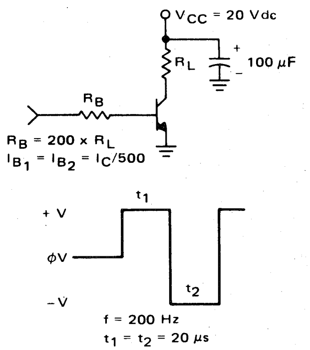
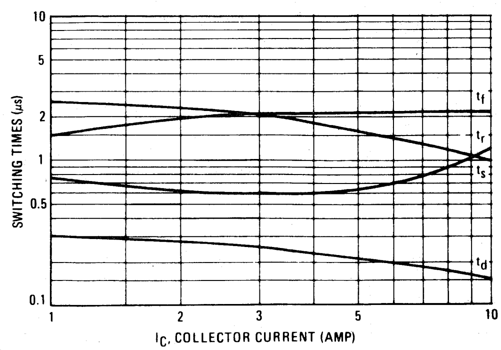
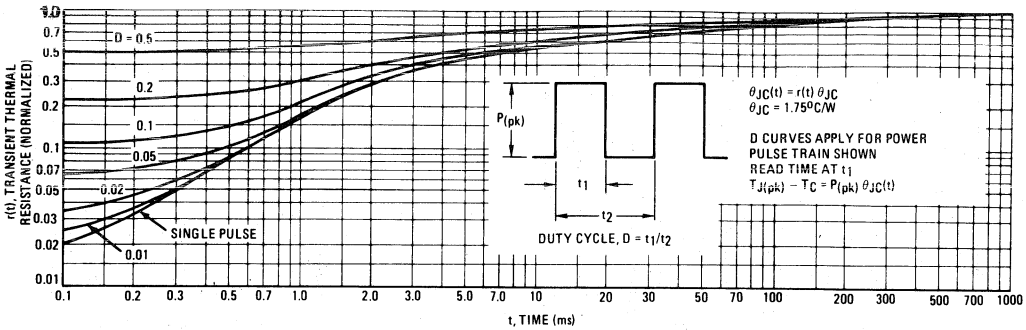


FIGURE 6 — SWITCHING TIMES



3

FIGURE 7 – THERMAL RESPONSE



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 8 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature.

$T_{J(pk)}$ may be calculated from the data in Figure 7. At high case temperatures, see Figure 9, thermal limitations will reduce the current that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do derate the same as thermal limitations. Allowable current at the voltages shown on Figure 8 may be found at any case temperature by derating linearly to 200°C.

FORWARD BIASED SAFE OPERATING AREA

FIGURE 8 – $T_C = 25^{\circ}C$

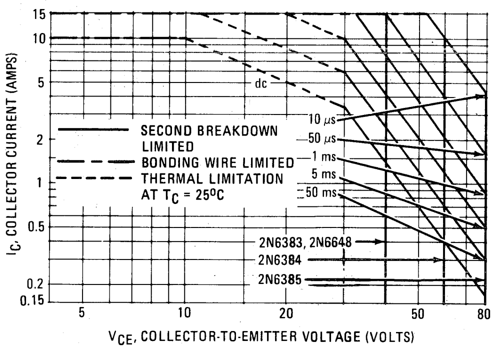


FIGURE 9 – $T_C = 100^{\circ}C$

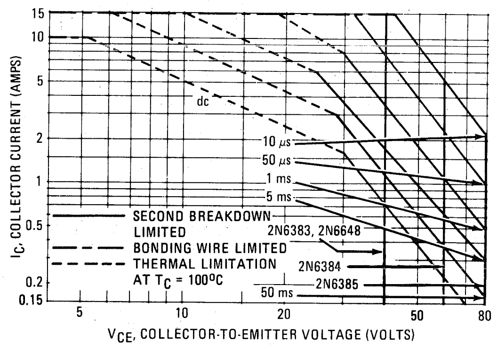
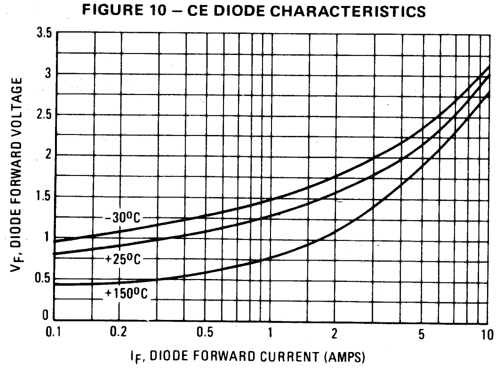


FIGURE 10 – CE DIODE CHARACTERISTICS



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

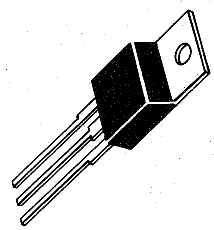
2N6386
2N6387
2N6388

PLASTIC MEDIUM-POWER SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 40 Vdc (Min) — 2N6386
  = 60 Vdc (Min) — 2N6387
  = 80 Vdc (Min) — 2N6388
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc — 2N6386
  = 2.0 Vdc (Max) @ I_C = 5.0 Adc — 2N6387, 2N6388
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON
8 AND 10 AMPERE
NPN SILICON POWER TRANSISTORS
40-60-80 VOLTS
65 WATTS



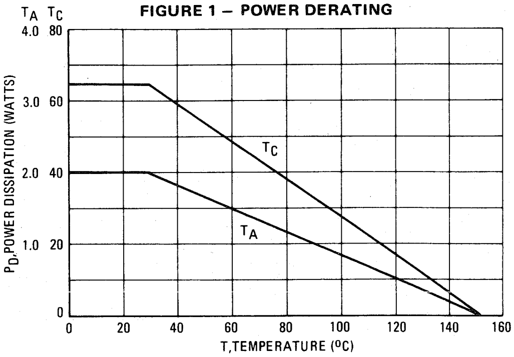
*MAXIMUM RATINGS

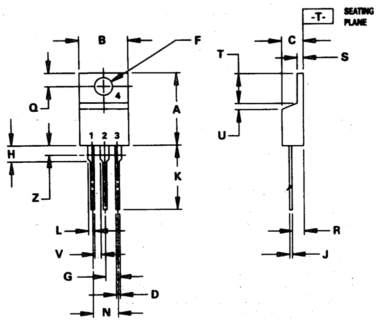
Rating	Symbol	2N6386	2N6387	2N6388	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	8.0 15	10 15	10 15	Adc
Base Current	I_B	← 250 →			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 65 → ← 0.52 →			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 0.016 →			Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	← −65 to +150 →			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6386		40	—	
	2N6387		60	—	
	2N6388		80	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6386		—	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6387		—	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N6388		—	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6386		—	300	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6387		—	300	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6388		—	300	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6386		—	3.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6387		—	3.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6388		—	3.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	2N6386		1000	20000	
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		1000	20000	
(I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)	2N6386		100	—	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		100	—	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 0.006 Adc)	2N6386		—	2.0	
(I_C = 5.0 Adc, I_B = 0.01 Adc)	2N6387, 2N6388		—	2.0	
(I_C = 8.0 Adc, I_B = 0.08 Adc)	2N6386		—	3.0	
(I_C = 10 Adc, I_B = 0.1 Adc)	2N6387, 2N6388		—	3.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	2N6386		—	2.8	
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		—	2.8	
(I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)	2N6386		—	4.5	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		—	4.5	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)		$\|h_{fe}\|$	20	—	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	200	pF
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	1000	—	—

* Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT

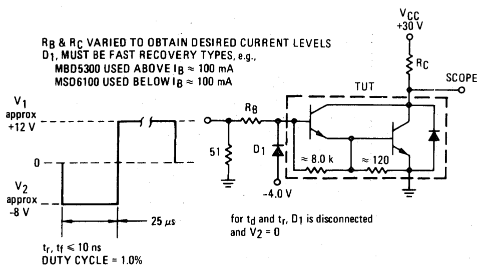


FIGURE 3 — SWITCHING TIMES

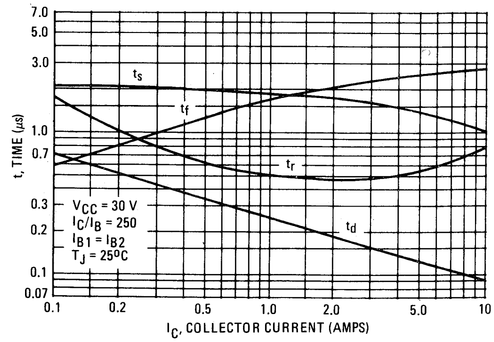


FIGURE 4 — THERMAL RESPONSE

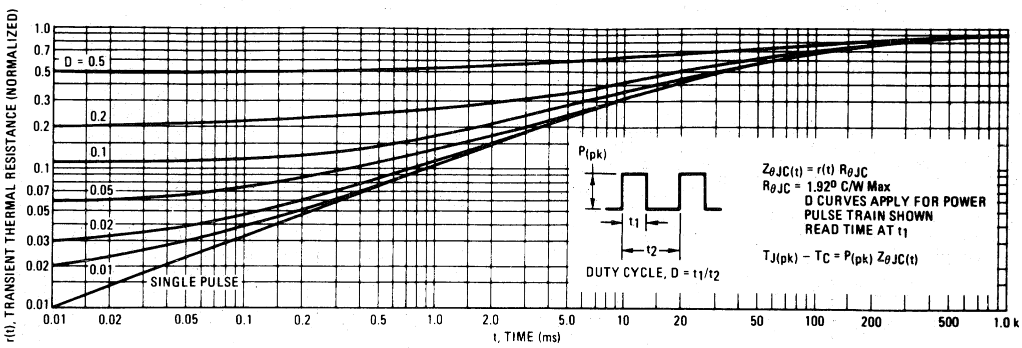
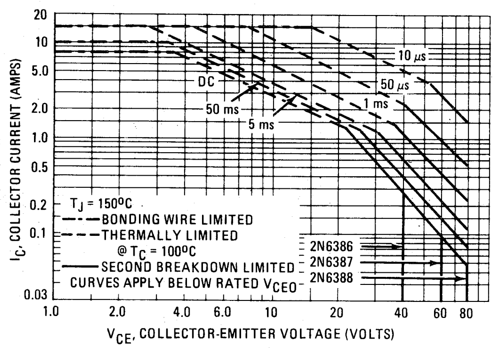


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

3

FIGURE 6 — SMALL-SIGNAL CURRENT GAIN

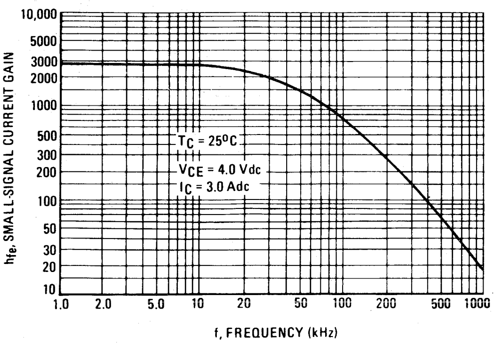


FIGURE 7 — CAPACITANCE

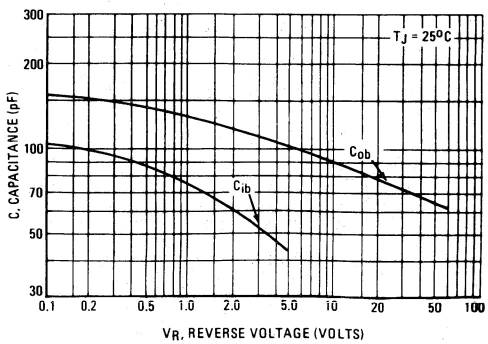


FIGURE 8 — DC CURRENT GAIN

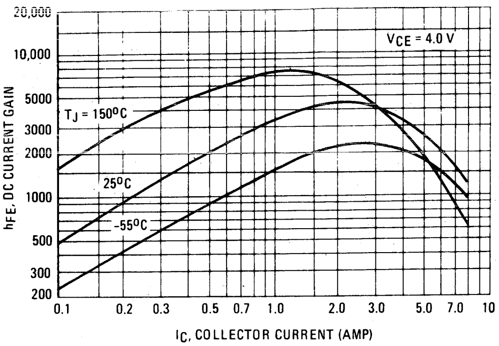


FIGURE 9 — COLLECTOR SATURATION REGION

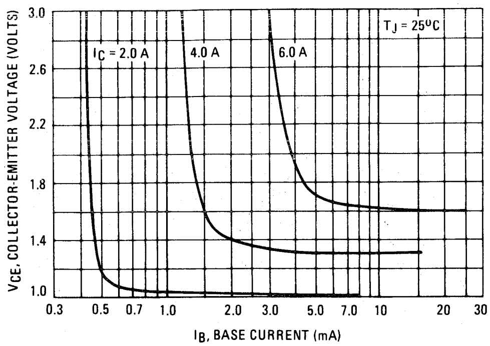


FIGURE 10 — "ON" VOLTAGES

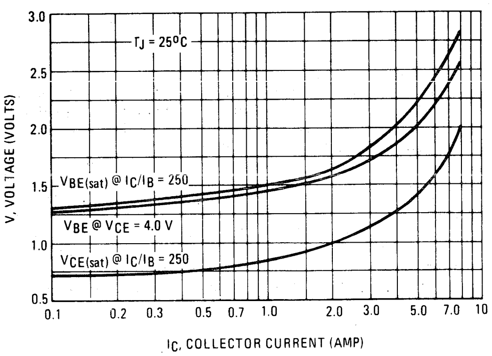
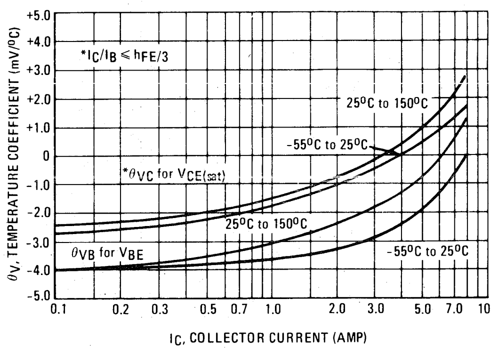


FIGURE 11 — TEMPERATURE COEFFICIENTS



3

FIGURE 12 — COLLECTOR CUT-OFF REGION

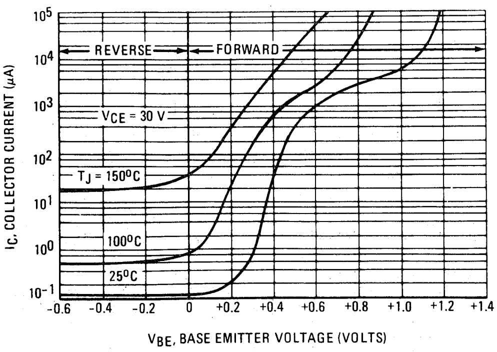
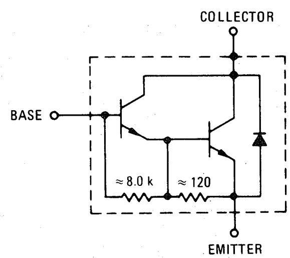


FIGURE 13 — DARLINGTON SCHEMATIC



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6420 thru 2N6422
See Page 3-20

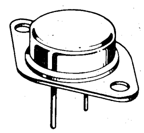
2N6436
2N6437, 2N6438

HIGH-POWER PNP SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — 2N6436
  = 100 Vdc (Min) — 2N6437
  = 120 Vdc (Min) — 2N6438
- High DC Current Gain —
  h_{FE} = 20-80 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 μs (Max)
  t_s = 1.0 μs (Max)
  t_f = 0.25 μs (Max)
- Complement to NPN 2N6338 thru 2N6341

25 AMPERE
POWER TRANSISTORS
PNP SILICON
80, 100, 120 VOLTS
200 WATTS



*MAXIMUM RATINGS

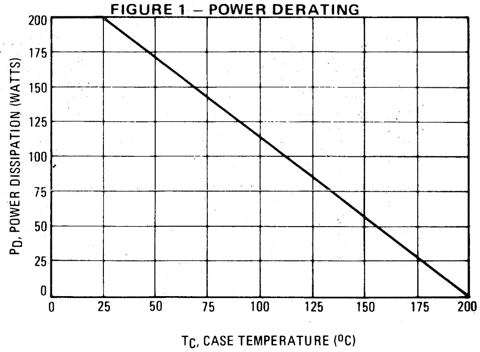
Rating	Symbol	2N6436	2N6437	2N6438	Unit
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Collector-Emitter Voltage	V_{CEO}	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 25 → ← 50 →			Adc
Base Current	I_B	← 10 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 200 → ← 1.14 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

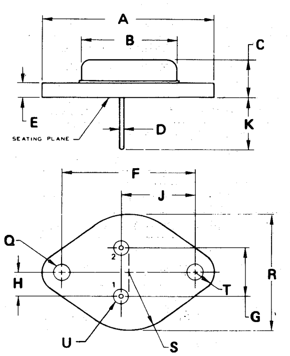
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120

CASE 1—04

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

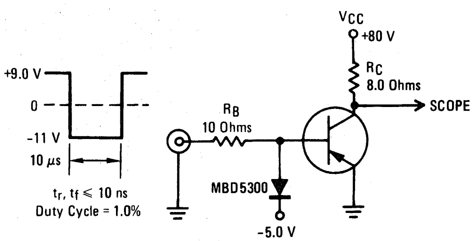
3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6436		80	–	
	2N6437		100	–	
	2N6438		120	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6436		–	50	
(V_{CE} = 50 Vdc, I_B = 0)	2N6437		–	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6438		–	50	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = −1.5 Vdc)	2N6436		–	10	
(V_{CE} = 110 Vdc, $V_{BE(off)}$ = −1.5 Vdc)	2N6437		–	10	
(V_{CE} = 130 Vdc, $V_{BE(off)}$ = −1.5 Vdc)	2N6438		–	10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = −1.5 Vdc, T_C = 150°C)	2N6436		–	1.0	mAdc
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = −1.5 Vdc, T_C = 150°C)	2N6437		–	1.0	
(V_{CE} = 120 Vdc, $V_{BE(off)}$ = −1.5 Vdc, T_C = 150°C)	2N6438		–	1.0	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 100 Vdc, I_E = 0)	2N6436		–	10	
(V_{CB} = 120 Vdc, I_E = 0)	2N6437		–	10	
(V_{CB} = 140 Vdc, I_E = 0)	2N6438		–	10	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			30	–	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)			20	120	
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)			12	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			–	1.0	
(I_C = 25 Adc, I_B = 2.5 Adc)			–	1.8	
Base-Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			–	1.8	
(I_C = 25 Adc, I_B = 2.5 Adc)			–	2.5	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	–	MHz
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	700	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = 1.0 Adc)		t_r	–	0.3	μs
Storage (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = I_{B2} = 1.0 Adc)		t_s	–	1.0	μs
Fall Time (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = I_{B2} = 1.0 Adc)		t_f	–	0.25	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ⩽300 μs; Duty Cycle ⩽2.0%.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 — TURN-ON TIME

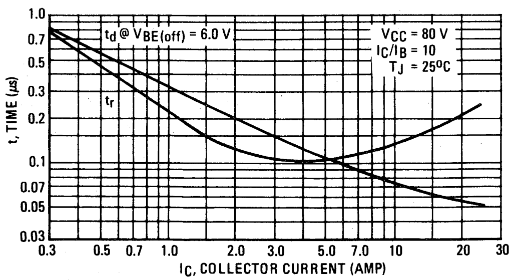


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FIGURE 4 – THERMAL RESPONSE

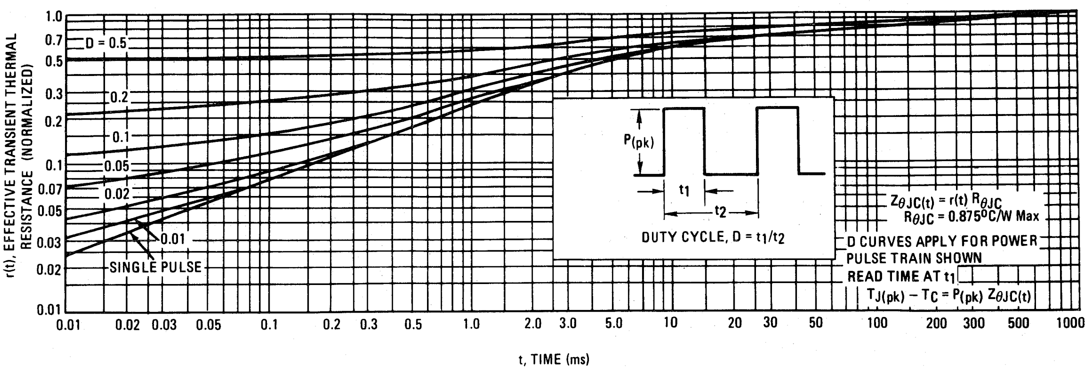
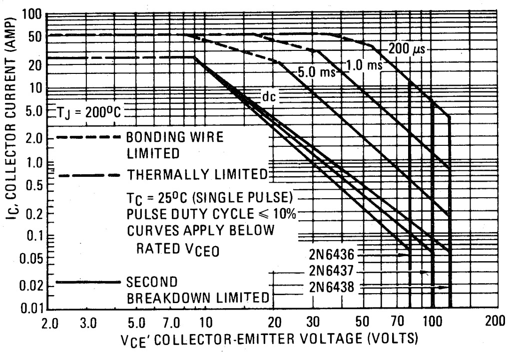


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

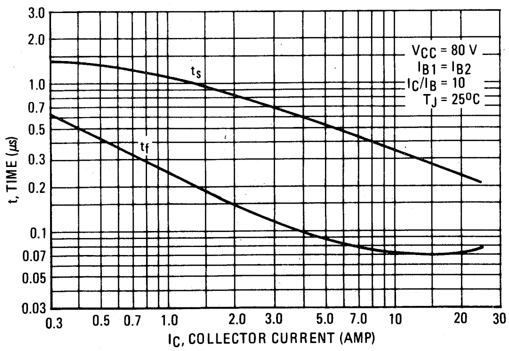
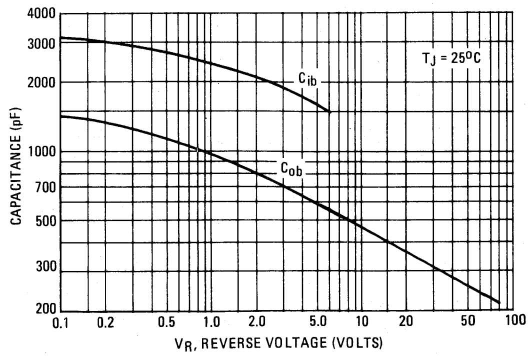


FIGURE 7 – CAPACITANCE



3

FIGURE 8 – DC CURRENT GAIN

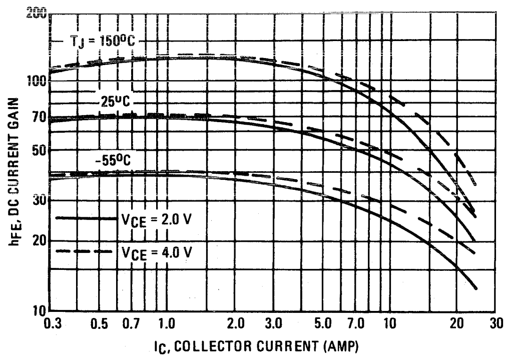


FIGURE 9 – COLLECTOR SATURATION REGION

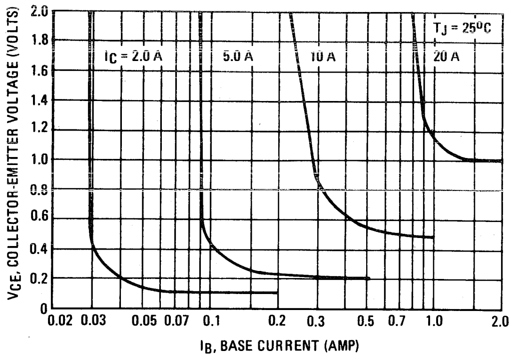


FIGURE 10 – "ON" VOLTAGE

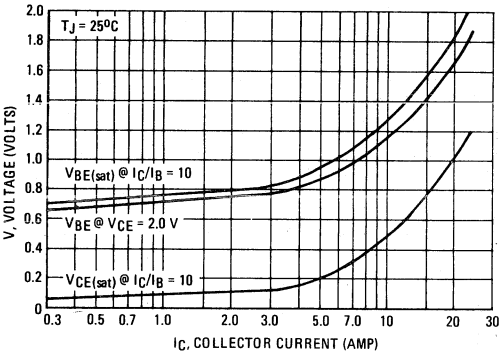


FIGURE 11 – TEMPERATURE COEFFICIENTS

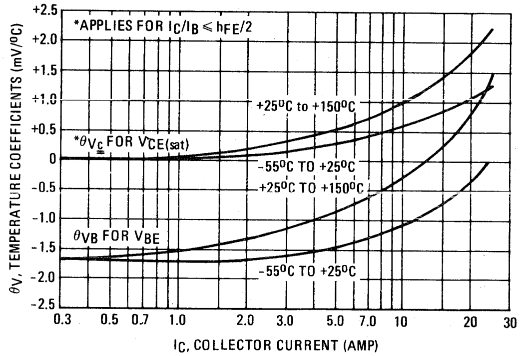


FIGURE 12 – COLLECTOR CUT-OFF REGION

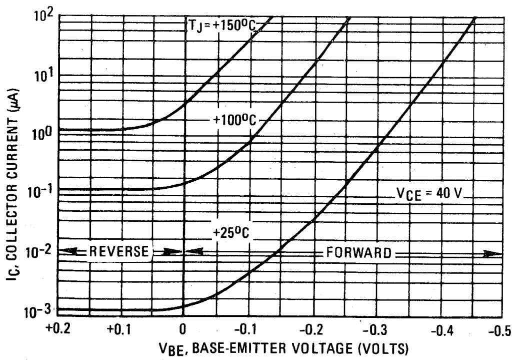
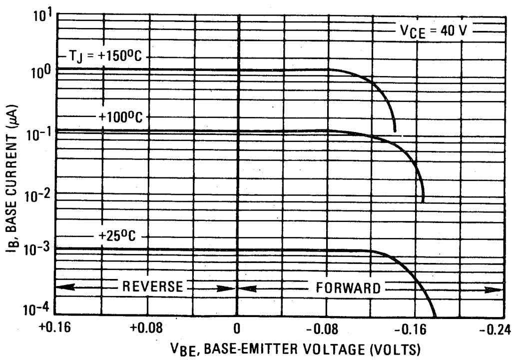


FIGURE 13 – BASE CUT-OFF REGION



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
2N6486	2N6489
2N6487	2N6490
2N6488	2N6491

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

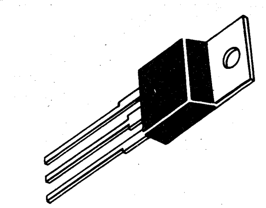
. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 15 Amperes
  h_{FE} = 20–150 @ I_C = 5.0 Adc
  = 5.0 (Min) @ I_C = 15 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO\,(sus)}$ = 40 Vdc (Min) — 2N6486, 2N6489
  = 60 Vdc (Min) — 2N6487, 2N6490
  = 80 Vdc (Min) — 2N6488, 2N6491
- High Current Gain — Bandwidth Product
  f_T = 5.0 MHz (Min) @ I_C = 1.0 Adc
- TO-220AB Compact Package
- TO-66 Leadform Also Available

15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40-60-80 VOLTS
75 WATTS



*MAXIMUM RATINGS

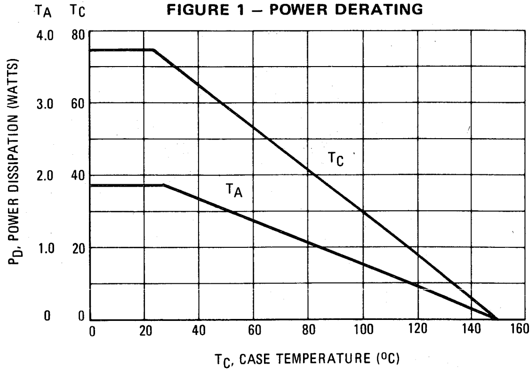
Rating	Symbol	2N6486 2N6489	2N6487 2N6490	2N6488 2N6491	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	50	70	90	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous	I_C		15		Adc
Base Current	I_B		5.0		Adc
Total Power Dissipation @ $T_C = 25°C$	P_D		75		Watts
Derate above 25°C			0.6		W/°C
Total Power Dissipation @ $T_A = 25°C$	P_D		1.8		Watts
Derate above 25°C			0.014		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +150		°C

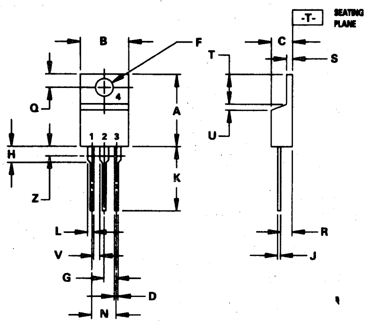
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

2N6486 2N6487 2N6488 NPN
2N6489 2N6490 2N6491 PNP

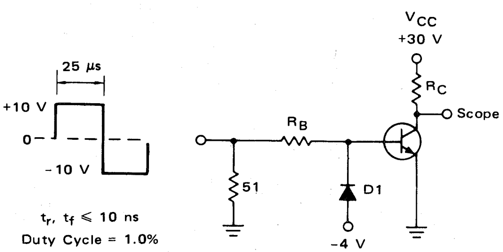
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N6486, 2N6489	$V_{CEO(sus)}$	40	–	Vdc
	2N6487, 2N6490		60	–	
	2N6488, 2N6491		80	–	
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, V_{BE} = 1.5 Vdc)	2N6486, 2N6489	V_{CEX}	50	–	Vdc
	2N6487, 2N6490		70	–	
	2N6488, 2N6491		90	–	
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	2N6486, 2N6489	I_{CEO}	–	1.0	mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N6487, 2N6490		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6488, 2N6491		–	1.0	
Collector Cutoff Current (V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6486, 2N6489	I_{CEX}	–	500	μAdc
(V_{CE} = 65 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6487, 2N6490		–	500	
(V_{CE} = 85 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6488, 2N6491		–	500	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6486, 2N6489		–	5.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6487, 2N6490		–	5.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6488, 2N6491		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	20	150	–
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	–	1.3	Vdc
(I_C = 15 Adc, I_B = 5.0 Adc)			–	3.5	
Base-Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.3	Vdc
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			–	3.5	
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)		f_T	5.0	–	MHz
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

*Indicates JEDEC Registered Data.
(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2)$f_T = |h_{fe}| \bullet f_{test}$.

3

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C varied to obtain desired current levels.
For PNP reverse all polarities.

D1 must be fast recovery type, e.g.;
MBD5300 used above $I_B \approx$ 100 mA
MSD6100 used below $I_B \approx$ 100 mA

FIGURE 3 – TURN-ON TIME

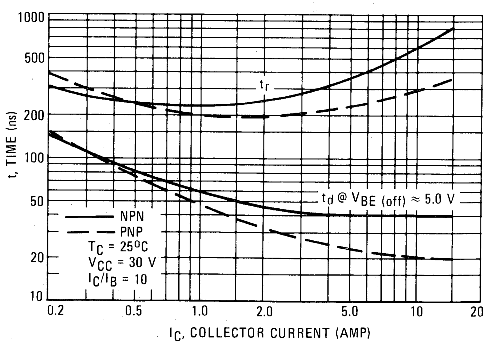


FIGURE 4 — THERMAL RESPONSE

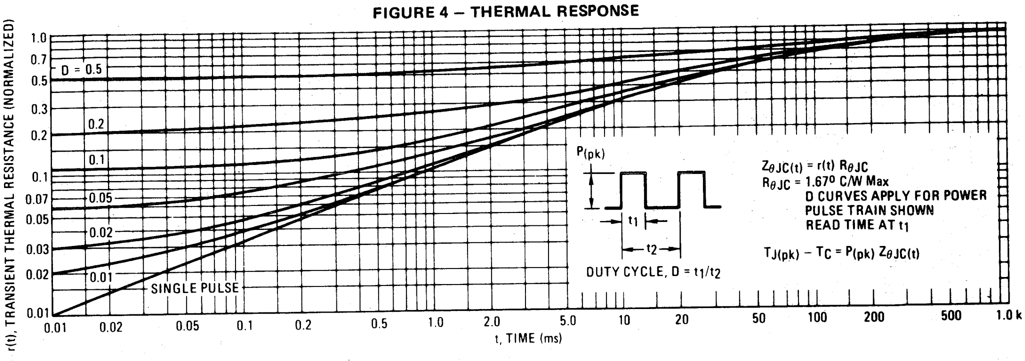
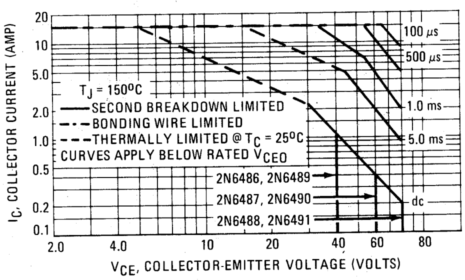


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

3

FIGURE 6 — TURN-OFF TIME

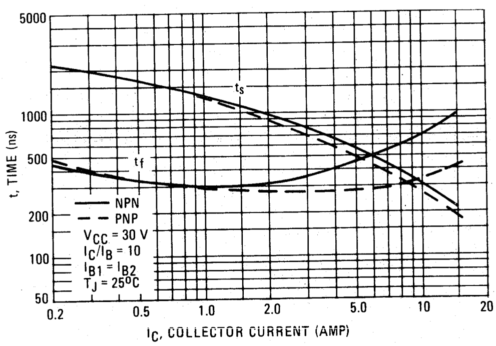
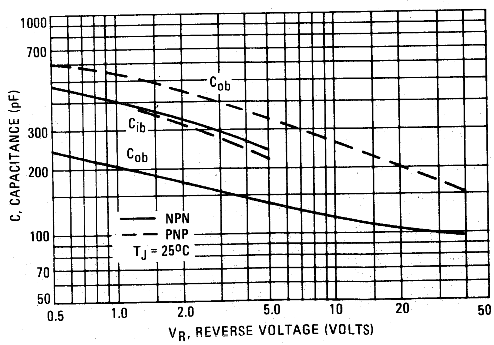


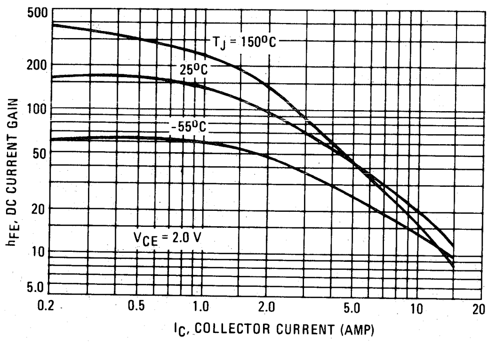
FIGURE 7 — CAPACITANCES



NPN
2N6486, 2N6487, 2N6488

PNP
2N6489, 2N6490, 2N6491

FIGURE 8 – DC CURRENT GAIN



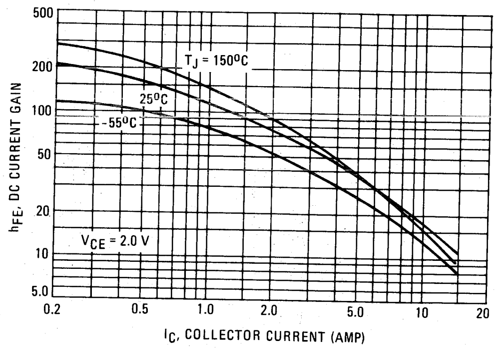
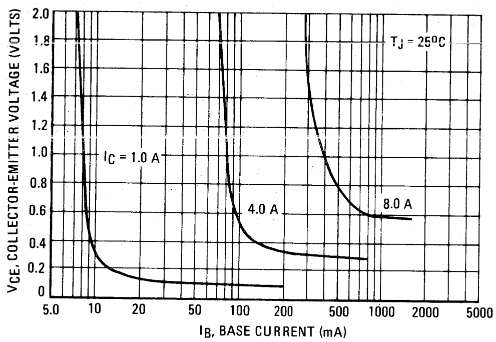


FIGURE 9 – COLLECTOR SATURATION REGION



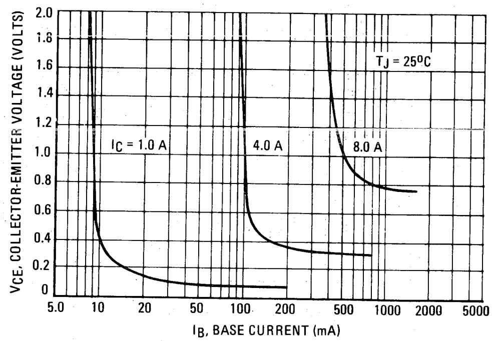
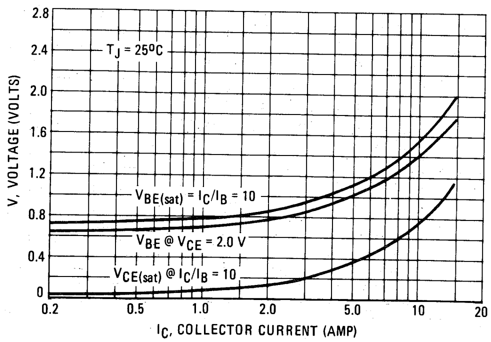
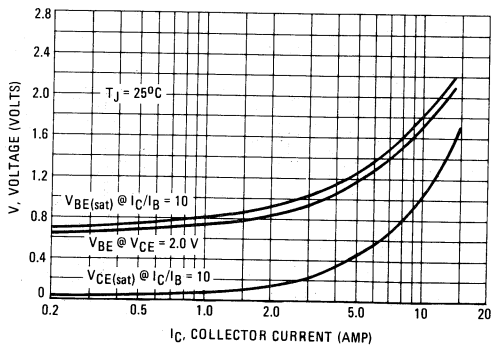


FIGURE 10 – "ON" VOLTAGES





3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

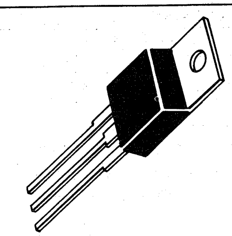
2N6497
2N6498

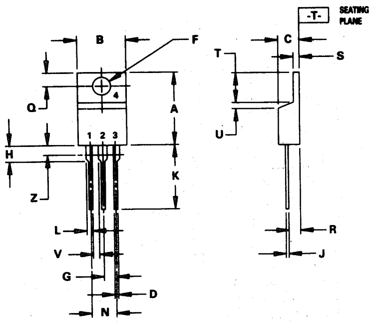
5 AMPERE
POWER TRANSISTORS
NPN SILICON
250 & 300 VOLTS
80 WATTS

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

. . . designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 250 Vdc (Min) — 2N6497
  = 300 Vdc (Min) — 2N6498
- Excellent DC Current Gain —
  h_{FE} = 10 — 75 @ I_C = 2.5 Adc
- Low Collector-Emitter Saturation Voltage @ I_C = 2.5 Adc —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) — 2N6497
  = 1.25 Vdc (Max) — 2N6498





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

*MAXIMUM RATINGS

Rating	Symbol	2N6497	2N6498	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	Vdc
Collector-Base Voltage	V_{CB}	350	400	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →		Vdc
Collector Current — Continuous — Peak	I_C	← 5.0 → ← 10 →		Adc
Base Current	I_B	← 2.0 →		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 80 → ← 0.64 →		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W

*Indicates JEDEC Registered Data.

3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 25 mAdc, I_B = 0) 2N6497	$V_{CEO(sus)}$	250	–	–	Vdc
2N6498		300	–	–	
Collector Cutoff Current (V_{CE} = 350 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N6497	I_{CEX}	–	–	1.0	mAdc
(V_{CE} = 400 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N6498		–	–	1.0	
(V_{CE} = 175 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C) 2N6497		–	–	10	
(V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C) 2N6498		–	–	10	
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 10 Vdc)	h_{FE}	10	–	75	–
(I_C = 5.0 Adc, V_{CE} = 10 Vdc)		3.0	–	–	
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 500 mAdc) 2N6497	$V_{CE(sat)}$	–	–	1.0	Vdc
2N6498		–	–	1.25	
(I_C = 5.0 Adc, I_B = 2.0 Adc) All Devices		–	–	5.0	
Base-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 500 mAdc)	$V_{BE(sat)}$	–	–	1.5	Vdc
(I_C = 5.0 Adc, I_B = 2.0 Adc)		–	–	2.5	
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	5.0	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	–	150	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = 0.5 Adc)	t_r	–	0.4	1.0	μs
Storage Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, V_{BE} = 5.0 Vdc, I_{B1} = I_{B2} = 0.5 Adc)	t_s	–	1.4	2.5	μs
Fall Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	t_f	–	0.45	1.0	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT

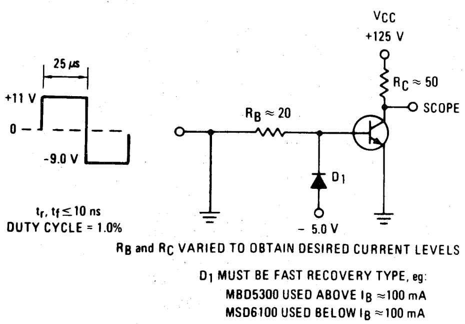


FIGURE 2 — TURN-ON TIME

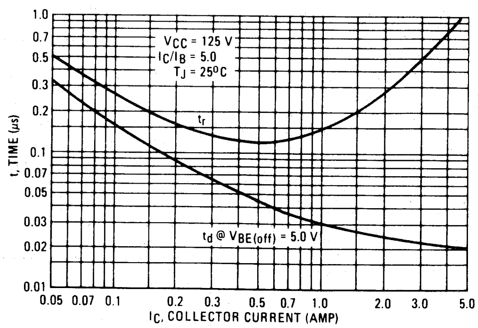


FIGURE 3 – THERMAL RESPONSE

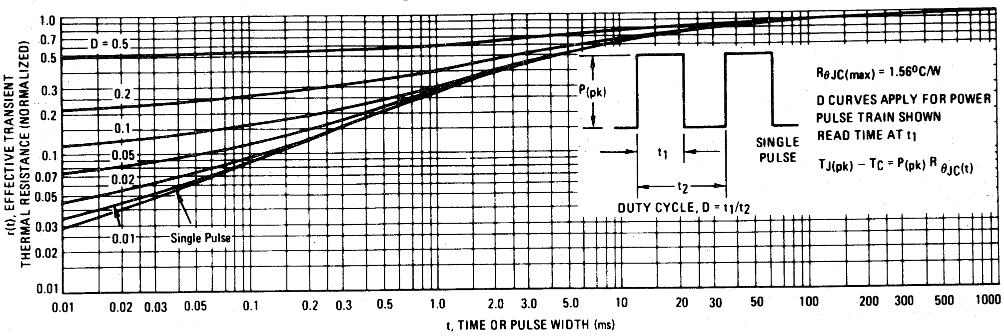
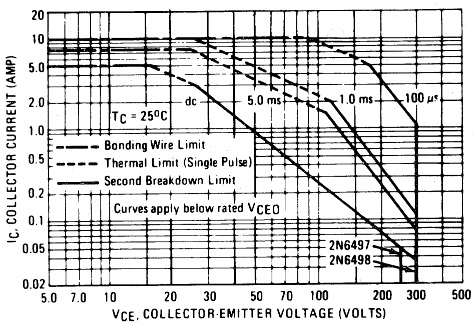


FIGURE 4 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 4 may be found at any case temperature by using the appropriate curve on Figure 6.

FIGURE 5 – TURN-OFF TIME

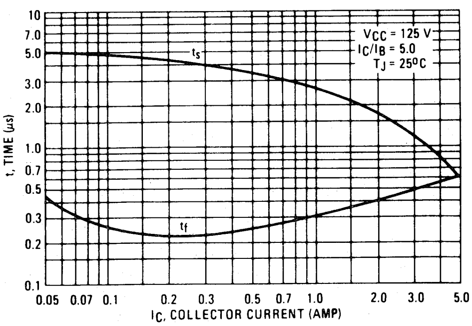


FIGURE 6 – POWER DERATING

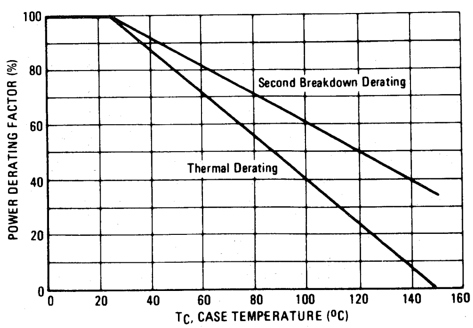


FIGURE 7 — DC CURRENT GAIN

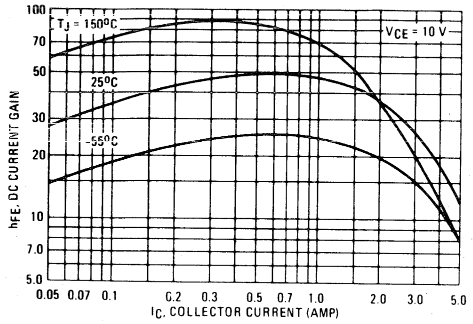


FIGURE 8 — COLLECTOR SATURATION REGION

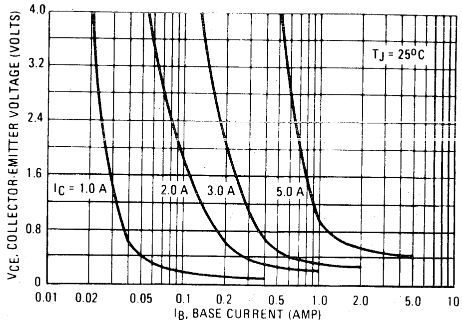


FIGURE 9 — "ON" VOLTAGES

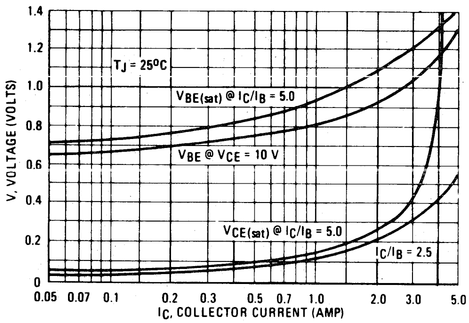
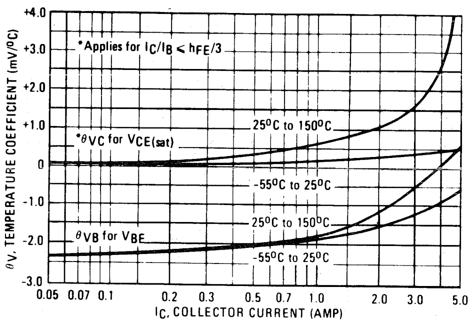


FIGURE 10 — TEMPERATURE COEFFICIENTS



3

FIGURE 11 — COLLECTOR CUTOFF REGION

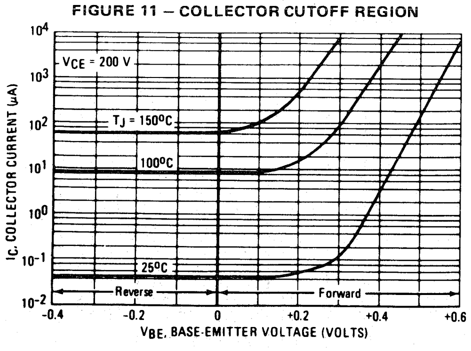
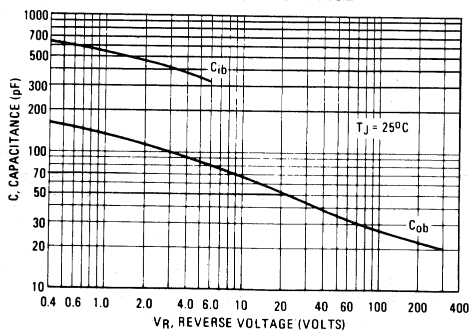


FIGURE 12 — CAPACITANCE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6543

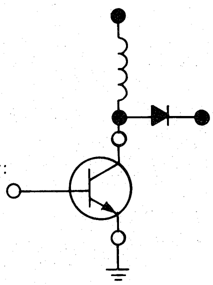
Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

This device is designed for high-voltage, high-speed, power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 200 volt line operated SWITCHMODE applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features —
- High Temperature Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



5 AMPERE
NPN SILICON
POWER TRANSISTOR
400 VOLTS
100 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

*MAXIMUM RATINGS

Rating	Symbol	2N6543	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 10	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	5.0 10	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	10 20	Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	100 57.2 0.57	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

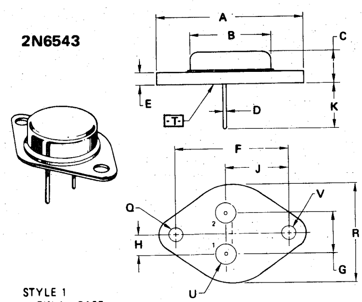
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

2N6543



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [-T-] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	ϕ.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	ϕ.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	400	–	Vdc
Collector-Emitter Sustaining Voltage (Table 2, Figure 12) (I_C = 2.6 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	$V_{CEX(sus)}$	450	–	Vdc
(I_C = 5.0 Adc, V_{clamp} = Rated V_{CEO} -100 V, T_C = 100°C)		300	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	0.5	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	3.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)	$I_{S/b}$	0.2 (See Figure 11)	–	Adc
Clamped Inductive SOA with base reverse biased	RBSOA	(See Figure 12)		
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	12	60	–
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)		7.0	35	
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)	$V_{CE(sat)}$	–	1.0	Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)		–	5.0	
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		–	2.0	
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)	$V_{BE(sat)}$	–	1.4	Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		–	1.4	
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	6.0	28	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)	C_{ob}	50	200	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 2)	Conditions	Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 250 Vdc, I_C = 3.0 A, I_{B1} = I_{B2} = 0.6 A, t_p = 100 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.05	μs
Rise Time		t_r	–	0.7	μs
Storage Time		t_s	–	4.0	μs
Fall Time		t_f	–	0.8	μs
Inductive Load, Clamped (Table 2)		**Symbol**	**Typ**	**Max**	**Unit**
Storage Time	(I_C = 3.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 0.6 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_{sv}	–	4.0	μs
Crossover Time		t_c	0.6	–	μs
Fall Time		t_{fi}	–	0.8	μs
Storage Time	(I_C = 3.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 0.6 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_{sv}	0.8	–	μs
Crossover Time		t_c	0.3	–	μs
Fall Time		t_{fi}	0.2	–	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

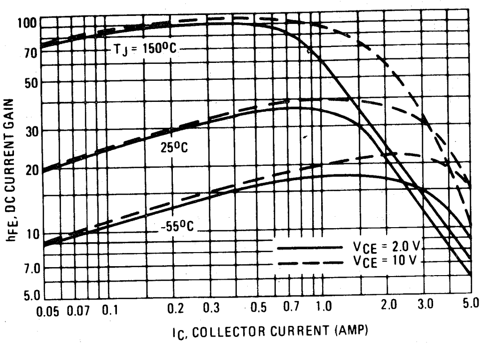


FIGURE 2 – COLLECTOR SATURATION REGION

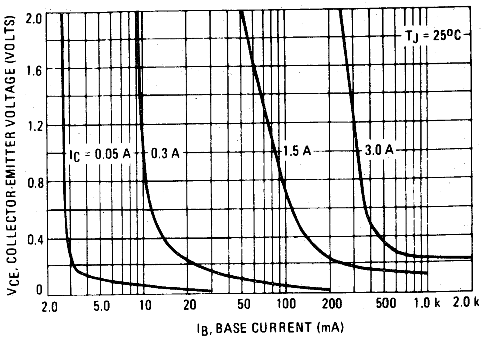


FIGURE 3 – "ON" VOLTAGE

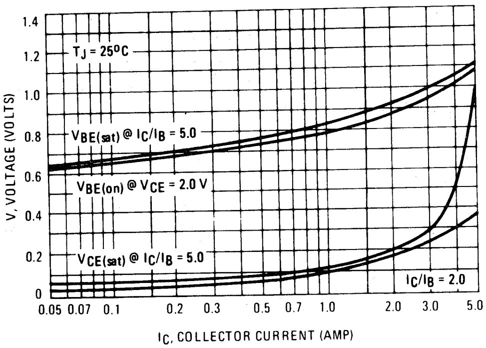


FIGURE 4 – TEMPERATURE COEFFICIENTS

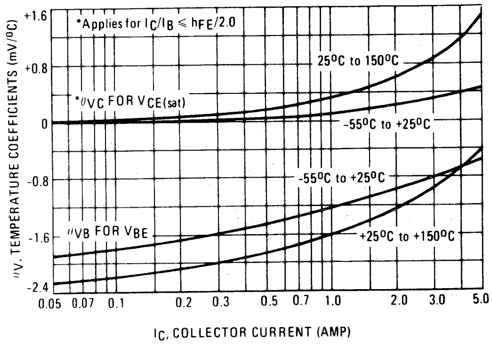


FIGURE 5 – COLLECTOR CUTOFF REGION

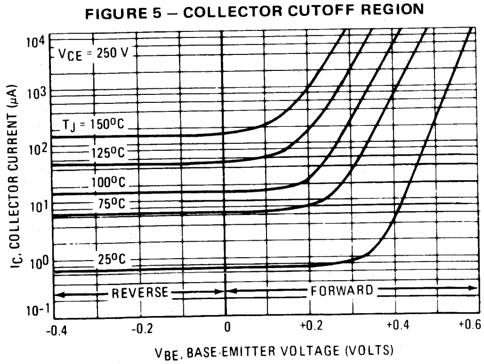
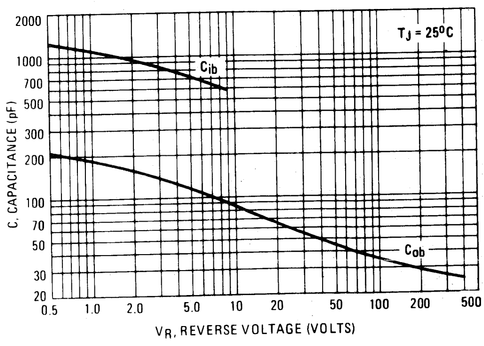


FIGURE 6 – CAPACITANCE



3

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

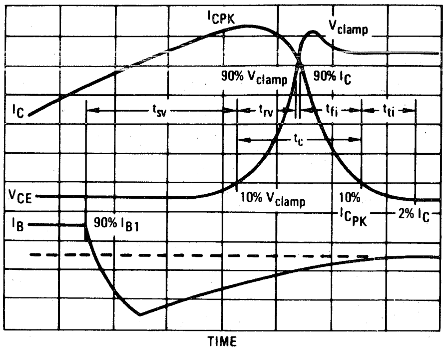


TABLE 1 — INDUCTIVE SWITCHING PERFORMANCE

I_C (A)	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
1.0	25	0.70	0.22	0.21	0.23	0.66
	100	1.20	0.37	0.19	0.39	0.95
3.0	25	1.10	0.09	0.12	0.08	0.29
	100	1.60	0.42	0.19	0.40	1.01
5.0	25	1.10	0.16	0.19	0.11	0.46
	100	1.70	0.45	0.37	0.26	1.08

Note: All Data Recorded in the Inductive Switching Circuit Shown in Table 2.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

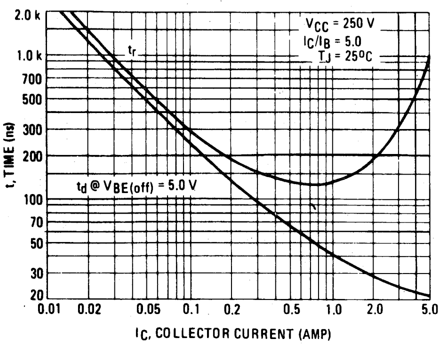


FIGURE 9 — TURN-OFF TIME

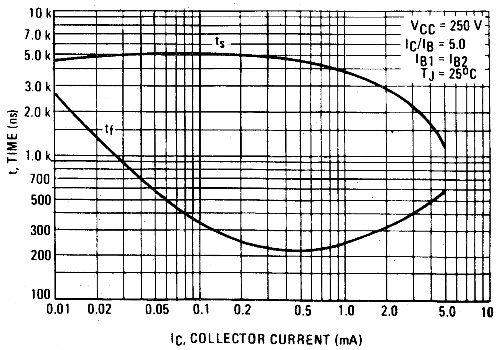


TABLE 2 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

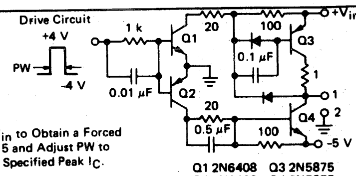
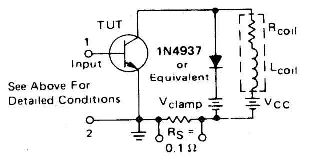
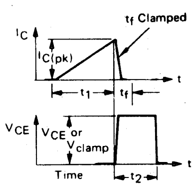
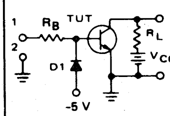
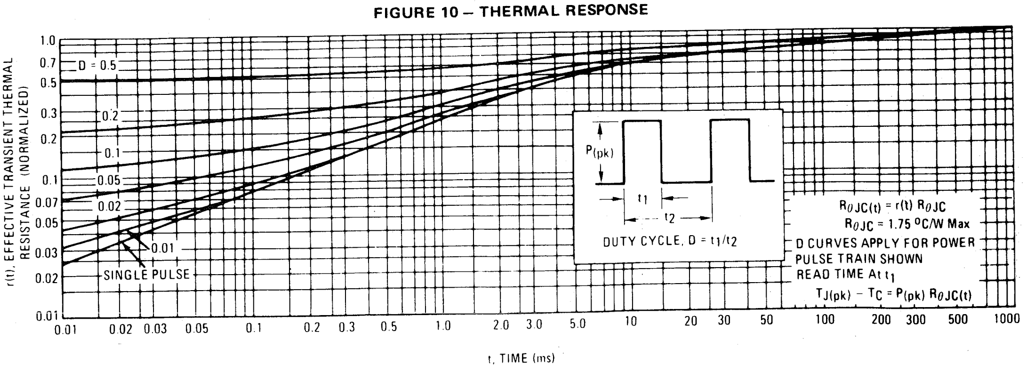
	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V; 20 Ω; 1; 0; 2 PW Varied to Attain I_C = 100 mA	Drive Circuit  Set $+V_{in}$ to Obtain a Forced h_{FE} = 5 and Adjust PW to Attain Specified Peak I_C. Duty Cycle ≤ 3% f = 1 kHz Q1 2N6408 Q3 2N5875 Q2 2N6406 Q4 2N5877 Diodes 1N4933	≈ +13 V; 1; 0; ≈ −11 V; 2 I_C = 3A PW ≈ 100 μs t_r ≤ 5 ns t_f ≤ 50 ns Duty Cycle ≤ 2%
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} (Unclamped)	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 83 Ω D1 = 1N5820 or Equiv. R_B = 20 Ω
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above For Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope-Tektronics 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 10 – THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATING AREA

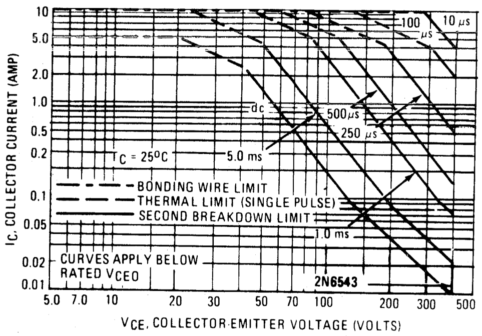


FIGURE 12 — REVERSE BIAS SAFE OPERATING AREA

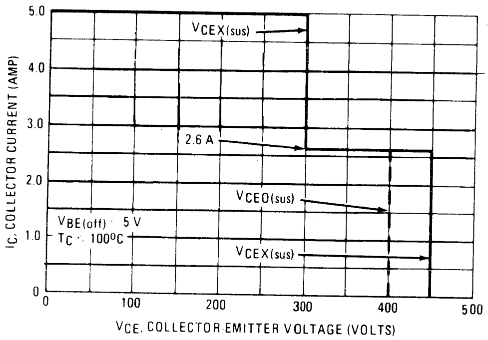
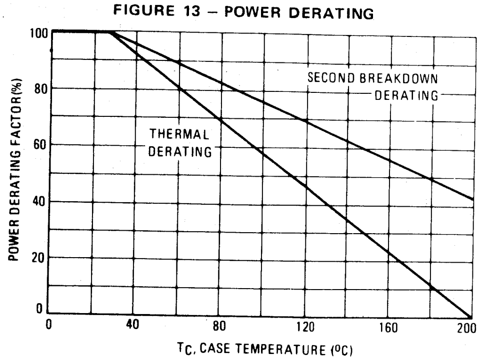


FIGURE 13 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6545

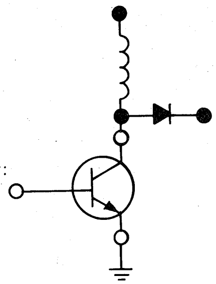
Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTOR

The 2N6545 transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features —
- High Temperature Performance Specified for:
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



8 AMPERE
NPN SILICON
POWER TRANSISTOR

400 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

*MAXIMUM RATINGS

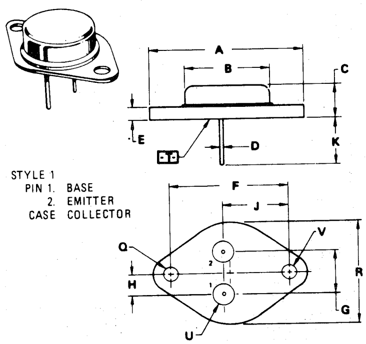
Rating	Symbol	2N6545	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	9.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8.0 16	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	8.0 16	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	16 32	Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	125 71.5 0.714	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   [⌖ | Ø.13 (0.005) Ⓜ | T | V Ⓜ]
   FOR LEADS:
   [⌖ | Ø.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ]
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
Collector-Emitter Sustaining Voltage (I_C = 100 mA, I_B = 0) 2N6545	$V_{CEO(sus)}$	400	–	Vdc
Collector-Emitter Sustaining Voltage (I_C = 4.5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	$V_{CEX(sus)}$	450	–	Vdc
(I_C = 8.0 A, V_{clamp} = Rated V_{CEO} −100 V, T_C = 100°C)		300	–	
Collector Cutoff Current	I_{CEV}			mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	0.5	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)	$I_{S/b}$	0.2	–	Adc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
(I_C = 2.5 Adc, V_{CE} = 3.0 Vdc)		12	60	
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		7.0	35	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)		–	1.5	
(I_C = 8.0 Adc, I_B = 2.0 Adc)		–	5.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		–	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)		–	1.6	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		–	1.6	
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 300 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	6.0	28	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)	C_{ob}	75	300	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Resistive Load					
Delay Time	(V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = I_{B2} = 1.0 A, t_p = 100 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.05	μs
Rise Time		t_r	–	1.0	μs
Storage Time		t_s	–	4.0	μs
Fall Time		t_f	–	1.0	μs
Inductive Load, Clamped					
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_s	–	4.0	μs
Fall Time		t_f	–	0.9	μs
			Typical		
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_s	1.2		μs
Fall Time		t_f	0.18		μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

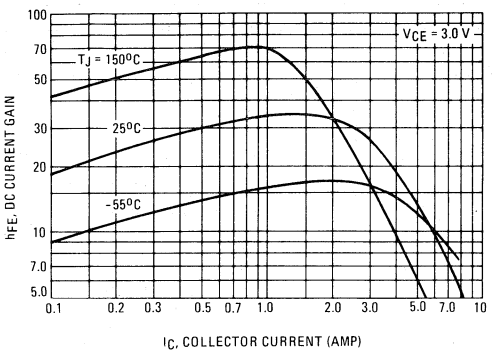


FIGURE 2 – COLLECTOR SATURATION REGION

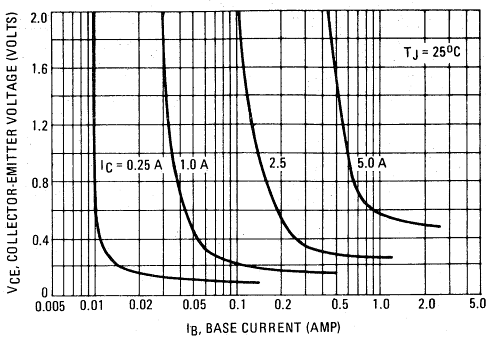


FIGURE 3 – "ON" VOLTAGE

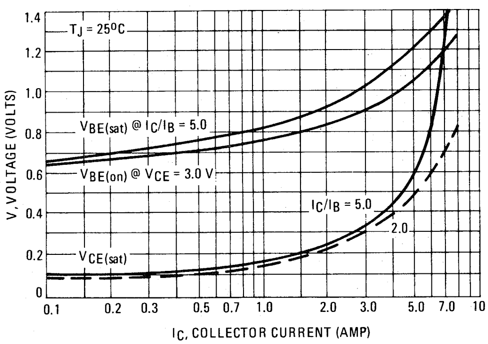


FIGURE 4 – TEMPERATURE COEFFICIENTS

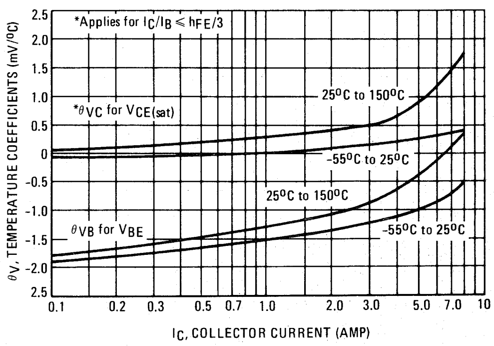


FIGURE 5 – TURN-ON TIME

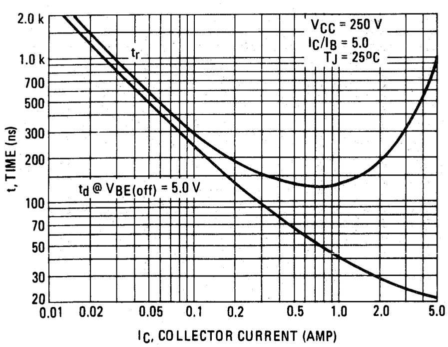
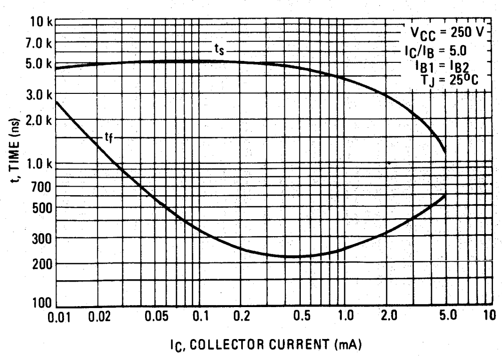


FIGURE 6 – TURN-OFF TIME



3

FIGURE 7 – FORWARD BIAS SAFE OPERATING AREA

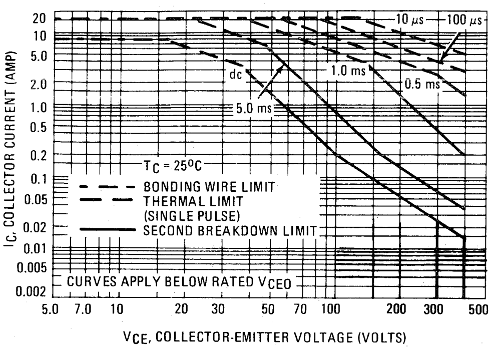


FIGURE 8 – REVERSE BIAS SAFE OPERATING AREA

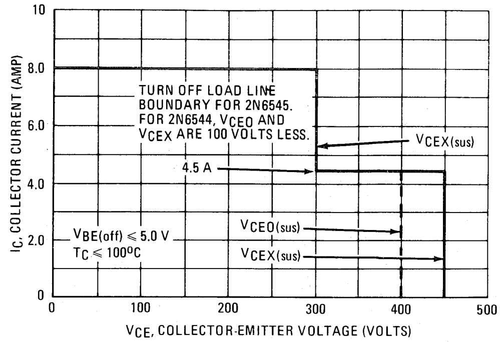
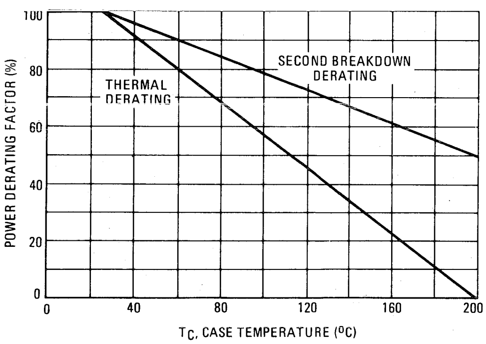


FIGURE 9 – POWER DERATING

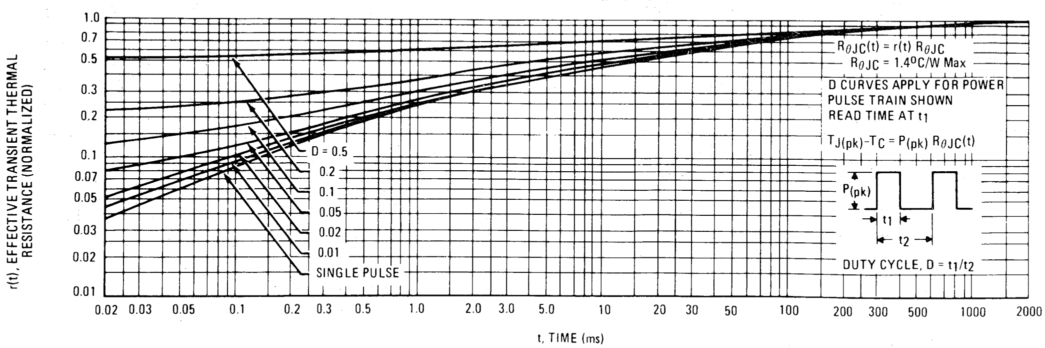


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. The reverse biased safe operating area (Figure 8) is the boundary the load line may traverse during turn-off.

FIGURE 10 – THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6546
2N6547

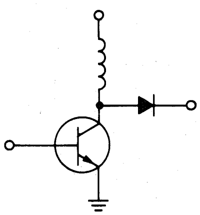
Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The 2N6546 and 2N6547 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features —
High Temperature Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



15 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

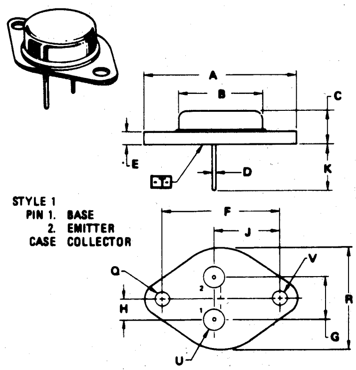
*MAXIMUM RATINGS

Rating	Symbol	2N6546	2N6547	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	350	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	850	Vdc
Emitter Base Voltage	V_{EB}	9.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 30		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 20		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	25 50		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	175 100 1.0		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [-T-] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 100 mA, I_B = 0)	2N6546	$V_{CEO(sus)}$	300	–	Vdc
	2N6547		400	–	
Collector-Emitter Sustaining Voltage (I_C = 8.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	2N6546	$V_{CEX(sus)}$	350	–	Vdc
	2N6547		450	–	
(I_C = 15 A, V_{clamp} = Rated V_{CEO} – 100 V, T_C = 100°C)	2N6546		200	–	
	2N6547		300	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	1.0	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	4.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)		$I_{S/b}$	0.2	–	Adc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	12	60	–
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)			6.0	30	
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc)		$V_{CE(sat)}$	–	1.5	Vdc
(I_C = 15 Adc, I_B = 3.0 Adc)			–	5.0	
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)			–	2.5	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc)		$V_{BE(sat)}$	–	1.6	Vdc
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C			–	1.6	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	6.0	28	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)		C_{ob}	125	500	pF
SWITCHING CHARACTERISTICS					
Resistive Load					
Delay Time	(V_{CC} = 250 V, I_C = 10 A, I_{B1} = I_{B2} = 2.0 A, t_p = 100 μs, Duty Cycle ⩽ 2.0%)	t_d	–	0.05	μs
Rise Time		t_r	–	1.0	μs
Storage Time		t_s	–	4.0	μs
Fall Time		t_f	–	0.7	μs
Inductive Load, Clamped					
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_s	–	5.0	μs
Fall Time		t_f	–	1.5	μs
			Typical		
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_s	2.0		μs
Fall Time		t_f	0.09		μs

*Indicates JEDEC Registered Data.

(1) Puse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

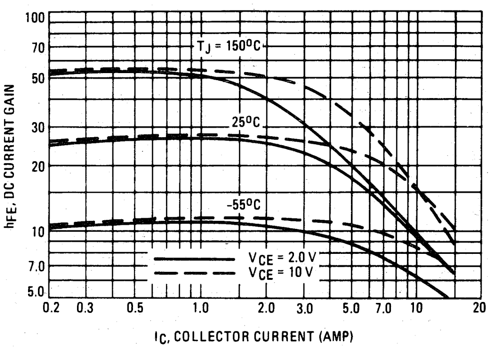


FIGURE 2 — COLLECTOR SATURATION REGION

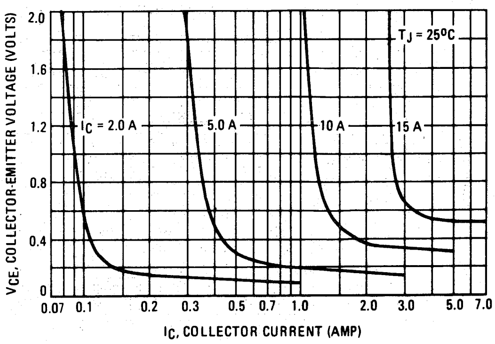


FIGURE 3 — "ON" VOLTAGE

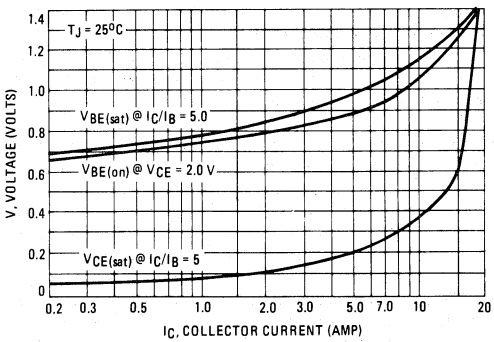


FIGURE 4 — TEMPERATURE COEFFICIENTS

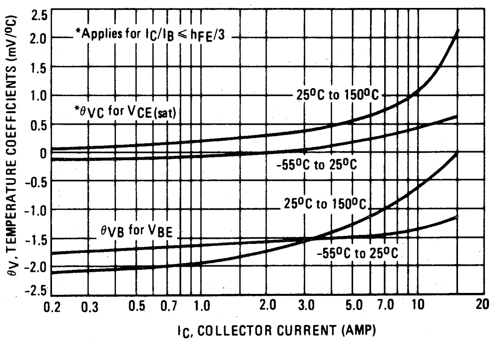


FIGURE 5 — TURN-ON TIME

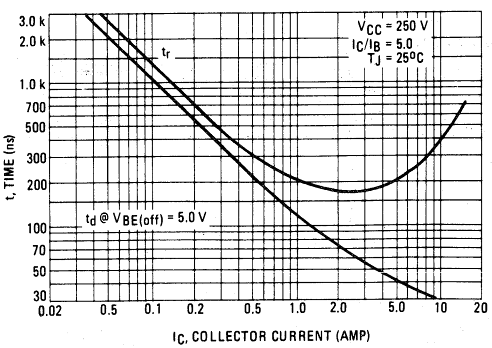
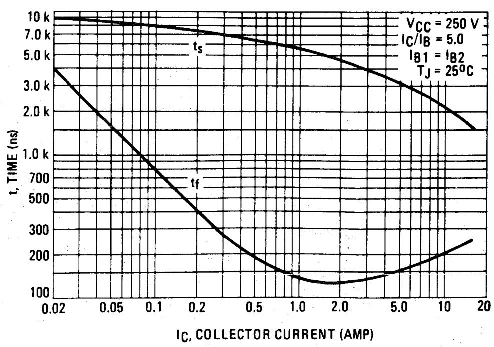


FIGURE 6 — TURN-OFF TIME



3

MAXIMUM RATED SAFE OPERATING AREAS

FIGURE 7 – FORWARD BIAS SAFE OPERATING AREA

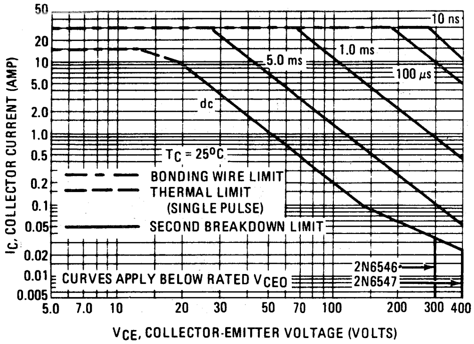


FIGURE 8 – REVERSE BIAS SAFE OPERATING AREA

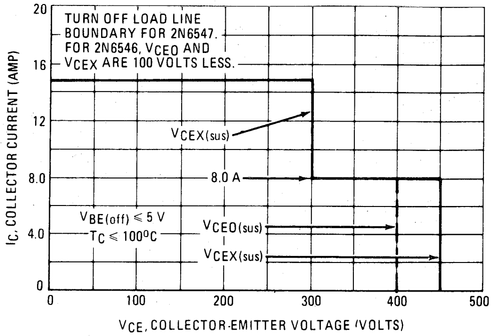
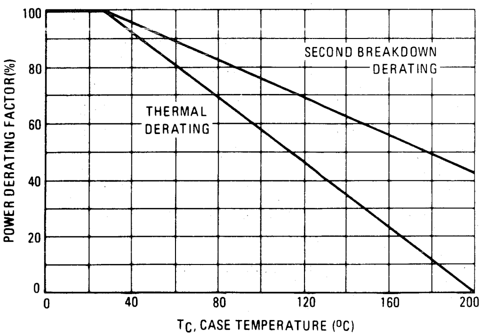


FIGURE 9 – POWER DERATING

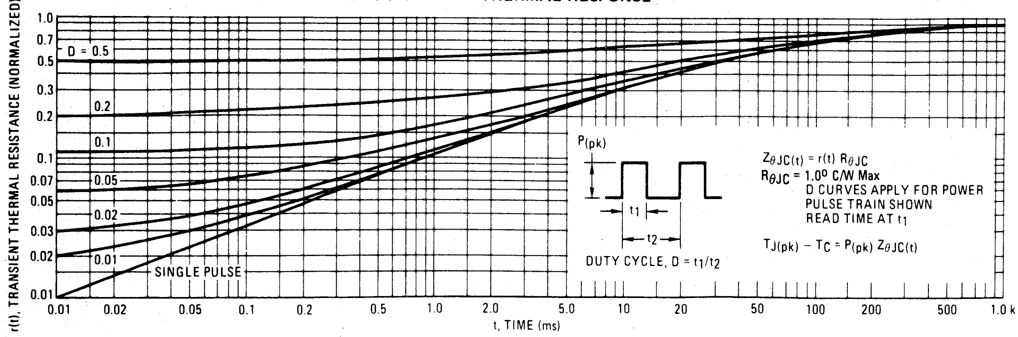


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 10 – THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6576
2N6577
2N6578

NPN SILICON POWER DARLINGTON TRANSISTORS

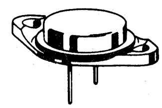
General-purpose EpiBase power Darlington transistors, suitable for linear and switching applications.

- Replacement for 2N3055 and Driver
- High Gain Darlington Performance
- Built-In Diode Protection for Reverse Polarity Protection
- Can Be Driven from Low-Level Logic
- Popular Voltage Range
- Operating Range — –65 to +200°C

15 AMPERE POWER TRANSISTORS

NPN SILICON DARLINGTON

60, 90, 120 VOLTS
120 WATTS



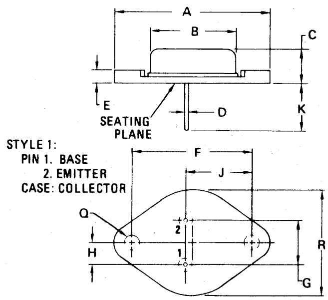
*MAXIMUM RATINGS

Rating	Symbol	2N6576	2N6577	2N6578	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current — Continuous — Peak	I_C	← 15 → ← 30 →			Adc
Base Current — Continuous — Peak	I_B	← 0.25 → ← 0.50 →			Adc
Emitter Current — Continuous — Peak	I_E	← 15.25 → ← 30.5 →			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 120 → ← 0.685 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	← –65 to +200 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.46	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for 10s.	T_L	265	°C

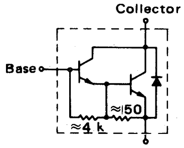
*Indicates JEDEC Registered Data



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03
TO-3

DARLINGTON SCHEMATIC



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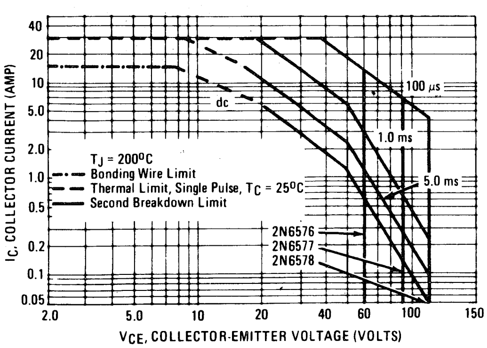
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage(1) (I_C = 200 mAdc, I_B = 0) 2N6576	$V_{CEO(sus)}$	60	–	Vdc
2N6577		90	–	
2N6578		120	–	
Collector Cutoff Current (V_{CE} = Rated Value)	I_{CEO}	–	1.0	mAdc
Collector Cutoff Current (V_{CER} = Rated $V_{CEO(sus)}$ Value, R_{BE} = 10 kΩ, T_C = 150°C)	I_{CER}	–	5.0	mAdc
Collector Cutoff Current V_{CEX} = Rated $V_{CEO(sus)}$ Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	5.0	mAdc
Collector Cutoff Current (V_{CB} = Rated Value)	I_{CBO}	–	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)		100	–	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)		500	5,000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		2000	20,000	
(I_C = 0.4 Adc, V_{CE} = 3.0 Vdc)		200	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 0.15 Adc)		–	4.0	
(I_C = 10 Adc, I_B = 0.1 Adc)		–	2.8	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 0.15 Adc)		–	4.5	
(I_C = 10 Adc, I_B = 0.1 Adc)		–	3.5	
Collector-Emitter Diode Voltage Drop (I_{EC} = 15 Adc)	V_F	–	4.5	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common-Emitter Small-Signal Short-Circuit Current Transfer Ratio (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$\|h_{fe}\|$	10	200	–
SWITCHING CHARACTERISTICS				
RESISTIVE LOAD (Figure 2)				
Delay Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.15	μs
Rise Time	t_r	–	1.0	μs
Storage Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_s	–	2.0	μs
Fall Time	t_f	–	7.0	μs

*Indicates JEDEC Registered Data
(1) Pulse test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

FIGURE 1 – RATED FORWARD BIASED SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%.

$T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – DC CURRENT GAIN

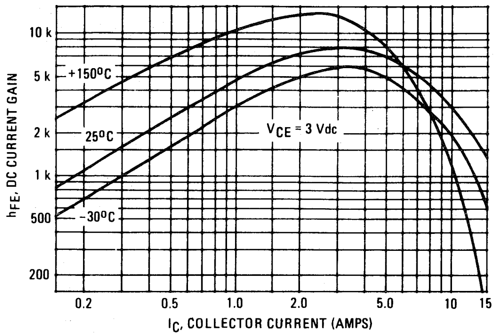


FIGURE 3 – COLLECTOR-SATURATION REGION

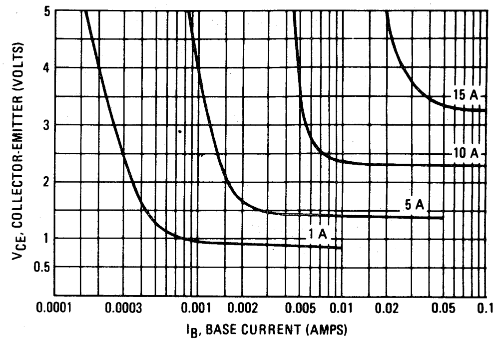


FIGURE 4 – COLLECTOR SATURATION VOLTAGE

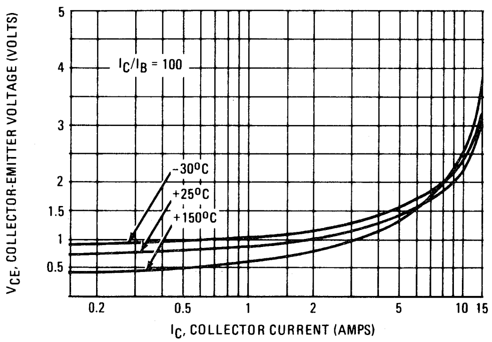


FIGURE 5 – BASE-EMITTER VOLTAGE

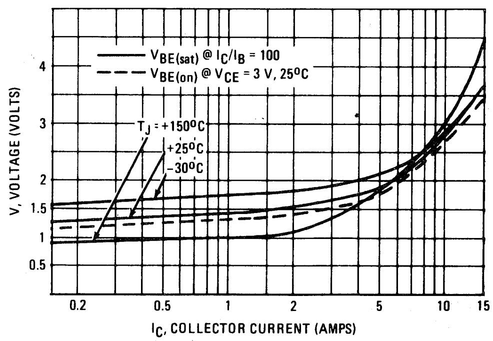
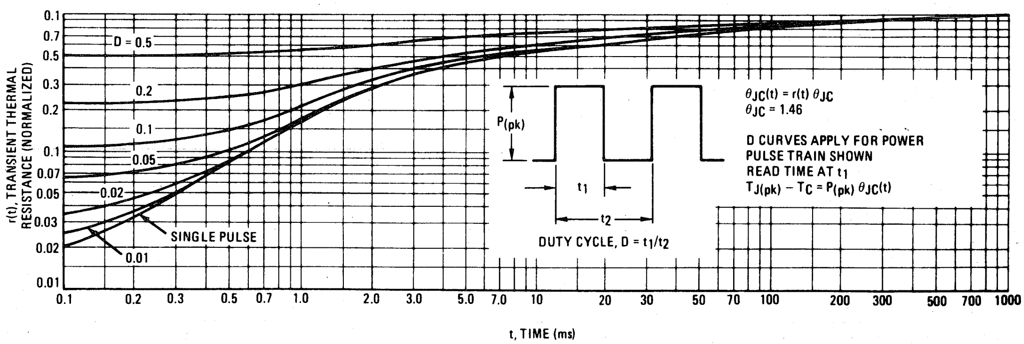


FIGURE 6 – THERMAL RESPONSE



3

2N6609
See Page
3-52

Darlington Silicon Power Transistors

2N6667
2N6668

. . . designed for general-purpose amplifier and low speed switching applications.

- High DC Current Gain — h_{FE} = 3500 (Typ) @ I_C = 4 Adc
- Collector-Emitter Sustaining Voltage — @ 200 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6667
  = 80 Vdc (Min) — 2N6668
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 2 Vdc (Max) @ I_C = 5 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- Complementary to 2N6387, 2N6388

PNP SILICON

DARLINGTON POWER TRANSISTORS

10 AMPERES
60–80 VOLTS
65 WATTS

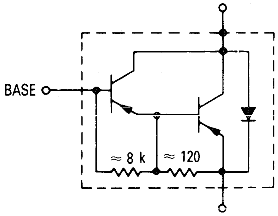
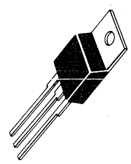


Figure 1. Darlington Schematic



CASE 221A-04
TO-220AB

***MAXIMUM RATINGS**

Rating	Symbol	2N6667	2N6668	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous — Peak	I_C	10 15		Adc
Base Current	I_B	250		mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.52		watts W/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 0.016		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

* Indicates JEDEC Registered Data

3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N6667 2N6668	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	2N6667 2N6668	I_{CEO}	— —	1 1	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	 2N6667 2N6668 2N6667 2N6668	I_{CEX}	 — — — —	 300 300 3 3	 μAdc mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	5	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5 Adc, V_{CE} = 3 Vdc) (I_C = 10 Adc, V_{CE} = 3 Vdc)		h_{FE}	1000 100	20000 —	—
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	— —	2 3	Vdc
Base-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	— —	2.8 4.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)		$\|h_{fe}\|$	20	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}	—	200	pF
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc, f = 1 kHz)		h_{fe}	1000	—	—

* Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

R_B & R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1, MUST BE FAST RECOVERY TYPES, .e.g,
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

FOR t_d AND t_r, D_1 IS DISCONNECTED AND V_2 = 0
t_r, $t_f \leq$ 10 ns
DUTY CYCLE = 1%

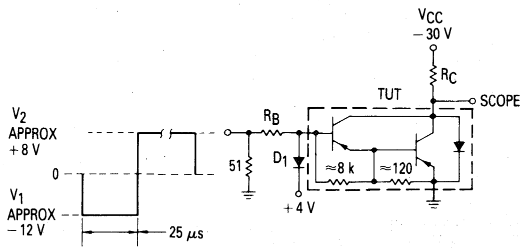


Figure 2. Switching Times Test Circuit

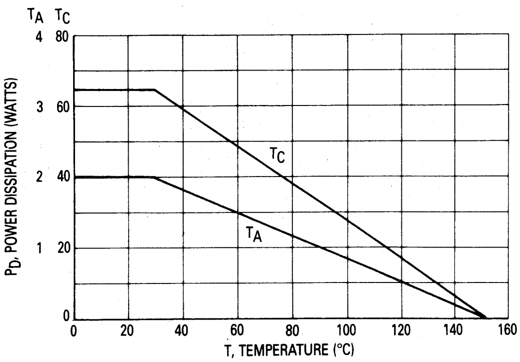


Figure 3. Power Derating

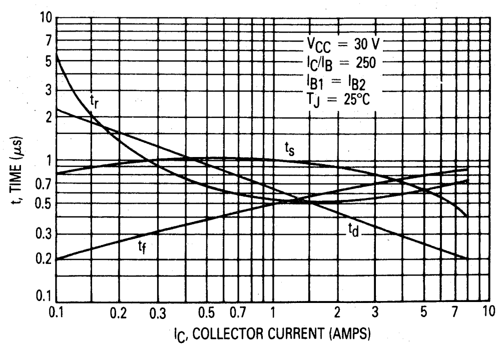


Figure 4. Typical Switching Times

3

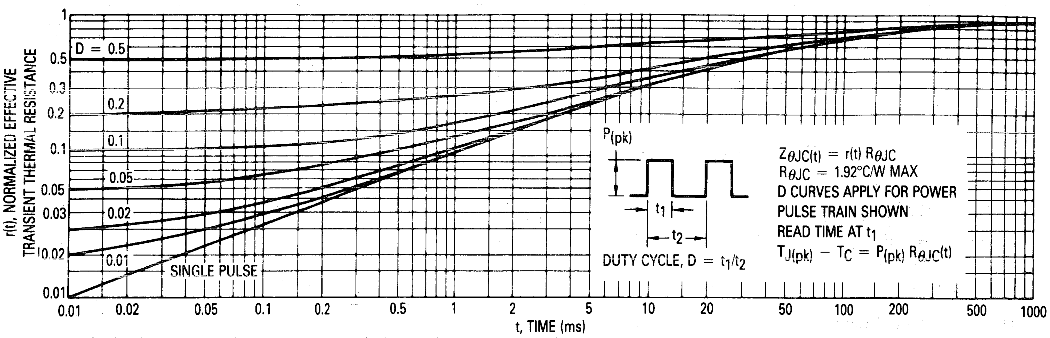
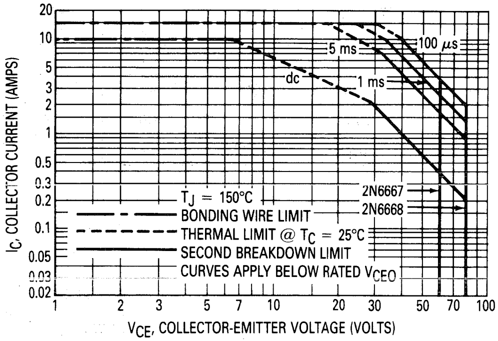


Figure 5. Thermal Response



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Figure 6. Maximum Safe Operating Area

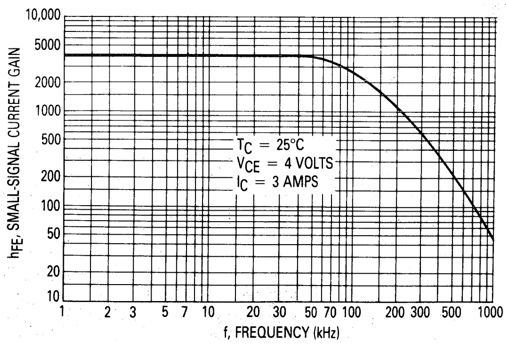


Figure 7. Typical Small-Signal Current Gain

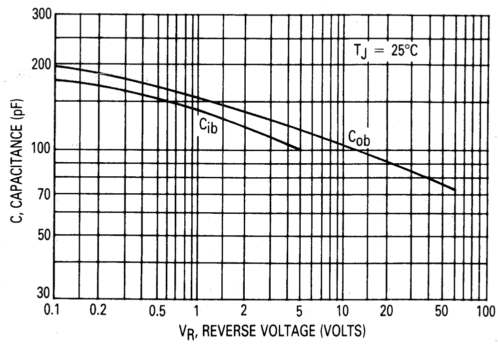


Figure 8. Typical Capacitance

3

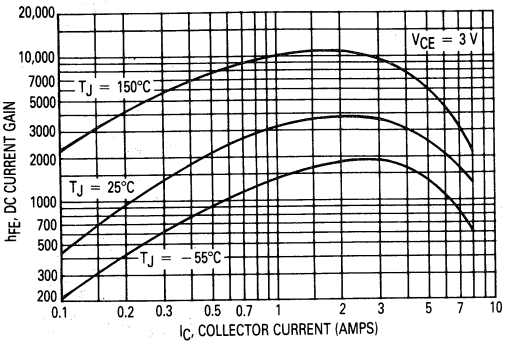


Figure 9. Typical DC Current Gain

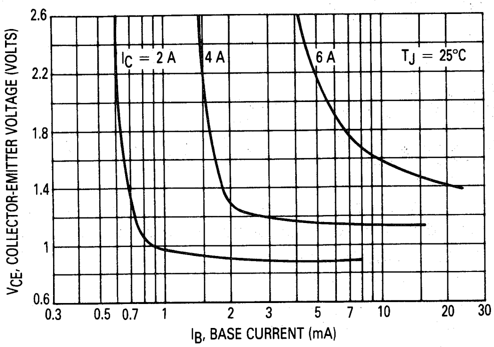


Figure 10. Typical Collector Saturation Region

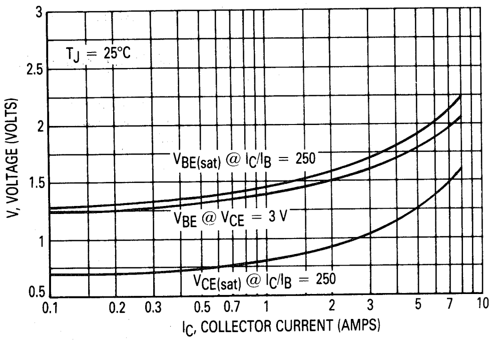


Figure 11. Typical "On" Voltages

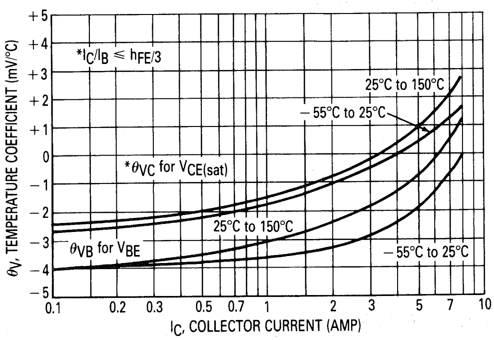


Figure 12. Typical Temperature Coefficients

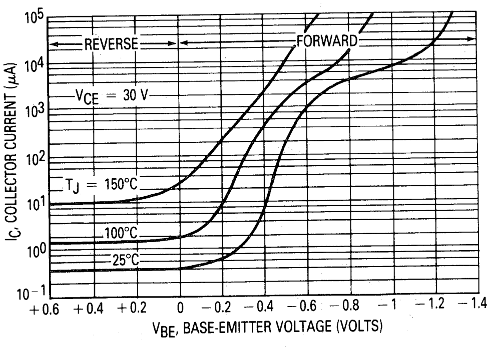
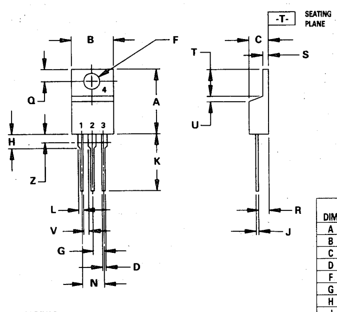


Figure 13. Typical Collector Cut-Off Region

OUTLINE DIMENSIONS



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

2N6648
See Page
3-209

NPN Silicon Power Transistors

2N6676
2N6677
2N6678
MJH6676
MJH6677
MJH6678

The 2N6676, 2N6677, 2N6678, MJH6676, MJH6677, and MJH6678 transistors are designed for high voltage switching applications such as:

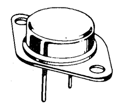
- Off-Line Supplies
- Converter Circuits
- Pulse Width Modulated Regulators

Specification Features —
High Voltage Capability
Fast Switching Speeds
Low Saturation Voltages
High SOA Ratings

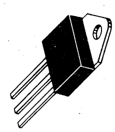
NPN SILICON

POWER TRANSISTORS

15 AMPERES
300, 350, 400 VOLTS
125 and 175 WATTS



CASE 1-05
TO-204AA
2N6676
2N6677
2N6678



CASE 340-01
TO-218AC
MJH6676
MJH6677
MJH6678

MAXIMUM RATINGS

Rating	Symbol	2N6676 MJH6676	2N6677 MJH6677	2N6678 MJH6678	Unit
Collector-Emitter Voltage	V_{CEV}	450	550	650	Vdc
Collector-Emitter Voltage	V_{CEX}	350	400	450	Vdc
Collector-Emitter Voltage	V_{CEO}	300	350	400	Vdc
Emitter-Base Voltage	V_{EBO}	8			Vdc
Collector Current — Continuous — Peak	I_C I_{CM}	15 20			Adc
Base Current — Continuous	I_B	5			Adc
Maximum Lead Temperature At Distance > 1/16 in. (1.58 mm) from seating plane for 10 s max		235			°C

MAXIMUM THERMAL RATINGS

Rating	Symbol	2N6676 2N6677 2N6678	MJH6676 MJH6677 MJH6678	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	1		°C/W
Power Dissipation $T_C = 25°C$ Derate above 25°C	P_T	175 1	125 1	Watts W/°C
Operating and Storage Junction	T_J, T_{stg}	−65 to +200	−65 to +150	°C

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	— —	0.1 1	mA
Emitter Cutoff Current (V_{EB} = 8 Vdc, I_C = 0)		I_{EBO}	—	2	mA
Collector-Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0)	2N6676, MJH6676 2N6677, MJH6677 2N6678, MJH6678	$V_{CEO(sus)}$	300 350 400	— — —	Vdc
Collector-Emitter Sustaining Voltage (I_C = 15 A, $V_{CE(pk)}$ = V_{clamp} = Rated V_{CEX})	2N6676, MJH6676 2N6677, MJH6677 2N6678, MJH6678	$V_{CEX(sus)}$	350 400 450	— — —	Vdc
SECOND BREAKDOWN					
Second Breakdown Collector with Base Forward Biased		$I_{S/b}$	See Figure 1		
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 2		
ON CHARACTERISTICS					
DC Current Gain (I_C = 15 A, V_{CE} = 3 V)		h_{FE}	8	—	—
Base-Emitter Saturation Voltage (I_C = 15 A, I_B = 3 A)		$V_{BE(sat)}$	—	1.5	Vdc
Collector-Emitter, Saturation Voltage (I_C = 15 A, I_B = 3 A) (I_C = 15 A, I_B = 3 A, T_C = 100°C)		$V_{CE(sat)}$	— —	1.5 2	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain (I_C = 1 A, V_{CE} = 10 Vdc, f = 5 MHz)		$\|h_{fe}\|$	3	10	—
Output Capacitance (I_C = 1 A, V_{CB} = 10 Vdc, f = 0.1 MHz)		C_{ob}	150	500	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Max	Unit
Resistive Load						
Delay Time	V_{CC} = 200 V, I_C = 15 A, I_{B1} = I_{B2} = 3 A, t_p = 20 μs, Duty Cycle ≤ 2 %, V_{B2} ≃ 6 V, R_L ≃ 13.5 Ω (See Figure 3)	T_C = 25°C	t_d	—	0.1	μs
Rise Time			t_r	—	0.6	
Storage Time			t_s	—	2.5	
Fall Time			t_f	—	0.5	
Delay Time		T_C = 100°C	t_d	—	0.4	
Rise Time			t_r	—	1	
Storage Time			t_s	—	4	
Fall Time			t_f	—	1	
Inductive Load						
Cross Over Time	L = 50 μH, $V_{CE(pk)}$ = V_{clamp} = Rated V_{CEX} (See Figure 3)	T_C = 25°C	t_c	—	0.5	μs
		T_C = 100°C		—	0.8	

3

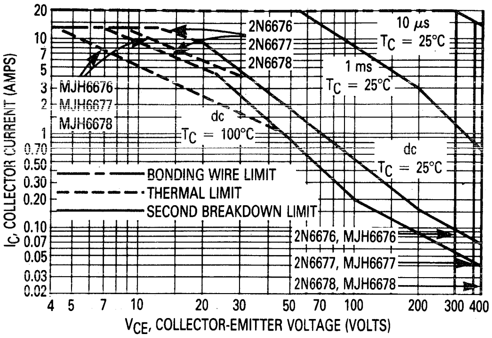


Figure 1. Maximum Rated Forward Biased Safe Operating Area

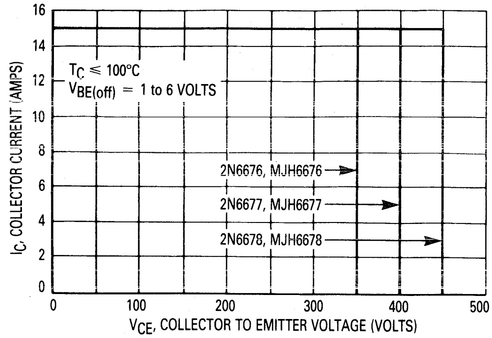


Figure 2. Maximum Rated Reverse Biased Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

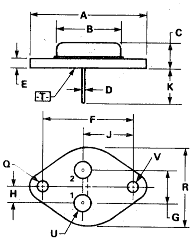
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C and T_C = 100°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 2 gives the RBSOA characteristics.

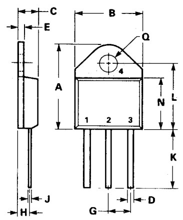
OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.130	0.210
V	3.81	4.19	0.151	0.165

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q: ⌖ 0.13 (0.005) Ⓜ T V Ⓜ
FOR LEADS: ⌖ 0.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

CASE 1-05
TO-204AA
(Formerly TO-3)
2N6676 thru 2N6678



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340-01
TO-218AC
MJH6676 thru MJH6678

3

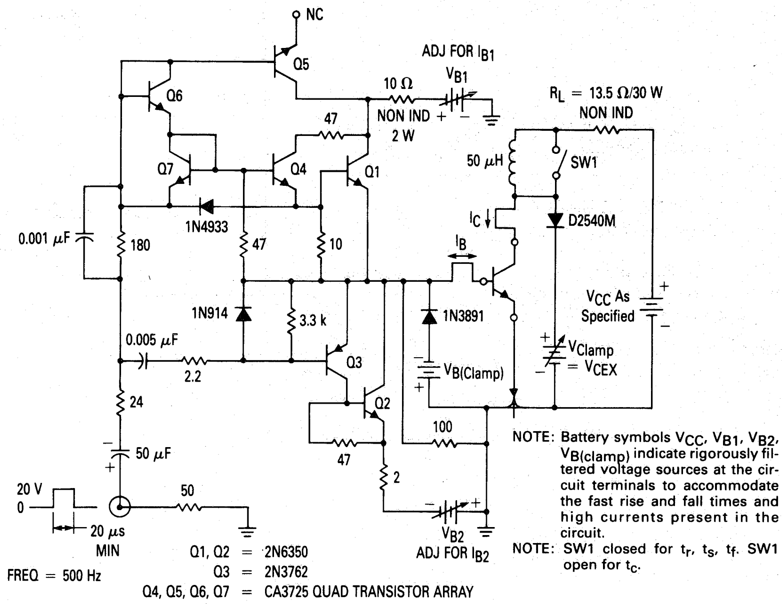
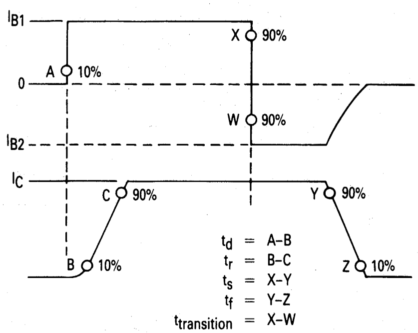


Figure 3. Switching Times Test Circuit



NOTE: TRANSITION TIME FROM 90% IB1 to 90% IB2 MUST BE LESS THAN 0.5 μs.

Figure 4. Switching Time Measurements

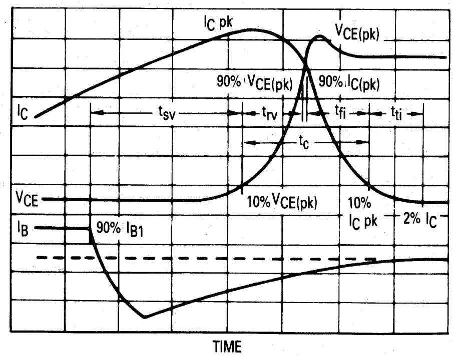


Figure 5. Inductive Switching Measurements

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6833
2N6834

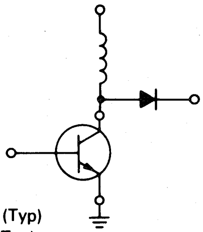
Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  - 50 ns Inductive Fall Time — 75°C (Typ)
  - 70 ns Inductive Crossover Time — 75°C (Typ)
  - 500 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +150°C
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



5.0 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
80 and 125 WATTS

MAXIMUM RATINGS

Rating	Symbol	2N6833	2N6834	Unit
Collector-Emitter Voltage*	$V_{CEO(sus)}$	450		Vdc
Collector-Emitter Voltage*	V_{CEV}	850		Vdc
Emitter Base Voltage*	V_{EB}	6.0		Vdc
Collector Current — Continuous* — Peak (1)	I_C I_{CM}	5.0 10		Adc
Base Current — Continuous* — Peak (1)	I_B I_{BM}	4.0 8.0		Adc
Total Power Dissipation @ T_C = 25°C* @ T_C = 100°C* Derate above 25°C*	P_D	80 32 0.64	125 71.5 0.714	Watts W/°C
Operating and Storage Junction Temperature Range*	T_J, T_{stg}	-65 to +150	-65 to +200	°C

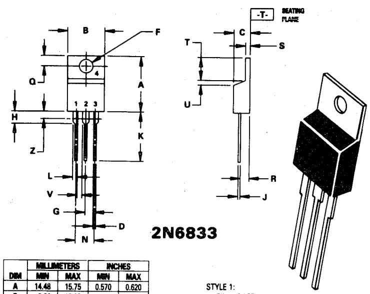
THERMAL CHARACTERISTICS

Characteristic	Symbol	2N6833	2N6834	Unit
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	1.56	1.40	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds*	T_L	275		°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
*Indicate JEDEC Registered Data

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



2N6833

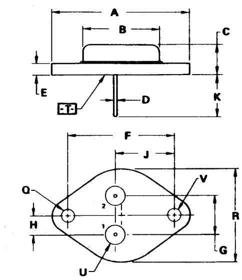
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

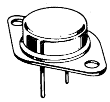
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

2N6834





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA (Formerly TO-3)

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.25*	
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5*	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0*	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figures 15* and 16*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 17			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)		—	—	1.0	
(I_C = 3.0 Adc, I_B = 0.4 Adc)		—	—	2.5*	
(I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)		—	—	2.5*	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 3.0 Adc, I_B = 0.4 Adc)		—	—	1.5*	
(I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)		—	—	1.5	
DC Current Gain	h_{FE}				—
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)		7.5*	—	30*	
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)		5.0	—	—	
DYNAMIC CHARACTERISTICS (2)					
Current Gain - Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.25 Adc, f_{test} = 10 MHz)	f_T	15*	—	75*	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	20*	—	200*	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 0.8 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100*	ns
Rise Time			t_r	—	100	300*	
Storage Time			t_s	—	1000	3000*	
Fall Time			t_f	—	60	300*	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	400	—	
Fall Time			t_f	—	130	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	500	1600*	ns
Fall Time			t_{fi}	—	100	200*	
Crossover Time			t_c	—	120	250*	
Storage Time		(T_C = 150°C)	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.
(2) $f_T = |h_{fe}| \cdot f_{test}$
*Indicates JEDEC Registered Limit

3

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

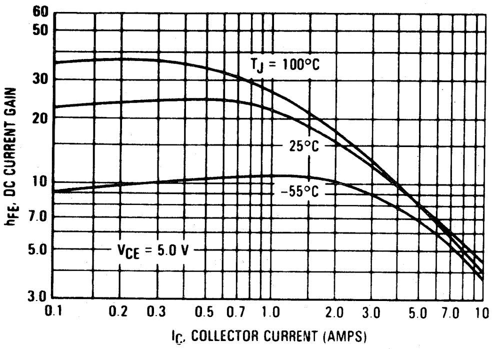


FIGURE 2 — COLLECTOR SATURATION REGION

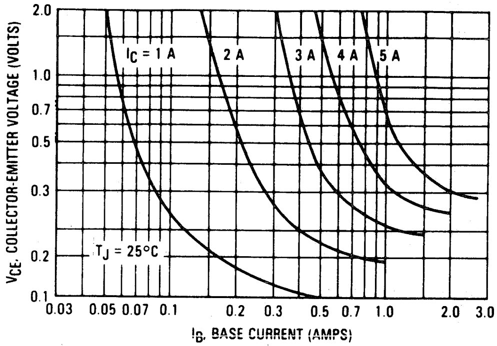


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

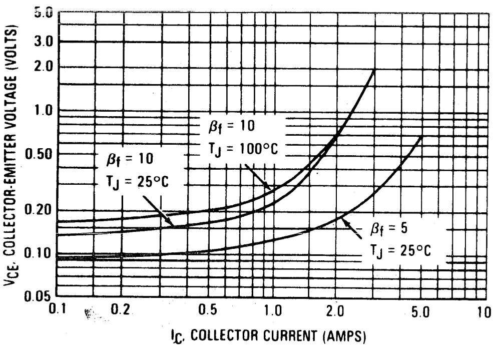


FIGURE 4 — BASE-EMITTER VOLTAGE

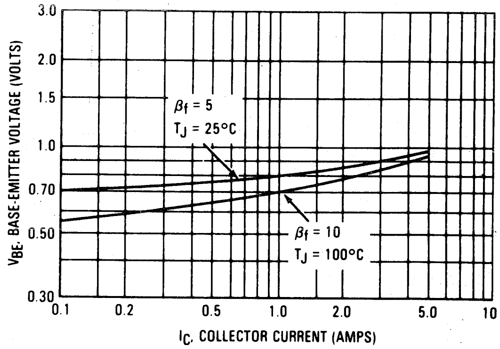


FIGURE 5 — COLLECTOR CUTOFF REGION

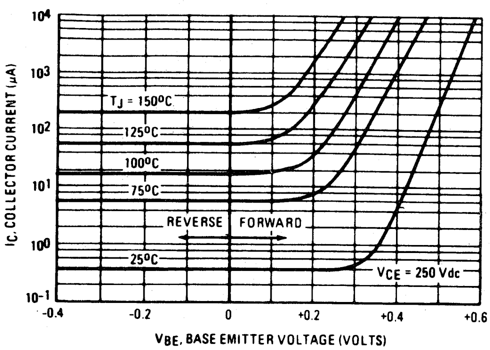
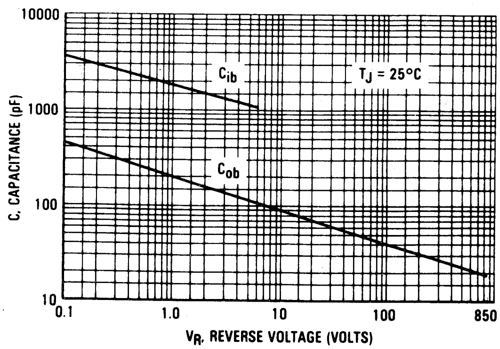


FIGURE 6 — CAPACITANCE



3

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

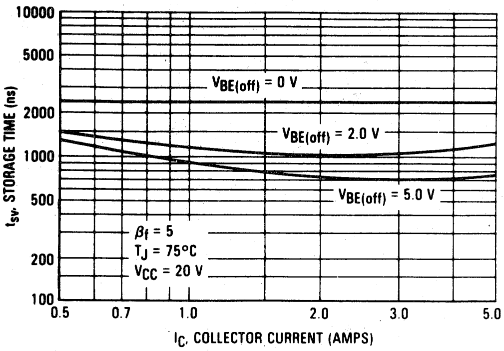


FIGURE 8 — STORAGE TIME

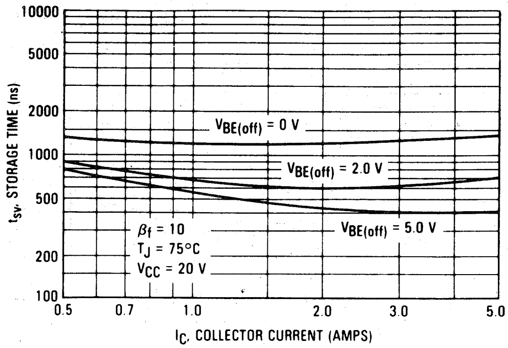


FIGURE 9 — COLLECTOR CURRENT FALL TIME

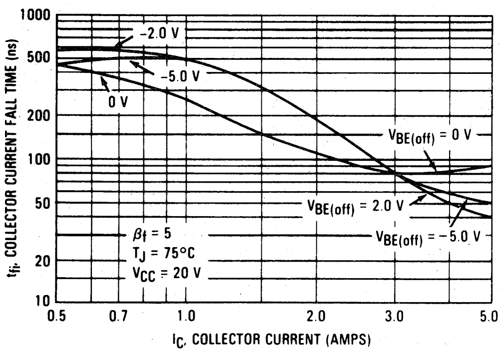


FIGURE 10 — COLLECTOR CURRENT FALL TIME

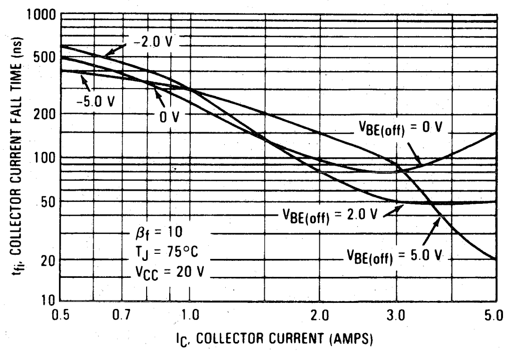


FIGURE 11 — CROSSOVER TIME

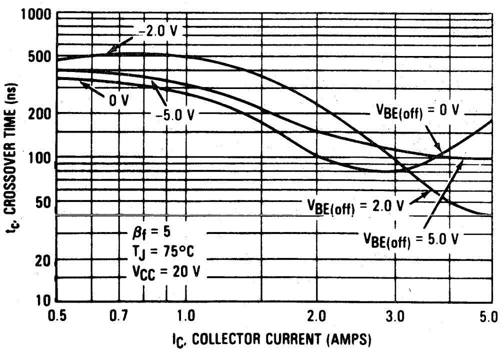


FIGURE 12 — CROSSOVER TIME

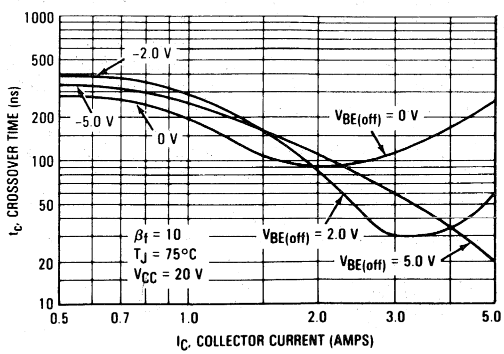


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

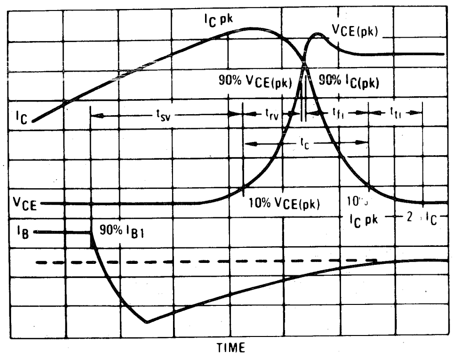
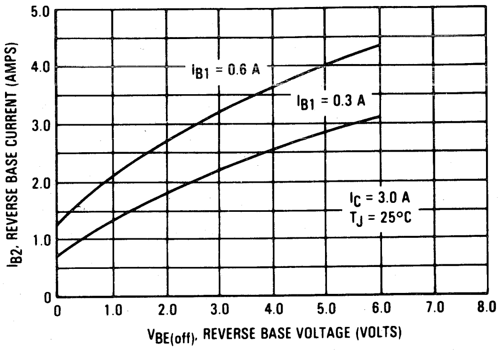


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA (2N6833)

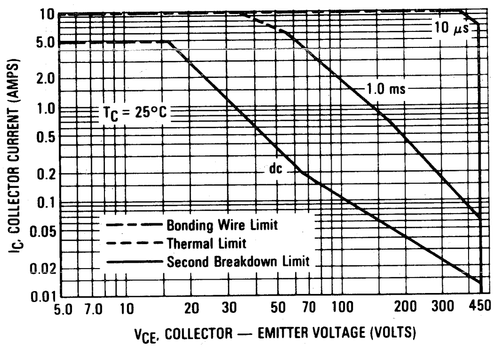
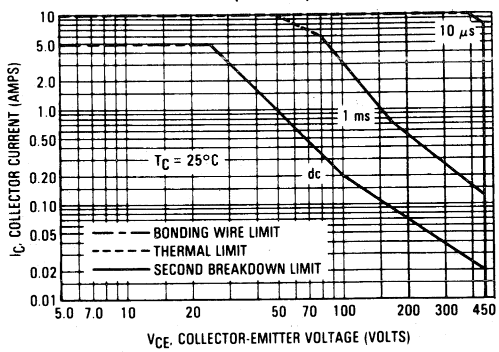


FIGURE 16 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA (2N6834)



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 15 and 16 are based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 15 and 16 may be found at any case temperature by using the appropriate curve on Figures 18 or 19.

$T_{J(pk)}$ may be calculated from the data in Figures 20 or 21. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable putting reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

FIGURE 17 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA

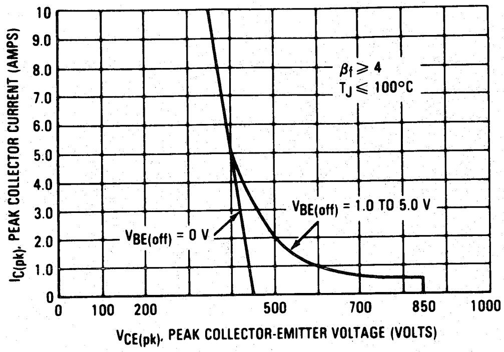


FIGURE 18 — POWER DERATING (2N6833)

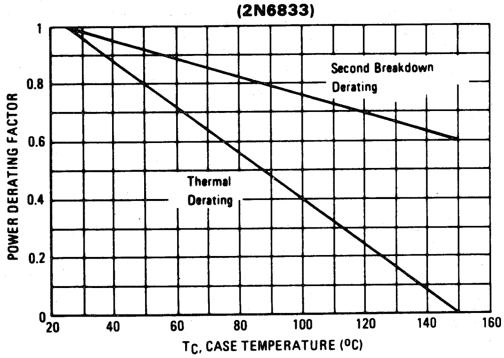


FIGURE 19 — POWER DERATING (2N6834)

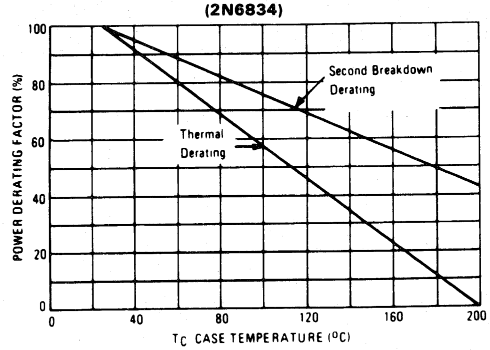
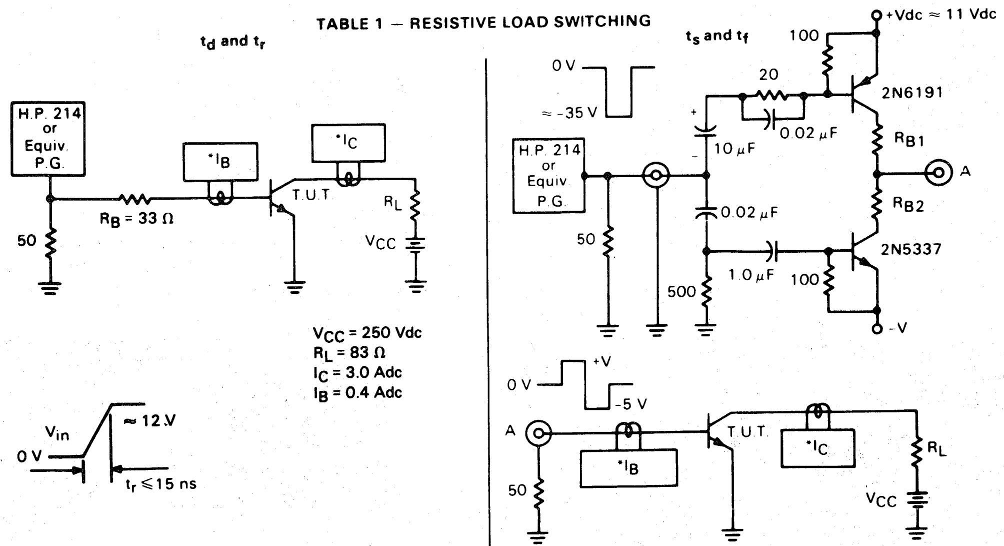


TABLE 1 — RESISTIVE LOAD SWITCHING

t_d and t_r

t_s and t_f



*Tektronix P-6042 or Equivalent

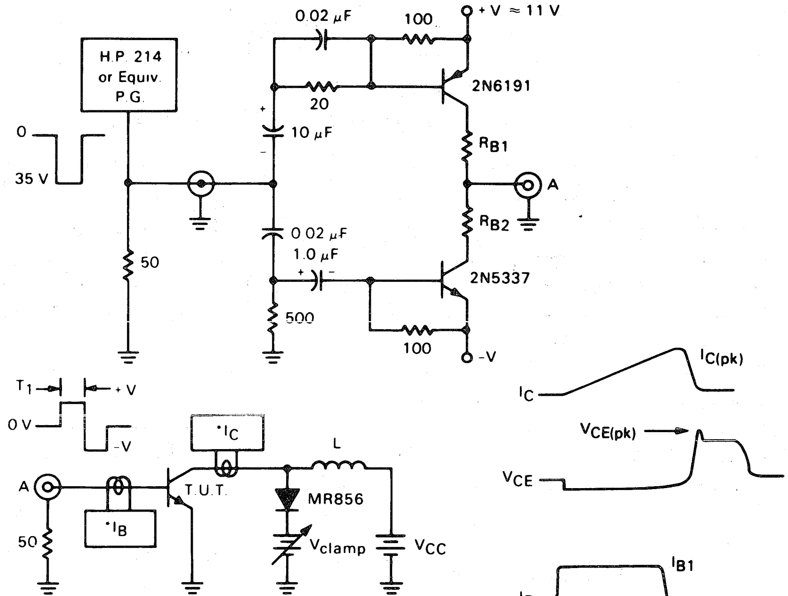
V_{CC} = 250
R_L = 83 Ω
I_C = 3.0 Adc

I_{B1} = 0.4 Adc
I_{B2} = 0.8 Adc
For $V_{BE(off)}$ = 5.0 V R_{B2} = 0 Ω

R_{B1} = 33 Ω
R_{B2} = 8.0 Ω

*Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



$T_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 Volts

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

*Tektronix
P-6042 or
Equivalent

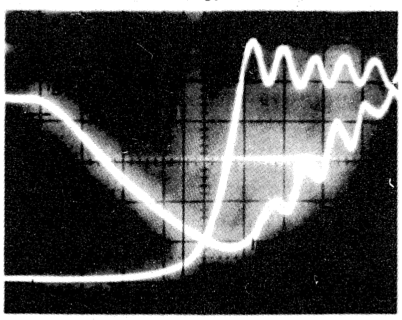
Scope - Tektronix
7403 or
Equivalent

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

3

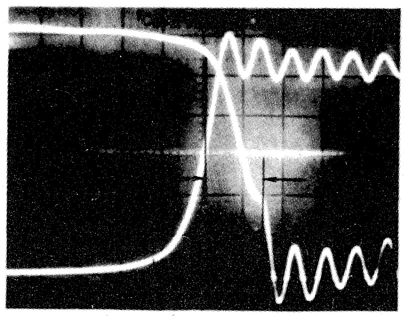
TYPICAL INDUCTIVE SWITCHING WAVEFORMS

t_{sv}



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.4 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base =
20 ns/cm

t_{fi}, t_c



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.4 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base =
20 ns/cm

THERMAL RESPONSE

FIGURE 20 — 2N6833

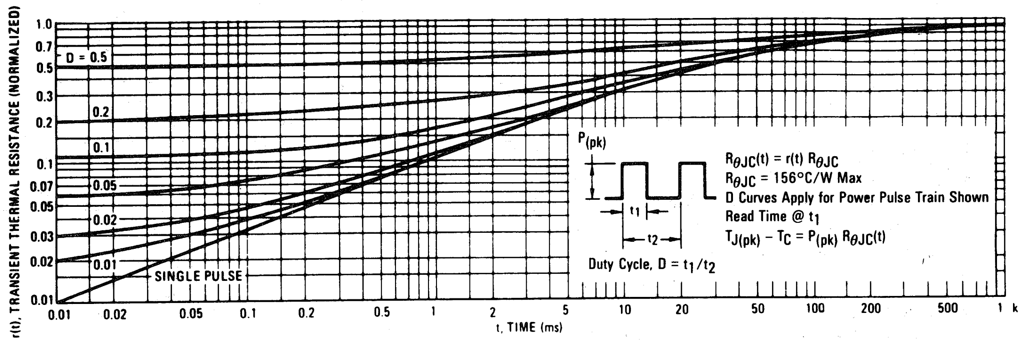
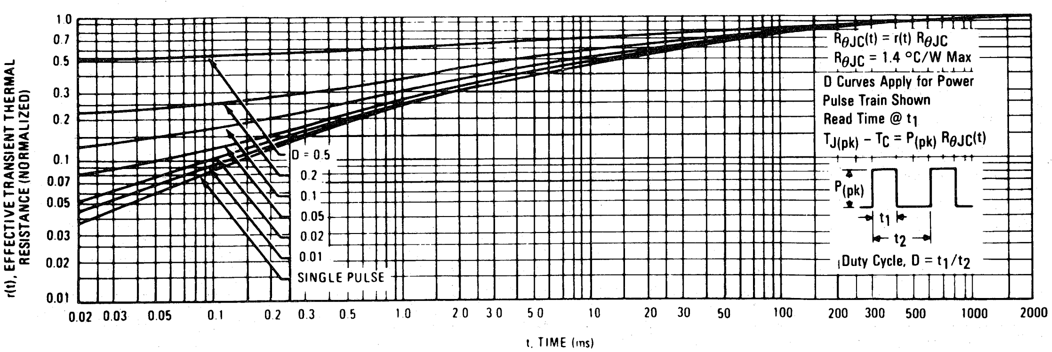


FIGURE 21 — 2N6834



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

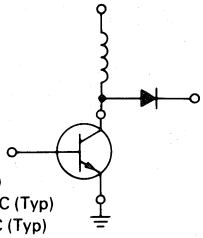
2N6835

Designer's Data Sheet

SWITCHMODE III SERIES
ULTRA-FAST NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

- Switching Regulators
- Inverters
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  - 90 ns Inductive Fall Time — 75°C (Typ)
  - 90 ns Inductive Crossover Time — 75°C (Typ)
  - 450 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



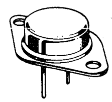
8 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



*MAXIMUM RATINGS

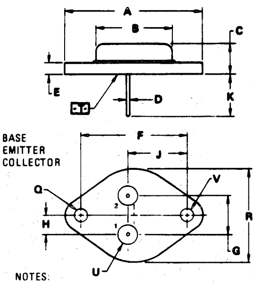
Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8.0 16	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6.0 12	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 85.5 0.86	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5.0 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

*Indicate JEDEC Registered Data



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	∅ 0.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	∅ 0.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA Type
(TO-3 Type)

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	 — —	 — —	 0.25* 1.5*	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, $R_{BE(off)}$ = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0*	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.40 Adc) (I_C = 5.0 Adc, I_B = 0.66 Adc) (I_C = 5.0 Adc, I_B = 0.66 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 1.2 2.5* 3.0*	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.66 Adc) (I_C = 5.0 Adc, I_B = 0.66 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 1.5* 1.5	Vdc
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 7.5* 4.0*	 — —	 30* —	—
DYNAMIC CHARACTERISTICS (2)					
Current Gain - Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.25 Adc, f_{test} = 10 MHz)	f_T	10*	—	75*	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	50*	—	350*	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 5.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.66 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 1.3 Adc, R_{B2} = 4.0 Ω)	t_d	—	20	50*	ns
Rise Time			t_r	—	85	250*	
Storage Time			t_s	—	1000	2500*	
Fall Time			t_f	—	70	250*	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	500	—	
Fall Time			t_f	—	100	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 5.0 Adc, I_{B1} = 0.66 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	700	1800*	ns
Fall Time			t_{fi}	—	80	200*	
Crossover Time			t_c	—	150	250*	
Storage Time		(T_C = 150°C)	t_{sv}	—	800	—	
Fall Time			t_{fi}	—	80	—	
Crossover Time			t_c	—	200	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.
(2) f_T = | she | f_{test}
*Indicates JEDEC Registered Limit

3

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

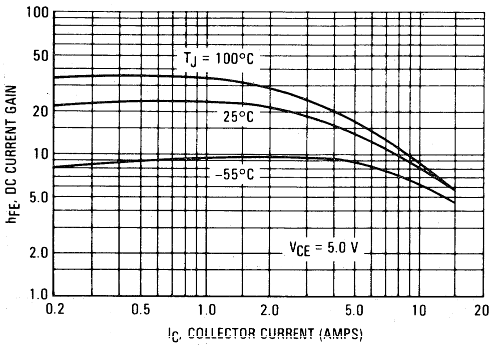


FIGURE 2 — COLLECTOR SATURATION REGION

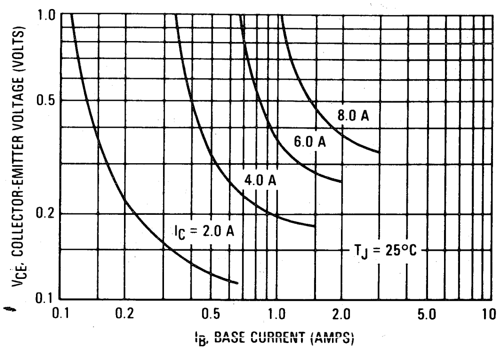


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

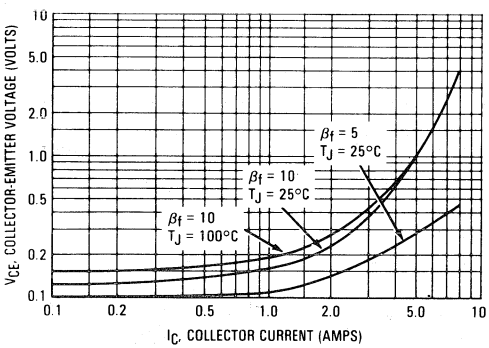


FIGURE 4 — BASE-EMITTER VOLTAGE

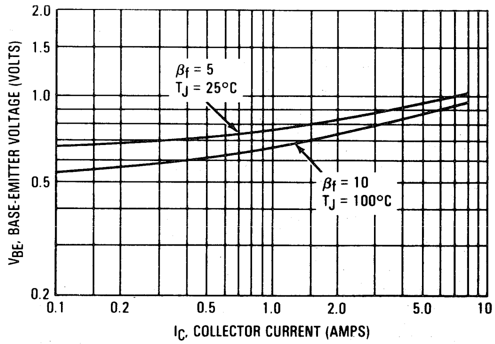


FIGURE 5 — COLLECTOR CUTOFF REGION

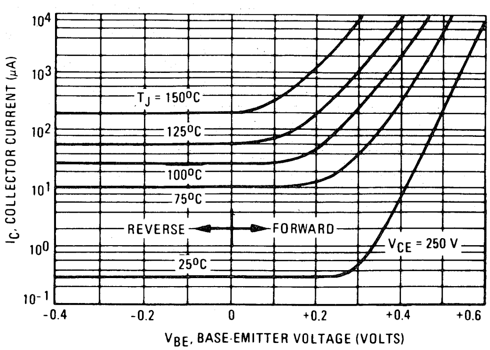
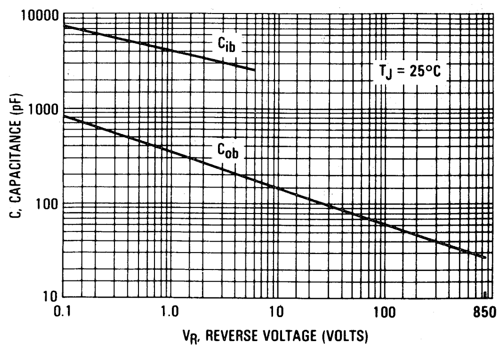


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

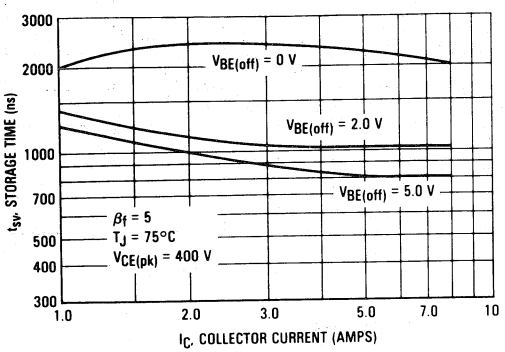


FIGURE 8 — STORAGE TIME

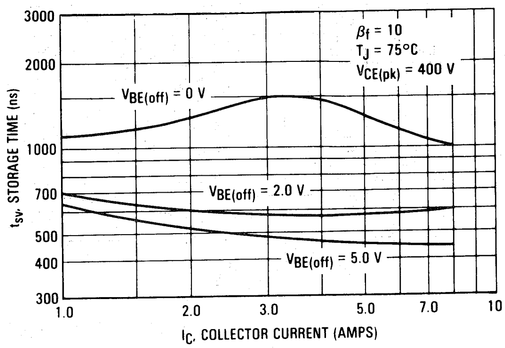


FIGURE 9 — COLLECTOR CURRENT FALL TIME

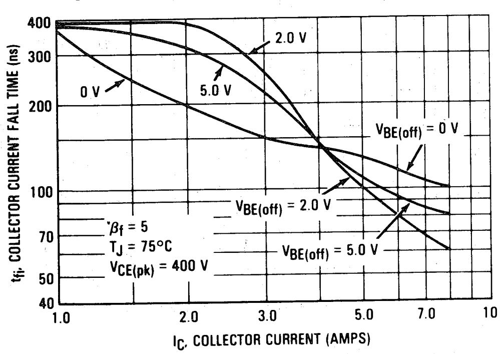


FIGURE 10 — COLLECTOR CURRENT FALL TIME

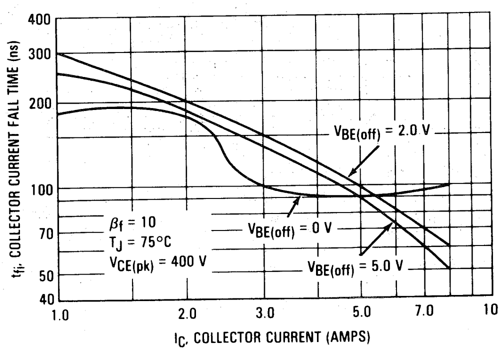


FIGURE 11 — CROSSOVER TIME

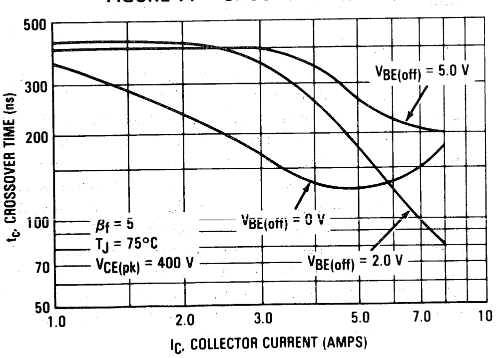


FIGURE 12 — CROSSOVER TIME

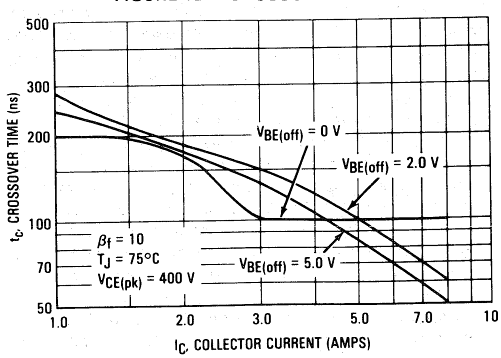


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FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

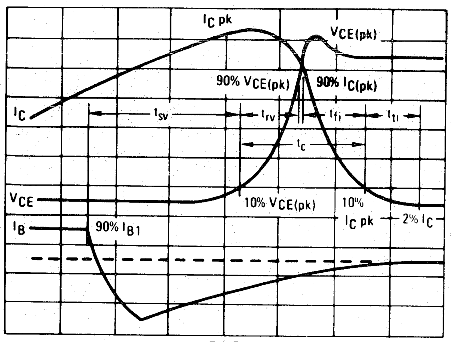
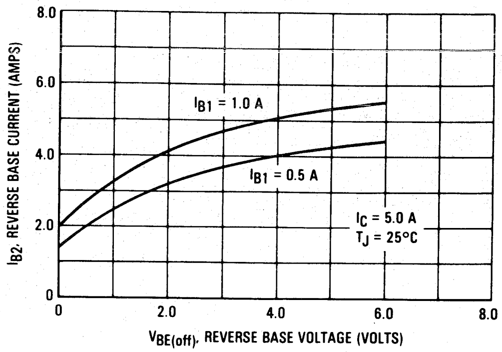


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

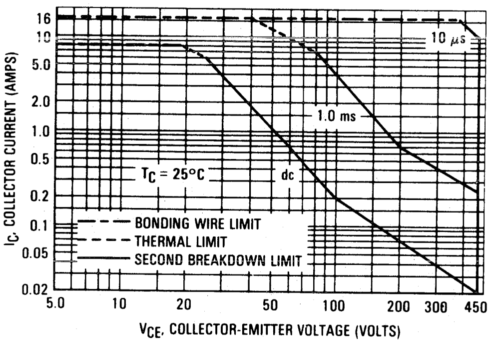
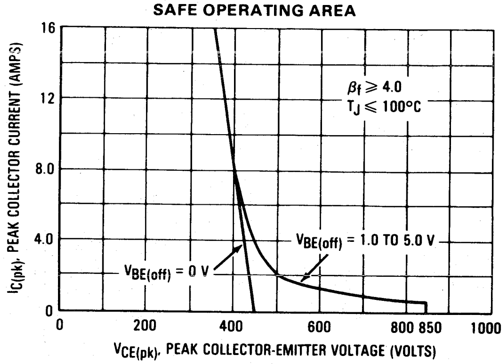


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

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FIGURE 17 — THERMAL RESPONSE

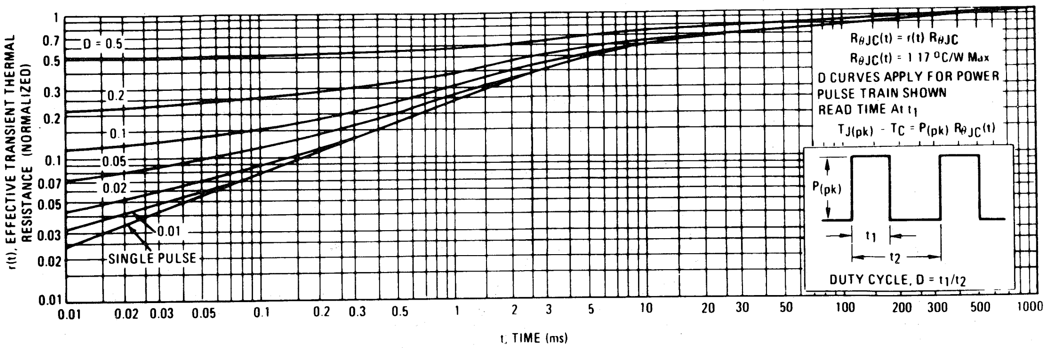


FIGURE 18 — POWER DERATING

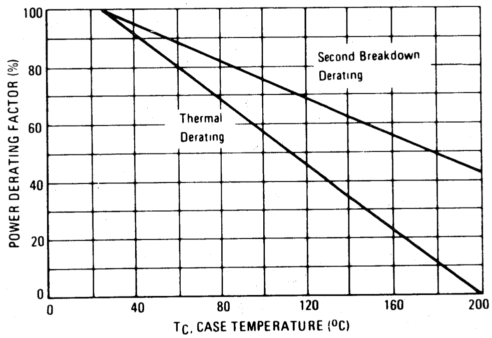
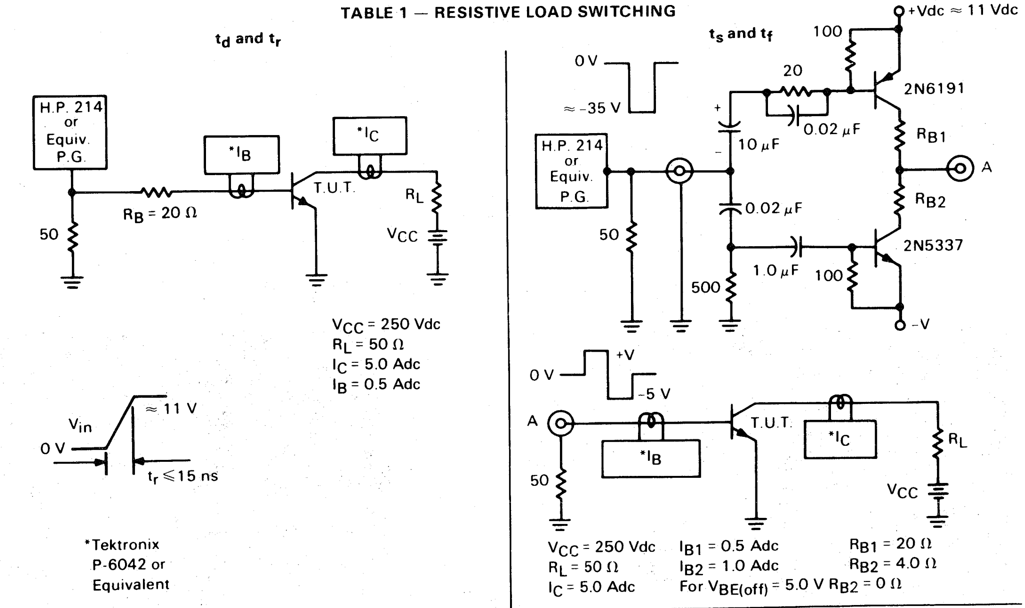


TABLE 1 — RESISTIVE LOAD SWITCHING



*Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

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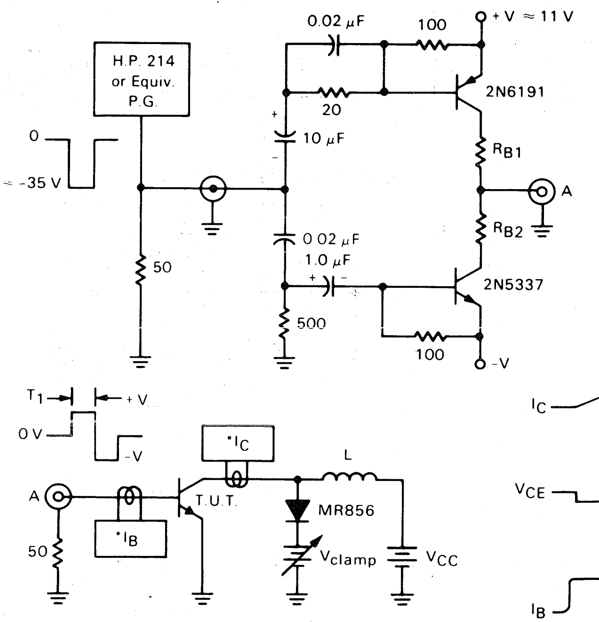
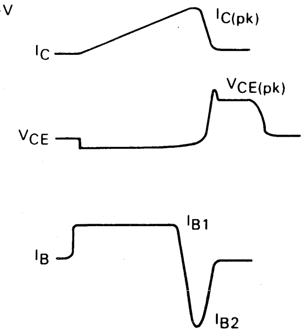
TABLE 2 — INDUCTIVE LOAD SWITCHING





$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

*Tektronix
P-6042 or
Equivalent

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

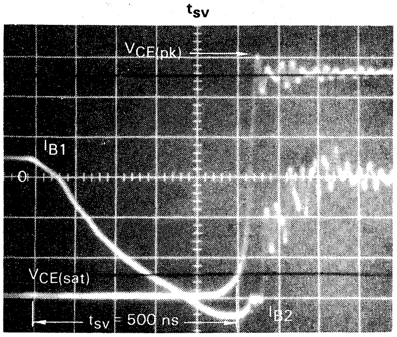
Scope - Tektronix
7403 or
Equivalent

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

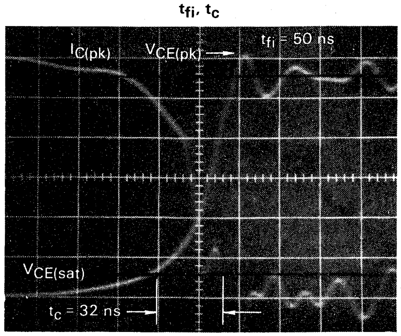
TYPICAL INDUCTIVE SWITCHING WAVEFORMS

t_{sv}



$I_{C(pk)}$ = 5.0 Amps
I_{B1} = 0.5 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base =
100 ns/cm

t_{fi}, t_c



$I_{C(pk)}$ = 5.0 Amps
I_{B1} = 0.5 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base =
20 ns/cm

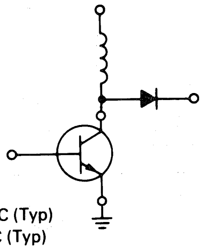
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6836

Designer's Data Sheet

SWITCHMODE III SERIES
ULTRA-FAST NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.



- Switching Regulators
- Inverters
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  - 30 ns Inductive Fall Time — 75°C (Typ)
  - 50 ns Inductive Crossover Time — 75°C (Typ)
  - 600 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range −65 to +200°C
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

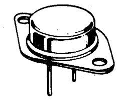
15 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



*MAXIMUM RATINGS

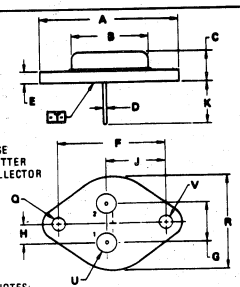
Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5.0 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

*Indicate JEDEC Registered Data



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅ 0.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA Type
(TO-3 Type)

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.25*	mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5*	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0*	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.7 Adc)	$V_{CE(sat)}$	—	—	1.2	Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)		—	—	2.5*	
(I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)		—	—	3.0*	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	—	—	1.5*	Vdc
(I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)		—	—	1.5	
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	8.0*	—	30*	—
(I_C = 15 Adc, V_{CE} = 5.0 Vdc)		5.0	—	—	
DYNAMIC CHARACTERISTICS (2)					
Current Gain - Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.25 Adc, f_{test} = 10 MHz)	f_T	10*	—	75*	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	50*	—	400*	pF

SWITCHING CHARACTERISTICS

Characteristic	Test Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.0 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I_{B2} = 2.6 Adc, R_{B2} = 1.6 Ω)	t_d	—	20	100*	ns
Rise Time			t_r	—	200	500*	
Storage Time			t_s	—	1200	3000*	
Fall Time			t_f	—	200	250*	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	650	—	
Fall Time			t_f	—	80	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	800	1500*	ns
Fall Time			t_{fi}	—	50	150*	
Crossover Time			t_c	—	90	200*	
Storage Time		(T_C = 150°C)	t_{sv}	—	1050	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.
(2) $f_T = |h_{fe}| \cdot f_{test}$
*Indicates JEDEC Registered Limit

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

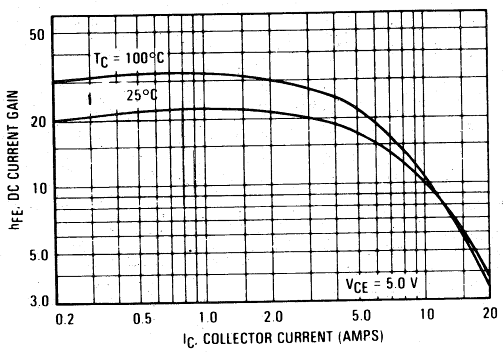


FIGURE 2 — COLLECTOR SATURATION REGION

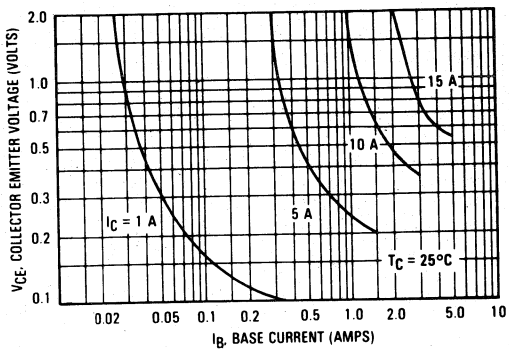


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

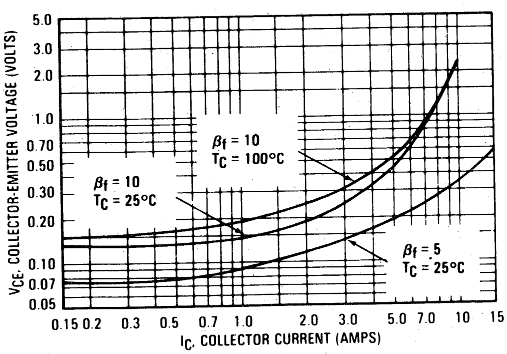


FIGURE 4 — BASE-EMITTER VOLTAGE

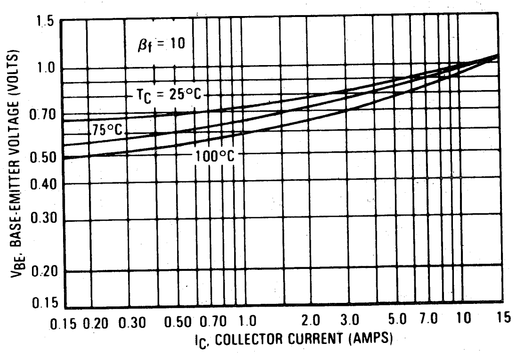


FIGURE 5 — COLLECTOR CUTOFF REGION

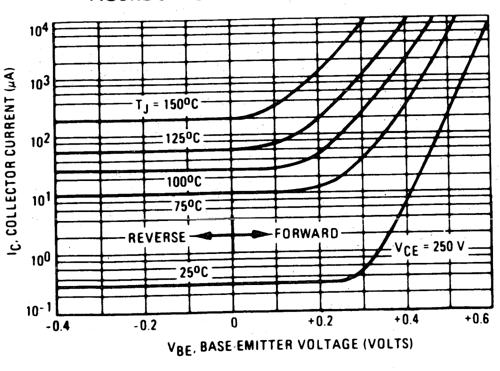
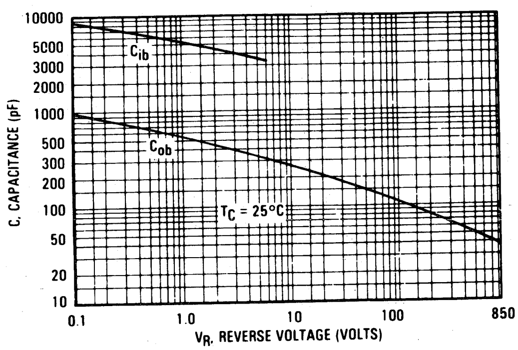


FIGURE 6 — CAPACITANCE



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TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

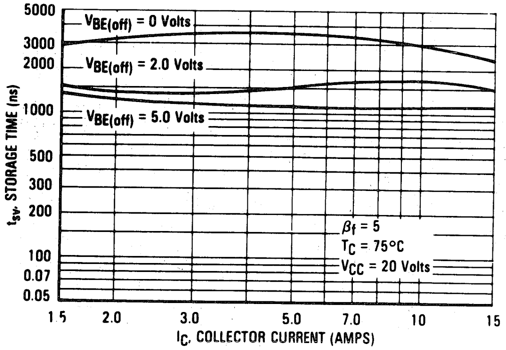

FIGURE 8 — STORAGE TIME

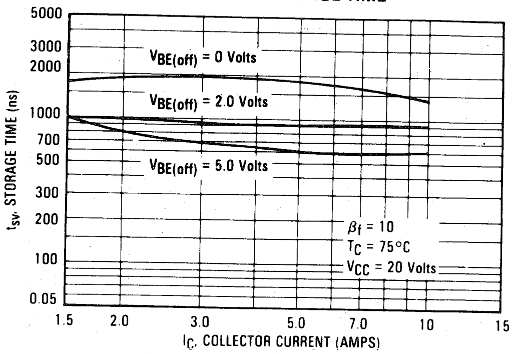

FIGURE 9 — COLLECTOR CURRENT FALL TIME

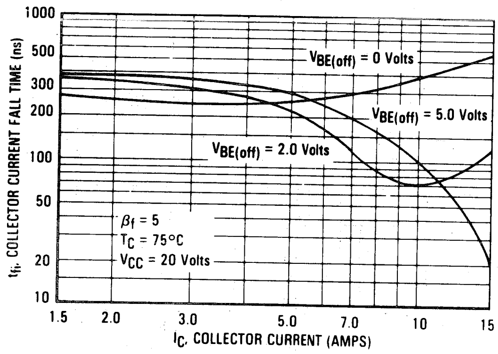

FIGURE 10 — COLLECTOR CURRENT FALL TIME

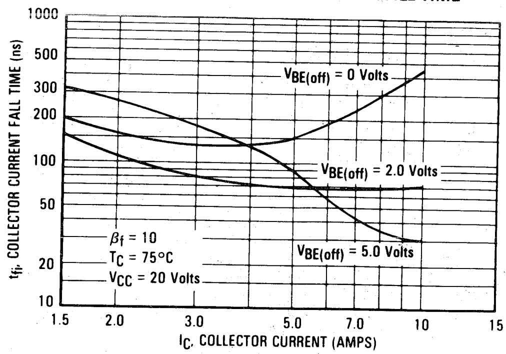

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FIGURE 11 — CROSSOVER TIME

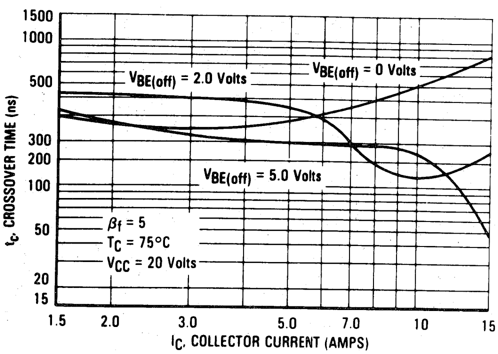


FIGURE 12 — CROSSOVER TIME

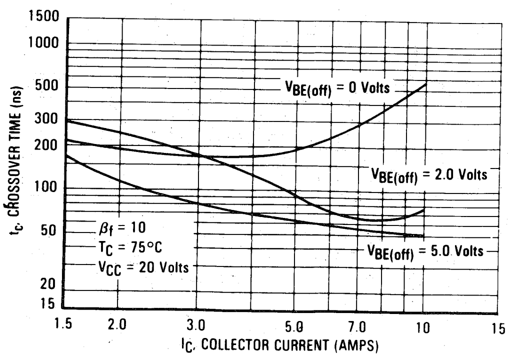


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

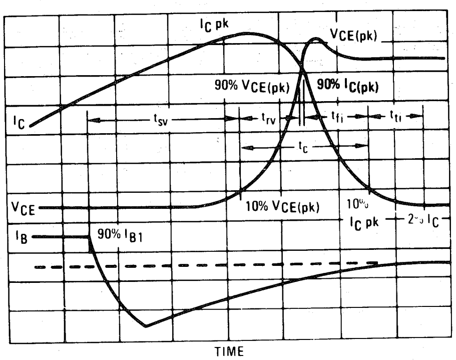
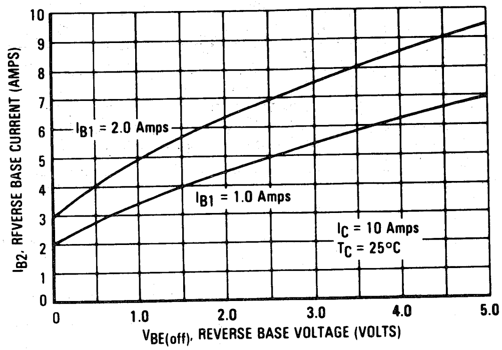


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

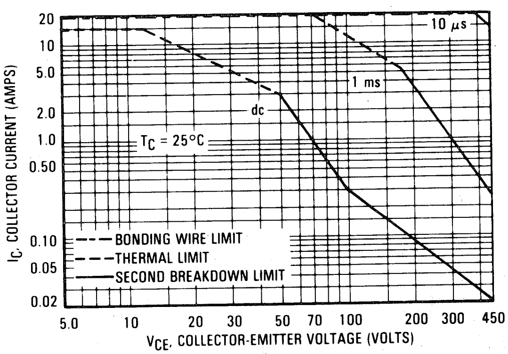
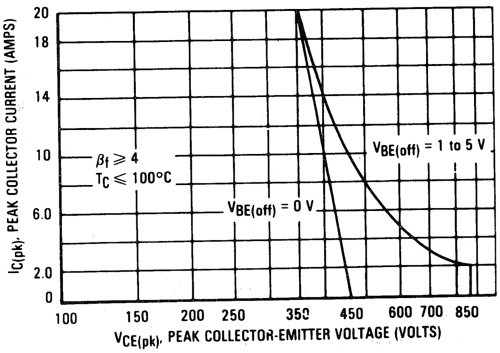


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

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$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

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FIGURE 17 — THERMAL RESPONSE

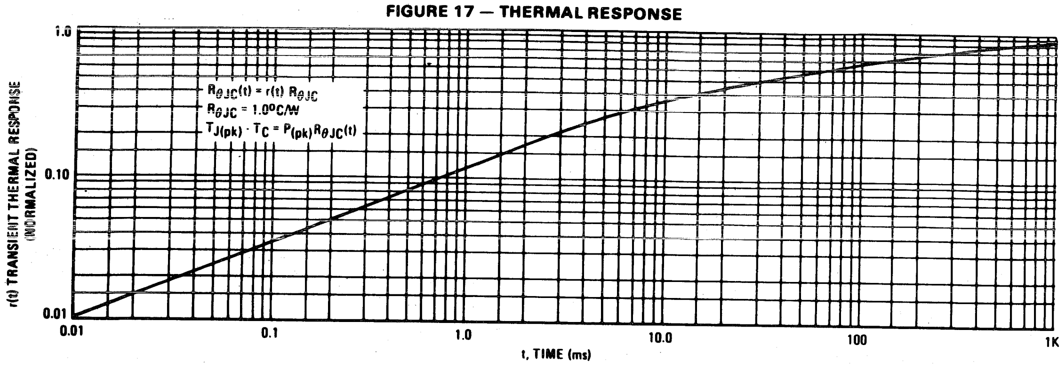


FIGURE 18 — POWER DERATING

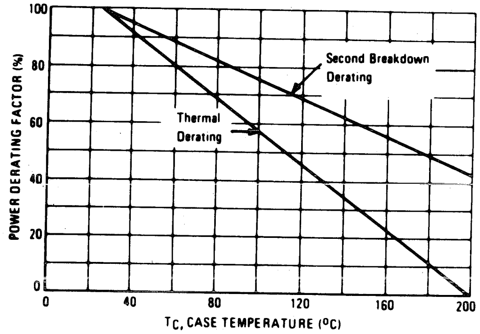
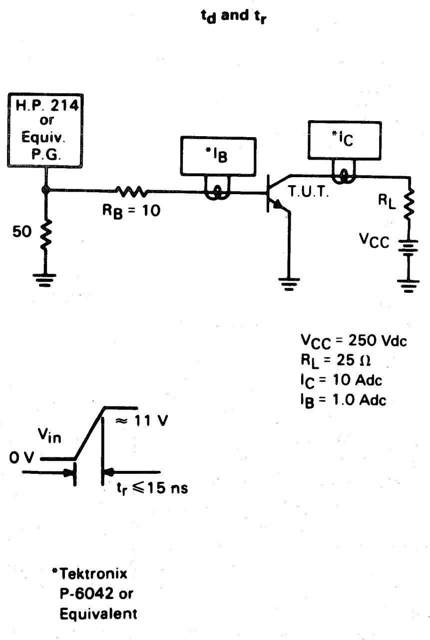
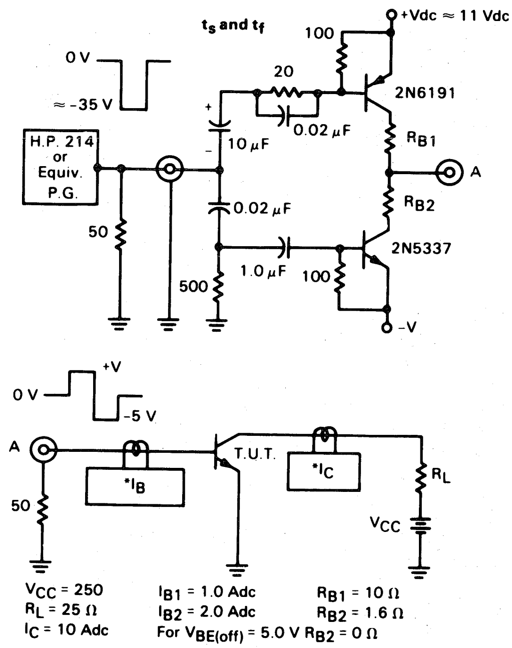


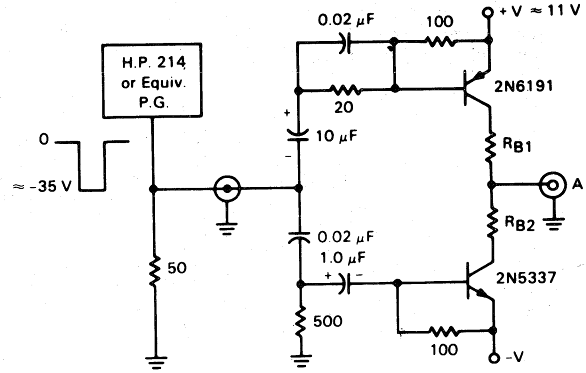
TABLE 1 — RESISTIVE LOAD SWITCHING

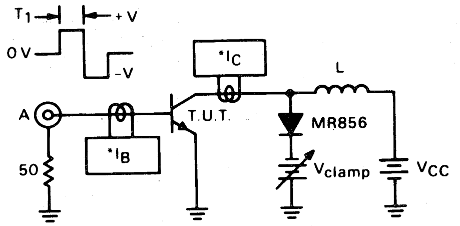


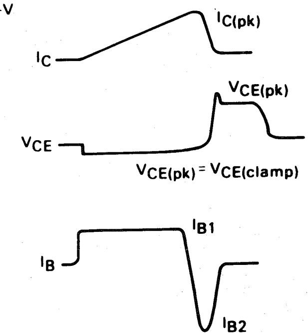


*Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING







$T_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

*Tektronix
P-6042 or
Equivalent

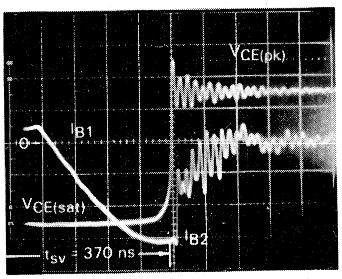
Scope - Tektronix
7403 or
Equivalent

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

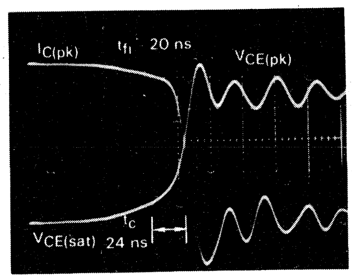
t_{sv}

$I_{C(pk)}$ = 10 Amps
I_{B1} = 1.0 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base = 100 ns/cm



t_{fi}, t_c

$I_{C(pk)}$ = 10 Amps
I_{B1} = 1.0 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base = 20 ns/cm



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6837

Designer's Data Sheet

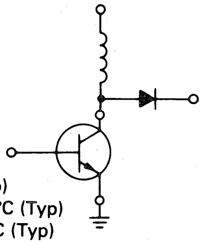
20 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
250 WATTS

SWITCHMODE III SERIES
ULTRA-FAST NPN SILICON POWER TRANSISTORS

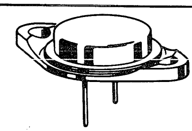
This transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.



Typical Applications:
- Switching Regulators
- Inverters
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  - 30 ns Inductive Fall Time — 75°C (Typ)
  - 40 ns Inductive Crossover Time — 75°C (Typ)
  - 800 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range −65 to +200°C
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



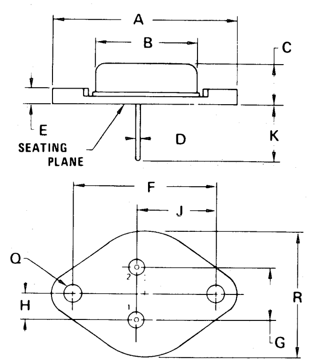
MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage*	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage*	V_{CEV}	850	Vdc
Emitter Base Voltage*	V_{EB}	6.0	Vdc
Collector Current — Continuous* — Peak (1)	I_C I_{CM}	20 30	Adc
Base Current — Continuous* — Peak (1)	I_B I_{BM}	15 20	Adc
Total Power Dissipation @ T_C = 25°C* @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43	Watts W/°C
Operating and Storage Junction* Temperature Range	T_J, T_{stg}	−65 to +200	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering* Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
*Indicate JEDEC Registered Data



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-204AE (Type) Modified TO-3

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.25*	mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5*	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0*	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.2 Adc)	$V_{CE(sat)}$	—	—	1.5	Vdc
(I_C = 15 Adc, I_B = 2.0 Adc)		—	—	3.0*	
(I_C = 15 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	—	3.0*	
Base-Emitter Saturation Voltage (I_C = 15 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	—	—	1.5*	Vdc
(I_C = 15 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	—	1.5	
DC Current Gain (I_C = 15 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	7.5*	—	30*	—
(I_C = 20 Adc, V_{CE} = 5.0 Vdc)		5.0	—	—	
DYNAMIC CHARACTERISTICS (2)					
Current Gain — Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.25 Adc, f_{test} = 10 MHz)	f_T	10*	—	75*	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	100*	—	500*	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 15 Adc, V_{CC} = 250 Vdc, I_{B1} = 2.0 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I_{B2} = 4.0 Adc, R_{B2} = 1.6 Ω)	t_d	—	20	100*	ns
Rise Time			t_r	—	200	500*	
Storage Time			t_s	—	1200	2700*	
Fall Time			t_f	—	200	350*	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	650	—	
Fall Time			t_f	—	80	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 15 Adc, I_{B1} = 2.0 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	800	2700*	ns
Fall Time			t_{fi}	—	50	200*	
Crossover Time			t_c	—	90	250*	
Storage Time		(T_C = 150°C)	t_{sv}	—	1050	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: PW — 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{FE}|\, f_{test}$
*Indicates JEDEC Registered Limit

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TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

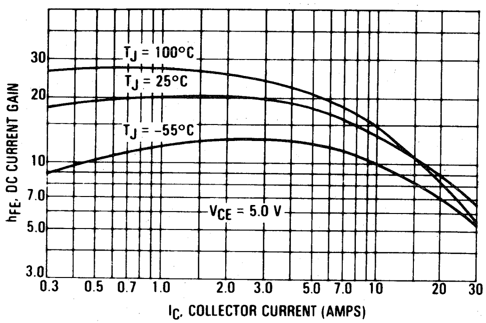


FIGURE 2 — COLLECTOR SATURATION REGION

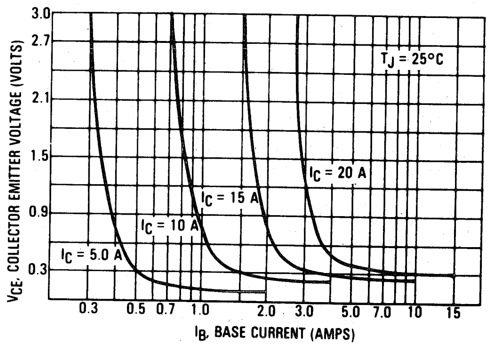


FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION

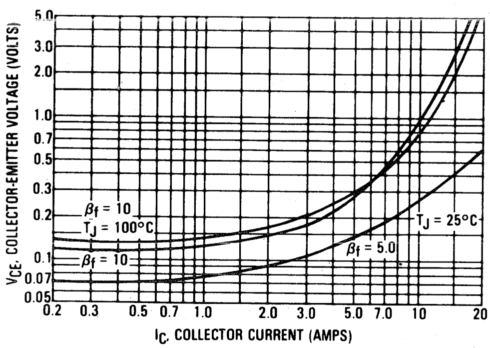


FIGURE 4 — BASE-EMITTER VOLTAGE

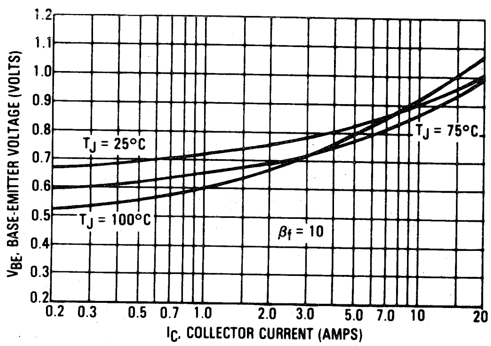


FIGURE 5 — COLLECTOR CUTOFF REGION

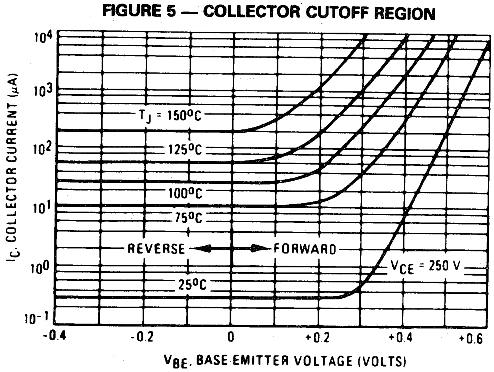
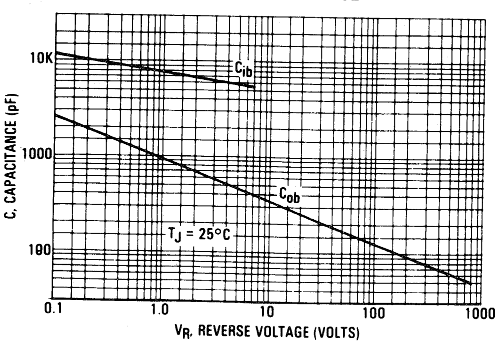


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

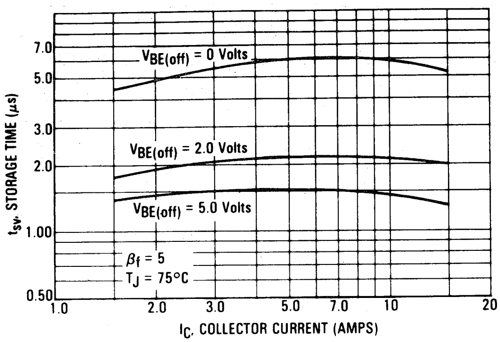


FIGURE 8 — STORAGE TIME

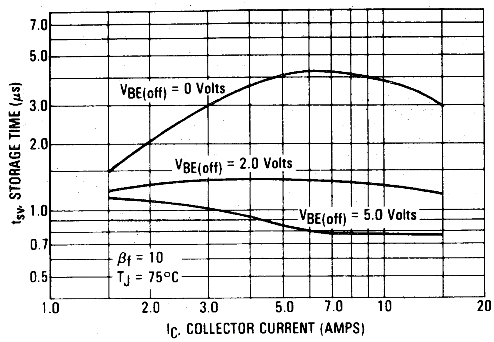


FIGURE 9 — COLLECTOR CURRENT FALL TIME

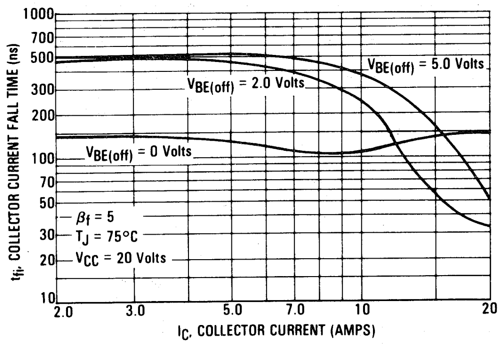


FIGURE 10 — COLLECTOR CURRENT FALL TIME

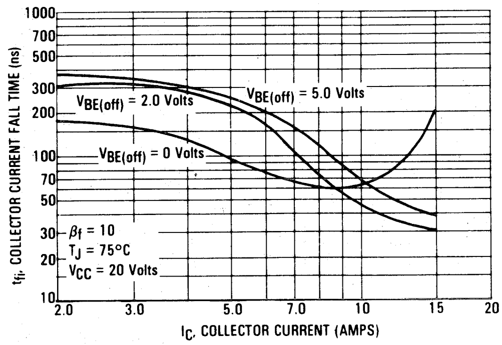


FIGURE 11 — CROSSOVER TIME

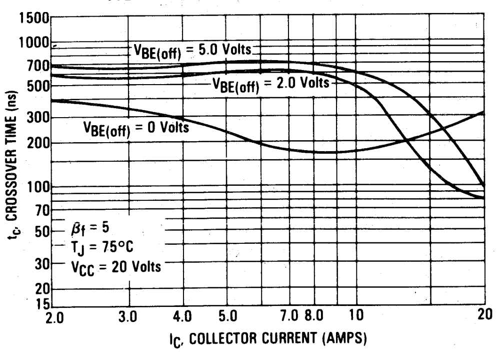


FIGURE 12 — CROSSOVER TIME

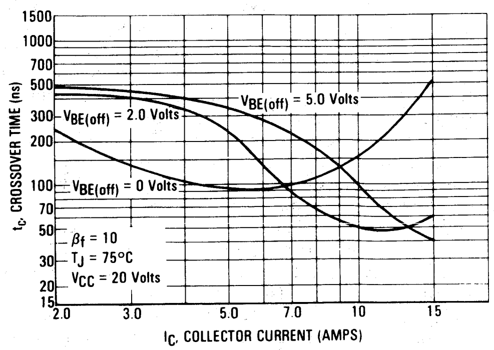


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FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

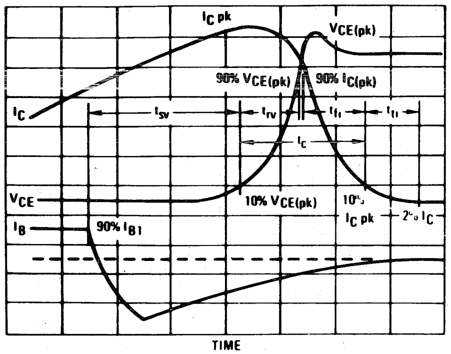
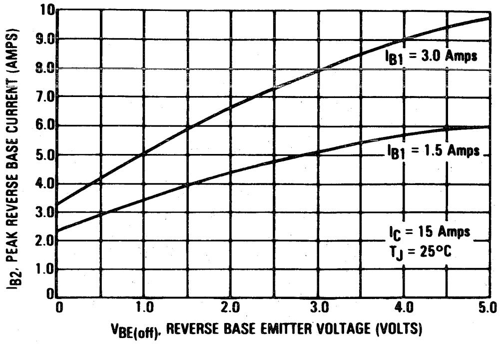


FIGURE 14 — REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

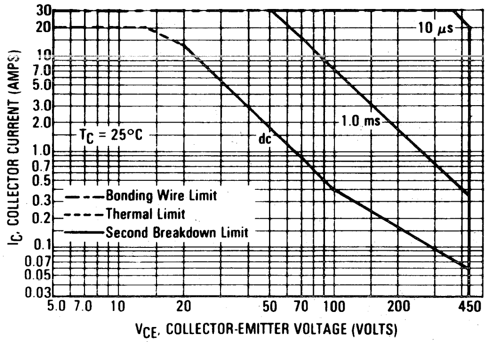
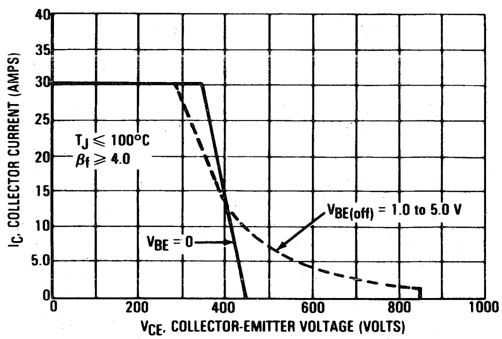


FIGURE 16 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

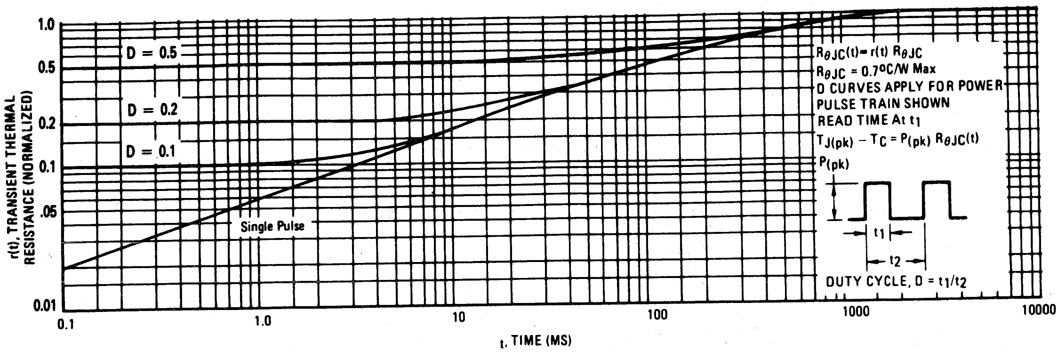


FIGURE 18 — POWER DERATING

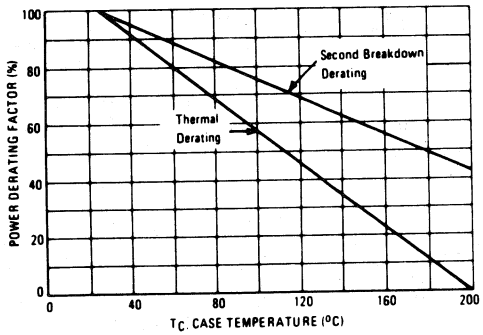
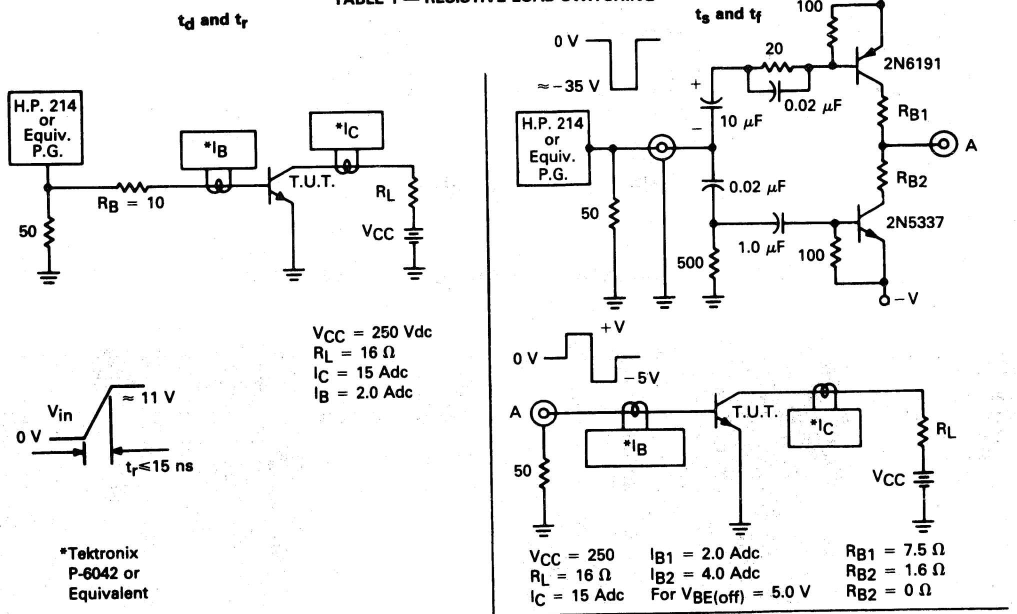


TABLE 1 — RESISTIVE LOAD SWITCHING



*Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

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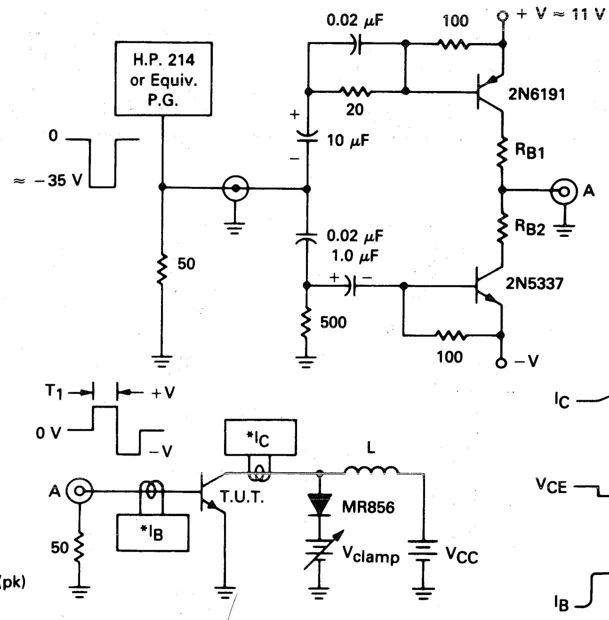
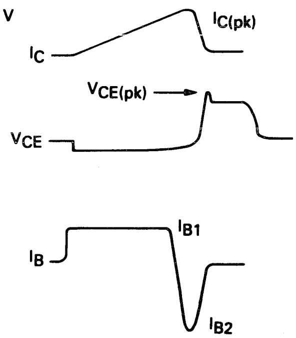
TABLE 2 — INDUCTIVE LOAD SWITCHING





$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
$L = 10$ mH
$R_{B2} = \infty$
$V_{CC} = 20$ Volts

*Tektronix
P-6042 or
Equivalent

Inductive Switching
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

Scope — Tektronix
7403 or
Equivalent

RBSOA
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

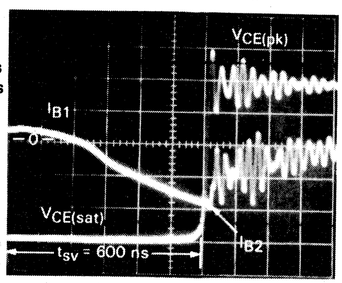
Note: Adjust — V to obtain desired $V_{BE(off)}$ at Point A.

3

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

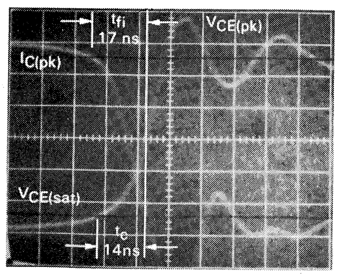
$I_{C(pk)} = 15$ A
$I_{B1} = 2.0$ A
$V_{BE(off)} = 5.0$ Volts
$V_{CE(pk)} = 400$ Volts
$T_C = 25°C$
Time Base = 200 ns/cm

t_{sv}



$I_{C(pk)} = 15$ A
$I_{B1} = 2.0$ A
$V_{BE(off)} = 5.0$ Volts
$V_{CE(pk)} = 400$ Volts
$T_C = 25°C$
Time Base = 200 ns/cm

t_{fi}, t_c



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD135,-6,-10,-16
BD137,-6,-10,-16
BD139,-6,-10,-16

PLASTIC MEDIUM POWER SILICON NPN TRANSISTOR

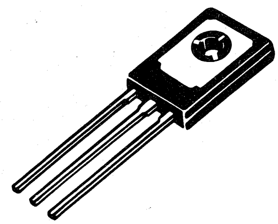
. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- Available in H_{FE} groups -6, -10, -16
- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 135, 137, 139 are complementary with BD 136, 138, 140

1.5 AMPERE POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
10 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 135 BD 137 BD 139	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 135 BD 137 BD 139	45 60 100	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		12.5 100	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to +150	°C

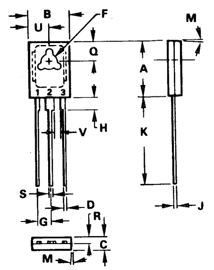
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)	BV_{CEO}*	BD 135 BD 137 BD 139	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125° C)	I_{CBO}		— — —	0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	10	μAdc
DC Current Gain (I_C = 0.005A, V_{CE} = 2 V) (I_C = 0.15A, V_{CE} = 2 V) (I_C = 0.5 A V_{CE} = 2 V)	h_{FE}*		25 40 25	— 250 —	—
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1	Vdc

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

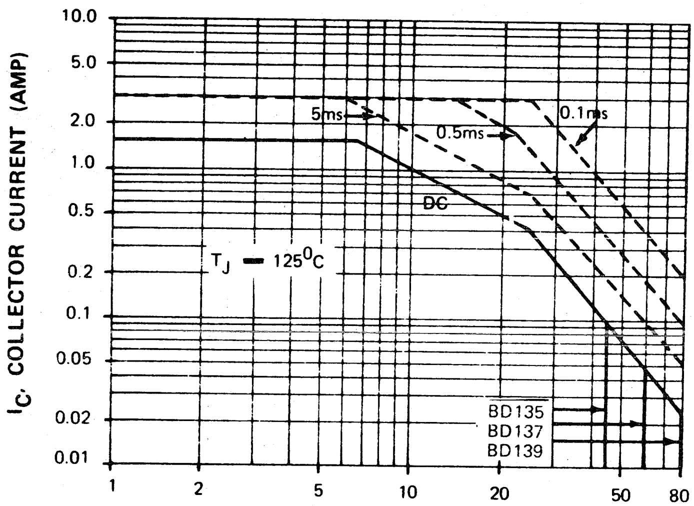
STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



Available in H_{FE} groups
(At I_C = 0.15 A, V_{CE} = 2 V) H_{FE} group:

	Min.	Max.
-6	40	100
-10	63	160
-16	100	250

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD136,-6,-10,-16
BD138,-6,-10,-16
BD140,-6,-10,-16

PLASTIC MEDIUM POWER
SILICON PNP TRANSISTOR

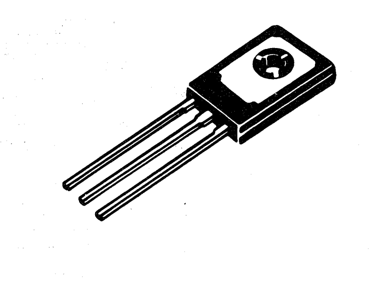
. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- Available in H_{FE} groups -6, -10, -16
- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 136, 138, 140 are complementary with BD 135, 137, 139

1.5 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
10 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 136 BD 138 BD 140	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 136 BD 138 BD 140	45 60 100	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		12.5 100	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to +150	°C

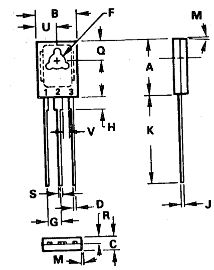
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)	BV_{CEO}*	BD 136 BD 138 BD 140	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125° C)	I_{CBO}		— — —	0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	10	μAdc
DC Current Gain (I_C = 0.005A, V_{CE} = 2 V) (I_C = 0.15A, V_{CE} = 2 V) (I_C = 0.5A, V_{CE} = 2 V)	h_{FE}*		25 40 25	— 250 —	—
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1	Vdc

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

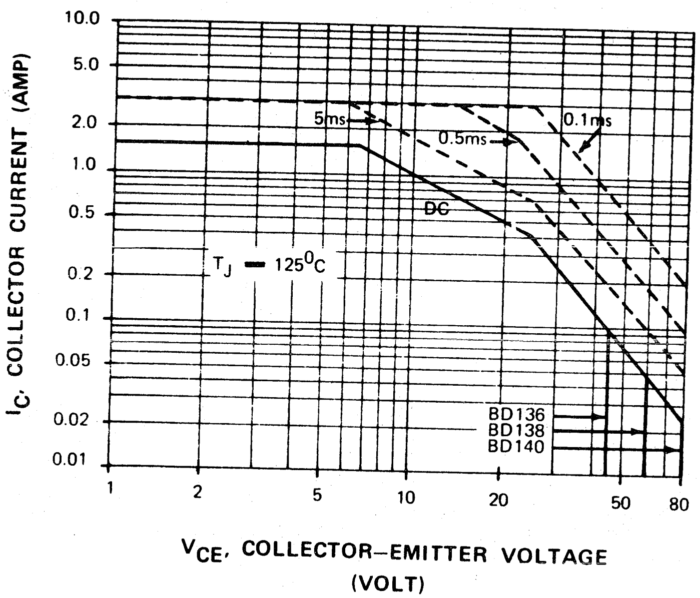
STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



Available in H_{FE} groups		Min.	Max.
(at I_C = 0.15 A, V_{CE} 2 V) H_{FE} group:	-6	40	100
	-10	63	160
	-16	100	250

3

BD157
BD158
BD159

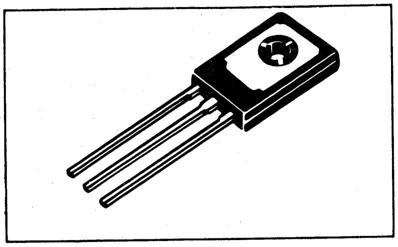
PLASTIC MEDIUM POWER NPN SILICON TRANSISTOR

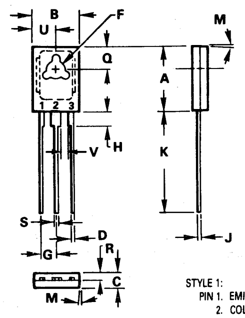
. . . designed for power output stages for television, radio, phonograph and other consumer product applications.

- Suitable for Transformerless, Line-Operated Equipment
- Thermopad† Construction Provides High Power Dissipation Rating for High Reliability

**0.5 AMPERE
POWER TRANSISTOR
NPN SILICON**

250-300-350 VOLTS
20 WATTS





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

**CASE 77-05
TO-126**

*MAXIMUM RATINGS

Rating	Symbol	BD 157	BD 158	BD 159	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector-Base Voltage	V_{CB}	275	325	375	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 0.5 → ← 1.0 →			Adc
Base Current	I_B	← 0.25 →			Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	← 20 → 0.16			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($I_C = 1.0$ mAdc, $I_B = 0$)	BV_{CEO}	BD 157 BD 158 BD 159	250 300 350	—	Vdc
Collector Cutoff Current (At rated voltage)	I_{CBO}		—	100	μAdc
Emitter Cutoff Current ($V_{EB} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	100	μAdc
ON CHARACTERISTICS					
DC Current Gain ($I_C = 50$ mAdc, $V_{CE} = 10$ Vdc)	h_{FE}		30	240	—

3

FIGURE 1 – POWER TEMPERATURE DERATING CURVE

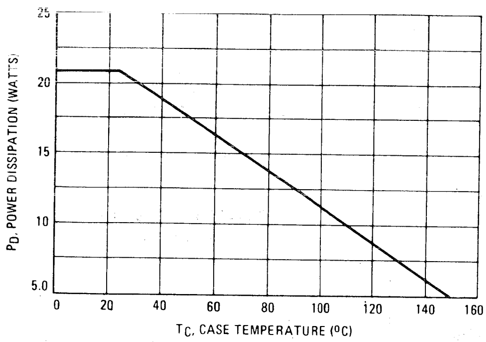


FIGURE 2 – "ON" VOLTAGES

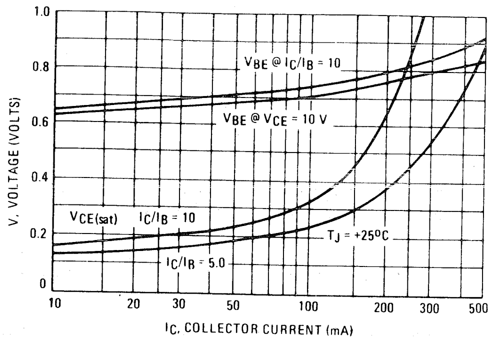
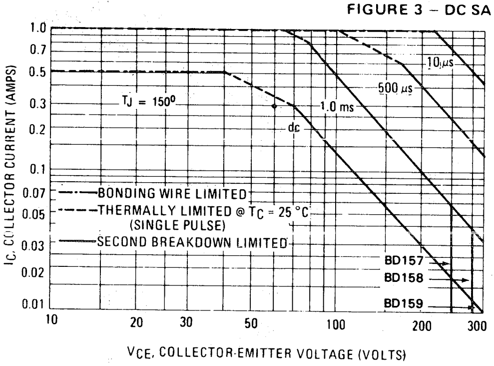


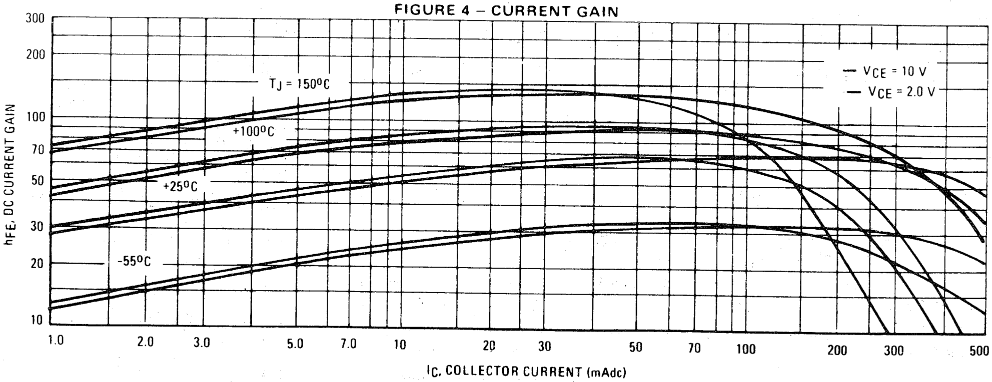
FIGURE 3 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

3

FIGURE 4 – CURRENT GAIN



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD165
BD167
BD169

PLASTIC MEDIUM POWER SILICON NPN TRANSISTOR

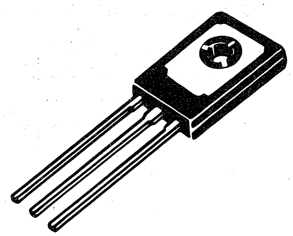
. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 165, 167, 169 are complementary with BD 166, 168, 170

1.5 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
20 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 165 BD 167 BD 169	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 165 BD 167 BD 169	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 8	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		20 160	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150	°C

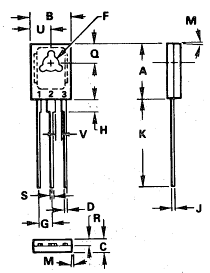
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 165 BD 167 BD 169	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 165 BD 167 BD 169	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A, V_{CE} = 2 V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	0.95	Vdc
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 2 Vdc, f = 1.0 MHz)	f_T		6.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

3

FIGURE 1 – P_D–T_C DERATING CURVE

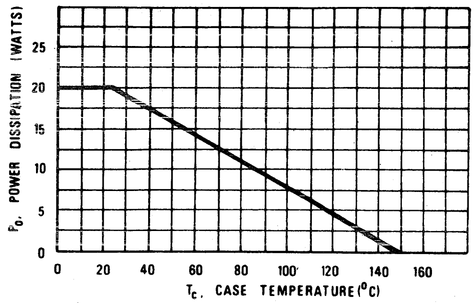
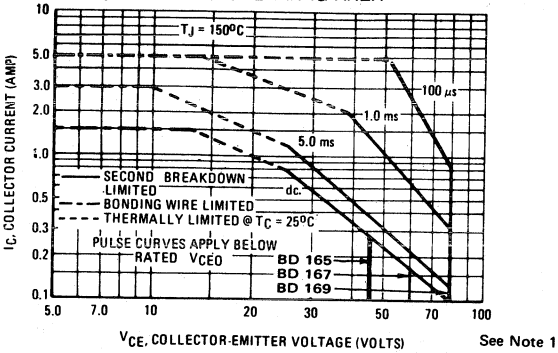


FIGURE 2 – SAFE OPERATING AREA



See Note 1

FIGURE 3 – COLLECTOR SATURATION REGION

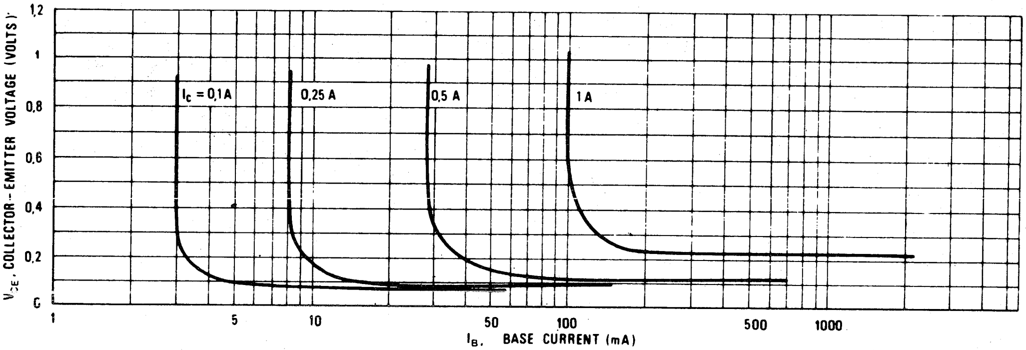


FIGURE 4 – CURRENT GAIN

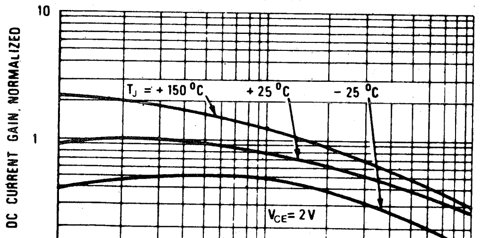
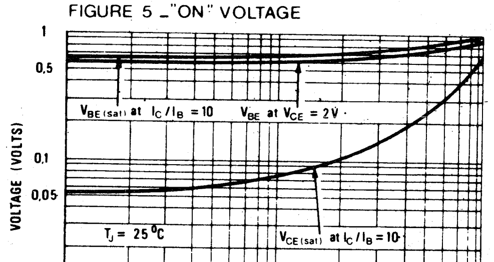


FIGURE 5 – "ON" VOLTAGE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD166
BD168
BD170

PLASTIC MEDIUM POWER SILICON PNP TRANSISTOR

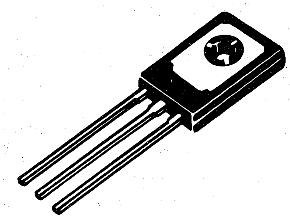
. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 166, 168, 170 are complementary with BD 165, 167, 169

1.5 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
20 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 166 BD 168 BD 170	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 166 BD 168 BD 170	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		20 160	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–65 to +150	°C

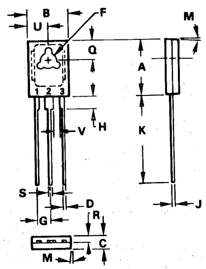
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}	BD 166 BD 168 BD 170	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 166 BD 168 BD 170	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A, V_{CE} = 2 V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$		—	0.95	Vdc
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 2 Vdc, f = 1.0 MHz)	f_T		6.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

FIGURE 1 – P_D-T_C DERATING CURVE

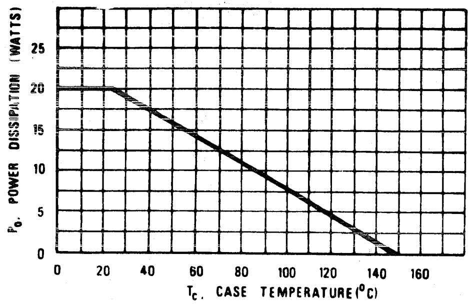
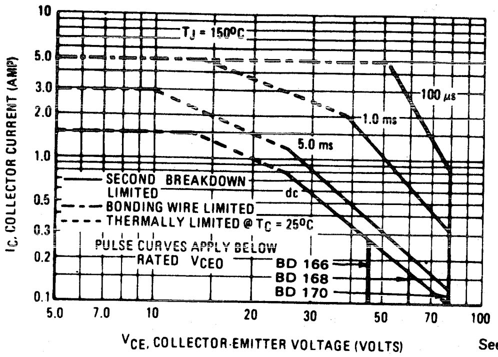


FIGURE 2 – SAFE OPERATING AREA



See Note

FIGURE 3 – COLLECTOR SATURATION REGION

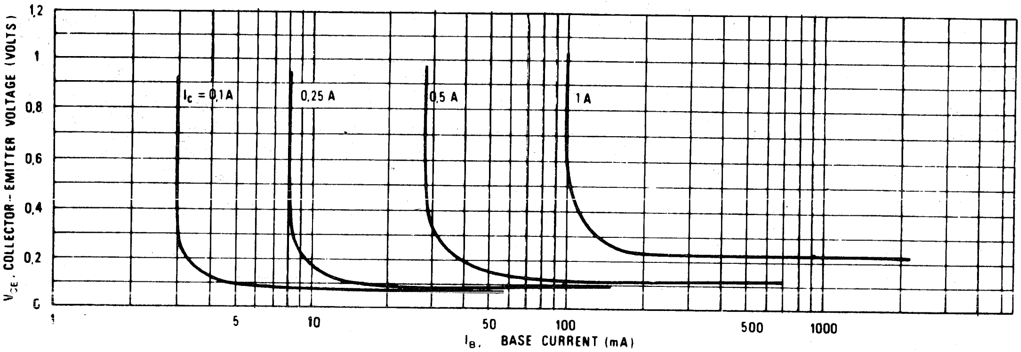


FIGURE 4 – CURRENT GAIN

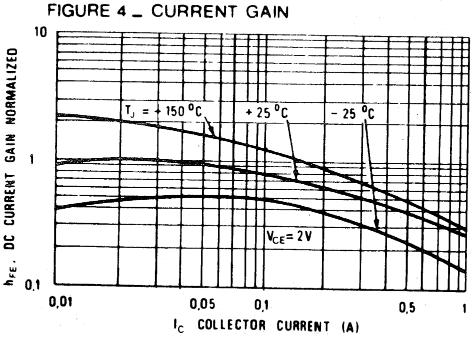
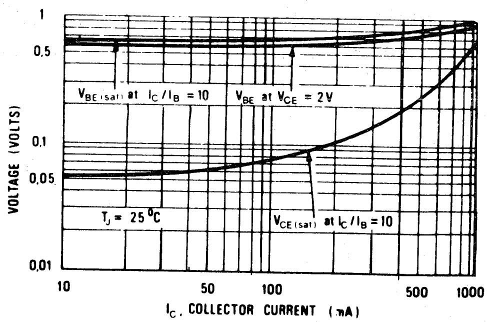


FIGURE 5 – "ON" VOLTAGE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD175,-6,-10,-16
BD177,-6,-10
BD179,-6,-10

PLASTIC MEDIUM POWER SILICON NPN TRANSISTOR

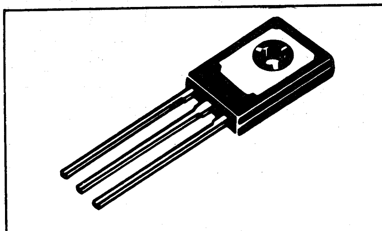
. . . designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 175, 177, 179 are complementary with BD 176, 178, 180
- Available in H_{FE} groups -6, -10, -16

3 AMPERE POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
30 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 175 BD 177 BD 179	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 175 BD 177 BD 179	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		3.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		30 240	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—65 to +150	°C

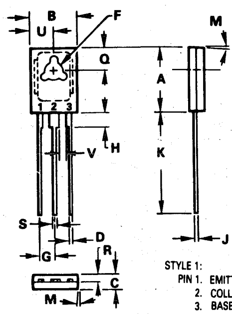
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		4.16	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 175 BD 177 BD 179	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 175 BD 177 BD 179	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) group -6 group -10 group -16 (I_C = 1 A, V_{CE} = 2 V)	h_{FE}*		40 63 100 15	100 160 250	
Collector-Emitter Saturation Voltage* (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$*		—	0.8	Vdc
Base-Emitter On Voltage* (I_C = 1 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.3	Vdc
Current-Gain-Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

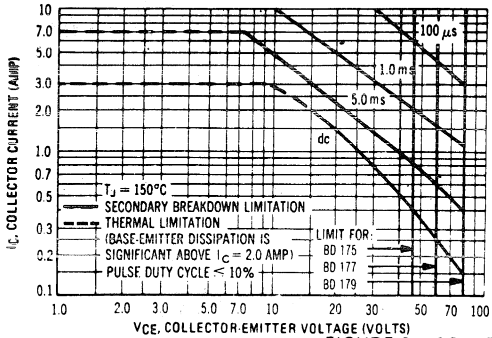
NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-126

3

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

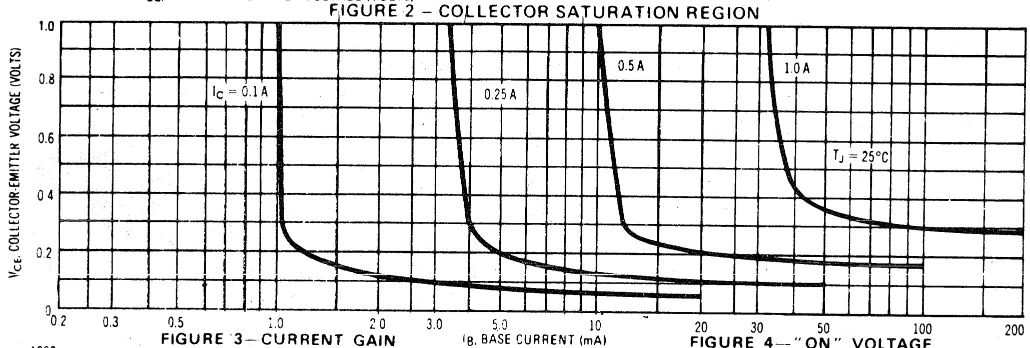


FIGURE 3 — CURRENT GAIN

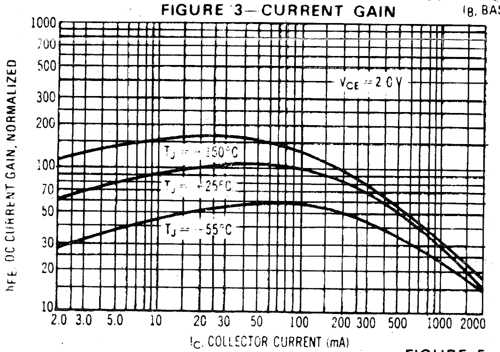


FIGURE 4 — "ON" VOLTAGE

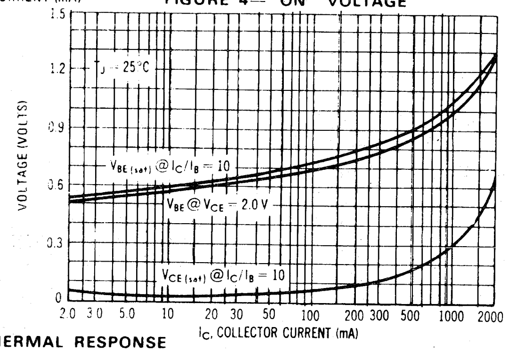
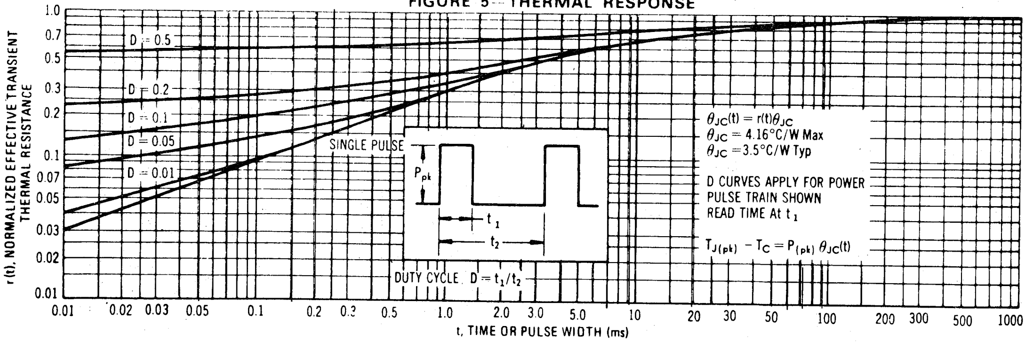


FIGURE 5 — THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD176,-6,-10,-16
BD178,-6,-10
BD180,-6,-10

PLASTIC MEDIUM POWER SILICON PNP TRANSISTOR

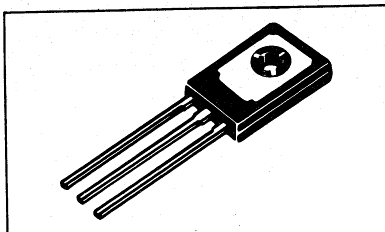
. . . designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—$h_{FE} = 40$ (Min) @ $I_C = 0.15$ Adc
- BD 176, 178, 180 are complementary with BD 175, 177, 179
- Available in H_{FE} groups -6, -10, -16

3 AMPERE POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
30 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 176 BD 178 BD 180	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 176 BD 178 BD 180	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		3.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation $T_C = 25°C$ Derate above 25°C	P_D		30 240	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–65 to +150	°C

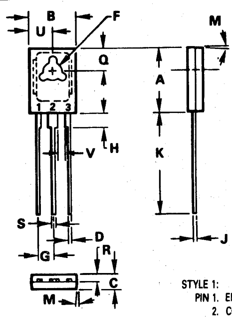
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		4.16	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$)	BV_{CEO}*	BD 176 BD 178 BD 180	45 60 80	— — —	Vdc
Collector Cutoff Current ($V_{CB} = 45$ Vdc, $I_E = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	I_{CBO}	BD 176 BD 178 BD 180	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mAdc
DC Current Gain ($I_C = 0.15$ A, $V_{CE} = 2$ V) group -6, -10, -16 ($I_C = 1$ A, $V_{CE} = 2$ V)	h_{FE}*		40 63 100 15	100 160 250	
Collector-Emitter Saturation Voltage* ($I_C = 1$ Adc, $I_B = 0.1$ Adc)	$V_{CE(sat)}$*		—	0.8	Vdc
Base-Emitter On Voltage* ($I_C = 1$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$*		—	1.3	Vdc
Current-Gain-Bandwidth Product ($I_C = 250$ mAdc, $V_{CE} = 10$ Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

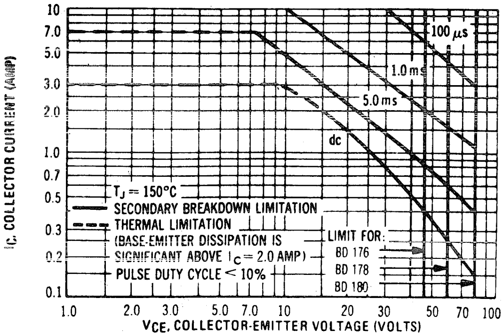
NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-126

3

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

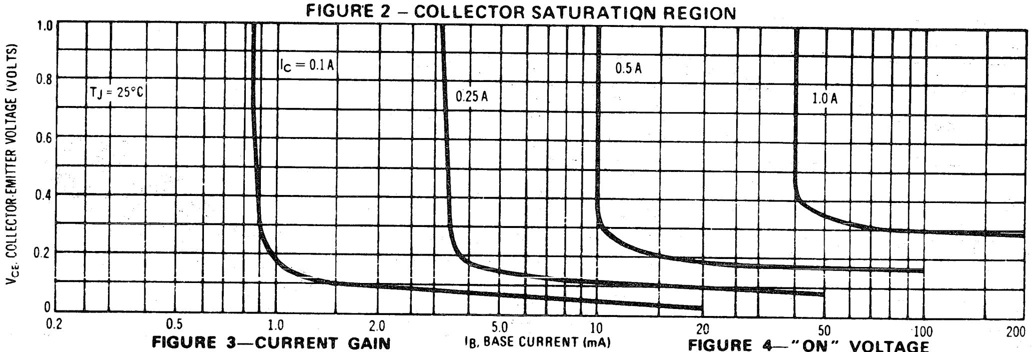


FIGURE 3—CURRENT GAIN

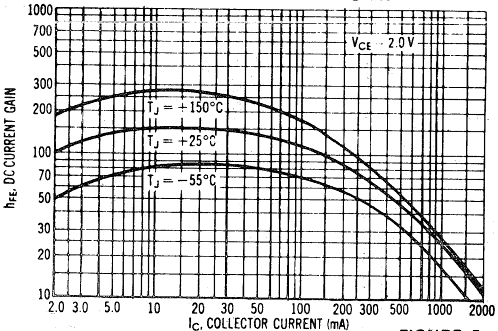


FIGURE 4—"ON" VOLTAGE

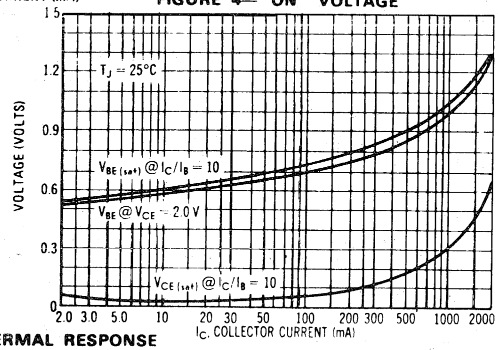
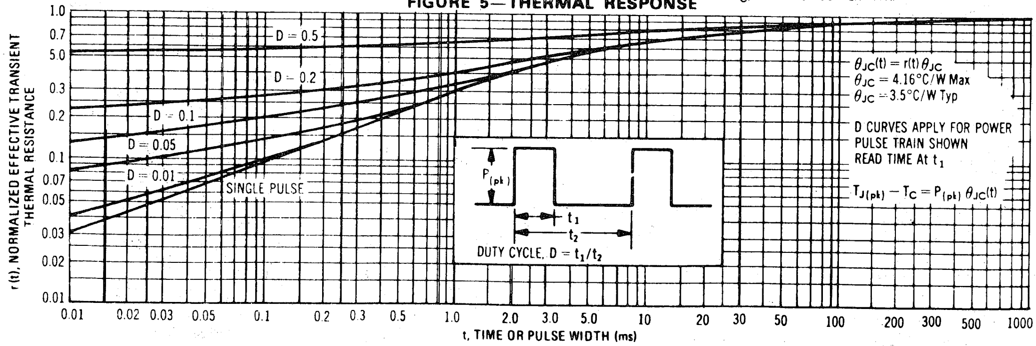


FIGURE 5—THERMAL RESPONSE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD185
BD187
BD189

PLASTIC MEDIUM POWER SILICON NPN TRANSISTOR

. . . designed for use in 5 to 10 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

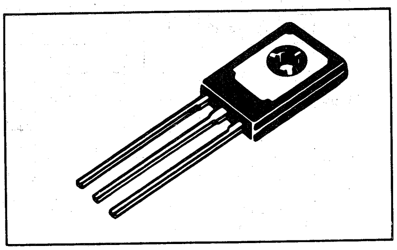
- DC Current Gain—$h_{FE} = 40$ (Min) @ $I_C = 0.5$ Adc
- BD 185, 187, 189 are complementary with BD 186, 188, 190

4 AMPERE
POWER TRANSISTOR

NPN SILICON

30, 45, 60 VOLTS
40 WATTS

MARCH 1970—E-003



MAXIMUM RANGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 185 BD 187 BD 189	30 45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 185 BD 187 BD 189	40 55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		4.0	Adc
Base Current	I_B		2.0	Adc
Total Device Dissipation $T_C = 25°C$ Derate above 25°C	P_D		40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—65 to +150	°C

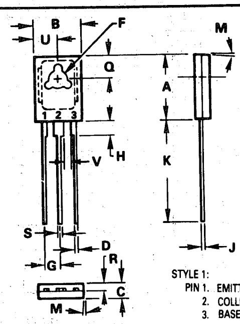
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		3.12	° C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$)	BV_{CEO}*	BD 185 BD 187 BD 189	30 45 60	— — —	Vdc
Collector Cutoff Current ($V_{CB} = 40$ Vdc, $I_E = 0$) ($V_{CB} = 55$ Vdc, $I_E = 0$) ($V_{CB} = 70$ Vdc, $I_E = 0$)	I_{CBO}	BD 185 BD 187 BD 189	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mAdc
DC current Gain ($I_C = 0.5$ A, $V_{CE} = 2$ V) ($I_C = 2$A, $V_{CE} = 2$ V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* ($I_C = 2$Adc, $I_B = 0.2$ Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* ($I_C = 2$Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$*		—	1.5	Vdc
Current-Gain-Bandwidth Product ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc, f = 1.0 MHz)	f_T		2.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

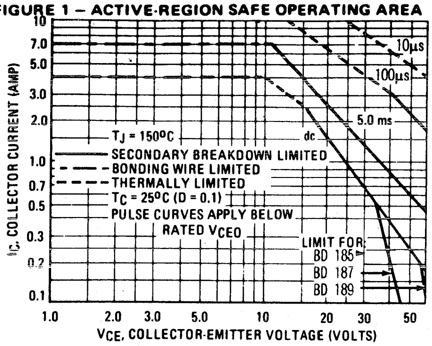
NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-126

3

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

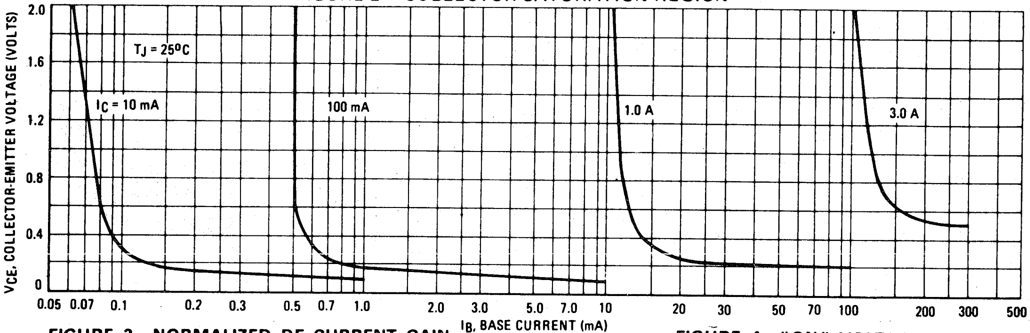


FIGURE 3—NORMALIZED DE CURRENT GAIN

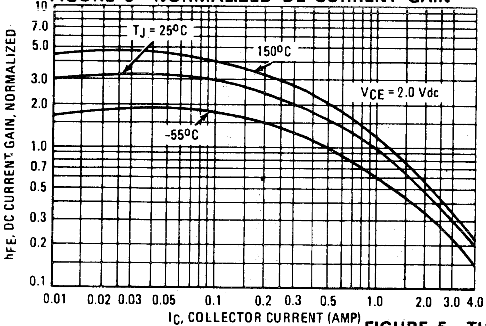


FIGURE 4—"ON" VOLTAGE

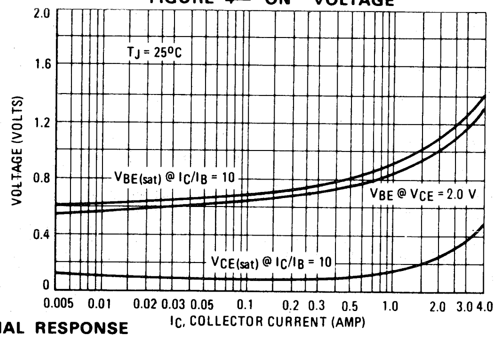
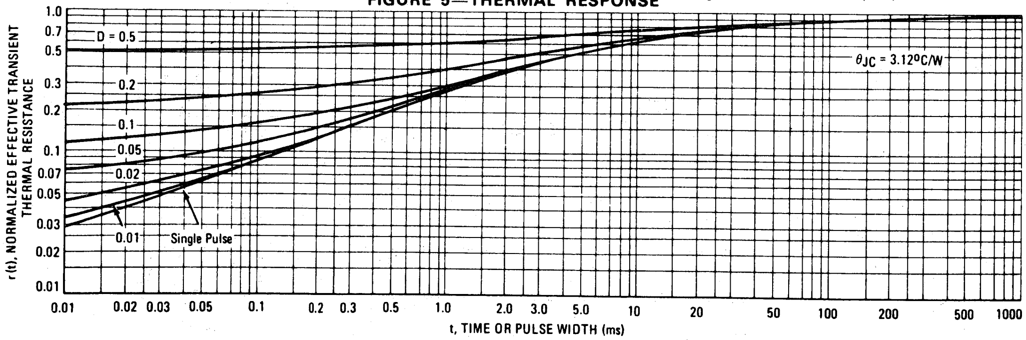


FIGURE 5—THERMAL RESPONSE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD186
BD188
BD190

PLASTIC MEDIUM POWER SILICON PNP TRANSISTOR

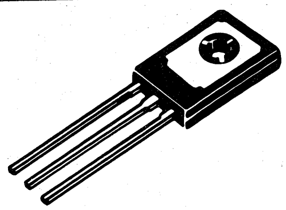
. . . designed for use in 5 to 10 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current—h_{FE} = 40 (Min) @ I_C = 0.5 Adc
- BD 186, 188, 190 are complementary with BD 185, 187, 189

4 AMPERE
POWER TRANSISTOR

PNP SILICON

30, 45, 60 VOLTS
40 WATTS



MAXIMUM RANGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 186 BD 188 BD 190	30 45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 186 BD 188 BD 190	40 55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		4.0	Adc
Base Current	I_B		2.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—65 to +150	°C

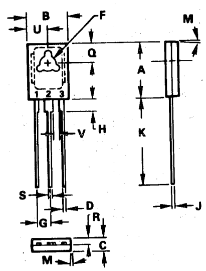
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		3.12	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 186 BD 188 BD 190	30 45 60	— — —	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	BD 186 BD 188 BD 190	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.5 A, V_{CE} = 2 V) (I_C = 2 A, V_{CE} = 2 V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.5	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		2.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs. Duty Cycle ≦ 2.0%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

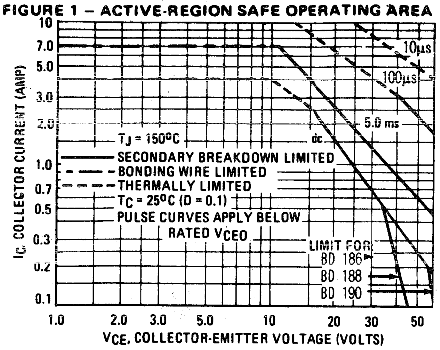
STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

3

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

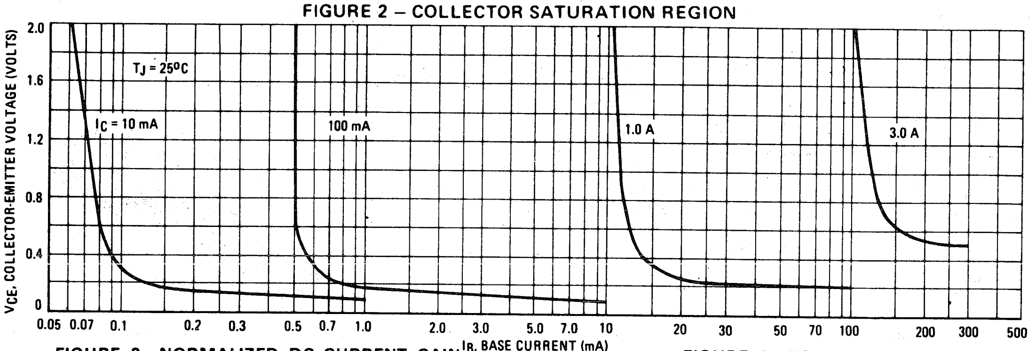


FIGURE 3—NORMALIZED DC CURRENT GAIN

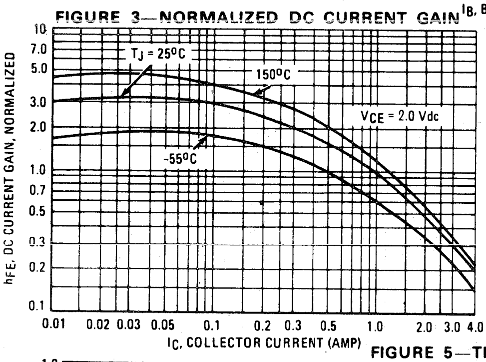


FIGURE 4—"ON" VOLTAGE

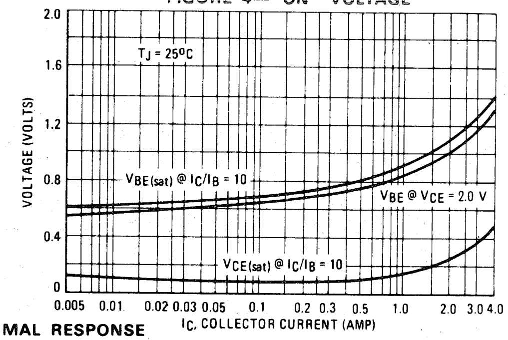
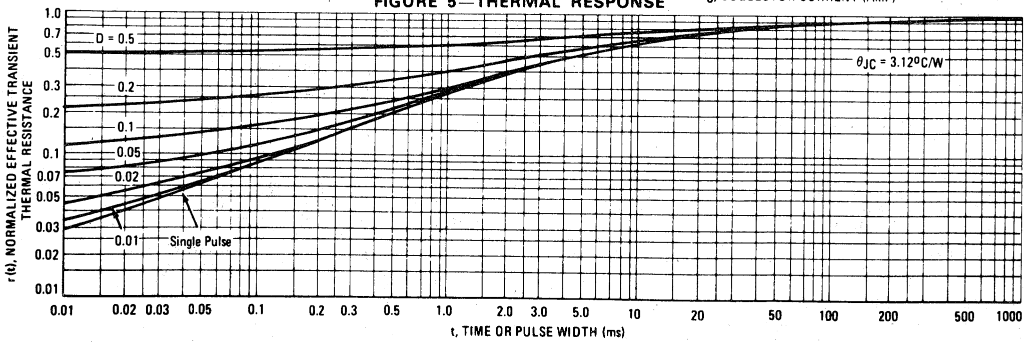


FIGURE 5—THERMAL RESPONSE



BD205
BD207

PLASTIC HIGH POWER
SILICON NPN TRANSISTOR

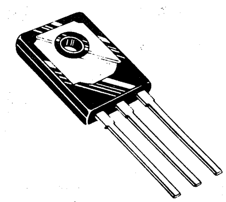
. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 30 (Min) @ I_C = 2.0 Adc
- BD 205, 207 are complementary with BD 206, 208

**10 AMPERE
POWER TRANSISTOR**

NPN SILICON

**45, 60 VOLTS
90 WATTS**

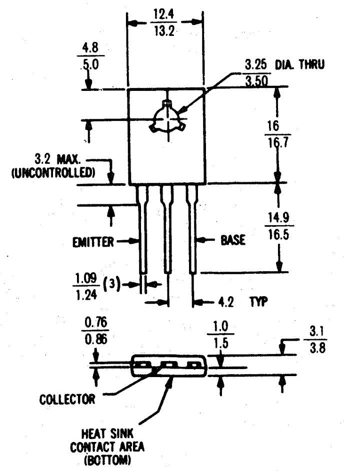


MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 205 BD 207	45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 205 BD 207	55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.39	° C/W



When mounting the device, torque not to exceed 0.09 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.
All dimensions in millimeters

CASE 90

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.2 Adc, I_B = 0)	BV_{CEO}*	BD 205 BD 207	45 60	— —	Vdc
Collector Cutoff Current (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	BD 205 BD 207	— —	1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	2.0	mAdc
DC current Gain (I_C = 2A, V_{CE} = 2 V) (I_C = 4A, V_{CE} = 2 V)	h_{FE}*		30 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$*		—	1.1	Vdc
Base-Emitter On Voltage* (I_C = 4 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		1.5	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

3

FIGURE 1 — ACTIVE REGION DC SAFE OPERATING AREA

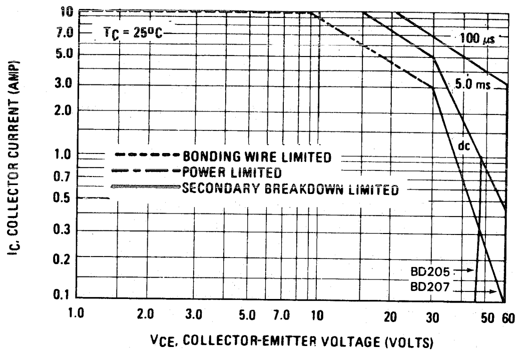


FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

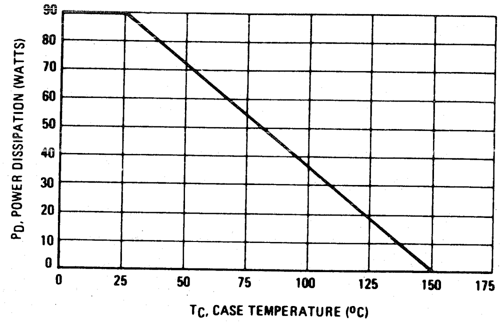


FIGURE 3 — "ON" VOLTAGES

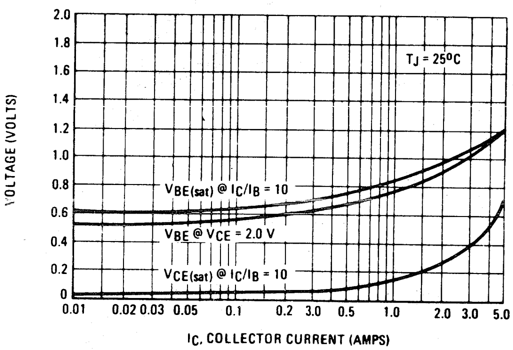


FIGURE 4 — CURRENT GAIN

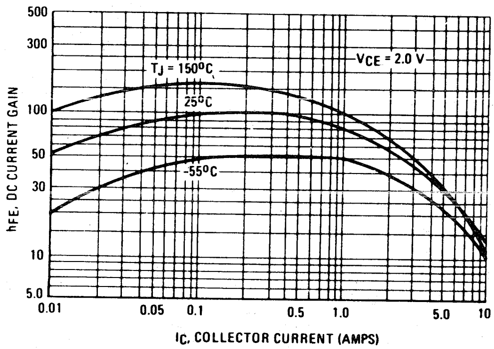


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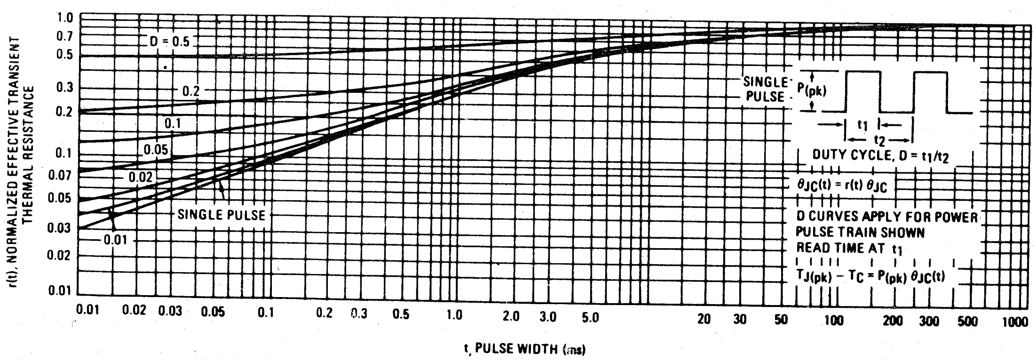
FIGURE 5 — THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD206
BD208

PLASTIC HIGH POWER SILICON PNP TRANSISTOR

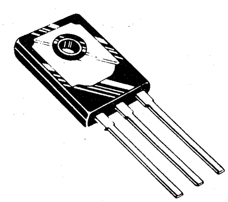
. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current—h_{FE} = 30 (Min) @ I_C = 2.0 Adc
- BD 206, 208 are complementary with BD 205, 207

10 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60 VOLTS
90 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 206 BD 208	45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 206 BD 208	55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

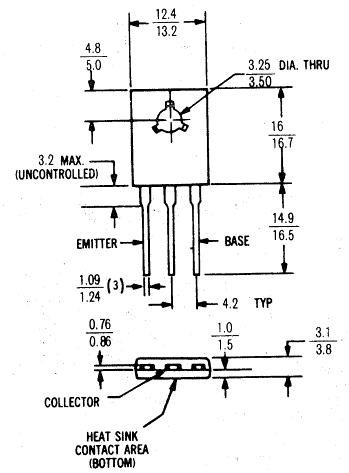
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.39	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.2 Adc, I_B = 0)	BV_{CEO}*	BD 206 BD 208	45 60	— —	Vdc
Collector Cutoff Current (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	BD 206 BD 208	— —	1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	2.0	mAdc
DC current Gain (I_C = 2A, V_{CE} = 2 V) (I_C = 4A, V_{CE} = 2 V)	h_{FE}*		30 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$*		—	1.1	Vdc
Base-Emitter On Voltage* (I_C = 4 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		1.5	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs. Duty Cycle ≦ 2.0%.



When mounting the device, torque not to exceed 0.09 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 90

3

FIGURE 1 — ACTIVE REGION DC SAFE OPERATING AREA

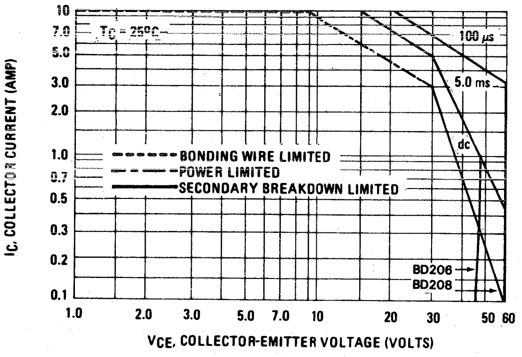


FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

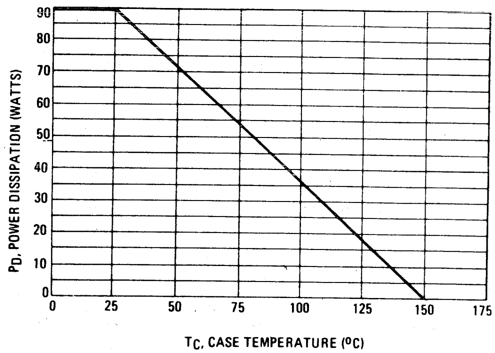


FIGURE 3 — "ON" VOLTAGES

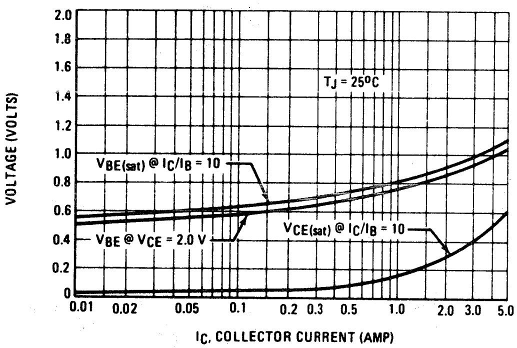


FIGURE 4 — CURRENT GAIN

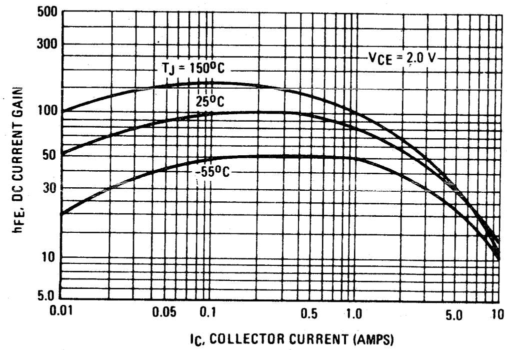
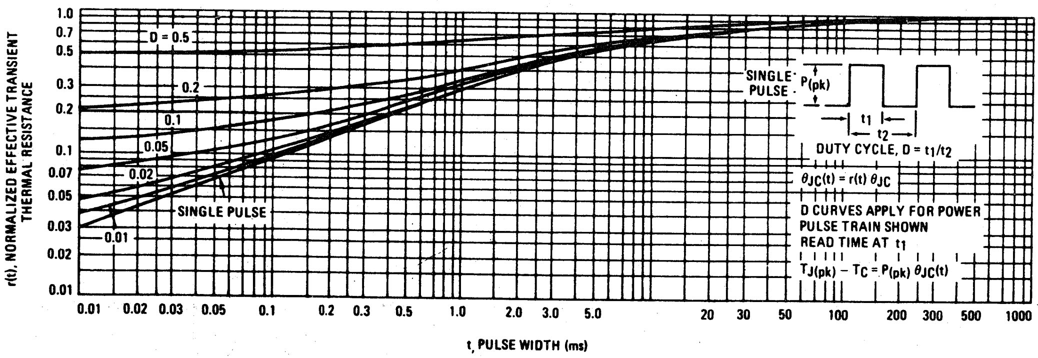


FIGURE 5 — THERMAL RESPONSE



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

BD232

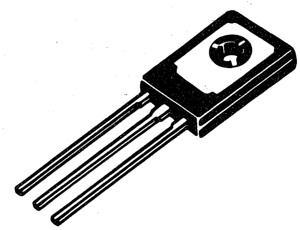
NPN SILICON MEDIUM POWER TRANSISTORS

- For Power Ouput Stages and Line Driver in Television Receivers

0.5 AMPERES

NPN SILICON POWER TRANSISTOR

300 VOLTS
20 WATTS



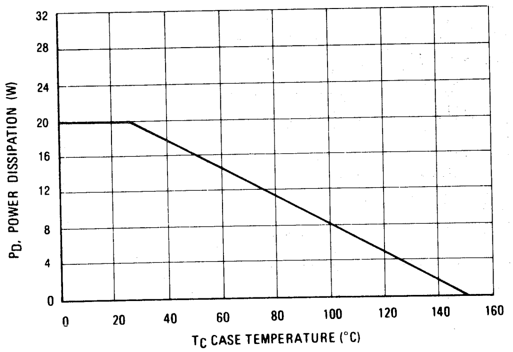
MAXIMUM RATINGS

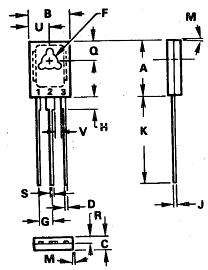
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Emitter Voltage	V_{CES}	500	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current — Continuous	I_C	0.5	Adc
Base Current	I_B	0.25	Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	20 160	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

FIGURE 1 — POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

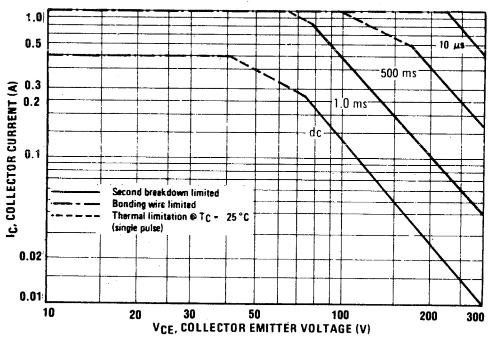
CASE 77-05
TO-126

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS (1)				
Collector-Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	–	Vdc
Collector Cutoff Current (V_{CE} = 500 Vdc, V_{BE} = 0)	I_{CES}	–	0.1	mAdc
Base-Emitter Voltage (V_{CE} = 5 Vdc, I_C = 150 mA)	V_{BE}	–	1.0	Vdc
DC Current Gain (V_{CE} = 5 V, I_C = 50 mA) (V_{CE} = 5 V, I_C = 150 mA)	h_{FE}	25 20	150	
Collector Emitter Saturation Voltage (I_C = 150 mA, I_B = 15 mA)	$V_{CE(sat)}$	–	1.0	Vdc

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

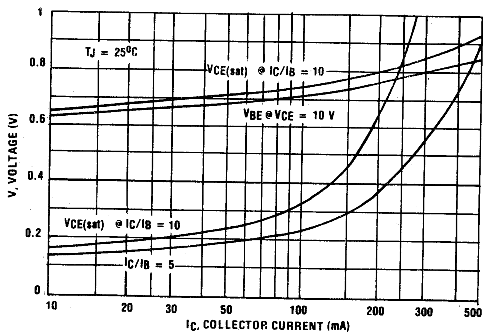


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 6 is based on $T_{J(pk)}$ = 150°C, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

3

FIGURE 3 – "ON" VOLTAGES



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD233
BD235
BD237

3

PLASTIC MEDIUM POWER SILICON NPN TRANSISTOR

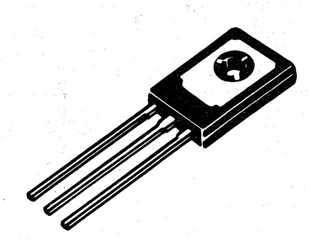
. . . designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—$h_{FE} = 40$ (Min) @ $I_C = 0.15$ Adc
- BD 233, 235, 237 are complementary with BD 234, 236, 238

2 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
25 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 233 BD 235 BD 237	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 233 BD 235 BD 237	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		2.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation $T_C = 25°C$	P_D		25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		55 to +150	°C

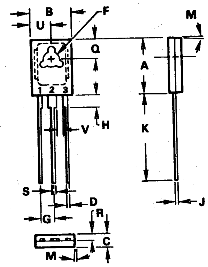
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		5.0	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$)	BV_{CEO}	BD 233 BD 235 BD 237	45 60 80	— — —	Vdc
Collector Cutoff Current ($V_{CB} = 45$ Vdc, $I_E = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	I_{CBO}	BD 233 BD 235 BD 237	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mAdc
DC current Gain ($I_C = 0.15$ A, $V_{CE} = 2$ V) ($I_C = 1$ A, $V_{CE} = 2$ V)	h_{FE1} h_{FE2}		40 25	— —	
Collector-Emitter Saturation Voltage* ($I_C = 1$ Adc, $I_B = 0.1$ Adc)	$V_{CE(sat)}$*		—	0.6	Vdc
Base-Emitter On Voltage* ($I_C = 1$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$*		—	1.3	Vdc
Current-Gain-Bandwidth Product ($I_C = 250$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



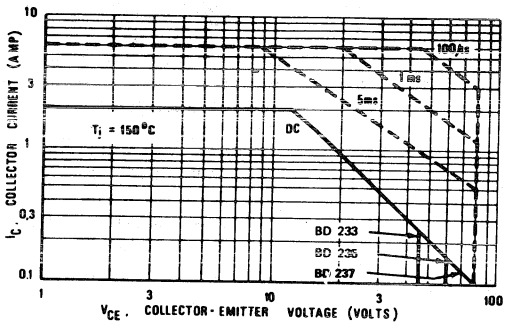
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C-V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

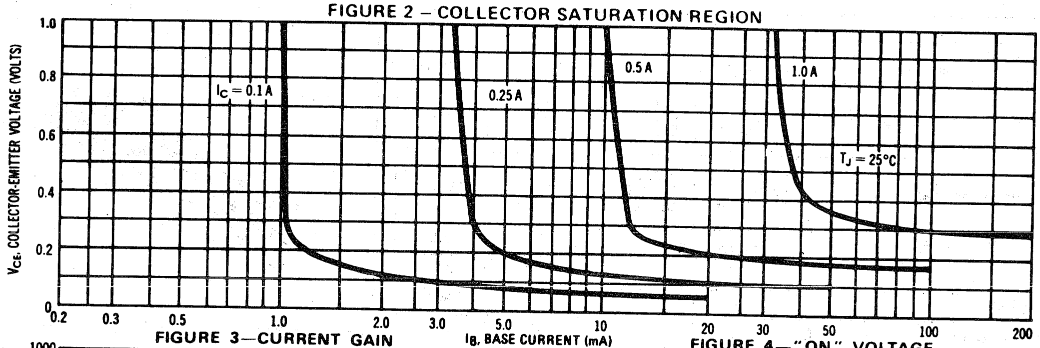


FIGURE 3—CURRENT GAIN

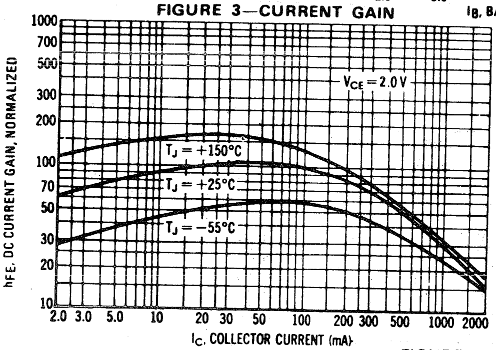


FIGURE 4—"ON" VOLTAGE

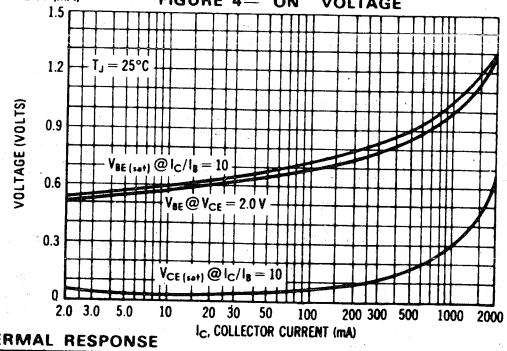
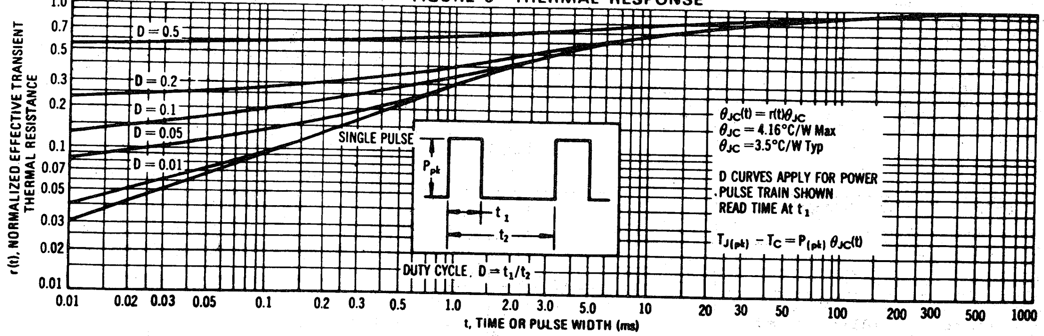


FIGURE 5—THERMAL RESPONSE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD234
BD236
BD238

PLASTIC MEDIUM POWER SILICON PNP TRANSISTOR

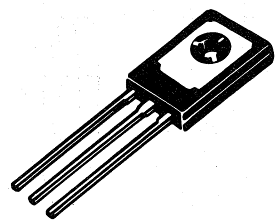
. . . designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 234, 236, 238 are complementary with BD 233, 235, 237

2 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
25 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 234 BD 236 BD 238	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 234 BD 236 BD 238	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		2.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation T_C=25°C	P_D		25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

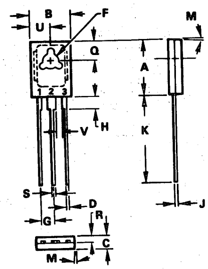
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		5.0	° C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C=0.1 Adc, I_B=0)	BV_{CEO}*	BD 234 BD 236 BD 238	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB}=45 Vdc, I_E=0) (V_{CB}=60 Vdc, I_E=0) (V_{CB}=80 Vdc, I_E=0)	I_{CBO}	BD 234 BD 236 BD 238	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE}=5.0 Vdc, I_C=0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C=0.15 A, V_{CE}=2 V) (I_C=1 A, V_{CE}=2 V)	 h_{FE1} h_{FE2}		 40 25	 — —	
Collector-Emitter Saturation Voltage* (I_C=1 Adc, I_B=0.1 Adc)	$V_{CE(sat)}$*		—	0.6	Vdc
Base-Emitter On Voltage* (I_C=1 Adc, V_{CE}=2.0 Vdc)	$V_{BE(on)}$*		—	1.3	Vdc
Current-Gain-Bandwidth Product (I_C=250 mAdc, V_{CE}=10 Vdc, f=1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

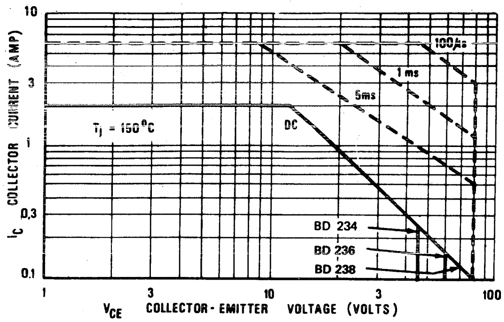
STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

3

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C-V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

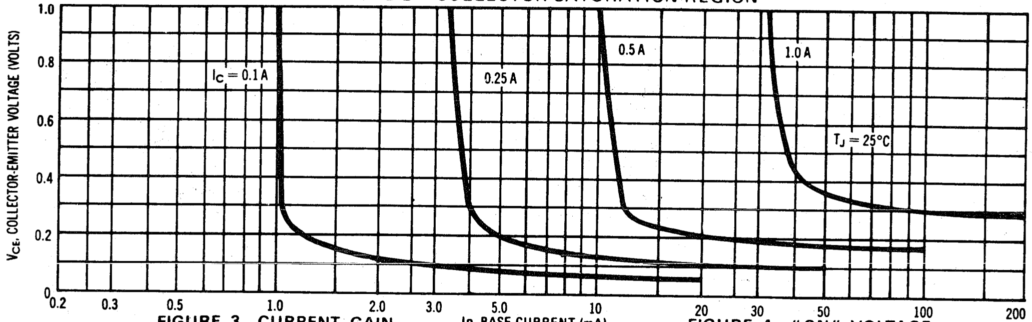


FIGURE 3—CURRENT GAIN

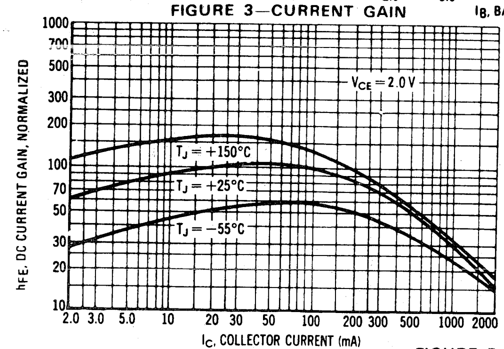


FIGURE 4—"ON" VOLTAGE

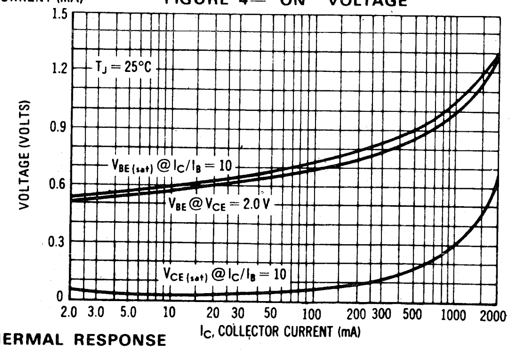
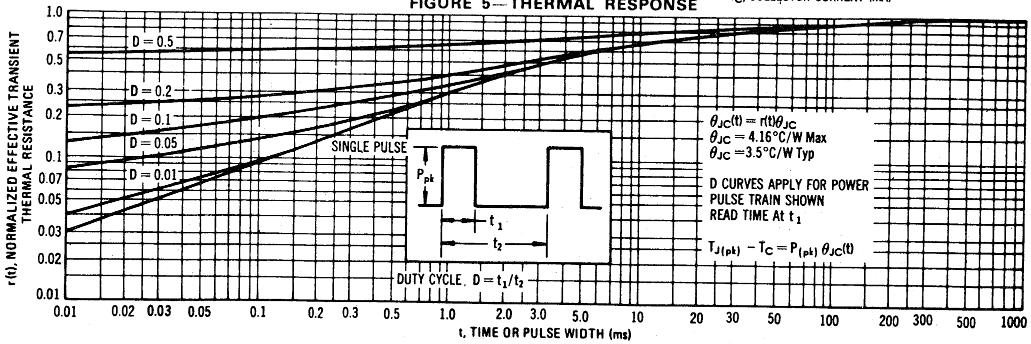


FIGURE 5—THERMAL RESPONSE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
BD239	BD240
BD239A	BD240A
BD239B	BD240B
BD239C	BD240C

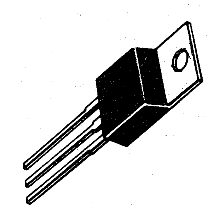
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications. Compact TO-220 AB package. TO-66 leadform also available ordered with "66" suffix.

2 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

45, 60, 80, 100 VOLTS
30 WATTS



MAXIMUM RATINGS

Rating	Symbol	BD239 BD240	BD239A BD240A	BD239B BD240B	BD239C BD240C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Emitter Voltage	V_{CB}	55	70	90	115	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current — Continuous Peak	I_C	← 2 → ← 4 →				Adc
Base Current	I_B	← 0.6 →				Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	← 30 → ← 0.24 →				Watts W/°C
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	← 2.0 → ← 0.016 →				Watts W/°C
Unclamped Inductive Load Energy (See Note 3)	E	← 32 →				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →				°C

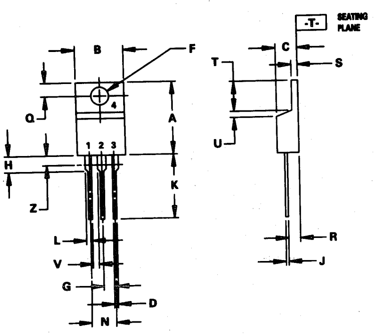
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.167	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	BD239, BD240 BD239A, BD240A BD239B, BD240B BD239C, BD240C	$V_{CEO(sus)}$	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	BD239A, BD240A BD239B,C, BD240B, C	I_{CEO}	– –	0.3 0.3	mAdc
Collector Cutoff Current (V_{CE} = 45 Vdc, V_{EB} = 0) (V_{CE} = 60 Vdc, V_{EB} = 0) (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	BD239, BD240 BD239A, BD240A BD239B, BD240A BD239C, BD240C	I_{CES}	– – – –	200 200 200 200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.2 Adc, V_{CE} = 4.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	40 15	–	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 200 mAdc)		$V_{CE(sat)}$	–	0.7	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$
(3) This rating based on testing with L_C = 20 mH, R_{BE} = 100 Ω, R_E = 0.1 Ω, I_C = 1.8 A.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

FIGURE 1 — DC CURRENT GAIN

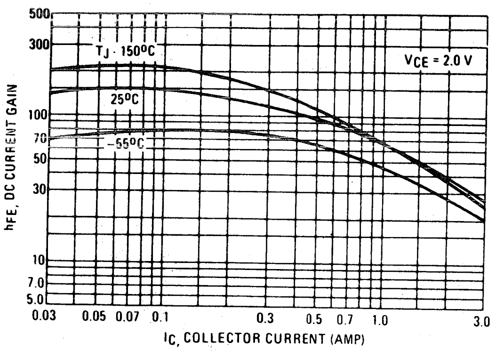


FIGURE 2 — TURN-OFF TIME

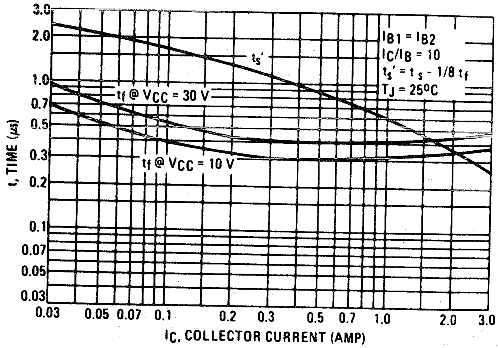


FIGURE 3 — SWITCHING TIME EQUIVALENT CIRCUIT

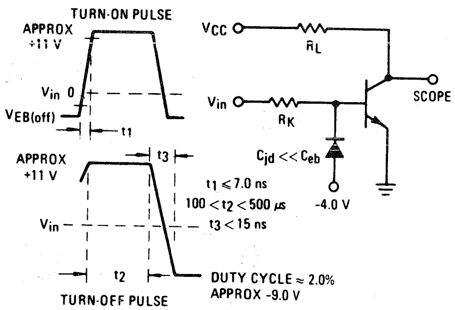


FIGURE 4 — TURN-ON TIME

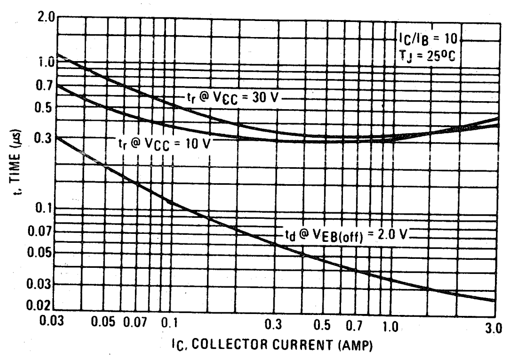
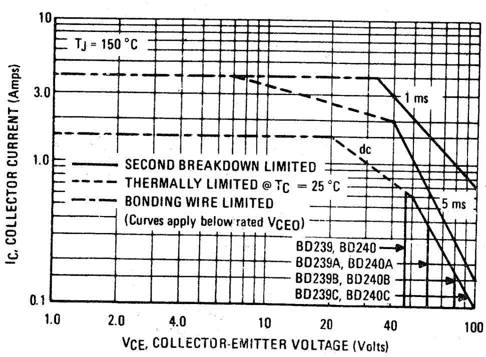


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^oC$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

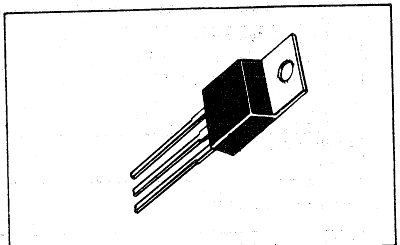
NPN	PNP
BD241	BD242
BD241A	BD242A
BD241B	BD242B
BD241C	BD242C

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage — V_{CE} = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 45 Vdc (Min.) BD241, BD242
  = 60 Vdc (Min.) BD241A, BD242A
  = 80 Vdc (Min.) BD241B, BD242B
  = 100 Vdc (Min.) BD241C, BD242C
- High Current Gain — Bandwidth Product f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220 AB Package
- TO-66 Leadform Also Available ordered with "–66" suffix.

3 AMPERE
POWER TRANSISTORS COMPLEMENTARY SILICON
45, 60, 80, 100 VOLTS
40 WATTS



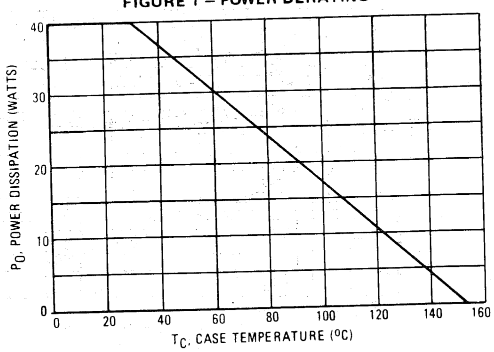
MAXIMUM RATINGS

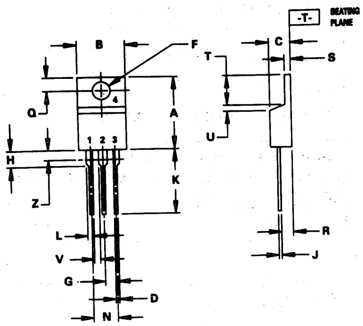
Rating	Symbol	BD241 BD242	BD241A BD242A	BD241B BD242B	BD241C BD242C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Emitter Voltage	V_{CES}	55	70	90	115	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current - Continuous Peak	I_C	← 3.0 → ← 5.0 →				Adc Adc
Base Current	I_B	← 1.0 →				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 40 → ← 0.32 →				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit.
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage[1] (I_C = 30 mAdc, I_B = 0)	BD241, BD242	V_{CEO}	45		Vdc
	BD241A, BD242A		60		
	BD241B, BD242B		80		
	BD241C, BD242C		100		
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	BD241, BD241A, BD242, BD242A,			0.3	
(V_{CE} = 60 Vdc, I_B = 0)	BD241B, BD241C, BD242B, BD242C			0.3	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 45 Vdc, V_{EB} = 0)	BD241, BD242			200	
(V_{CE} = 60 Vdc, V_{EB} = 0)	BD241A, BD242A			200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	BD241B, BD242B			200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	BD241C, BD242C			200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		1.0	mAdc
ON CHARACTERISTICS[1]					
DC Current Gain		h_{FE}			
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			25		
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			10		
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 600 Adc)		$V_{CE(sat)}$		1.2	Vdc
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$		1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product[2] (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0		MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1kHz)		h_{fe}	20		

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
[2] $f_T = |h_{fe}| \bullet f_{test}$

3

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

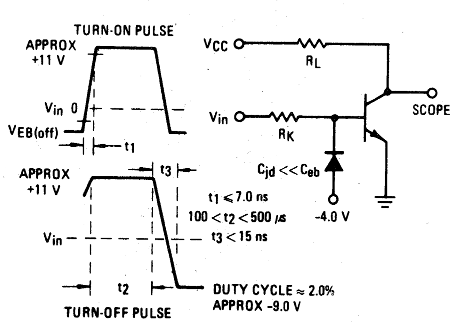


FIGURE 3 – TURN-ON TIME

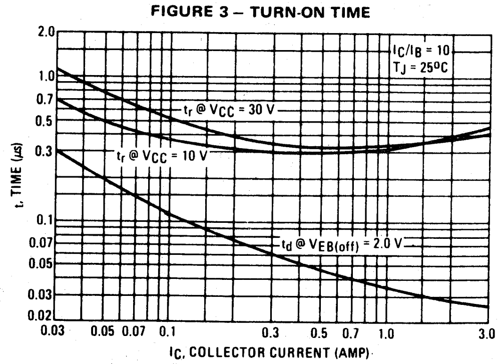


FIGURE 4 – THERMAL RESPONSE

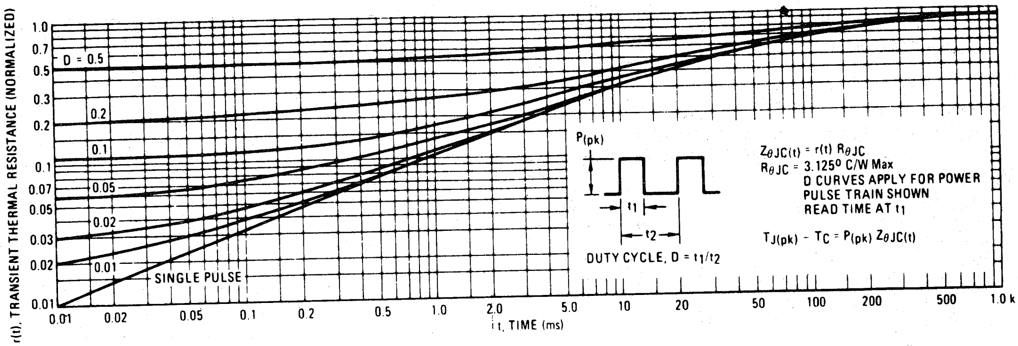
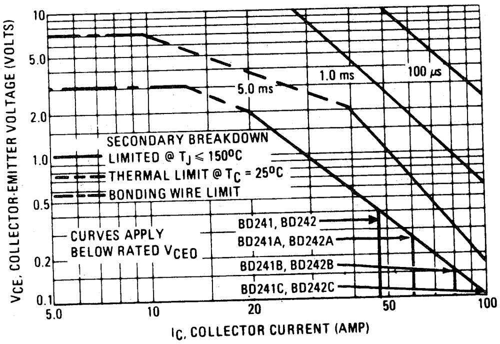


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 6 – TURN-OFF TIME

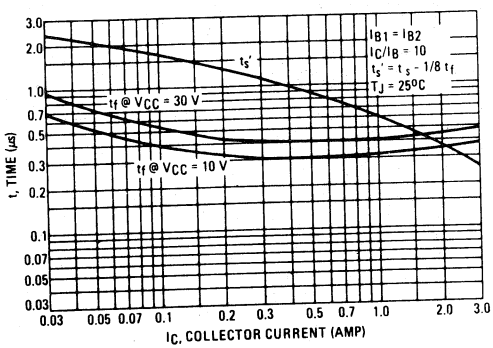


FIGURE 7 – CAPACITANCE

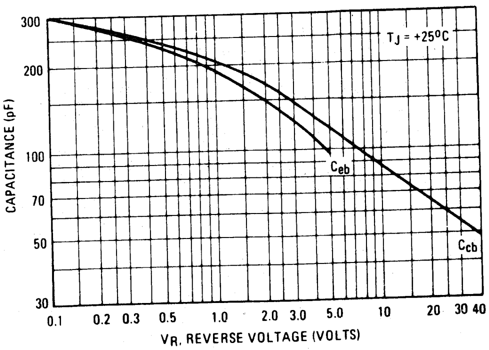


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FIGURE 8 – DC CURRENT GAIN

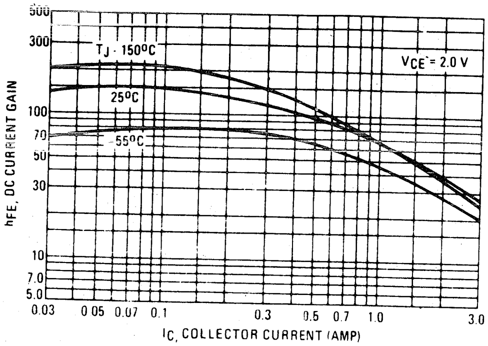


FIGURE 9 – COLLECTOR SATURATION REGION

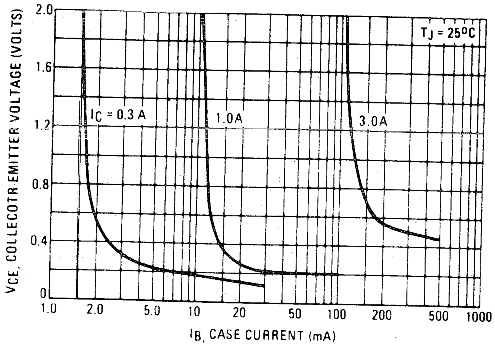


FIGURE 10 – "ON" VOLTAGES

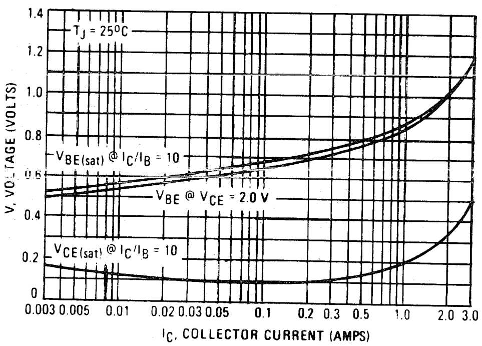


FIGURE 11 – TEMPERATURE COEFFICIENTS

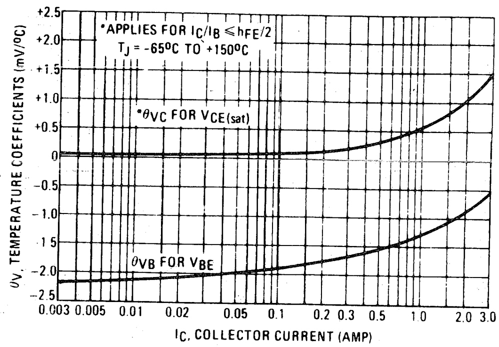


FIGURE 12 – COLLECTOR CUT-OFF REGION

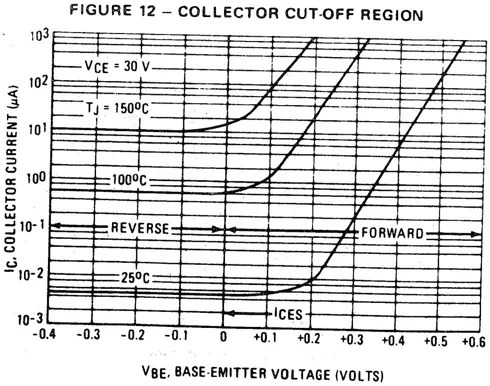
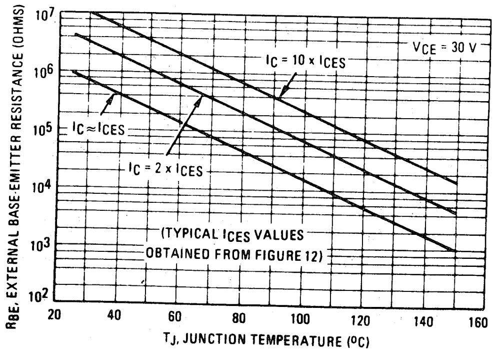


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD243 BD243A BD243B BD243C BD244 BD244A BD244B BD244C

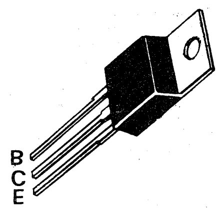
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 45 Vdc (Min) — BD243, BD244
  = 60 Vdc (Min) — BD243A, BD244A
  = 80 Vdc (Min) — BD243B, BD244B
  = 100 Vdc (Min) — BD243C, BD244C
- High Current Gain — Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220 AB Package

6 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

45-60-80-100 VOLTS
65 WATTS



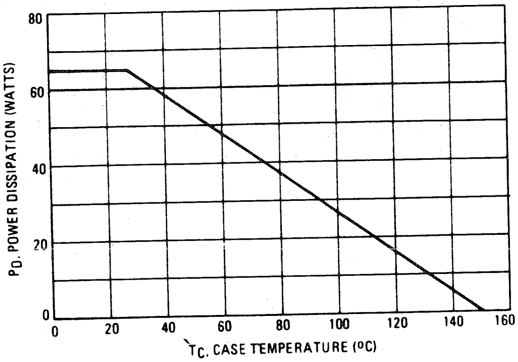
*MAXIMUM RATINGS

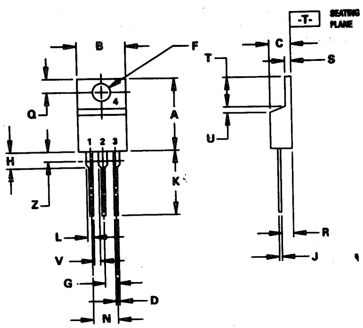
Rating	Symbol	BD243 BD244	BD243A BD244A	BD243B BD244B	BD243C BD244C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current Continuous Peak	I_C	6 10				Adc
Base Current	I_B	2.0				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.52				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

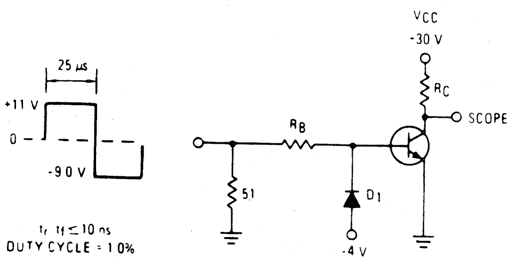
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	BD243, BD244 BD243A, BD244A BD243B, BD244B BD243C, BD244C	$V_{CEO(sus)}$	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	BD243, BD243A, BD244, BD244A BD243B, BD243C, BD244B, BD244C	I_{CEO}	– –	0.7 0.7	mAdc
Collector Cutoff Current (V_{CE} = 45 Vdc, V_{EB} = 0) (V_{CE} = 60 Vdc, V_{EB} = 0) (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	BD243, BD244 BD243A, BD244A BD243B, BD244B BD243C, BD244C	I_{CES}	– – – –	400 400 400 400	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	30 15	– –	–
Collector-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 1 Adc)		$V_{CE(sat)}$	–	1.5	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20	–	–

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = h_{fe} \bullet f_{test}$

3

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS
D1 MUST BE FAST RECOVERY TYPE eg
MBD5300 USED ABOVE IB 100 mA
MSD6100 USED BELOW IB 100 mA

FIGURE 3 – TURN-ON TIME

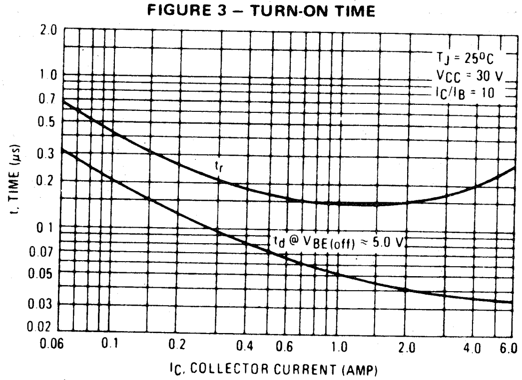


FIGURE 4 — THERMAL RESPONSE

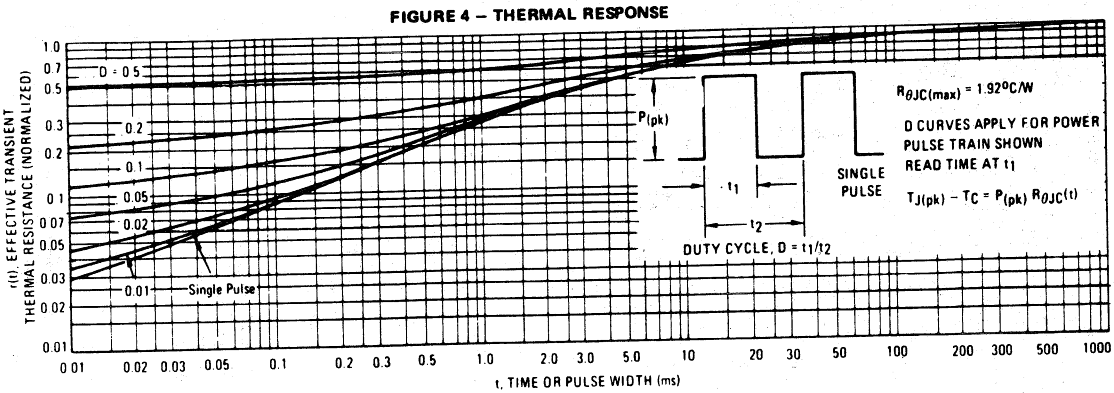
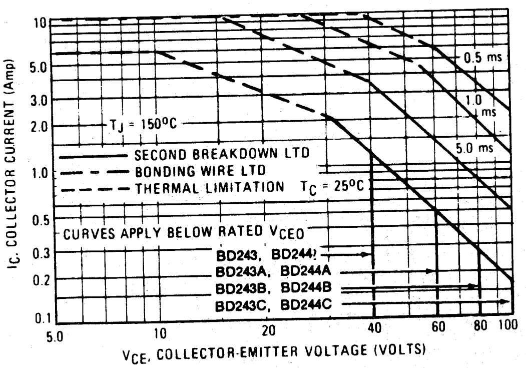


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 6 — TURN-OFF TIME

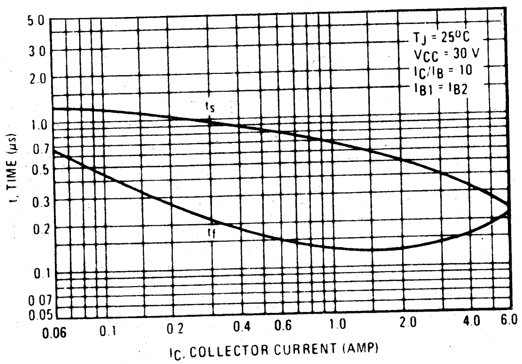
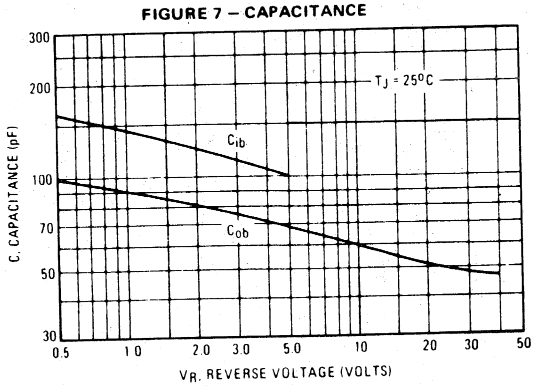


FIGURE 7 — CAPACITANCE



3

FIGURE 8 – DC CURRENT GAIN

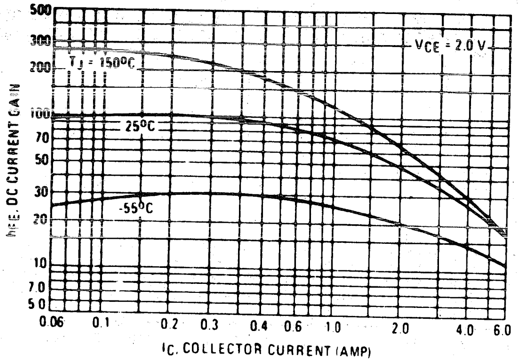


FIGURE 9 – COLLECTOR SATURATION REGION

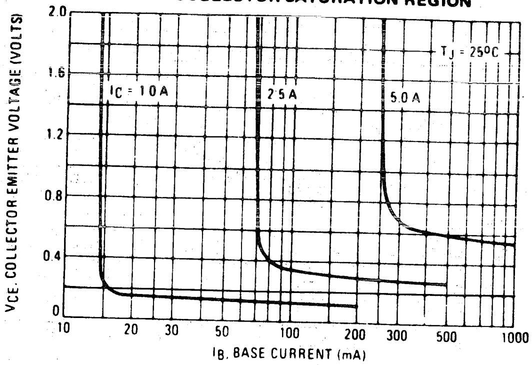


FIGURE 10 – "ON" VOLTAGES

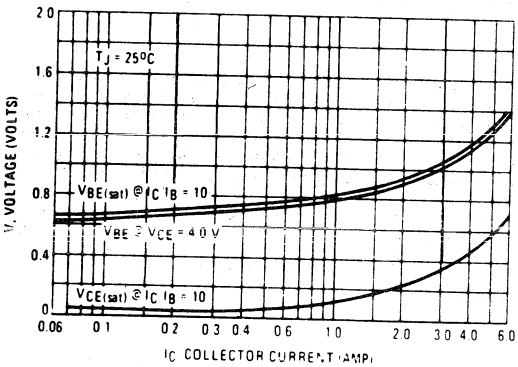


FIGURE 11 – TEMPERATURE COEFFICIENTS

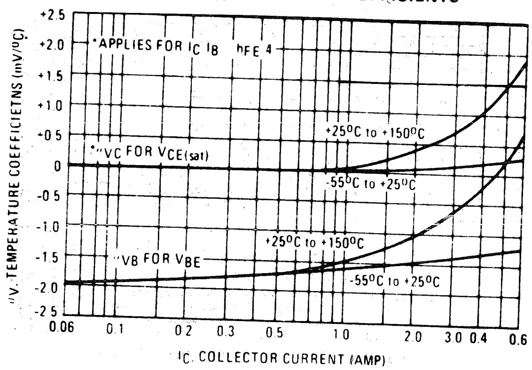


FIGURE 12 – COLLECTOR CUT-OFF REGION

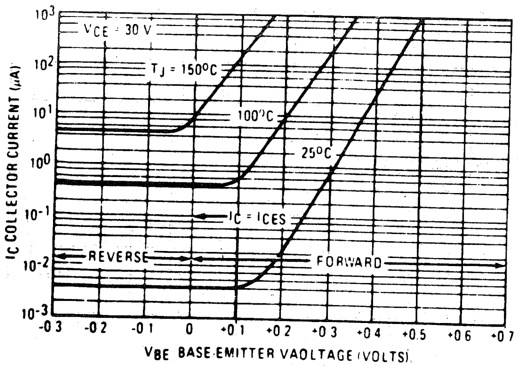
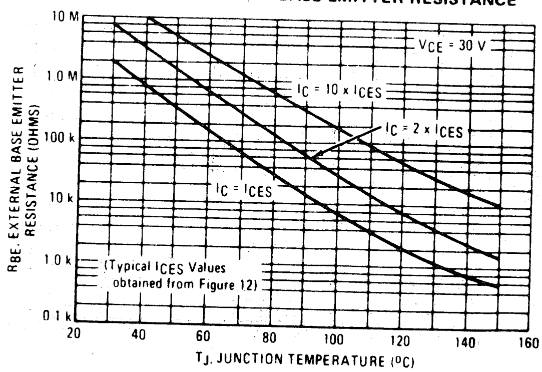


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
BD311
PNP
BD312

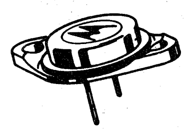
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for high quality amplifiers operating up to 60 Watts into 4 ohm load.

- High DC Current Gain
- Excellent Safe Operating Area
- High Current Gain — Bandwidth Product — Typical f_T = 4.0 MHz @ I_C = 0.5 A

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60 VOLTS
115 WATTS



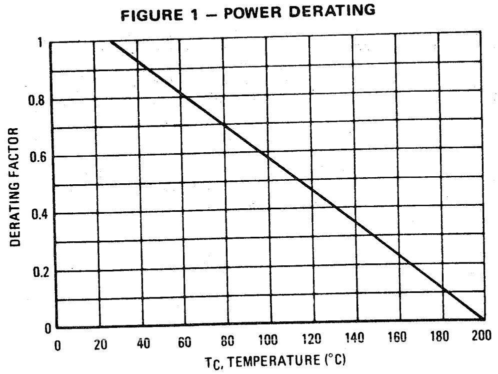
MAXIMUM RATINGS

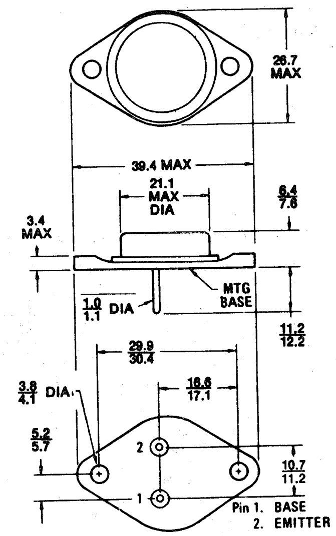
Rating	Symbol	BD311/312	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak	I_C	10 20	Adc
Base Current	I_B	4.0	Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	115 0.658	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit.
Thermal Resistance, Junction to Case	θ_{JC}	1.52	°C/W

FIGURE 1 — POWER DERATING





Dimensions in millimeters
Collector connected to case

CASE 11
TO-3

3

ELECTIRCAL CHARACTERISTICS* (T_C = 25 °C unless otherwise noted)

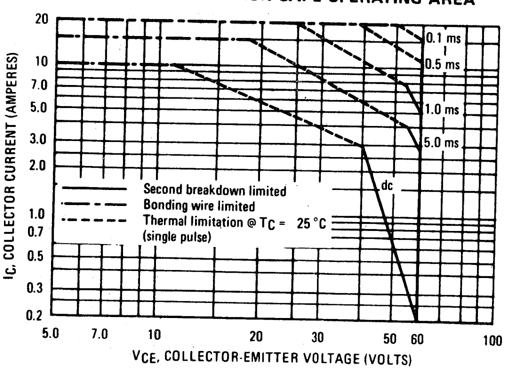
Characteristic	Symbol	Min.	Max.	Unit.
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage[1] (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60		Vdc
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}		1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}		1.0	mAdc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 5.0 Vdc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	H_{FE}	25 5		–
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc)	$V_{CE(sat)}$		1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc)	$V_{BE(sat)}$		1.8	Vdc
Base-Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS[1]				
Current-Gain — Bandwidth Product[2] (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0		MHz
SECOND BREAKDOWN				
Second Breakdown Collector Current (V_{CE} = 39 Vdc, t = 0.5 sec.) (V_{CE} = 50 Vdc, t = 0.5 sec.)	$I_{S/B}$	2.95 0.60		Adc

[1] Pulse test: Pulse width ≤ 300 μs, Duty Cycle ≥ 2%

[2] $f_T = |h_{fe}| \cdot f_{test}$

3

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



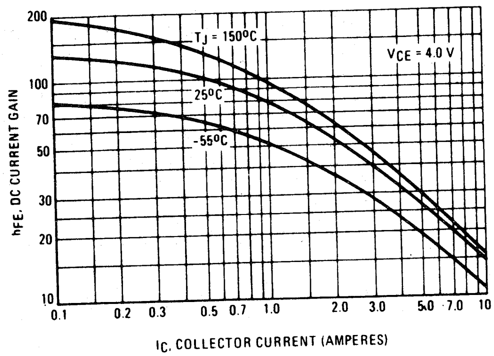
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
Second breakdown pulse limits are valid for duty cycles to 10%.

At high case temperatures, thermal limitation may reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PNP DEVICE
BD312

NPN DEVICE
BD311

FIGURE 3 — DC CURRENT GAIN



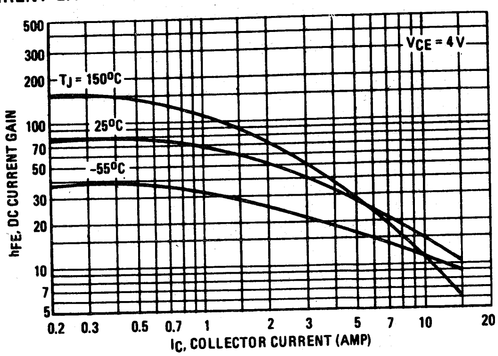
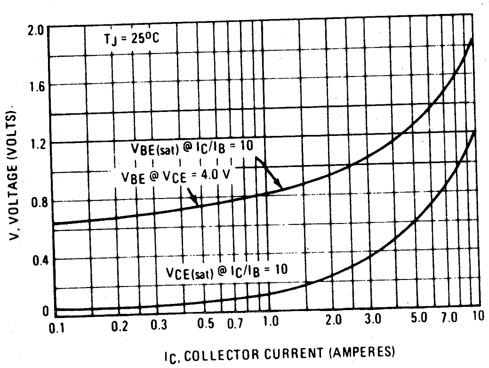
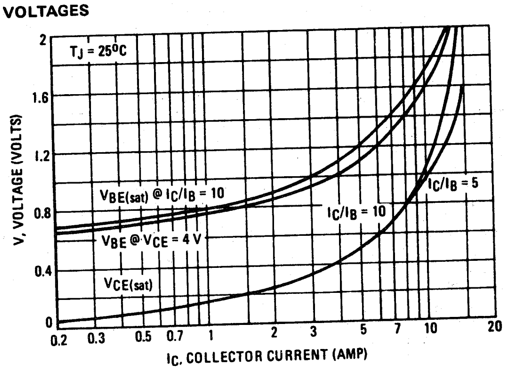


FIGURE 4 — "ON" VOLTAGES





3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
BD315, BD316
PNP
BD317, BD318

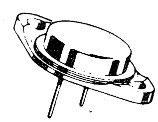
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

... designed for high quality amplifiers operating up to 100 Watts into 4 ohm load with BD315, BD316 and into 8 ohm load with BD317, BD318.

- High DC Current Gain
- Excellent Safe Operating Area
- High Current Gain — Bandwidth Product — Typical f_T = 2.0 MHz @ I_C = 1.0 A

16 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

80-100 VOLTS
200 WATTS



MAXIMUM RATINGS

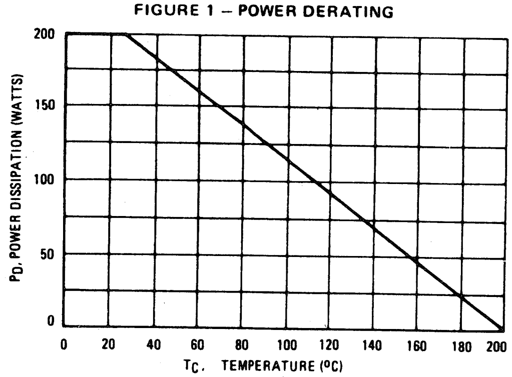
Rating	Symbol	BD315 BD316	BD317 BD318	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current – Continuous Peak	I_C	16 20		Adc
Base Current — Continuous	I_B	5.0		Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	200 1.14		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

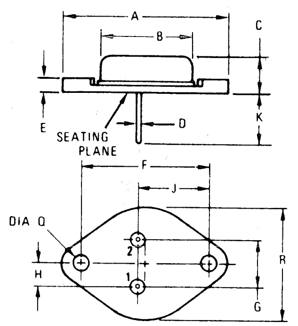
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	$^oC/W$

3

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37	–	1.550
B		21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E		3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	–	1.050

Collector connected to case

CASE 11 (TO-3)

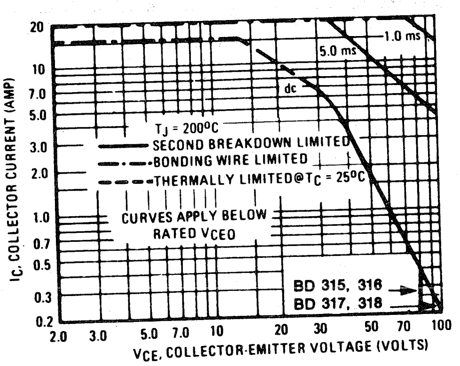
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	BD315, BD316 BD317, BD318	$V_{CEO(sus)}$	80 100	— —	Vdc
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain I_C = 5.0 Adc, V_{CE} = 4.0 Vdc I_C = 8.0 Adc, V_{CE} = 4.0 Vdc I_C = 10 Adc, V_{CE} = 4.0 Vdc	BD317, BD318 BD315, BD316 All Types	h_{FE}	25 25 15		—
Collector-Emitter Saturation Voltage I_C = 8.0 Adc, I_B = 0.8 Adc		$V_{CE(sat)}$	—	1.0	Vdc
Base-Emitter Saturation Voltage I_C = 8.0 Adc, I_B = 0.8 Adc		$V_{BE(sat)}$	—	1.8	Vdc
Base-Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	—	MHz

(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩾ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

3

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



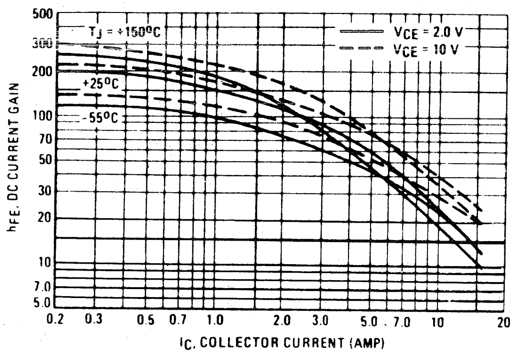
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ <200°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

PNP DEVICES
BD316 and BD318

NPN DEVICES
BD315 and BD317

FIGURE 3 — DC CURRENT GAIN



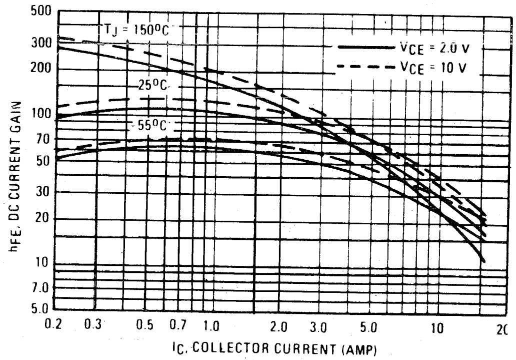
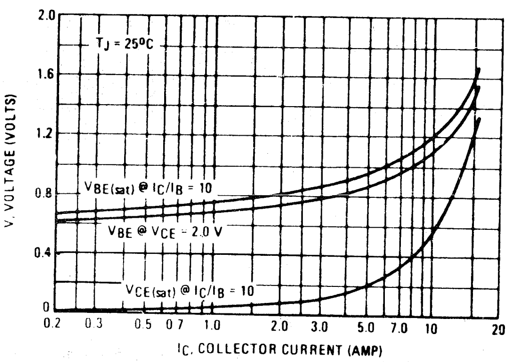
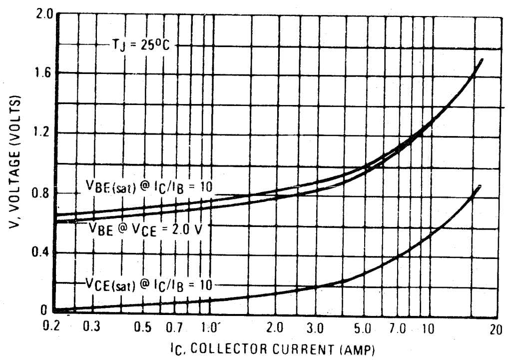


FIGURE 4 — "ON" VOLTAGES





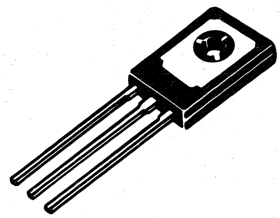
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD433, BD435
BD437, BD439
BD441

PLASTIC MEDIUM POWER SILICON
NPN TRANSISTOR

. . . for amplifier and switching applications Complementary types: BD434/436/438/440/442

4 AMPERE
POWER TRANSISTOR
NPN SILICON

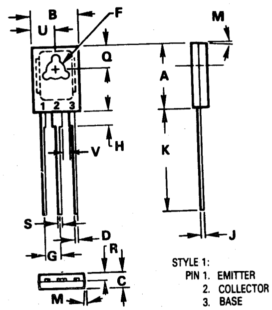


MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector Emitter Voltage	V_{CEO}	BD433 BD435 BD437 BD439 BD441	22 32 45 60 80	Vdc
Collector Base Voltage	V_{CBO}	BD433 BD435 BD437 BD439 BD441	22 32 45 60 80	Vdc
Emitter Base Voltage	V_{EBO}		5	Vdc
Collector current	I_C		4	Adc
Base Current	I_B		1	Adc
Total Device Dissipation $T_C = 25°C$ Derate above 25°C	P_D		36 288	Watts mW/°C
Operating and Storage Junction Temperature range.	I_J, I_{stg}		−55 to +150	°C

THERMAL CHARACTERISTICS

	Symbol	Max.	Unit
Thermal Resistance Junction to Case	θ_{JC}	3.5	°C/W



NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-126

3

ELECTRICAL CHARACTERISTICS (T_C – 25 °C unless otherwise noted)

Characteristics		Symbol	Min.	Typ.	Max.	Unit
Collector Emitter Breakdown Voltage (I_C = 100 mA, I_B = 0)	BD433 BD435 BD437 BD439 BD441	BV_{CEO}	22 32 45 60 80			Vdc
Collector Base Breakdown Voltage (I_C = 100 μA, I_B = 0)	BD433 BD435 BD437 BD439 BD441	BV_{CBO}	22 32 45 60 80			Vdc
Emitter Base Breakdown Voltage (I_E = 100 μA, I_C = 0)		BV_{EBO}	5			Vdc
Collector Cutoff Current (V_{CB} = 22 V, I_E = 0) (V_{CB} = 32 V, I_E = 0) (V_{CB} = 45 V, I_E = 0) (V_{CB} = 60 V, I_E = 0) (V_{CB} = 80 V, I_E = 0)	BD433 BD435 BD437 BD439 BD441	I_{CBO}			0.1 0.1 0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5 V)		I_{EBO}			1	mAdc
DC Current Gain (I_C = 10 mA, V_{CE} = 5 V)	BD433 BD435 BD437 BD439 BD441	H_{FE}	40 40 30 20 15			
DC Current Gain (I_C = 500 mA, V_{CE} = 1 V)	BD433 BD435 BD437 BD439 BD441	H_{FE}	85 85 85 40 40		475 475 375 475 475	
DC Current Gain (I_C = 2 A, V_{CE} = 1 V)	BD433 BD435 BD437 BD439 BD441	H_{FE}	50 50 40 25 15			
Collector Saturation Voltage (I_C = 2 A, I_B = 0.2 A) (I_C = 3 A, I_B = 0.3 A)	BD433 BD435 BD437 BD439 BD441	$V_{CE\ (sat)}$			0.5 0.5 0.7 0.8 0.8	Vdc
Base – Emitter on voltage (I_C = 2 A, V_{CE} = 1 V)	**BD433/435/437** **BD439/441**	$V_{BE(ON)}$			1.1 1.5	Vdc
Current Gain Bandwidth Product (V_{CE} = 1 V, I_C = 250 mA, f = 1 MHz)		f_T	3			MHz

FIGURE 1 – COLLECTOR SATURATION REGION

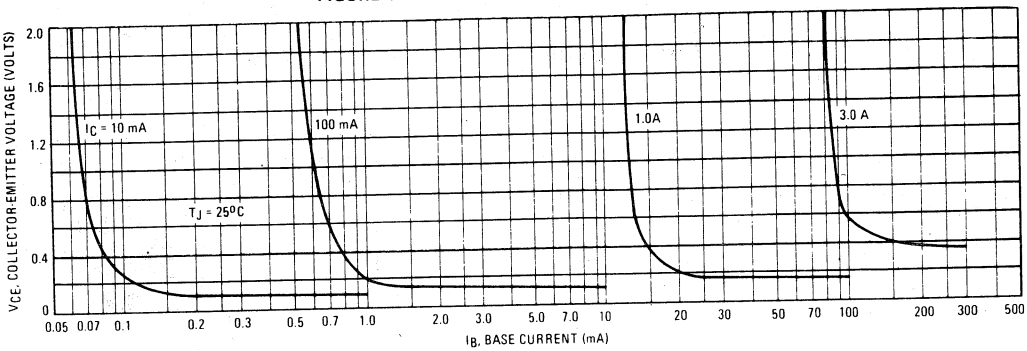


FIGURE 2 – CURRENT GAIN

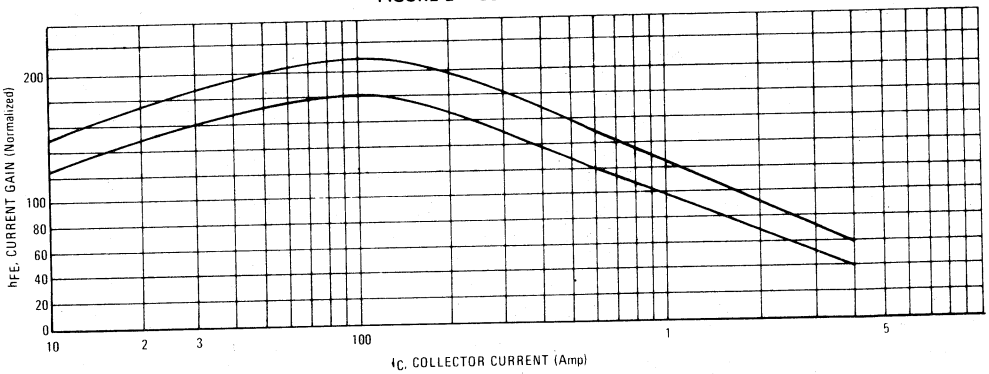


FIGURE 3 – "ON" VOLTAGE

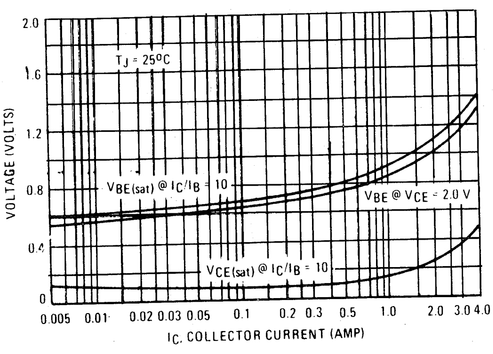
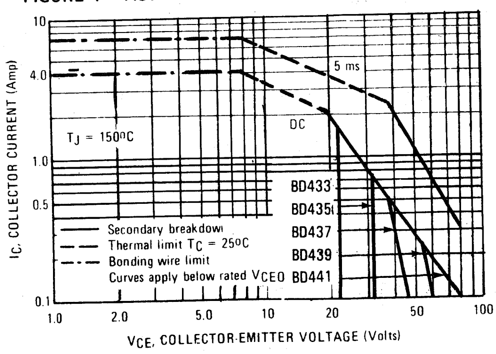


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



3

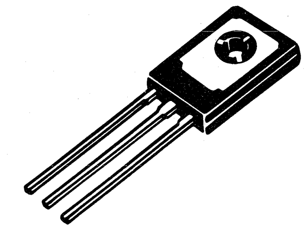
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD434, BD436 BD438, BD440 BD442

PLASTIC MEDIUM POWER SILICON PNP TRANSISTOR

. . . for amplifier and switching applications Complementary types: BD433/435/437/439/441.

4 AMPERE POWER TRANSISTOR PNP SILICON

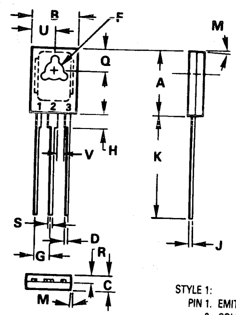


MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector Emitter Voltage	V_{CEO}	BD434 BD436 BD438 BD440 BD442	22 32 45 60 80	Vdc
Collector Base Voltage	V_{CBO}	BD434 BD436 BD438 BD440 BD442	22 32 45 60 80	Vdc
Emitter Base Voltage	V_{EBO}		5	Vdc
Collector current	I_C		4	Adc
Base Current	I_B		1	Adc
Total Device Dissipation $T_C = 25°C$ Derate above 25°C	P_D		 36 288	Watts mW/°C
Operating and Storage Junction Temperature range.	T_J, T_{stg}		−55 to +150	°C

THERMAL CHARACTERISTICS

	Symbol	Max.	Unit
Thermal Resistance Junction to Case	θ_{JC}	3.5	°C/W



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-126

3

ELECTRICAL CHARACTERISTICS (T_C – 25 °C unless otherwise noted)

Characteristics		Symbol	Min.	Typ.	Max.	Unit
Collector Emitter Breakdown Voltage (I_C = 100 mA, I_B = 0)	BD434	BV_{CEO}	22			Vdc
	BD436		32			
	BD438		45			
	BD440		60			
	BD442		80			
Collector Base Breakdown Voltage (I_C = 100 μA, I_B = 0)	BD434	BV_{CBO}	22			Vdc
	BD436		32			
	BD438		45			
	BD440		60			
	BD442		80			
Emitter Base Breakdown Voltage (I_E = 100 μA, I_C = 0)		BV_{EBO}	5			Vdc
Collector Cutoff Current (V_{CB} = 22 V, I_E = 0)	BD434	CBO			0.1	mAdc
(V_{CB} = 32 V, I_E = 0)	BD436				0.1	
(V_{CB} = 45 V, I_E = 0)	BD438				0.1	
(V_{CB} = 60 V, I_E = 0)	BD440				0.1	
(V_{CB} = 80 V, I_E = 0)	BD442				0.1	
Emitter Cutoff Current (V_{EB} = 5 V)		I_{EBO}			1	mAdc
DC Current Gain (I_C = 10 mA, V_{CE} = 5 V)	BD434	H_{FE}	40			
	BD436		40			
	BD438		30			
	BD440		20			
	BD442		15			
DC Current Gain (I_C = 500 mA, V_{CE} = 1 V)	BD434	H_{FE}	85		475	
	BD436		85		475	
	BD438		85		375	
	BD440		40		475	
	BD442		40		475	
DC Current Gain (I_C = 2 A, V_{CE} = 1 V)	BD434	H_{FE}	50			
	BD436		50			
	BD438		40			
	BD440		25			
	BD442		15			
Collector Saturation Voltage (I_C = 2 A, I_B = 0.2 A)	BD434	$V_{CE\ (sat)}$			0.5	Vdc
	BD436				0.5	
(I_C = 3 A, I_B = 0.3 A)	BD438				0.7	
	BD440				0.8	
	BD442				0.8	
Base–Emitter on voltage (I_C = 2 A, V_{CE} = 1 V)	BD434/436/438	$V_{BE(ON)}$			1.1	Vdc
	BD440/442				1.5	
Current Gain Bandwidth Product (V_{CE} = 1 V, I_C = 250 mA, f = 1 MHz)		f_T	3			MHz

FIGURE 1 — COLLECTOR SATURATION REGION

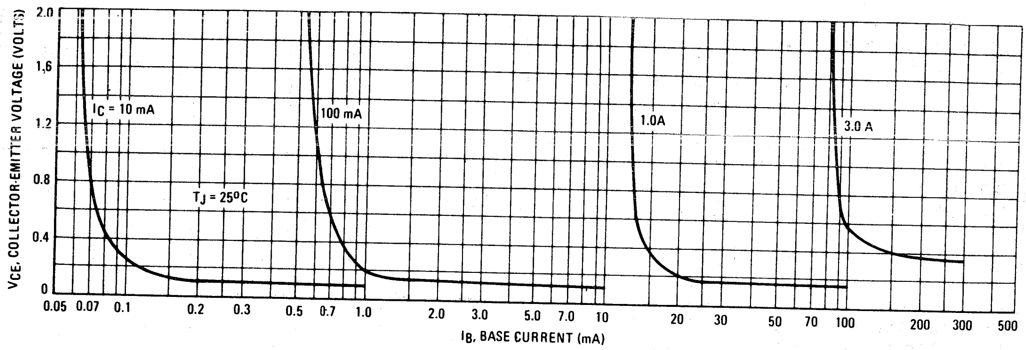
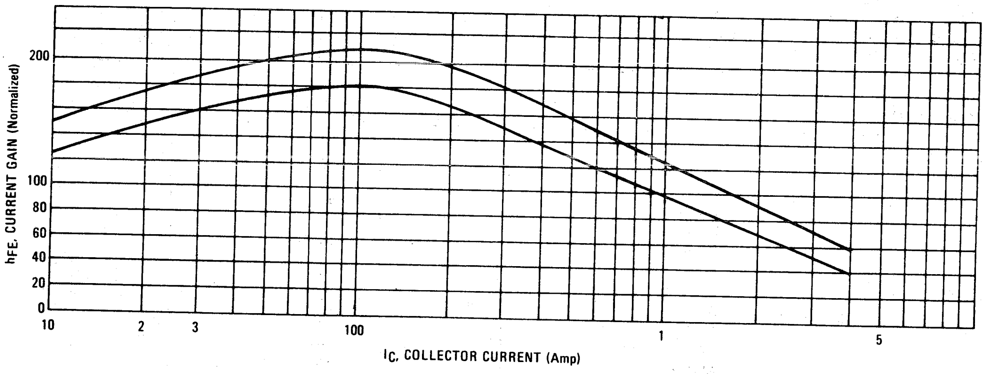


FIGURE 2 — CURRENT GAIN



3

FIGURE 3 — "ON" VOLTAGE

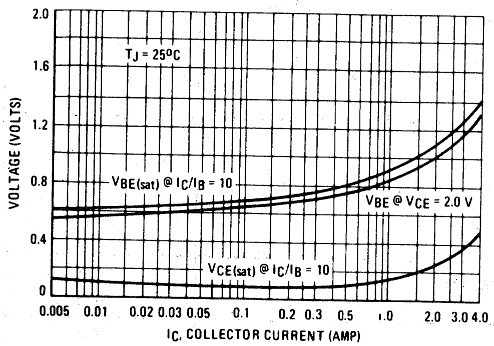
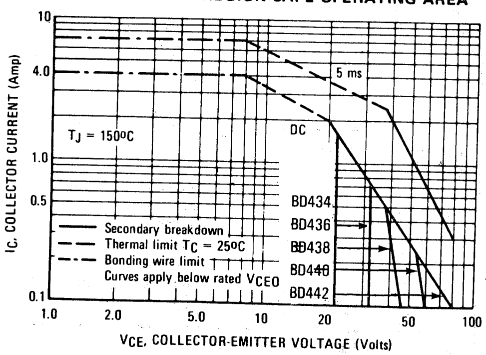


FIGURE 4 — ACTIVE REGION SAFE OPERATING AREA



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD505
BD507
BD509

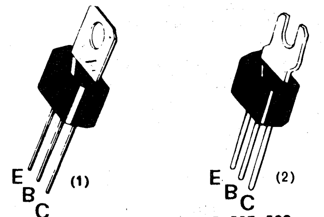
NPN SILICON ANNULAR♦ TRANSISTORS

. . . designed for complementary symmetry audio circuits

- Excellent Current Gain Linearity — 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 1.0 Adc
- Complements to PNP BD506, BD508, BD510
- Uniwatt▲ Package for Excellent Thermal Properties — 1.0 Watt @ T_A = 25°C; 10.0 Watts @ T_C = 25°C

NPN SILICON AUDIO TRANSISTORS

20 - 30 - 40 VOLTS
10 WATTS



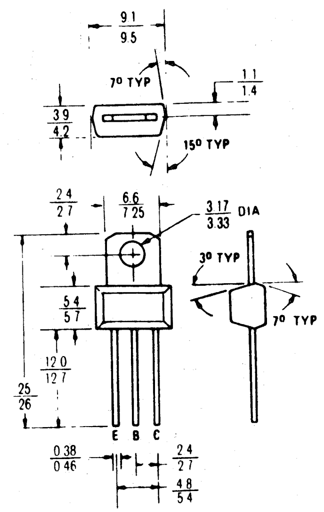
(1) Standard package: BD505, 507, 509
(2) Tab formed for flat mounting BD505-1, 507-1, 509-1
Also available with leads formed to TO-5 configuration BD505-5, 507-5, 509-5

MAXIMUM RATINGS

Rating	Symbol	BD505	BD507	BD509	Unit
Collector-Emitter Voltage	V_{CEO}	20	30	40	Vdc
Collector-Base Voltage	V_{CB}	30	40	50	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current Continuous	I_C		2.0		Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.0 8.0		Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD505 BD507 BD509	BV_{CEO}	20 30 40	— — —	— — —	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5	—	—	Vdc
Collector Cutoff Current (VCB = 20, 30, 40 Vdc, I_E = 0)	BD505 BD507 BD509	I_{CBO}	— — —	— — —	100 100 100	nAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 250 mAdc, V_{CE} = 2 Vdc) (I_C = 1.0 Adc, V_{CE} = 2 Vdc)		h_{FE}	 60 40	 160 90	 — —	—
Collector-Emitter Saturation Voltage(1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.30	0.7	Vdc
Base-Emitter On Voltage (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	0.91	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain–Bandwidth Product (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	250	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	—	30	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 1 — DC CURRENT GAIN

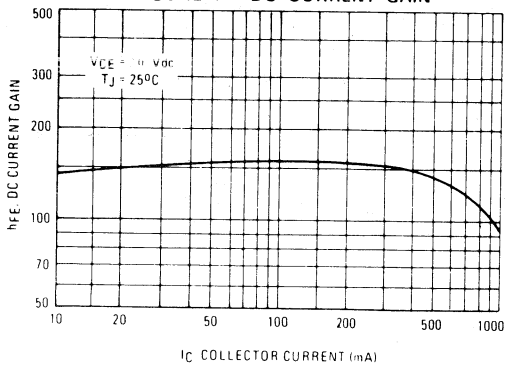


FIGURE 2 — "ON" VOLTAGES

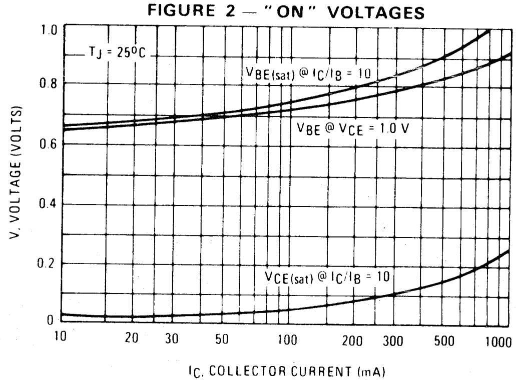
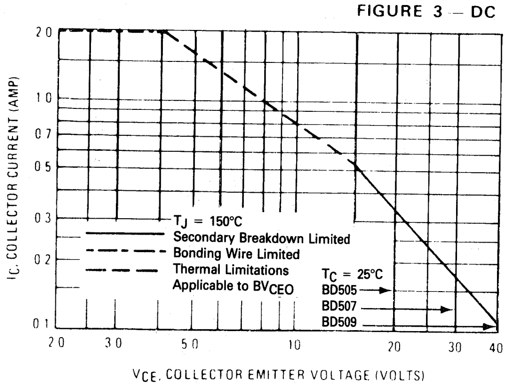


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD506
BD508
BD510

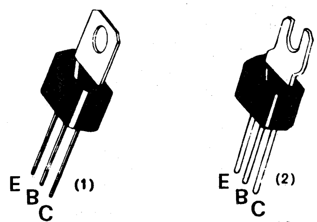
PNP SILICON AUDIO TRANSISTORS

20 - 30 - 40 VOLTS
10 WATTS

PNP SILICON ANNULAR◆ TRANSISTORS

. . . designed for complementary symmetry audio circuits

- Excellent Current Gain Linearity — 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 1.0 Adc
- Complements to NPN BD505, BD507, BD509
- Uniwatt▲ Package for Excellent Thermal Properties — 1.0 Watt @ T_A = 25°C; 10.0 Watts @ T_C = 25°C



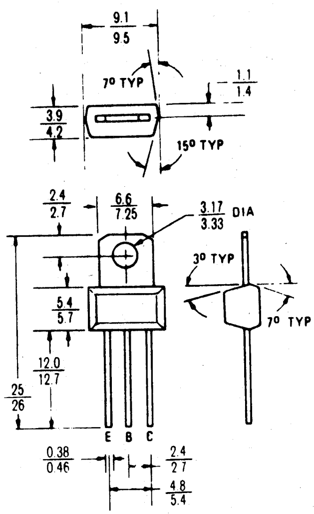
(1) Standard package: BD506, 508, 510
(2) Tab formed for flat mounting: BD506-1, 508-1, 510-1
Also available with leads formed to TO-5 configuration: BD506-5, 508-5, 510-5

MAXIMUM RATINGS

Rating	Symbol	BD506	BD508	BD510	Unit
Collector-Emitter Voltage	V_{CEO}	20	30	40	Vdc
Collector-Base Voltage	V_{CB}	30	40	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current Continuous	I_C	2.0			Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0			Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD506 BD508 BD510	BV_{CEO}	20 30 40	— — —	— — —	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 20, 30, 40 Vdc, I_E = 0)	BD506 BD508 BD510	I_{CBO}	— — —	— — —	100 100 100	nAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 250 mAdc, V_{CE} = 2.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	 60 40	 135 90	 — —	—
Collector-Emitter Saturation Voltage(1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.40	0.7	Vdc
Base-Emitter On Voltage (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	0.92	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain--Bandwidth Product (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	180	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	—	30	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

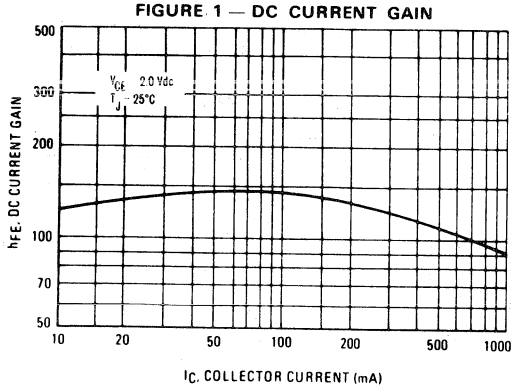


FIGURE 2 — "ON" VOLTAGES

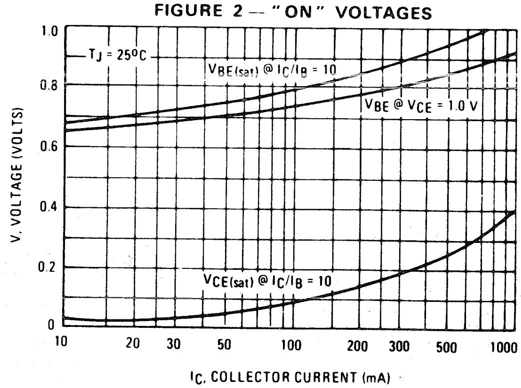
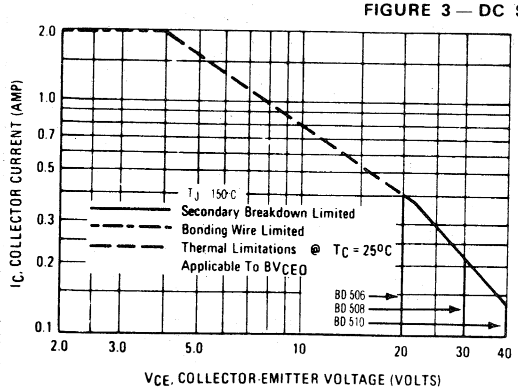


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD515
BD517
BD519

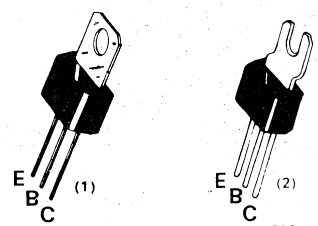
NPN SILICON ANNULAR AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 45 Vdc (Min) @ I_C = 1 mAdc — BD515
  60 Vdc (Min) @ I_C = 1 mAdc — BD517
  80 Vdc (Min) @ I_C = 1 mAdc — BD519
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complements to BD516, BD518, BD520

NPN SILICON AMPLIFIER TRANSISTORS

45 - 60 - 80 VOLTS
10 WATTS



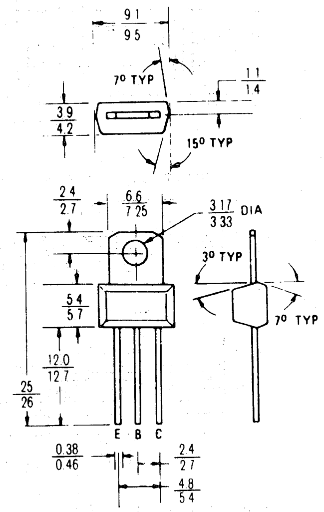
(1) Standard package: BD515, 517, 519
(2) Tab formed for flat mounting: BD515-1, 517-1, 519-1
Also available with leads formed to TO-5 configuration: BD515-5, 517-5, 519-5

MAXIMUM RATINGS

Rating	Symbol	BD515	BD517	BD519	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}		4.0		Vdc
Collector Current – Continuous	I_C		2.0		Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.0 8.0		Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD515 BD517 BD519	BV_{CEO}	45 60 80	— — —	— — —	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0)	BD515 BD517 BD519	I_{CBO}	— — —	— — —	100 100 100	nAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 10 mAdc, V_{CE} = 2.0 Vdc) (I_C = 150 mAdc, V_{CE} = 2.0 Vdc) (I_C = 500 mAdc, V_{CE} = 2.0 Vdc)		h_{FE}	— 60 25	115 125 55	— 350 —	—
Collector-Emitter Saturation Voltage (1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 500 mAdc, I_B = 25 mAdc)		$V_{CE(sat)}$	— —	0.18 0.24	0.5 —	Vdc
Base-Emitter On Voltage (1) (I_C = 500 mAdc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	0.74	1.0	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain–Bandwidth Product (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	160	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	6.0	12	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — TYPICAL DC CURRENT GAIN

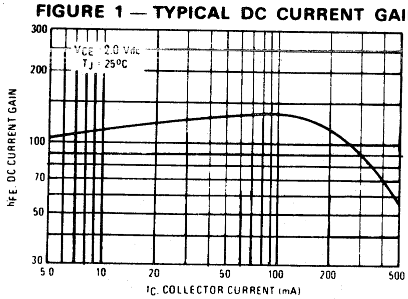


FIGURE 2 — "SATURATION" AND "ON" VOLTAGES

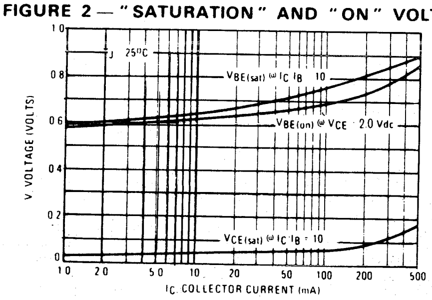


FIGURE 3 — DC SAFE OPERATING AREA

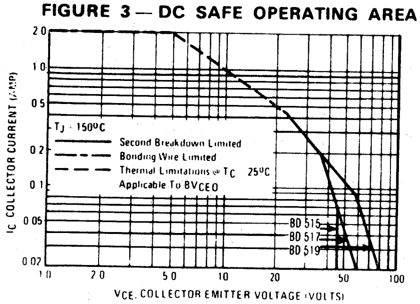
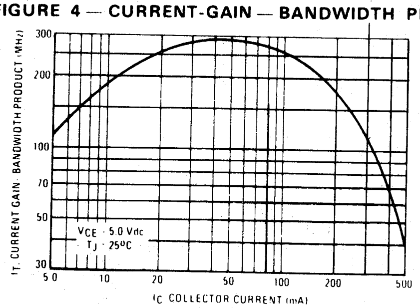


FIGURE 4 — CURRENT-GAIN — BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150 °C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD516
BD518
BD520

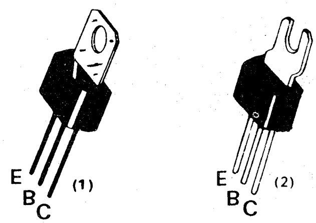
PNP SILICON ANNULAR AMPLIFIER TRANSISTORS

45 - 60 - 80 VOLTS
10 WATTS

PNP SILICON ANNULAR AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 45 Vdc (Min) @ I_C = 1 mAdc — BD516
  60 Vdc (Min) @ I_C = 1 mAdc — BD518
  80 Vdc (Min) @ I_C = 1 mAdc — BD520
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complements to BD515, BD517, BD519



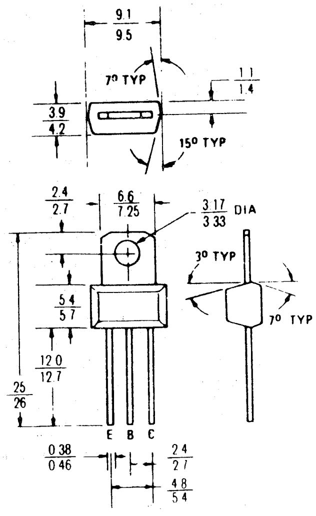
(1) Standard package: BD516, 518, 520
(2) Tab formed for flat mounting: BD516-1, 518-1, 520-1
Also available with leads formed to TO-5 configuration: BD516-5, 518-5, 520-5

MAXIMUM RATINGS

Rating	Symbol	BD516	BD518	BD520	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}		4.0		Vdc
Collector Current — Continuous	I_C		2.0		Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.0 8.0		Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD516 BD518 BD520	BV_{CEO}	45 60 80	— — —	— — —	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0)	BD516 BD518 BD520	I_{CBO}	— — —	— — —	100 100 100	nAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 10 mAdc, V_{CE} = 2.0 Vdc) (I_C = 150 mAdc, V_{CE} = 2.0 Vdc) (I_C = 500 mAdc, V_{CE} = 2.0 Vdc)		h_{FE}	— 60 25	150 130 80	— 350 —	—
Collector-Emitter Saturation Voltage (1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 500 mAdc, I_B = 25 mAdc)		$V_{CE(sat)}$	— —	0.24 0.32	0.5 —	Vdc
Base-Emitter On Voltage (1) (I_C = 500 mAdc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	0.78	1.0	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	125	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	10	15	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

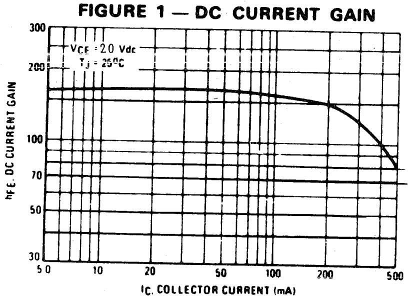


FIGURE 2 — "ON" VOLTAGES

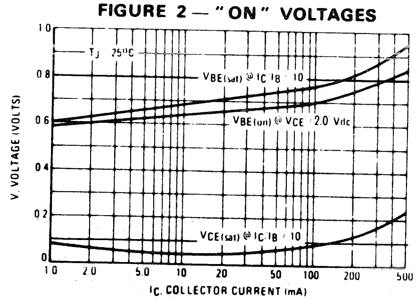


FIGURE 3 — DC SAFE OPERATING AREA

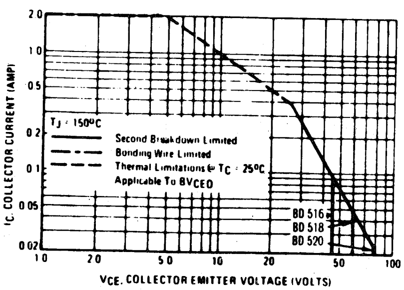
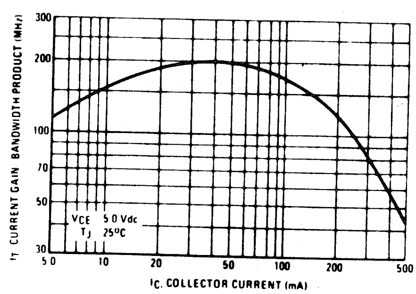


FIGURE 4 — CURRENT-GAIN—BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD525
BD527
BD529

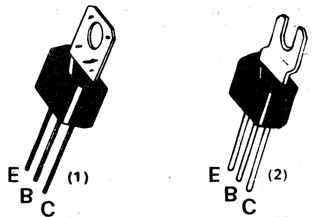
NPN SILICON ANNULAR♦ AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mAdc — BD525
  80 Vdc (Min) @ I_C = 1.0 mAdc — BD527
  100 Vdc (Min) @ I_C = 1.0 mAdc — BD529
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complements to PNP BD526, BD528, BD530

NPN SILICON AMPLIFIER TRANSISTORS

60 - 80 - 100 VOLTS
10 WATTS



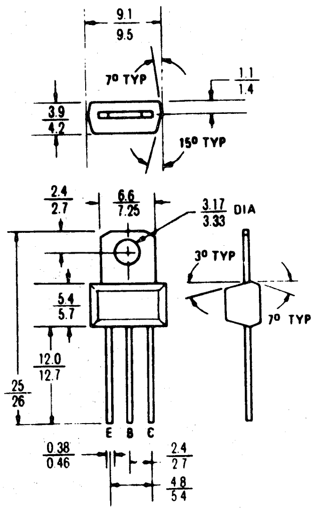
(1) Standard package: BD525, 527, 529
(2) Tab formed for flat mounting: BD525-1, 527-1, 529-1
Also available with leads formed to TO-5 configuration: BD525-5, 527-5, 529-5

MAXIMUM RATINGS

Rating	Symbol	BD525	BD527	BD529	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}		4.0		Vdc
Collector Current – Continuous	I_C		2.0		Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.0 8.0		Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD525 BD527 BD529	BV_{CEO}	60 80 100	— — —	— — —	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	 BD525 BD527 BD529	I_{CBO}	— — —	— — —	100 100 100	nAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 2.0 Vdc) (I_C = 250 mAdc, V_{CE} = 2.0 Vdc)		h_{FE}	 60 30	 115 95	 — —	—
Collector-Emitter Saturation Voltage(1) (I_C = 250 mAdc, I_B = 10 mAdc) (I_C = 250 mAdc, I_B = 25 mAdc)		$V_{CE(sat)}$	 — —	 0.18 0.1	 0.5 —	Vdc
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	0.74	1.0	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain--Bandwidth Product (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	150	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	6.0	12	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — TYPICAL DC CURRENT GAIN

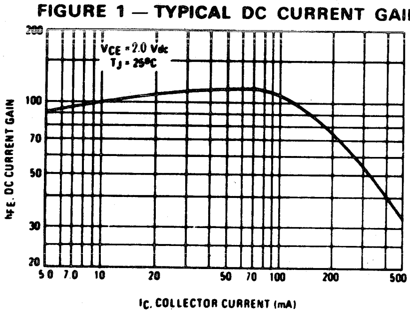


FIGURE 2 — "SATURATION" AND "ON" VOLTAGES

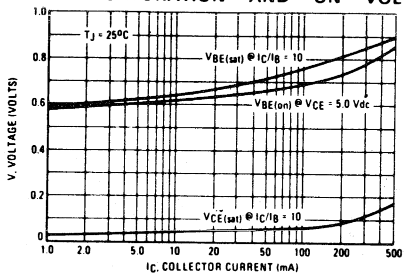


FIGURE 3 — SAFE OPERATING AREA

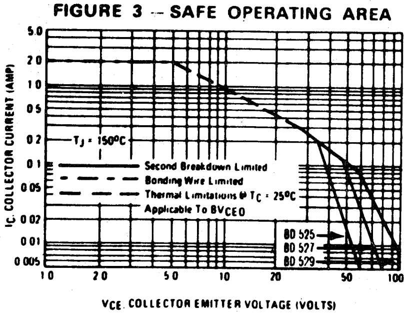
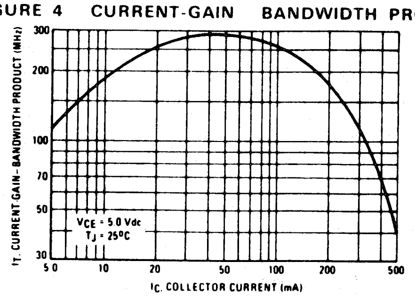


FIGURE 4 CURRENT-GAIN BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD526
BD528
BD530

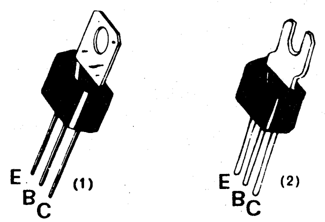
PNP SILICON ANNULAR♦ AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mAdc — BD526
  80 Vdc (Min) @ I_C = 1.0 mAdc — BD528
  100 Vdc (Min) @ I_C = 1.0 mAdc — BD530
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complements to NPN BD525, BD527 BD529

PNP SILICON AMPLIFIER TRANSISTORS

60 - 80 - 100 VOLTS
10 WATTS



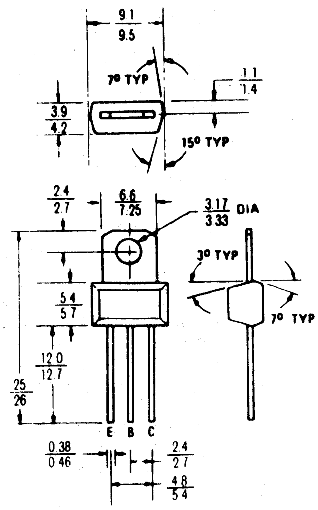
(1) Standard package: BD526, 528, 530
(2) Tab formed for flat mounting BD526-1, 528-1, 530-1
Also available with leads formed to TO-5 configuration: BD526-5, 528-5, 530-5

MAXIMUM RATINGS

Rating	Symbol	BD526	BD528	BD530	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}		4.0		Vdc
Collector Current Continuous	I_C		2.0		Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.0 8.0		Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD526 BD528 BD530	BV_{CEO}	60 80 100	— — —	— — —	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	BD526 BD528 BD530	I_{CBO}	— — —	— — —	100 100 100	nAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 2.0 Vdc) (I_C = 250 mAdc, V_{CE} = 2.0 Vdc)		h_{FE}	60 30	153 98	— —	—
Collector-Emitter Saturation Voltage(1) (I_C = 250 mAdc, I_B = 10 mAdc) (I_C = 250 mAdc, I_B = 25 mAdc)		$V_{CE(sat)}$	— —	0.22 0.15	0.5 —	Vdc
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	0.78	1.0	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	100	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	10	15	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

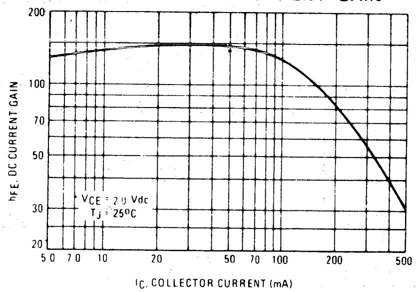


FIGURE 2 — "ON" VOLTAGES

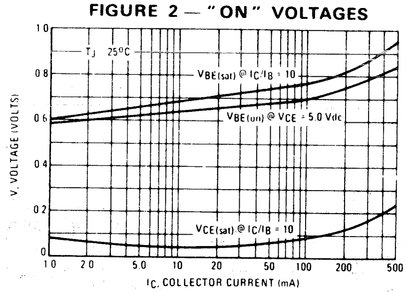


FIGURE 3 — DC SAFE OPERATING AREA

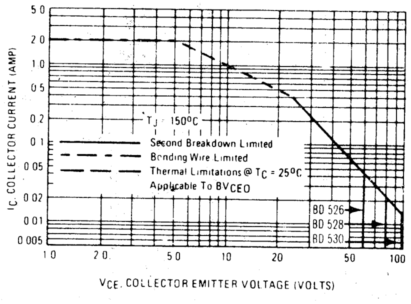
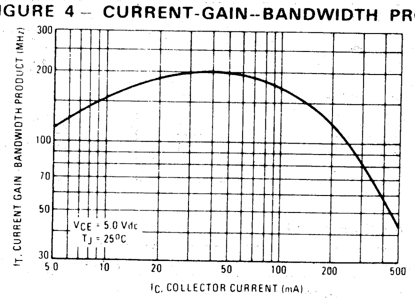


FIGURE 4 — CURRENT-GAIN—BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

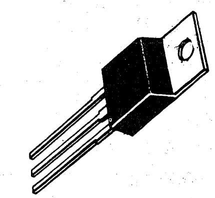
NPN	PNP
BD533	BD534
BD535	BD536
BD537	BD538

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage — V_{CE} = 0.8 Vdc (Max) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 45 Vdc (Min) BD533, BD534
  = 60 Vdc (Min) BD535, BD536
  = 80 Vdc (Min) BD537, BD538
- High Current Gain — Bandwidth Product f_T = 3.0 MHz (Min) @ I_C = 250 mAdc
- Compact TO-220 AB Package
- TO-66 Leadform Also Available ordered with "—66" suffix

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
45, 60, 80 VOLTS
50 WATTS



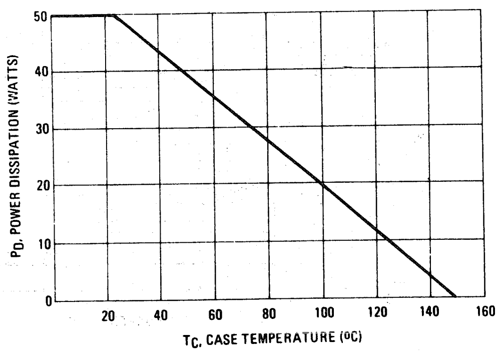
MAXIMUM RATINGS

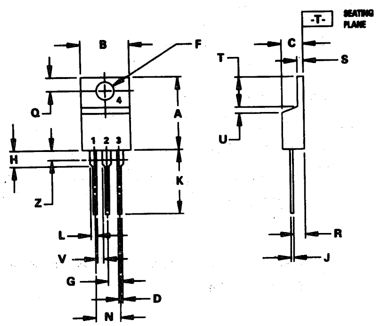
Rating	Symbol	BD533 BD534	BD535 BD536	BD537 BD538	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current - Continuous Peak	I_C	← 4.0 → ← 8.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 50 → ← 0.4 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage[1] (I_C = 0.1 Adc, I_B = 0)	BD533, BD534	$V_{CEO(sus)}$	45		Vdc
	BD535, BD536		60		
	BD537, BD538		80		
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0)	BD533, BD534	I_{CBO}		0.1	mAdc
(V_{CB} = 60 Vdc, I_E = 0)	BD535, BD536			0.1	
(V_{CB} = 80 Vdc, I_E = 0)	BD537, BD538			0.1	
Collector Cutoff Current (V_{CE} = 45 Vdc, V_{EB} = 0)	BD533, BD534	I_{CES}		100	μAdc
(V_{CE} = 60 Vdc, V_{EB} = 0)	BD535, BD536			100	
(V_{CE} = 80 Vdc, V_{EB} = 0)	BD537, BD538			100	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		1.0	mAdc
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 5 Vdc)	BD533, BD534	h_{FE}	20		
	BD535, BD536		20		
	BD537, BD538		15		
(I_C = 500 mAdc, V_{CE} = 2 Vdc)			40		
(I_C = 2 Adc, V_{CE} = 2 Vdc)	BD533, BD534		25		
	BD535, BD536		25		
	BD537, BD538		15		
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$		0.8	Vdc
Base-Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product[2] (I_C = 250 mAdc, V_{CE} = 1 Vdc, f_{test} = 1 MHz)		f_T	3.0		MHz

[1] Pulse test = Pulse width ≤300 μs, Duty Cycle ≤2.0%.
[2] $f_T = |h_{fe}| \cdot f_{test}$

3

FIGURE 2 — SWITCHING TIME EQUIVALENT CIRCUIT

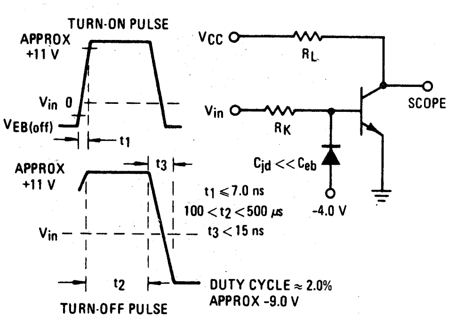


FIGURE 3 — TURN-ON TIME

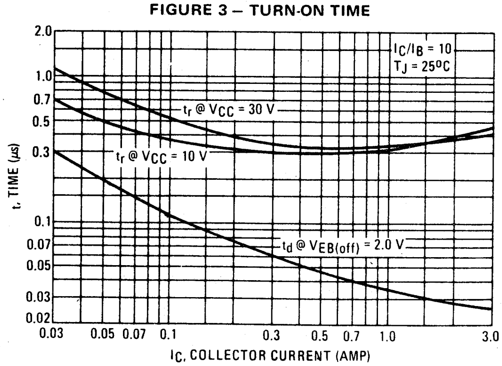


FIGURE 4 — THERMAL RESPONSE

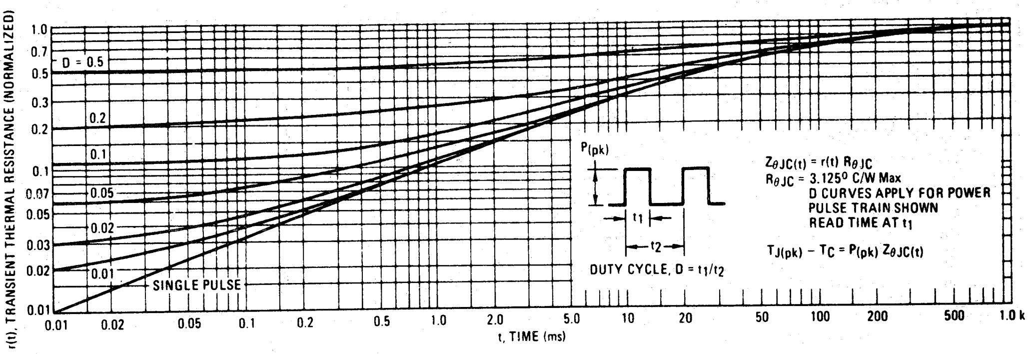
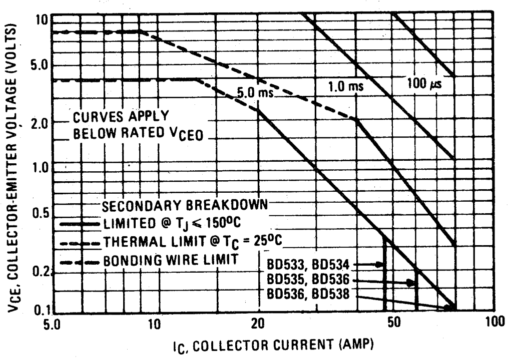


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 6 — TURN-OFF TIME

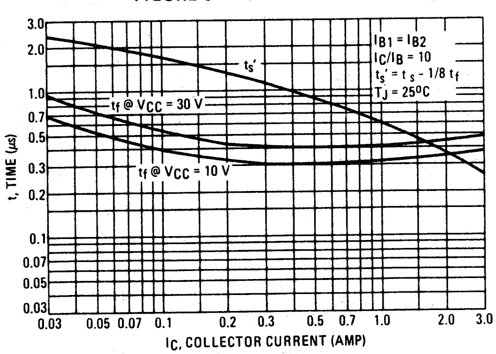
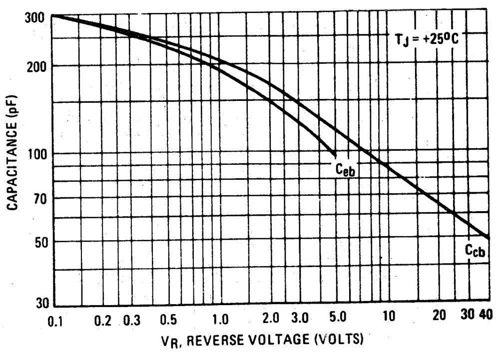


FIGURE 7 — CAPACITANCE



3

FIGURE 8 – DC CURRENT GAIN

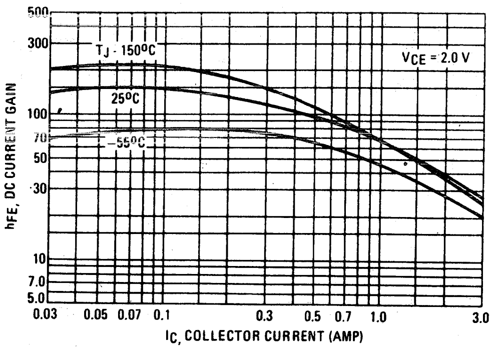


FIGURE 9 – COLLECTOR SATURATION REGION

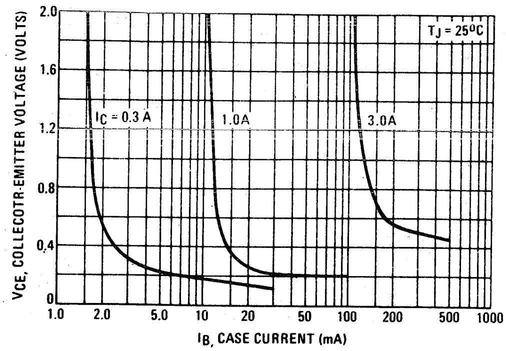


FIGURE 10 – "ON" VOLTAGES

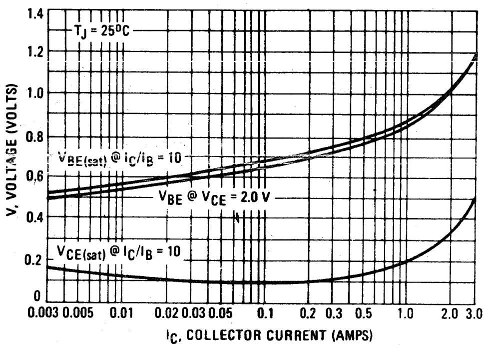


FIGURE 11 – TEMPERATURE COEFFICIENTS

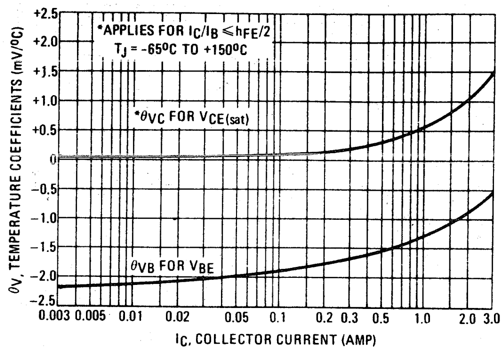


FIGURE 12 – COLLECTOR CUT-OFF REGION

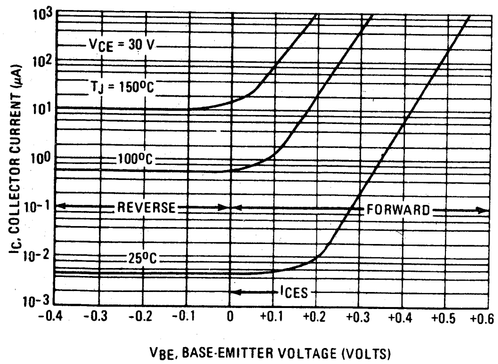
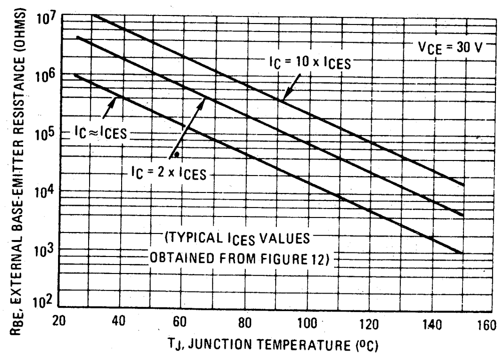


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD675, BD675A
BD677, BD677A
BD679, BD679A
BD681

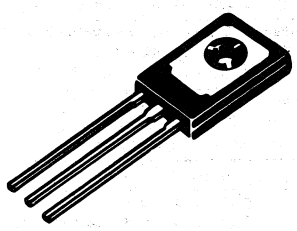
4.0 AMPERE
DARLINGTON
POWER TRANSISTORS
NPN SILICON

45, 60, 80, 100 VOLTS
40 WATTS

PLASTIC MEDIUM-POWER SILICON NPN DARLINGTONS

. . . for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain — h_{FE} = 750 (Min) @ I_C = 1.5 and 2.0 Adc
- Monolithic Construction
- BD675, 675A, 677, 677A, 679, 679A, 681 are complementary with BD676, 676A, 678, 678A, 680, 680A, 682
- BD 677, 677A, 679, 679A are equivalent to MJE 800, 801, 802, 803



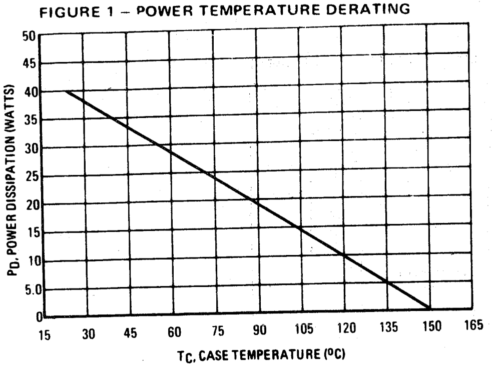
MAXIMUM RATINGS

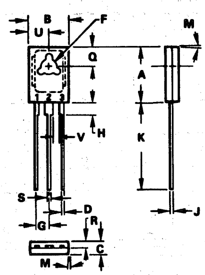
Rating	Symbol	BD675 BD675A	BD677 BD677A	BD679 BD679A	BD681	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	4.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	40 0.32				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	−55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.13	°C/W

FIGURE 1 — POWER TEMPERATURE DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

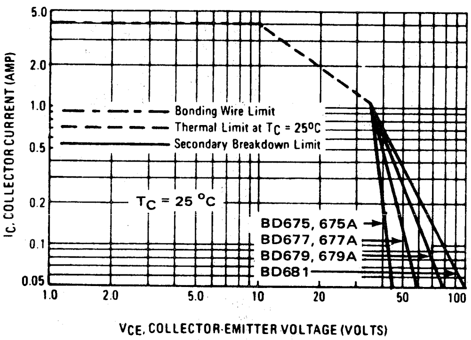
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 50 mAdc, I_B = 0)	BD675, 675A BD677, 677A BD679, 679A BD681	BV_{CEO}	45 60 80 100	– – –	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	– –	0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	 BD675, 677, 679, 681 BD 675A, 677A, 679A	h_{FE}	750 750	– –	–
Collector-Emitter Saturation Voltage(1) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc)	 BD 677, 679, 681 BD 675A, 677A, 679A	$V_{CE(sat)}$	– –	2.5 2.8	Vdc
Base-Emitter On Voltage(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	 BD 677, 679, 681 BD 675A, 677A, 679A	$V_{BE(on)}$	– –	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

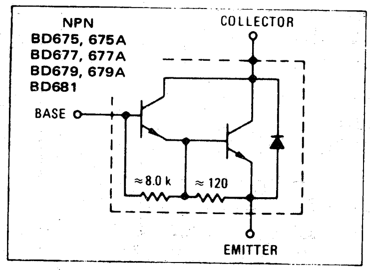
FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 DARLINGTON CIRCUIT SCHEMATIC



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD676, BD676A
BD678, BD678A
BD680, BD680A
BD682

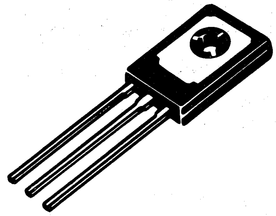
PLASTIC MEDIUM-POWER SILICON PNP DARLINGTONS

. . . for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain —
  h_{FE} = 750 (Min) @ I_C = 1.5 and 2.0 Adc
- Monolithic Construction
- BD676, 676A, 678, 678A, 680, 680A, 682 are complementary with BD675, 675A, 677, 677A, 679, 679A, 681
- BD 678, 678A, 680, 680A are equivalent to MJE 700, 701, 702, 703

4.0 AMPERE
DARLINGTON
POWER TRANSISTORS
PNP SILICON

45, 60, 80, 100 VOLTS
40 WATTS



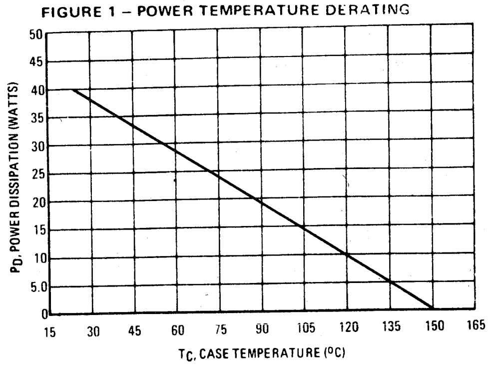
MAXIMUM RATING

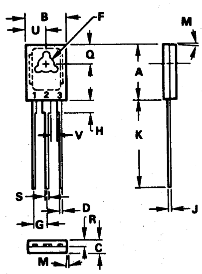
Rating	Symbol	BD676 BD676A	BD678 BD678A	BD680 BD680A	BD682	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	4.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	40 0.32				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	−55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.13	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

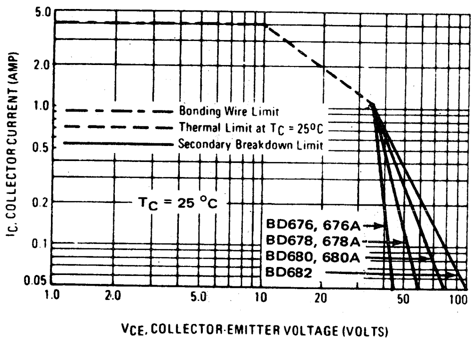
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 50 mAdc, I_B = 0)	BD676, 676A BD678, 678A BD680, 680A BD682	BV_{CEO}	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	– –	0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	BD676, 678, 680, 682 BD 676A, 678A, 680A	h_{FE}	750 750	– –	–
Collector-Emitter Saturation Voltage(1) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc)	BD 678, 680, 682 BD 676A, 678A, 680A	$V_{CE(sat)}$	– –	2.5 2.8	Vdc
Base-Emitter On Voltage(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	BD 678, 680, 682 BD 676A, 678A, 680A	$V_{BE(on)}$	– –	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

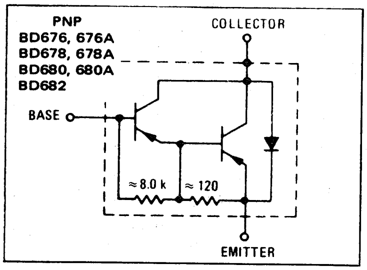
FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 – DARLINGTON CIRCUIT SCHEMATIC



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

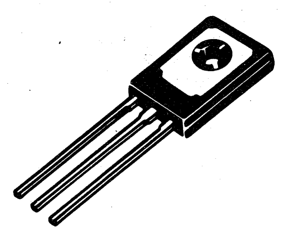
NPN	PNP
BD775	BD776
BD777	BD778
BD779	BD780

PLASTIC DARLINGTON COMPLEMENTARY SILICON ANNULAR◇ POWER TRANSISTORS

. . . designed for general purpose amplifier and high-speed switching applications such as hammer drivers for desk calculators.

- High DC Current Gain
  h_{FE} = 1400 (Typ) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage — @ 10 mAdc
  $V_{CEO\,(sus)}$ = 45 Vdc (Min) — BD775, 776
  = 60 Vdc (Min) — BD777, 778
  = 80 Vdc (Min) — BD779, 780
- Reverse Voltage Protection Diode
- Monolithic Construction with Built-in Base-Emitter output Resistor
- Thermopad II△ Construction with Hard Solder for High Reliability.

DARLINGTON 4-AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS
45, 60, 80 VOLTS
15 WATTS



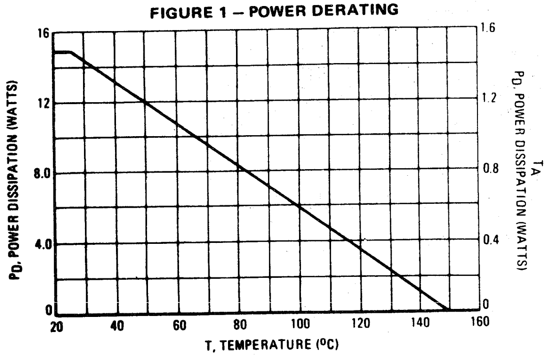
MAXIMUM RATINGS

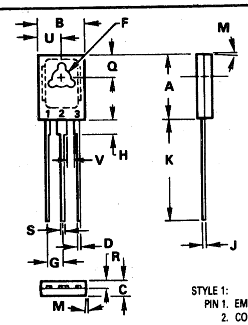
Rating	Symbol	BD775 BD776	BD777 BD778	BD779 BD780	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	4.0 6.0			Adc
Base Current	I_B	100			mAdc
Total Device Dissipation T_C = 25°C — Derate above 25°C	P_D	15 0.12			Watts W/°C
Operating and Storage junction Temperature Range	T_J, T_{stg}	− 65 to + 150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R\theta JC$	8.34	°C/W
Thermal Resistance, junction to Ambient	$R\theta JA$	83.3	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-126

◇ Annular Semiconductors Patented by Motorola Inc.
△ Trademark of Motorola Inc.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
OFF CHARACTERISTICS				
Collector-Emitter Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0) BD775, BD776 BD777, BD778 BD779, BD780	V_{CEO} (sus)	45 60 80		Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) BD775, BD776 (V_{CE} = 30 Vdc, I_B = 0) BD777, BD778 (V_{CE} = 40 Vdc, I_B = 0) BD779, BD780	I_{CEO}		100 100 100	μAdc
Collector Cutoff Current (V_{CB} = Rated, V_{CEO} (sus), I_E = 0) (V_{CB} = Rated, V_{CEO} (sus), I_E = 0, I_C = 100 °C)	I_{CBO}		1.0 100	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		1.0	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	H_{FE}	750		
Collector-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 6mAdc)	V_{CE} (Sat)		1.5	Vdc
Base Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 6 mAdc)	V_{BE} (Sat)		2.5	Vdc
Base-Emitter On Voltage (I_C = 1.5Adc, V_{CE} = 3 Vdc)	V_{BE} (On)		2.3	Vdc
Output Diode Voltage Drop (I_{EC} = 2.0 Adc)	V_{EC}		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	f_T	20		MHz
	SYMBOL		**TYP.**	**UNIT**
Turn-On Time (I_C = 250 mA/V_{CE} = 2 V) BD775-777-779 BD776-778-780	t_{on}	25	250 250 150	ns
Turn Off Time (I_C = 250 mA, V_{CE} = 2 V) BD775-777-779 BD776-778-780	t_{off}		600 400	ns

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

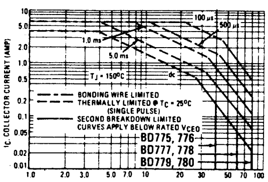


FIGURE 3 – TYPICAL DC CURRENT GAIN

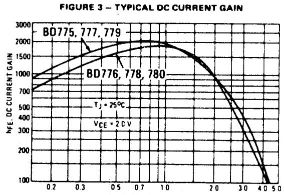
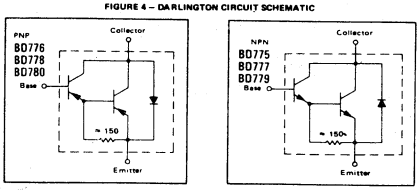


FIGURE 4 – DARLINGTON CIRCUIT SCHEMATIC



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

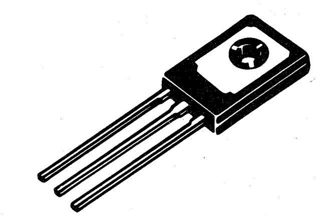
NPN
BD785, BD787
PNP
BD786, BD788

COMPLEMENTARY PLASTIC SILICON ANNULAR♦ POWER TRANSISTORS

. . . designed for low power audio amplifier and low current, high-speed switching applications.

- Low Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ 45 Vdc (Min) – BD785, BD786
  60 Vdc (Min) – BD787, BD788
- High Current-Gain – Bandwidth Product –
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- DC Current Gain Specified at 0.2, 1.0, 2.0 and 4.0 Adc
- Collector-Emitter Saturation Voltage Specified at 0.5, 1.0, 2.0 and 4.0 Adc

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
45, 60 VOLTS
15 WATTS



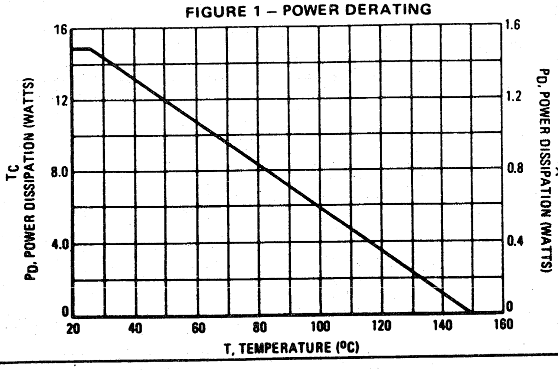
*MAXIMUM RATINGS

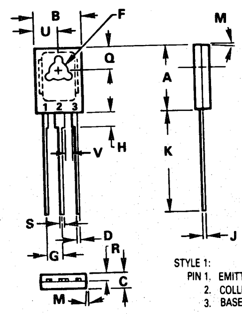
Rating	Symbol	BD785 BD786	BD787 BD788	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	Vdc
Collector-Base Voltage	V_{CBO}	60	80	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current – Continuous – Peak	I_C	4.0 8.0		Adc Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ $T_C = 25°C$ Derate Above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-126

3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

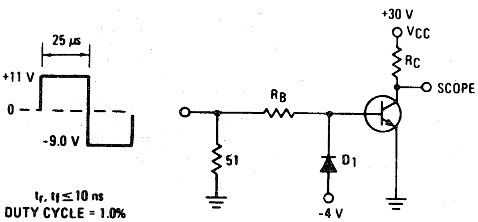
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	BD785, BD786	$V_{CEO(sus)}$	45	–	Vdc
	BD787, BD788		60	–	
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	BD785, BD786	I_{CEO}	–	100	μAdc
(V_{CE} = 30 Vdc, I_B = 0)	BD787, BD788		–	100	
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	BD785, BD786	I_{CEX}	–	1.0	μAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	BD787, BD788		–	1.0	
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	BD785, BD786		–	0.1	mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C	BD787, BD788		–	0.1	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 3.0 Vdc)		h_{FE}	40	250	–
(I_C = 1.0 Adc, V_{CE} = 3.0 Vdc)			25	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			20	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)		$V_{CE(sat)}$	–	0.4	Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	0.6	
(I_C = 2.0 Adc, I_B = 200 mAdc)			–	0.8	
(I_C = 4.0 Adc, I_B = 800 mAdc)			–	2.5	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter on Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	50	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_C = 0) f = 0.1 MHz)	BD785, BD787	C_{ob}	–	50	pF
	BD786, BD788		–	70	
Small-Signal Current Gain (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	10	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

3

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 — TURN-ON TIME

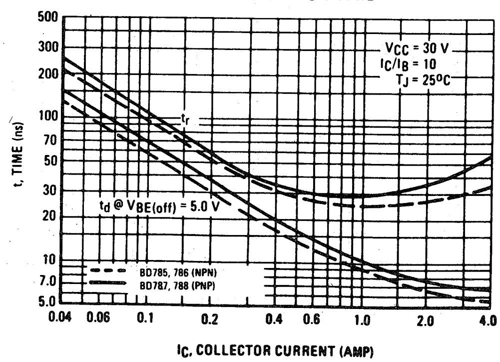


FIGURE 4 – THERMAL RESPONSE

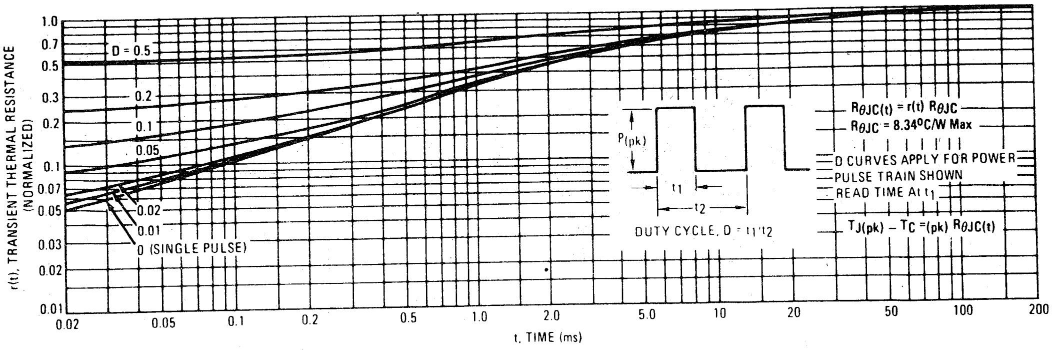
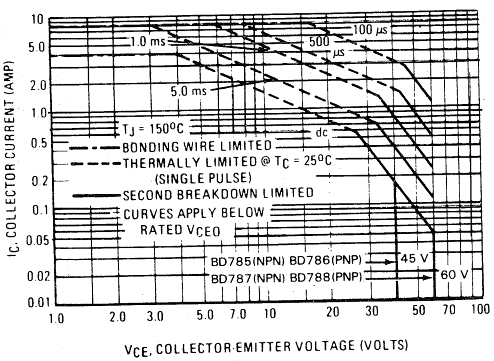


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 6 – TURN-OFF TIME

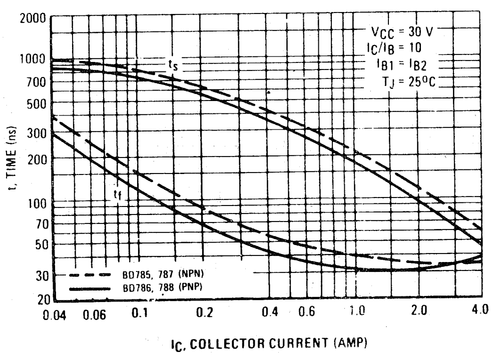
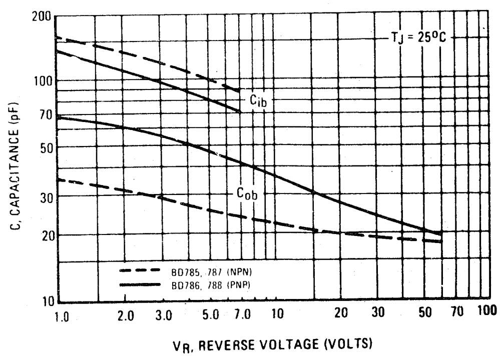


FIGURE 7 – CAPACITANCE



3

NPN BD785, BD787 | **PNP BD786, BD788**

FIGURE 8 – DC CURRENT GAIN

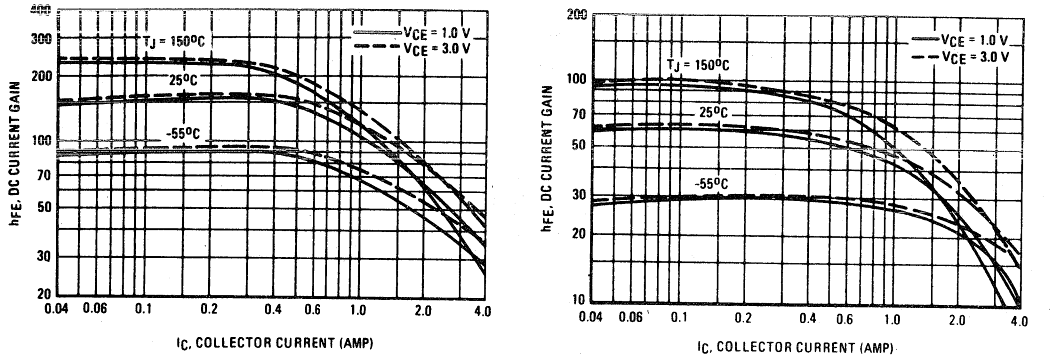


FIGURE 9 – "ON" VOLTAGES

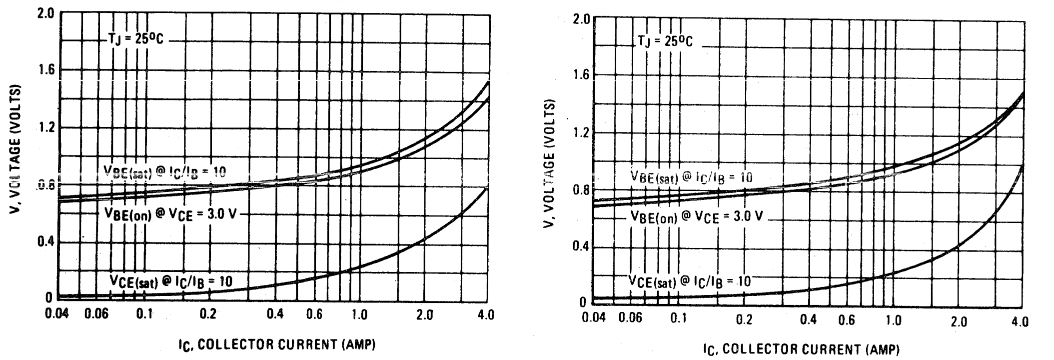
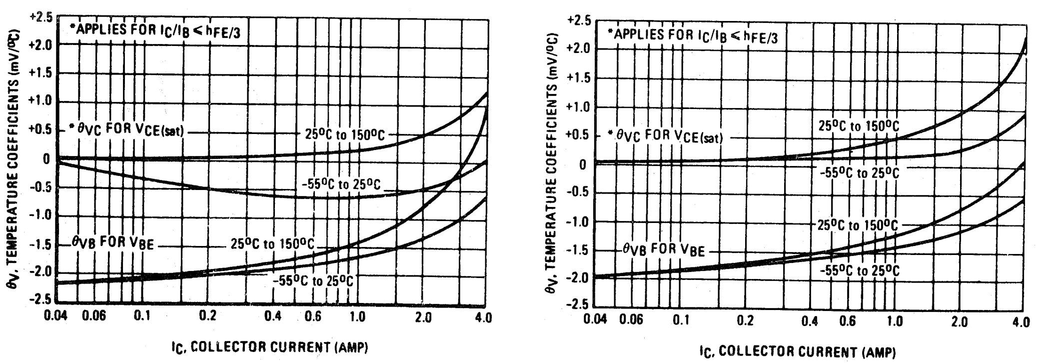


FIGURE 10 – TEMPERATURE COEFFICIENTS



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

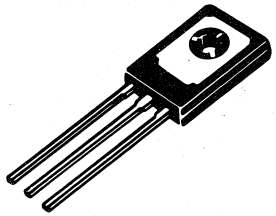
NPN
BD789, BD791
PNP
BD790, BD792

COMPLEMENTARY PLASTIC SILICON ANNULAR◆ POWER TRANSISTORS

. . . designed for low power audio amplifier and low-current, high speed switching applications.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — BD789, BD790
  = 100 Vdc (Min) —BD791, BD792
- High DC Current Gain @ I_C = 200 mAdc
  h_{FE} = 40-250
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 500 mAdc
- High Current Gain — Bandwidth Product —
  f_T = 40 MHz (Min) @ I_C = 100 mAdc)

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
80, 100 VOLTS
15 WATTS



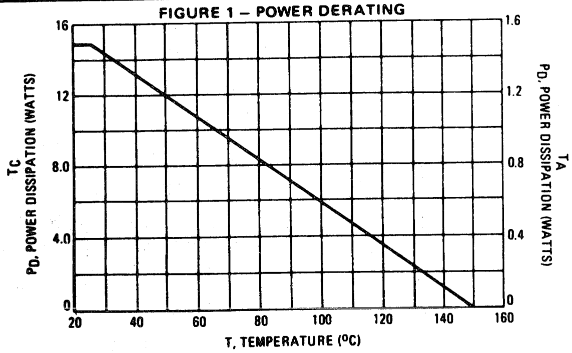
*MAXIMUM RATINGS

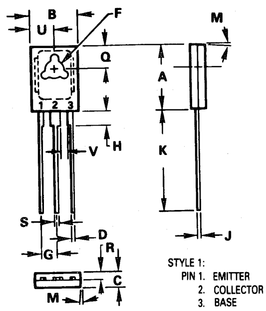
Rating	Symbol	BD789 BD790	BD791 BD792	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current — Continuous — Peak	I_C	4.0 8.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	15 0.12		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	$^oC/W$

FIGURE 1 — POWER DERATING





NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-126

3

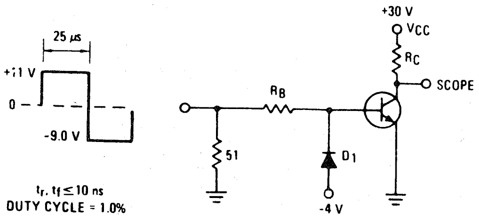
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0) BD789, BD790	$V_{CEO(sus)}$	80	–	Vdc
BD791, BD792		100	–	
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) BD789, BD790	I_{CEO}	–	100	μAdc
(V_{CE} = 50 Vdc, I_B = 0) BD791, BD792		–	100	
Collector Cutoff Current (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) BD789, BD790	I_{CEX}	–	1.0	μAdc
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) BD791, BD792		–	1.0	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) BD789, BD790		–	0.1	mAdc
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) BD791, BD792		–	0.1	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 200 mAdc, V_{CE} = 3.0 Vdc)	h_{FE}	40	250	–
(I_C = 1.0 Adc, V_{CE} = 3.0 Vdc)		20	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		10	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		5.0	–	
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	–	0.5	Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc)		–	1.0	
(I_C = 2.0 Adc, I_B = 200 mAdc)		–	2.5	
(I_C = 4.0 Adc, I_B = 800 mAdc)		–	3.0	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	–	1.8	Vdc
Base-Emitter On Voltage (I_C = 200 mAdc, V_{CE} = 3.0 Vdc)	$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)	f_T	40	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_C = 0, f = 0.1 MHz) BD789, BD791	C_{ob}	–	50	pF
BD790, BD792		–	70	
Small-Signal Current Gain (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	10	–	–

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 — TURN-ON TIME

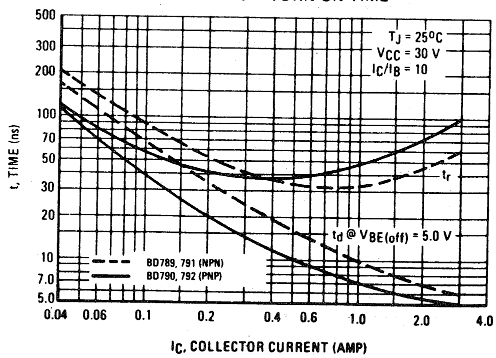


FIGURE 4 – THERMAL RESPONSE

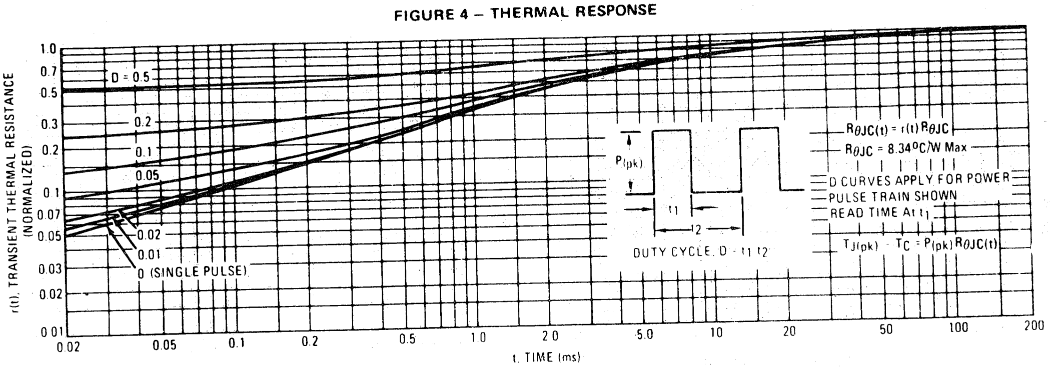
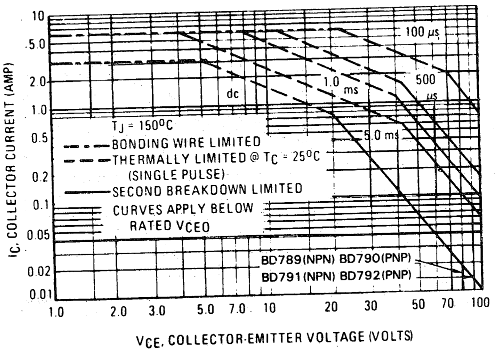


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 6 – TURN-OFF TIME

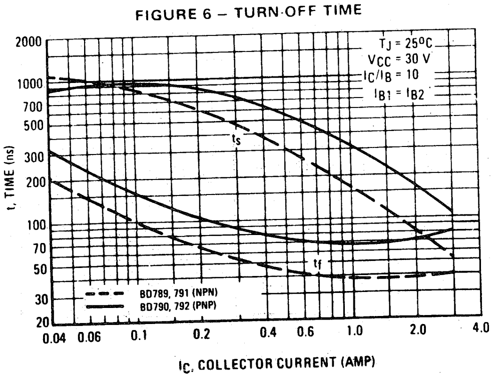
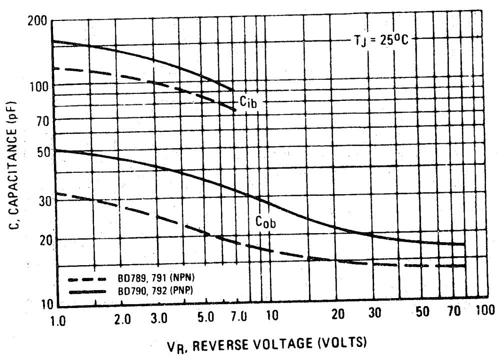


FIGURE 7 – CAPACITANCE



3

NPN
BD789, BD791

PNP
BD790, BD792

FIGURE 8 – DC CURRENT GAIN

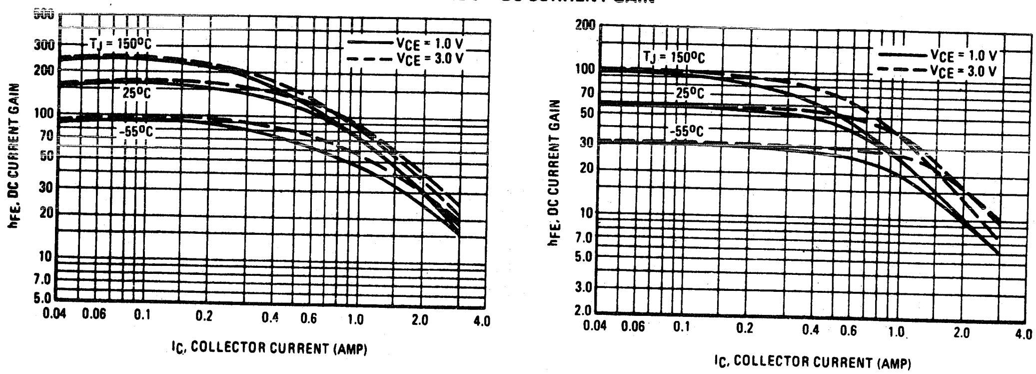


FIGURE 9 – "ON" VOLTAGES

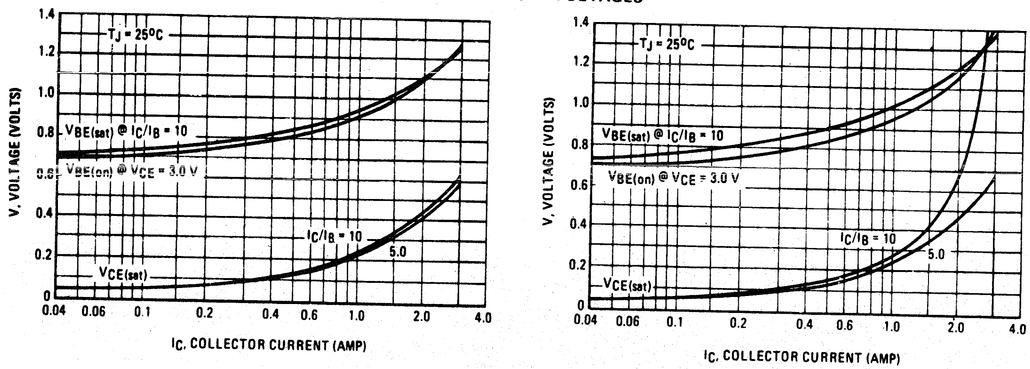
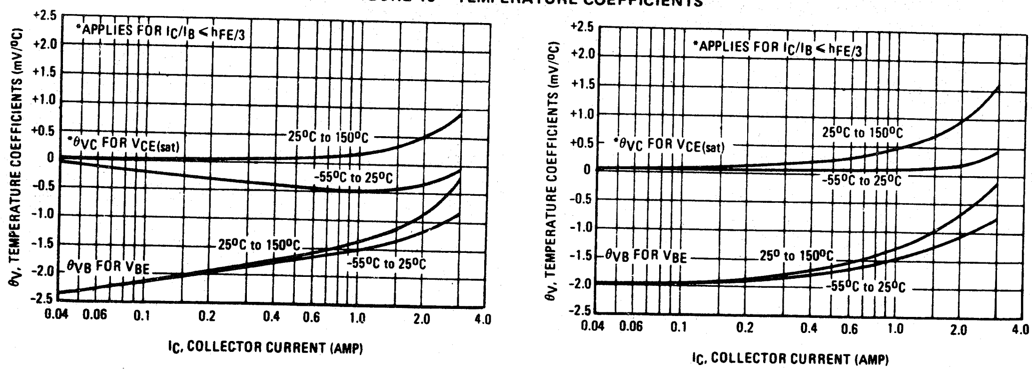


FIGURE 10 – TEMPERATURE COEFFICIENTS



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD795 BD797 BD799 BD801

PLASTIC HIGH POWER SILICON NPN TRANSISTOR

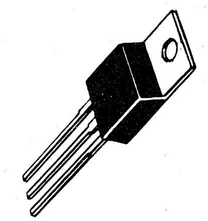
. . . designed for use up to 30 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- **BD 795, 797, 799, 801 are complementary with BD 796, 798, 800, 802**

8 AMPERE POWER TRANSISTOR

NPN SILICON

45, 60, 80, 100 VOLTS
65 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD795 BD797 BD799 BD801	45 60 80 100	Vdc
Collector-Base Voltage	V_{CBO}	BD795 BD797 BD799 BD801	45 60 80 100	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		8	Adc
Base Current	I_B		3	Adc
Total Device Dissipation T_C = 25°C Derate avove 25°C	P_D		65 522	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

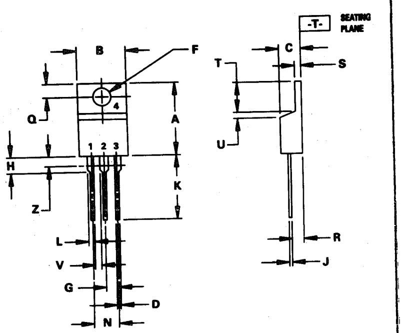
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.92	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) (I_C = 0.05 Adc, I_B = 0)	BV_{CEO}*	BD795 BD797 BD799 BD801	45 60 80 100	— — — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	BD795 BD797 BD799 BD801	— — — —	0.1 0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 1 A, V_{CE} = 2 V) (I_C = 3 A, V_{CE} = 2 V)	h_{FE}*	BD 795/797 BD 799/801 BD 795/797 BD 799/801	40 30 25 15	— — — —	
Collector-Emitter Saturation Voltage* (I_C = 3 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 3 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 0.25Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

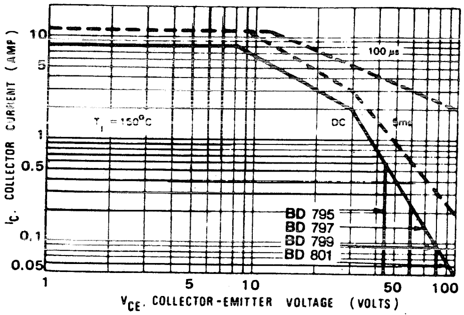
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

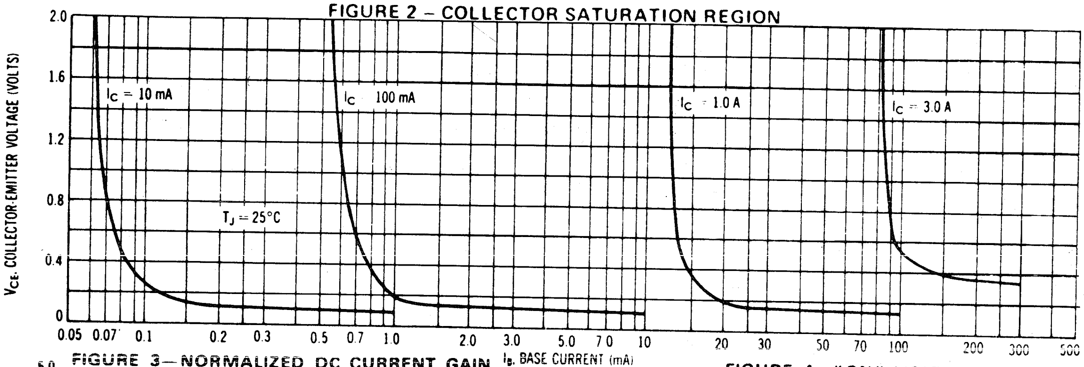


FIGURE 3 – NORMALIZED DC CURRENT GAIN

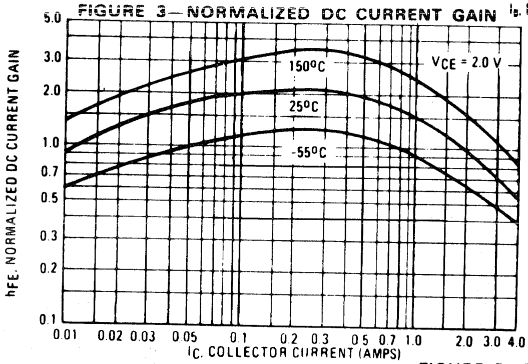


FIGURE 4 – "ON" VOLTAGE

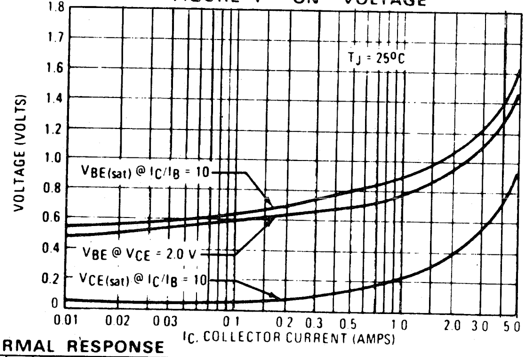
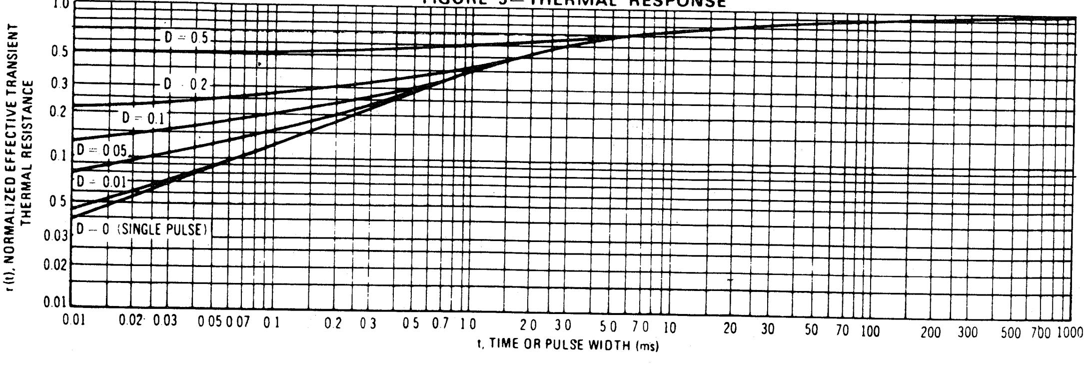


FIGURE 5 – THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD796 BD798 BD800 BD802

PLASTIC HIGH POWER SILICON PNP TRANSISTOR

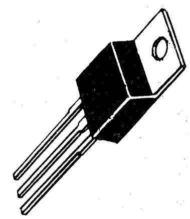
. . . designed for use up to 30 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- BD 796, 798, 800, 802 are complementary with BD 795, 797, 799, 801

8 AMPERE POWER TRANSISTOR

PNP SILICON

45, 60, 80, 100 VOLTS 65 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD796 BD798 BD800 BD802	45 60 80 100	Vdc
Collector-Base Voltage	V_{CBO}	BD796 BD798 BD800 BD802	45 60 80 100	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		8	Adc
Base Current	I_B		3	Adc
Total Device Dissipation T_C=25°C Derate avove 25°C	P_D		65 522	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to +150	°C

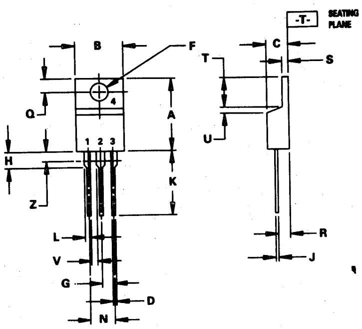
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.92	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) (I_C = 0.05 Adc, I_B = 0)	BV_{CEO}*	BD796 BD798 BD800 BD802	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	BD796 BD798 BD800 BD802	– – – –	0.1 0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 1 A, V_{CE} = 2 V) (I_C = 3 A, V_{CE} = 2 V)	h_{FE}*	BD 796/798 BD 800/802 BD 796/788 BD 800/802	40 30 25 15	– – – –	
Collector-Emitter Saturation Voltage* (I_C = 3 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 3 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 0.25Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

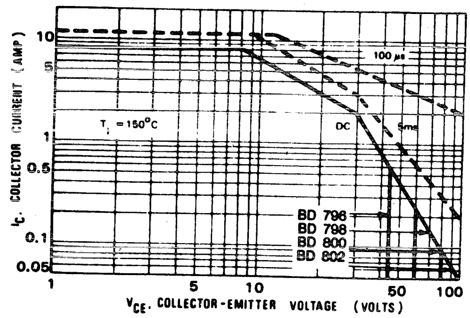
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

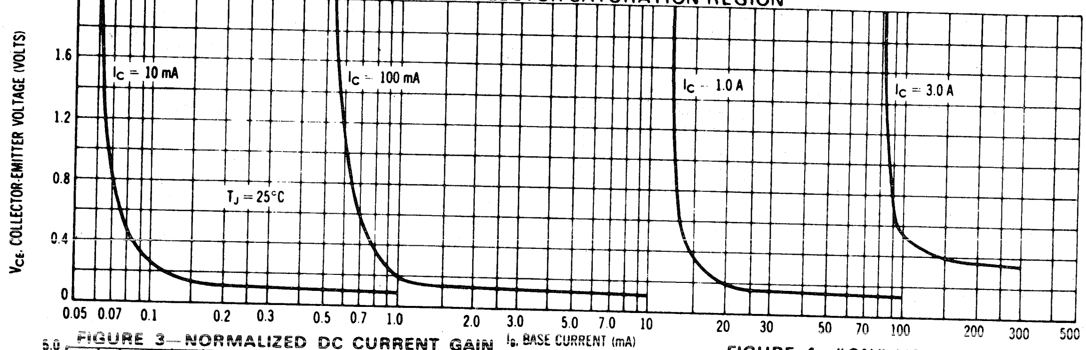


FIGURE 3 – NORMALIZED DC CURRENT GAIN

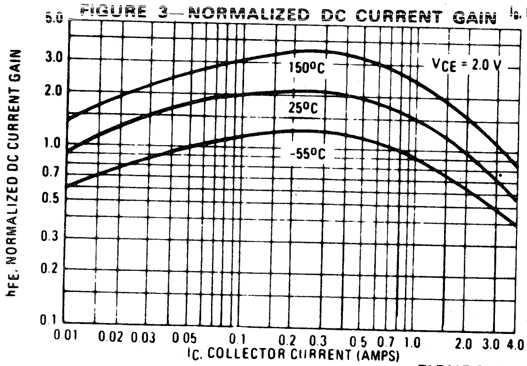


FIGURE 4 – "ON" VOLTAGE

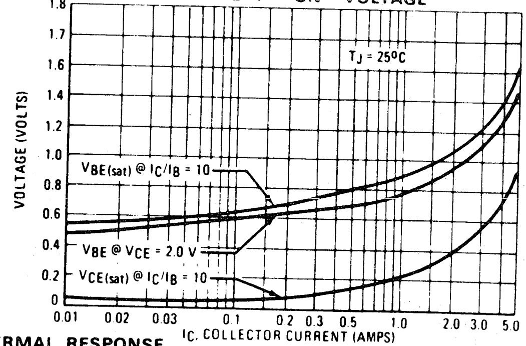
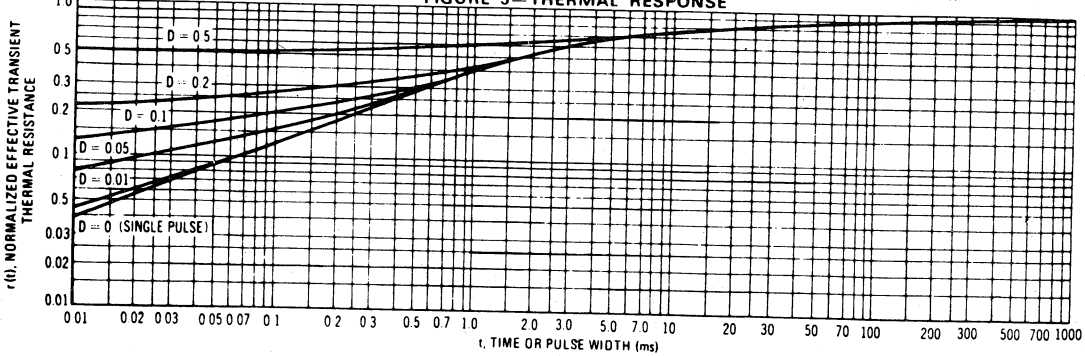


FIGURE 5 – THERMAL RESPONSE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD805
BD807
BD809

PLASTIC HIGH POWER SILICON NPN TRANSISTOR

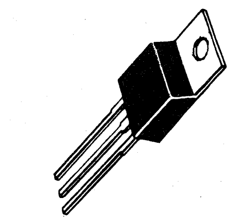
. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current—h_{FE} = 30 (Min) @ I_C = 2.0 Adc
- BD 805, 807, 809 are complementary with BD 806, 808, 810

10 AMPERE POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
90 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD805 BD807 BD809	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD805 BD807 BD809	55 70 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

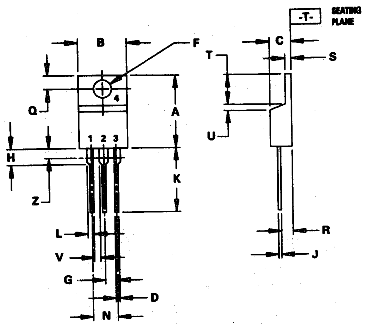
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.39	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.2 Adc, I_B = 0)	BV_{CEO}*	BD805 BD807 BD809	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD805 BD807 BD809	— — —	1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	2.0	mAdc
DC current Gain (I_C = 2A, V_{CE} = 2 V) (I_C = 4A, V_{CE} = 2 V)	h_{FE}*		30 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$*		—	1.1	Vdc
Base-Emitter On Voltage* (I_C = 4 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		1.5	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



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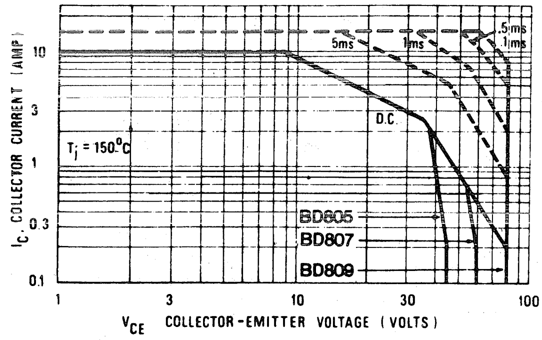
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

FIGURE 1 — ACTIVE REGION DC SAFE OPERATING AREA



See Note 1

FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

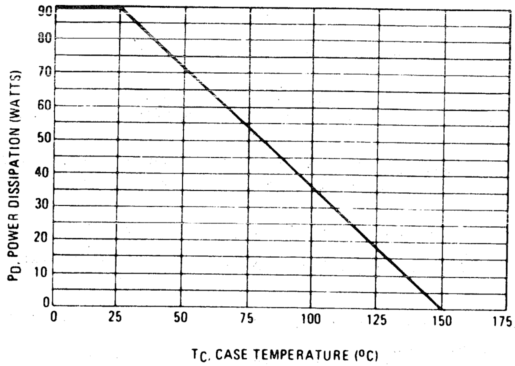


FIGURE 3 — "ON" VOLTAGES

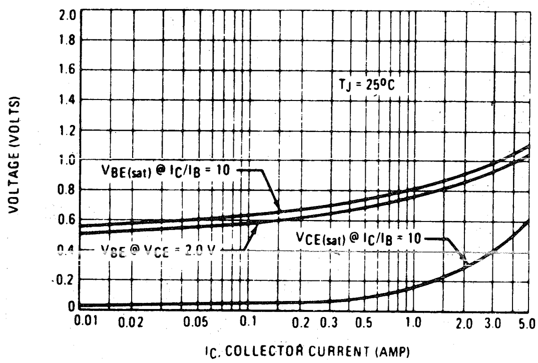


FIGURE 4 — CURRENT GAIN

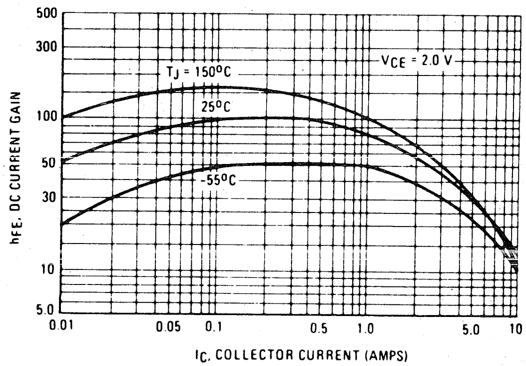
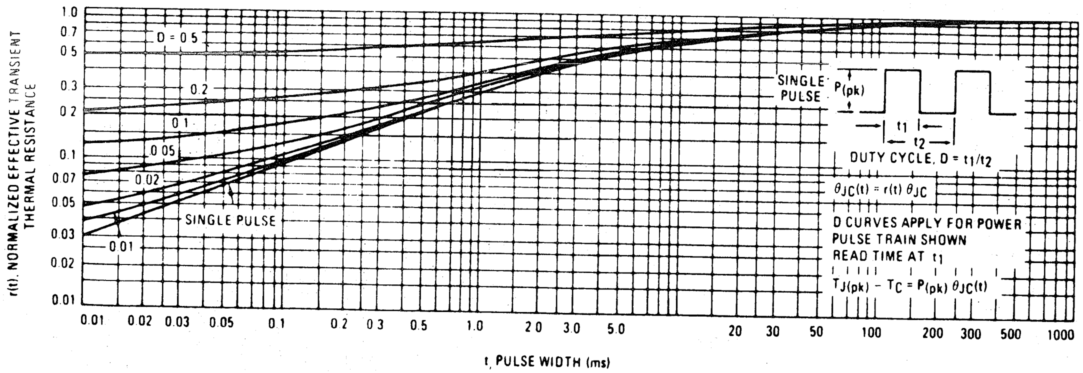


FIGURE 5 — THERMAL RESPONSE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD806
BD808
BD810

PLASTIC HIGH POWER SILICON PNP TRANSISTOR

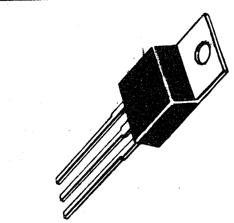
. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current—h_{FE} = 30 (Min) @ I_C = 2.0 Adc
- BD 806, 808, 810 are complementary with BD 805, 807, 809

10 AMPERE POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS 90 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD806 BD808 BD810	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD806 BD808 BD810	55 70 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to +150	°C

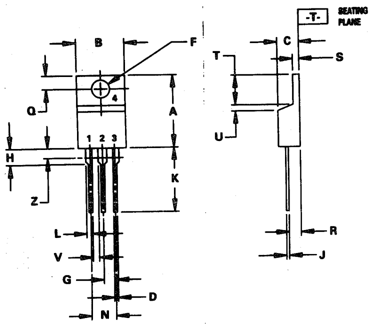
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Résistance, Junction to Case	θ_{JC}		1.39	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.2 Adc, I_B = 0)	BV_{CEO}*	BD806 BD808 BD810	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD806 BD808 BD810	— — —	1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	2.0	mAdc
DC current Gain (I_C = 2A, V_{CE} = 2 V) (I_C = 4A, V_{CE} = 2 V)	h_{FE}*		30 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$*		—	1.1	Vdc
Base-Emitter On Voltage* (I_C = 4 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		1.5	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

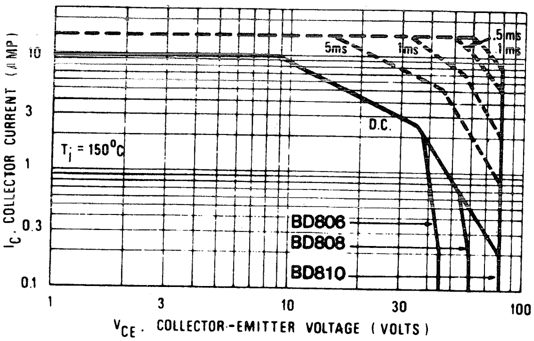
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

FIGURE 1 – ACTIVE REGION DC SAFE OPERATING AREA



See Note 1

FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

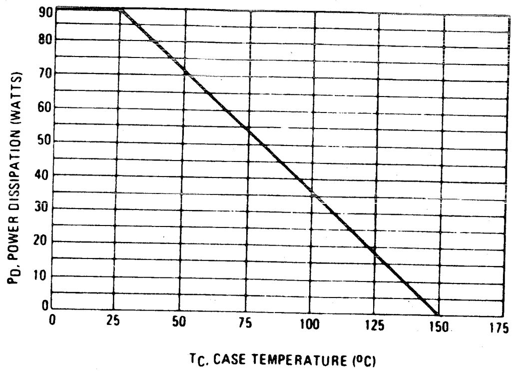


FIGURE 3 – "ON" VOLTAGES

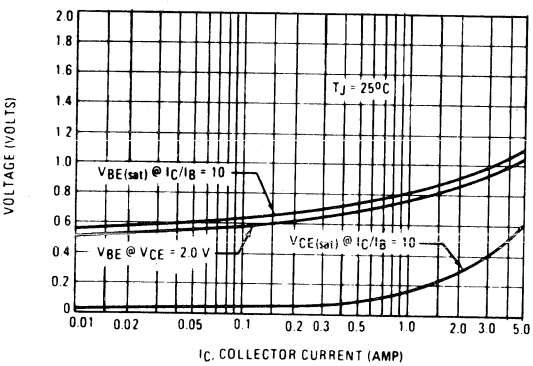


FIGURE 4 – CURRENT GAIN

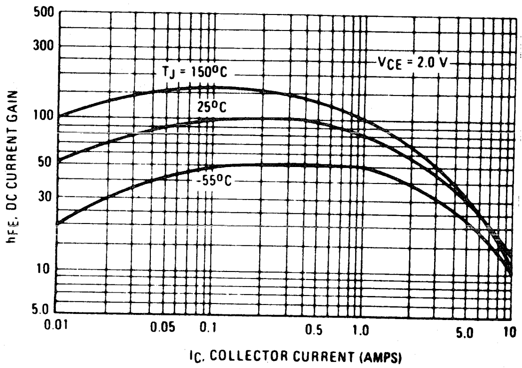
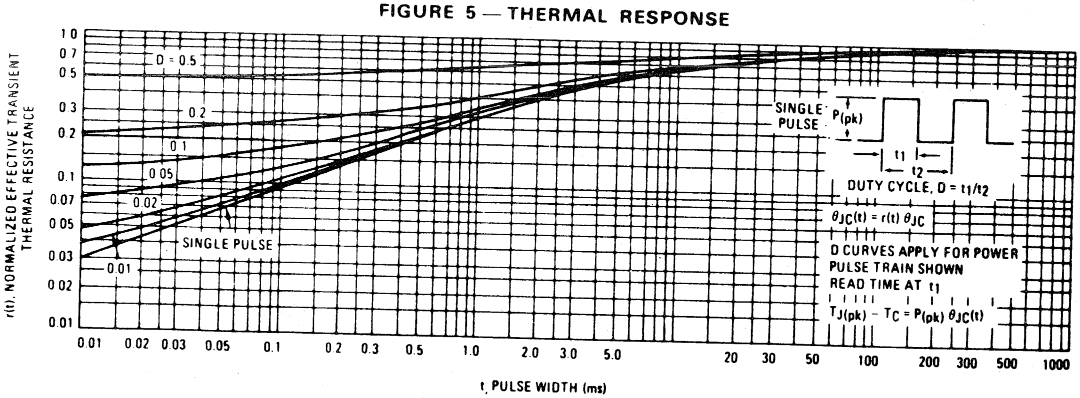


FIGURE 5 — THERMAL RESPONSE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD895, BD895A
BD897, BD897A
BD899, BD899A
BD901

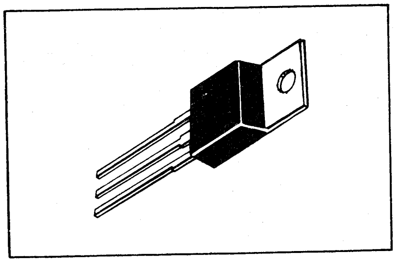
PLASTIC POWER SILICON NPN DARLINGTONS

. . . for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain — h_{FE} = 750 (Min) @ I_C = 3.0 and 4.0 Adc
- Monolithic Construction
- BD895, 895A, 897, 897A, 899, 899A, 901 are complementary with BD896, 896A, 898, 898A, 900, 900A, 902.
- Electrical equivalents to BD695A, 697, 697A, 699, 699A, 701.

DARLINGTON
8 AMPERE
NPN SILICON
POWER TRANSISTORS

45-60-80-100 VOLTS
70 WATTS

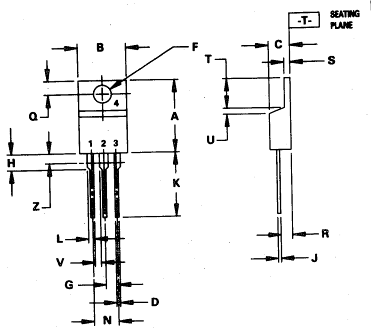


MAXIMUM RATINGS

Rating	Symbol	BD895 BD895A	BD897 BD897A	BD899 BD899A	BD901	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	8.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	70 0.56				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.79	°C/W



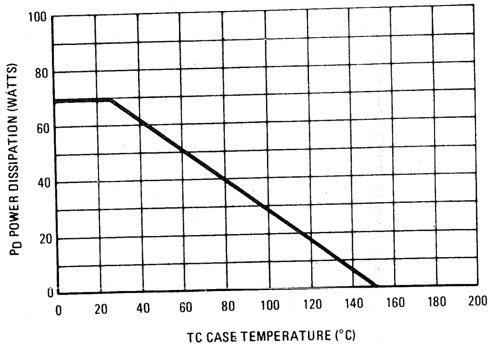
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

FIGURE 1 — POWER TEMPERATURE DERATING CURVE



3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage[1] (I_C = 100 mAdc, I_B = 0)	BD895, 895A BD897, 897A BD899, 899A BD901	BV_{CEO}	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	—	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100 °C)		I_{CBO}	– –	0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	BD895, 897, 899, 901 BD895A, 897A, 899A	h_{FE}	750 750	– –	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc) (I_C = 4.0 Adc, I_B = 16 mAdc)	BD895, 897, 899, 901 BD895A, 897A, 899A	$V_{CE(sat)}$	– –	2.5 2.8	Vdc
Base-Emitter On Voltage[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	BD895, 897, 899, 901 BD895A, 897A, 899A	$V_{BE(on)}$	– –	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

[1] Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2.0%.

There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown (see AN-415).

FIGURE 2 — DC SAFE OPERATING AREA

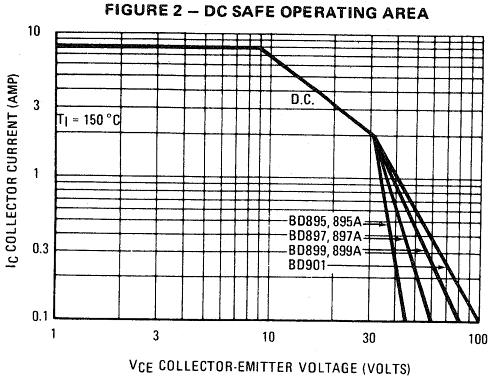
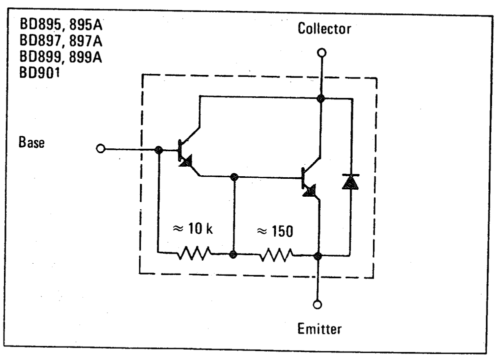


FIGURE 3 — DARLINGTON CIRCUIT SCHEMATIC



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD896, BD896A
BD898, BD898A
BD900, BD900A
BD902

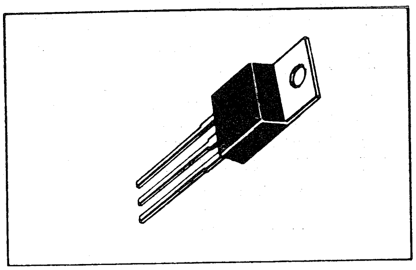
PLASTIC MEDIUM-POWER PNP TRANSISTORS

. . . for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain – h_{FE} = 750 (Min) @ I_C = 3.0 and 4.0 Adc
- Monolithic Construction
- **BD896A, 898, 898A, 900, 900A, 902 are complementary with BD895A, 897, 897A, 899, 899A, 901**
- **Electrical equivalents to BD696A, 698, 698A, 700, 700A, 702**

DARLINGTON
8 AMPERE
SILICON
POWER TRANSISTORS

45-60-80-100 VOLTS
70 WATTS



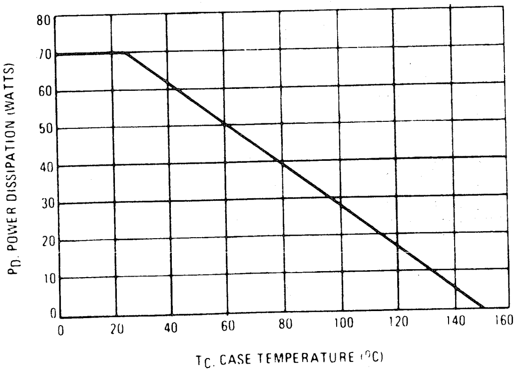
MAXIMUM RATINGS

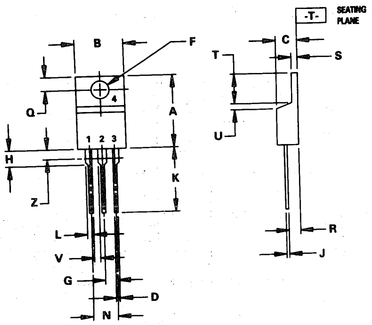
Rating	Symbol	BD696 BD696A	BD898 BD898A	BD900 BD900A	BD902	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	8.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	70 0.56				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	-55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.79	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING CURVE





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

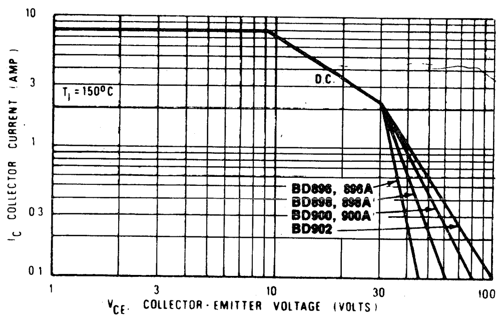
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage[1] (I_C = 100 mAdc, I_B = 0)	BD896, 896A BD898, 898A BD900, 900A BD902	BV_{CEO}	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	– –	0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	BD896, 898, 900, 902 BD896A, 898A, 900A	h_{FE}	750 750	– –	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc) (I_C = 4.0 Adc, I_B = 16 mAdc)	BD896, 898, 900, 902 BD896A, 898A, 900A	$V_{CE(sat)}$	– –	2.5 2.8	Vdc
Base-Emitter On Voltage[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	BD896, 898, 900, 902 BD896A, 898A, 900A	$V_{BE(on)}$	– –	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

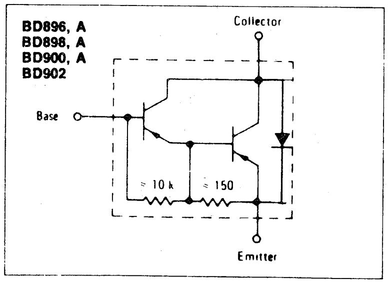
FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 - DARLINGTON CIRCUIT SCHEMATIC



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
BDV65	**BDV64**
BDV65A	**BDV64A**
BDV65B	**BDV64B**
BDV65C	**BDV64C**

COMPLEMENTARY SILICON PLASTIC POWER DARLINGTONS

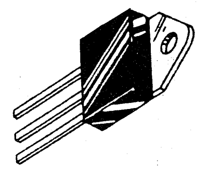
. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain
  HFE = 1000 (min.) @ 5 Adc
- Monolithic Construction with Built-in Base Emitter Shunt Resistors

DARLINGTONS
10 AMPERES

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80-100-120 VOLTS
125 WATTS

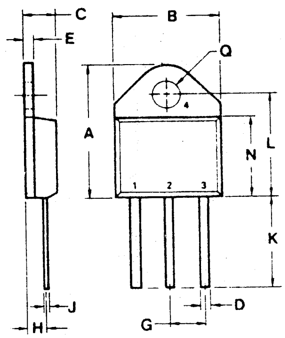


MAXIMUM RATINGS

Rating	Symbol	BDV 65 BDV 64	BDV 65A BDV 64A	BDV 65B BDV 64B	BDV 65C BDV 64C	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	120	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	5				Vdc
Collector Current – Continuous – Peak	I_C	10 20				Adc
Base Current	I_B	0.5				Adc
Total Device Dissipation @ Tc = 25°C Derate above 25°C	P_D	125 1				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150				°C

THERMAL CHARACTERISTICS

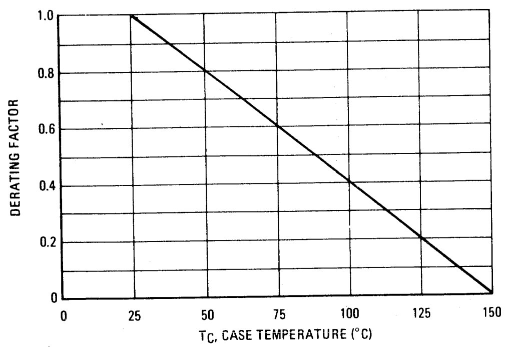
Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1	°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
(TO-218AC)

FIGURE 1 – POWER DERATING



3

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO\ (sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	BDV65 -BDV64		60		
	BDV65A-BDV64A		80		
	BDV65B-BDV64B		100		
	BDV65C-BDV64C		120		
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	BDV65 -BDV64			1	
(V_{CE} = 40 Vdc, I_B = 0)	BDV65A-BDV64A			1	
(V_{CE} = 50 Vdc, I_B = 0)	BDV65B-BDV64B			1	
(V_{CE} = 60 Vdc, I_B = 0)	BDV65C-BDV64C			1	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	BDV65 -BDV64			.4	
(V_{CB} = 80 Vdc, I_E = 0)	BDV65A-BDV64A			.4	
(V_{CB} = 100 Vdc, I_E = 0)	BDV65B-BDV64B			.4	
(V_{CB} = 120 Vdc, I_E = 0)	BDV65C-BDV64C			.4	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 30 Vdc, I_E = 0, T_C = 150°C)	BDV65 -BDV64			2	
(V_{CB} = 40 Vdc, I_E = 0, T_C = 150°C)	BDV65A-BDV64A			2	
(V_{CB} = 50 Vdc, I_E = 0, T_C = 150°C)	BDV65B-BDV64B			2	
(V_{CB} = 60 Vdc, I_E = 0, T_C = 150°C)	BDV65C-BDV64C			2	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}		5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5 Adc, V_{CE} = 4 Vdc)		HFE	1000		
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.02 Adc)		$V_{CE\ (sat)}$		2	Vdc
Base-Emitter Saturation Voltage (I_C = 5 Adc, V_{CE} = 4 Vdc)		$V_{BE\ (on)}$		2.5	Vdc

3

NPN

PNP

FIGURE 2 – DC CURRENT GAIN

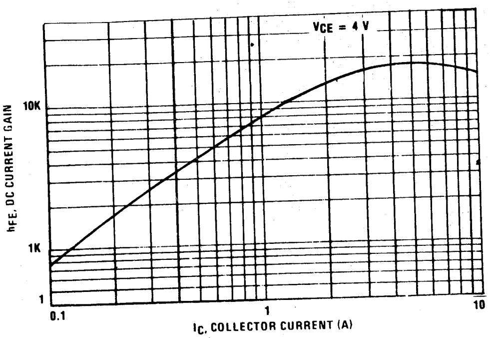


FIGURE 3 – DC CURRENT GAIN

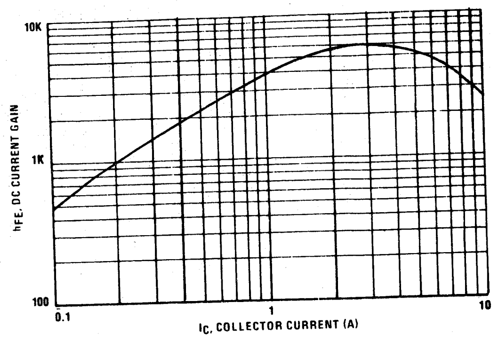


FIGURE 4 – "ON" VOLTAGES

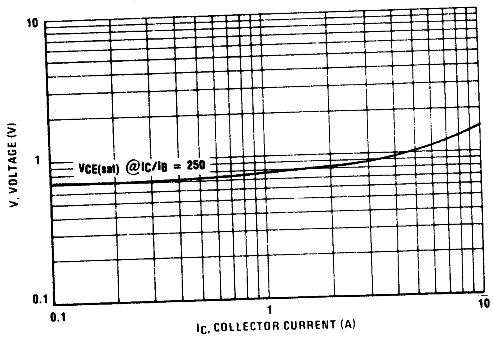


FIGURE 5 – "ON" VOLTAGES

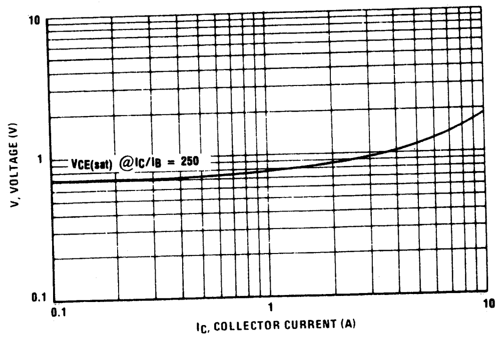
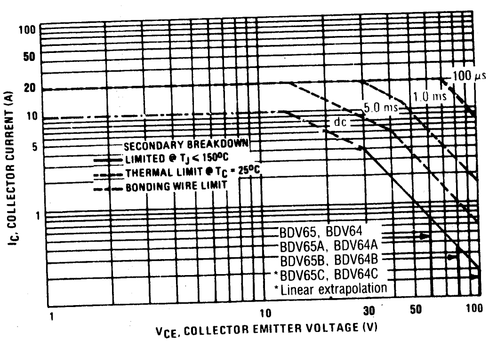


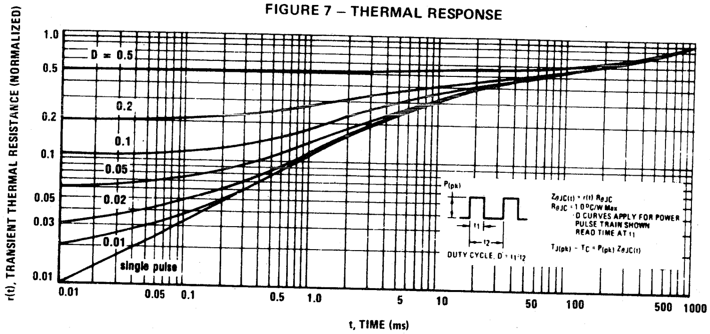
FIGURE 6 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 6 is based on $T_{J(pk)}$ 150°C, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. $T_{J(pk)}$ may be calculated from the data in figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 7 – THERMAL RESPONSE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

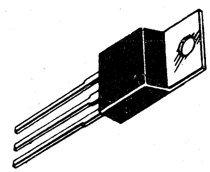
NPN	PNP
BDW39 thru BDW43	BDW44 thru BDW48

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general purpose and low speed switching applications.

- High DC Current Gain — h_{FE} = 2500 (typ.) @ I_C = 5.0 Adc.
- Collector Emitter Sustaining Voltage @ 30 mAdc:
  $V_{CEO(sus)}$ = 45 Vdc (min.) — BDW39/BDW44
  60 Vdc (min.) — BDW40/BDW45
  80 Vdc (min.) — BDW41/BDW46
  100 Vdc (min.) — BDW42/BDW47
  120 Vdc (min.) — BDW43/BDW48
- Low Collector Emitter Saturation Voltage:
  $V_{CE(sat)}$ = 2.0 Vdc (max.) @ I_C = 5.0 Adc
  3.0 Vdc (max.) @ I_C = 10.0 Adc
- Monolithic Construction with Built-In Base Emitter Shunt resistors
- TO-220AB Compact Package
- TO-66 Lead form also available ordered with "-66" suffix.

DARLINGTON
15 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
45-60-80-100-120 VOLTS
85 WATTS



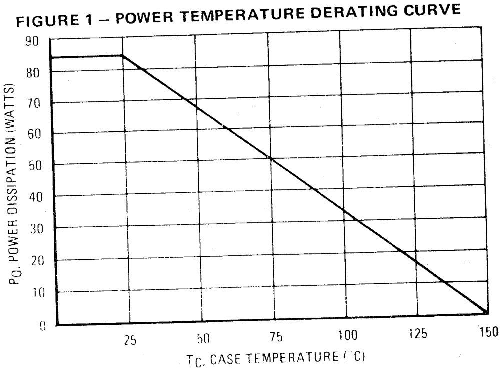
MAXIMUM RATINGS

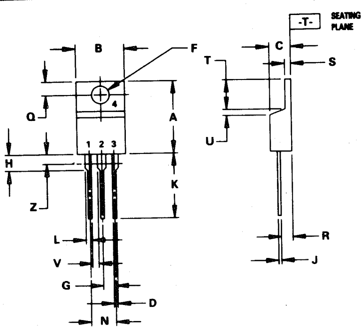
Rating	Symbol	BDW39 BDW44	BDW40 BDW45	BDW41 BDW46	BDW42 BDW47	BDW43 BDW48	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	120	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	5.0					Vdc
Collector Current – Continuous	I_C	15					Adc
Base Current	I_B	0.5					Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	85 0.68					Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150					°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.47	°C/W

FIGURE 1 — POWER TEMPERATURE DERATING CURVE





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit	
OFF CHARACTERISTICS						
Collector Emitter Sustaining Voltage [1]		$V_{CEO(sus)}$				Vdc
(I_C = 30 mAdc, I_B = 0)	BDW39/BDW44		45			
	BDW40/BDW45		60			
	BDW41/BDW46		80			
	BDW42/BDW47		100			
	BDW43/BDW48		120			
Collector Cutoff Current		I_{CEO}				mAdc
(V_{CE} = 22.5 Vdc, I_B = 0)	BDW39/BDW44			2		
(V_{CE} = 30 Vdc, I_B = 0)	BDW40/BDW45			2		
(V_{CE} = 40 Vdc, I_B = 0)	BDW41/BDW46			2		
(V_{CE} = 50 Vdc, I_B = 0)	BDW42/BDW47			2		
(V_{CE} = 60 Vdc, I_B = 0)	BDW43/BDW48			2		
Collector Cutoff Current		I_{CBO}				mAdc
(V_{CB} = 45 Vdc, I_E = 0)	BDW39/BDW44			1		
(V_{CB} = 60 Vdc, I_E = 0)	BDW40/BDW45			1		
(V_{CB} = 80 Vdc, I_E = 0)	BDW41/BDW46			1		
(V_{CB} = 100 Vdc, I_E = 0)	BDW42/BDW47			1		
(V_{CB} = 120 Vdc, I_E = 0)	BDW43/BDW48			1		
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		2		mAdc
ON CHARACTERISTICS[1]						
DC Current Gain		h_{FE}				
(I_C = 5 Adc, V_{CE} = 4.0 Vdc)			1000			
(I_C = 10 Adc, V_{CE} = 4.0 Vdc) for all except BDW43/48			250			
for BDW 43/48					250	
Collector-Emitter Saturation Voltage		$V_{CE\ (sat.)}$				Vdc
(I_C = 5 Adc, I_B = 10 mAdc)				2		
(I_C = 10 Adc, I_B = 50 mAdc)				3		
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 4 Vdc)		$V_{BE\ (on)}$		3		Vdc
SECOND BREAKDOWN[2]						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$			Adc	
BDW39/BDW40/BDW41/BDW42/BDW43	V_{CE} = 28.4 Vdc		3			
	V_{CE} = 40 Vdc		1.2			
BDW44/BDW45/BDW46/BDW47/BDW48	V_{CE} = 22.5 Vdc		3.8			
	V_{CE} = 36 Vdc		1.2			
DYNAMIC CHARACTERISTICS						
Magnitude of common emitter small signal short circuit current transfer ratio (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		f_T	4.0		MHz	
Output capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}			PF	
	BDW39/BDW40/BDW41/BDW42/BDW43			200		
	BDW44/BDW45/BDW46/BDW47/BDW48			300		
Small signal current gain I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300			

Indicates JEDEC Registered Data.

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0 %.
[2] Pulse Test non repetitive: Pulse Width = 250 ms.

3

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

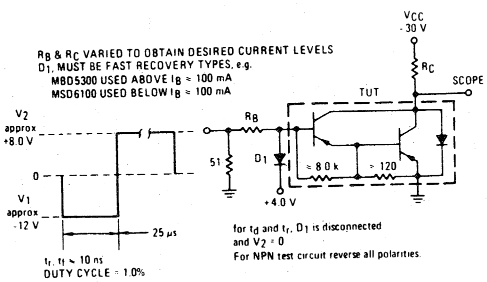


FIGURE 3 – SWITCHING TIMES

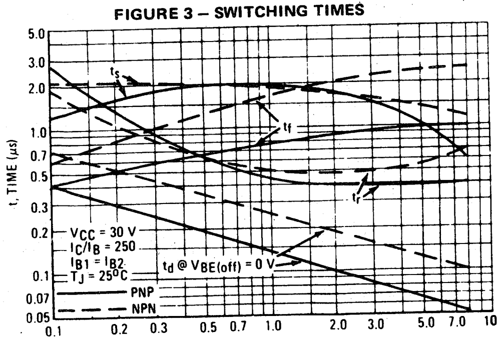
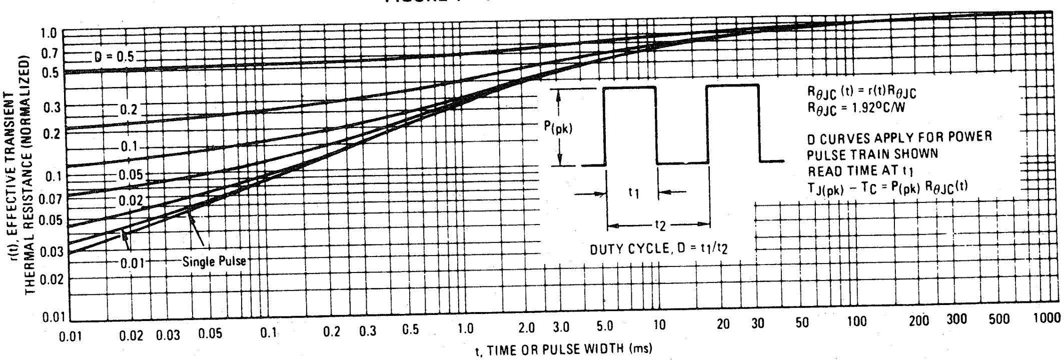


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – BDW39 THRU BDW43

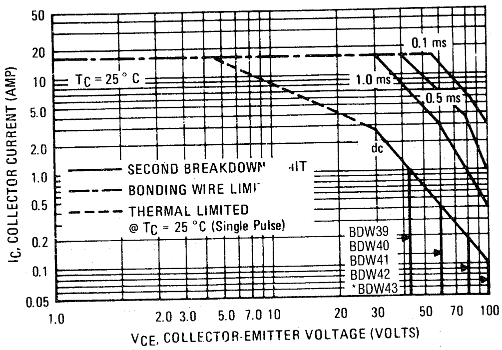
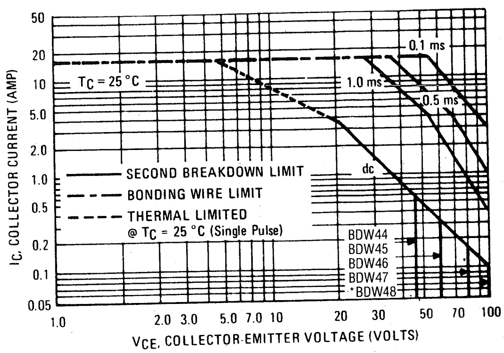


FIGURE 6 – BDW44 THRU BDW48



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Fig. 5 and 6 is based on $T_{J(pk)}$ = 200 °C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200$ °C. $T_{J(pk)}$ may be calculated from the data in Fig. 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See an-415).

*Linear extrapolation

3

FIGURE 7 — SMALL-SIGNAL CURRENT GAIN

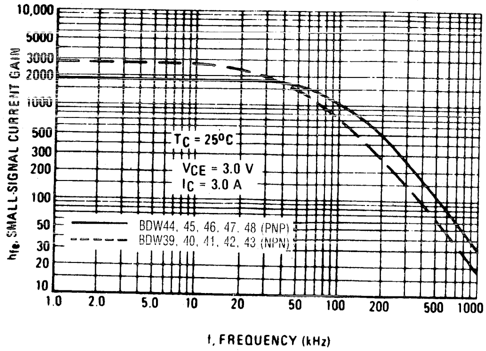
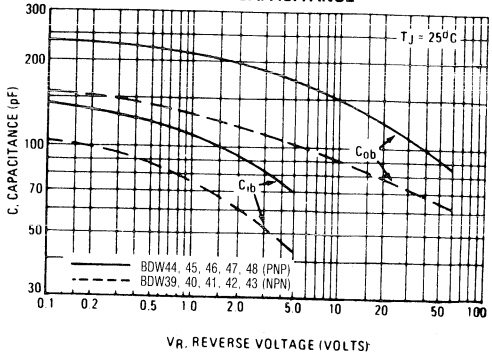


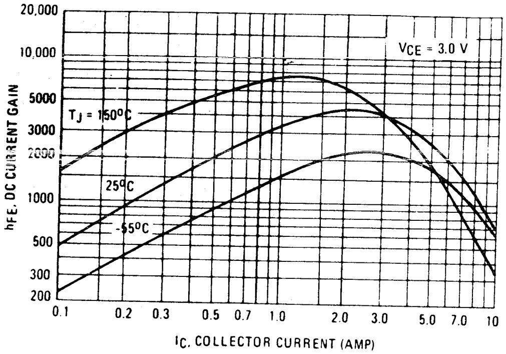
FIGURE 8 — CAPACITANCE

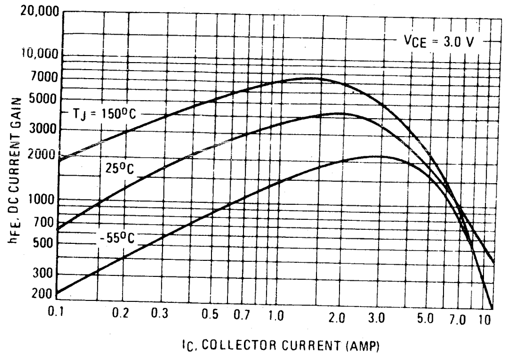


BDW39, 40, 41, 42, 43 (NPN)

BDW44, 45, 46, 47, 48 (PNP)

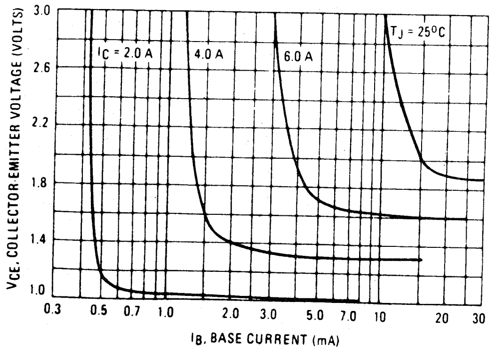
FIGURE 9 — DC CURRENT GAIN

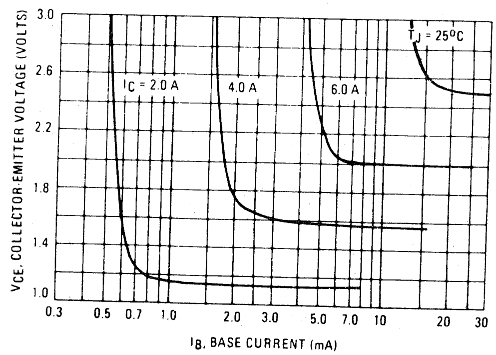




3

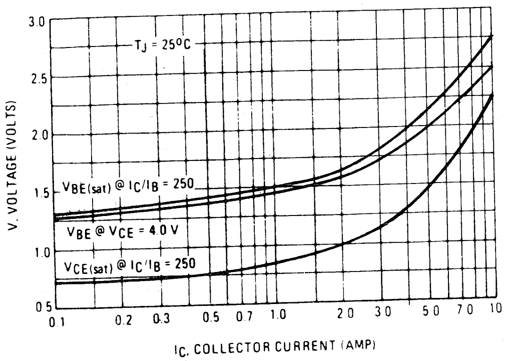
FIGURE 10 — COLLECTOR SATURATION REGION





BDW39, 40, 41, 42, 43 (NPN) | **BDW44, 45, 46, 47, 48 (PNP)**

FIGURE 11 — "ON" VOLTAGES



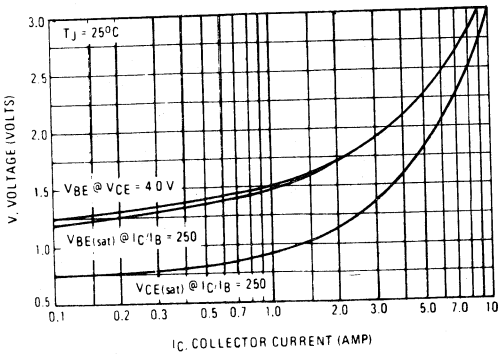
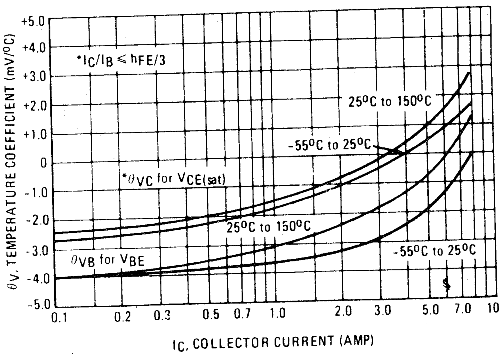


FIGURE 12 — TEMPERATURE COEFFICIENTS



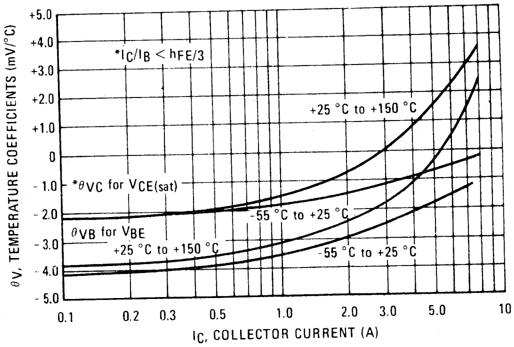
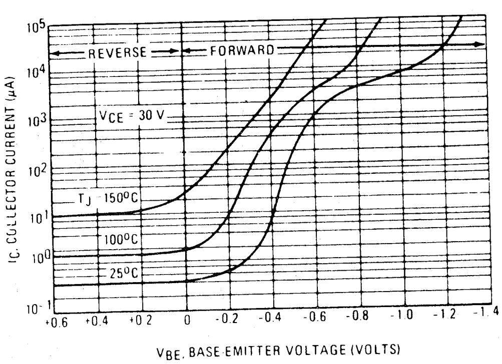
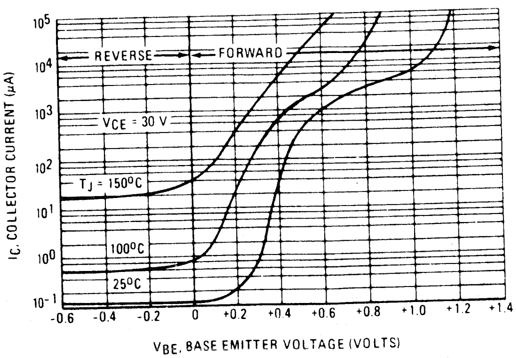


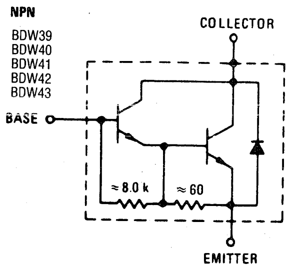
FIGURE 13 — COLLECTOR CUT-OFF REGION

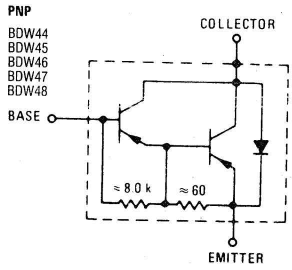




3

FIGURE 14 — DARLINGTON SCHEMATIC





3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

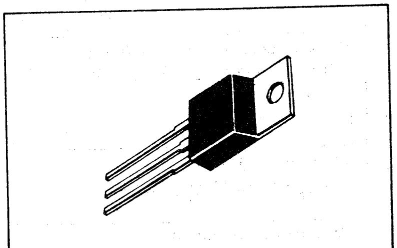
NPN	PNP
BDX33	**BDX34**
BDX33A	**BDX34A**
BDX33B	**BDX34B**
BDX33C	**BDX34C**

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general purpose and low speed switching applications.

- High DC Current Gain — h_{FE} = 2500 (typ.) at I_C = 4.0 Adc
- Collector Emitter sustaining Voltage at 100 mAdc
  $V_{CEO(sus)}$ = 45 Vdc (min.) — BDX33, 34
  60 Vdc (min.) — BDX33A, 34A
  80 Vdc (min.) — BDX33B, 34B
  100 Vdc (min.) — BDX33C, 34C
- Low Collector Emitter Saturation Voltage
  $V_{CE(sat)}$ = 2.5 Vdc (max.) at I_C = 4.0 Adc — BDX33, 33A/34, 34A
  2.5 Vdc (max.) at I_C = 3.0 Adc — BDX33B, 33C/34B, 34C
- Monolithic Construction with Built-In Base Emitter Shunt resistors
- TO-220AB Compact Package
- TO-66 Lead form also available ordered with "-66" suffix.

DARLINGTON
10 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
45-60-80-100 VOLTS
70 Watts

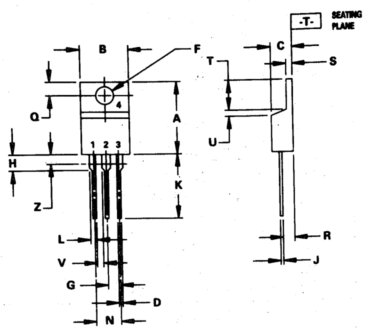


MAXIMUM RATINGS

Rating	Symbol	BDX33 BDX34	BDX33A BDX34A	BDX33B BDX34B	BDX33C BDX34C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous Peak	I_C	10 15				Adc
Base Current	I_B	0.25				Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	70 0.56				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.78	°C/W



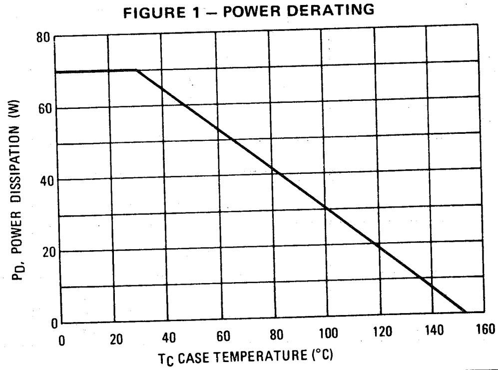
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

FIGURE 1 — POWER DERATING



3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0)	BDX33/BDX34 BDX33A/BDX34A BDX33B/BDX34B BDX33C/BDX34C	$V_{CEO(sus)}$	45 60 80 100		Vdc
Collector-Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0, R_{BE} = 100)	BDX33/BDX34 BDX33A/BDX34A BDX33B/BDX34B BDX33C/BDX34C	$V_{CER(sus)}$	45 60 80 100		Vdc
Collector-Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0, V_{BE} = 1.5 Vdc)	BDX33/BDX34 BDX33A/BDX34A BDX33B/BDX34B BDX33C/BDX34C	$V_{CEX(sus)}$	45 60 80 100		Vdc
Collector Cutoff Current (V_{CE} = ½ rated V_{CEO}, I_B = 0)	T_C = 25 °C T_C = 100 °C	I_{CEO}		0.5 10	mAdc
Collector Cutoff Current (V_{CB} = rated V_{CBO}, I_E = 0)	T_C = 25 °C T_C = 100 °C	I_{CBO}		1 5	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		10	mAdc
ON CHARACTERISTICS					
DC Current Gain[1] (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BDX33, 33A/34, 34A BDX33B, 33C/34B, 34C	h_{FE}	750 750		–
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 8 mAdc) (I_C = 3.0 Adc, I_B = 6 mAdc)	BDX33, 33A/34, 34A BDX33B, 33C/34B, 34C	$V_{CE(sat)}$		2.5 2.5	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 3 V) (I_C = 3.0 Adc, V_{CE} = 3 Vdc)	BDX33, 33A/34, 34A BDX33B, 33C/34B, 34C	$V_{BE(on)}$		2.5 2.5	Vdc
Diode Forward Voltage (I_C = 8 Adc)		V_F		4	Vdc
SECOND BREAKDOWN[2]					
Second Breakdown Collector Current With Base Forward Biased (V_{CE} = 25 Vdc) (V_{CE} = 20 Vdc) (V_{CE} = 36 Vdc) (V_{CE} = 33 Vdc)	BDX33 Series BDX34 Series BDX33 Series BDX34 Series	$I_{S/b}$	2.8 3.5 1.0 1.0		Adc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (T_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1 MHz)		h_{FE}	1000		–
Current Gain-Bandwidth product (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 MHz)		f_T	3		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDX33 Series BDX34 Series	C_{ob}		200 300	pF

[1] Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2%
[2] Pulse Test non repetitive: Pulse Width = 0.25 s.

3

FIGURE 2 — THERMAL RESPONSE

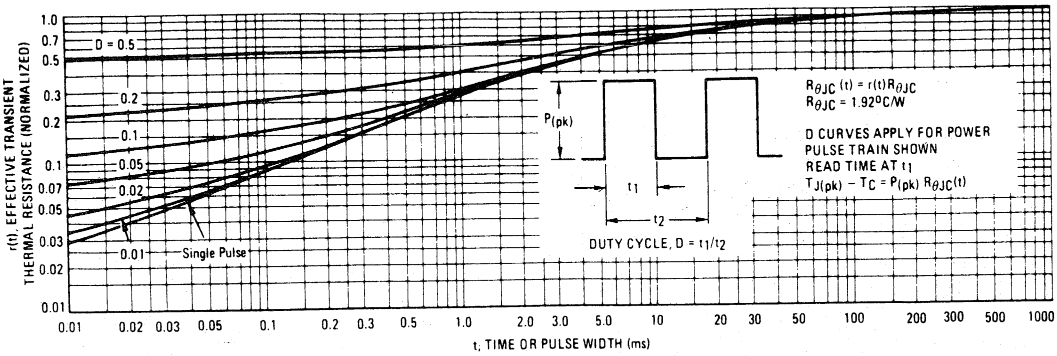
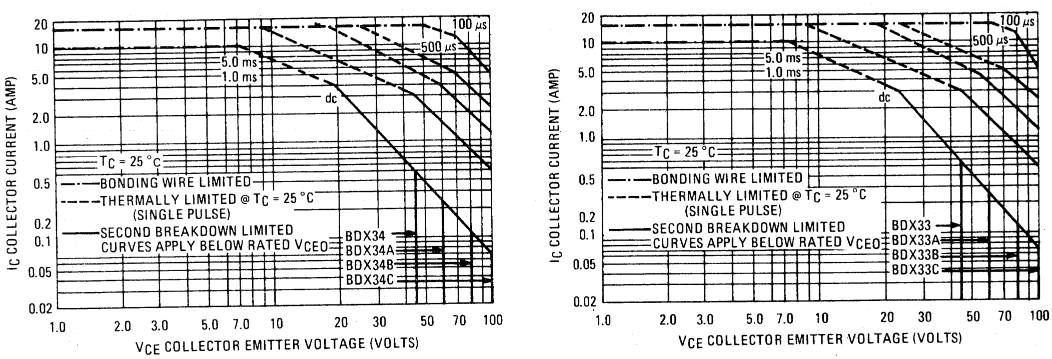


FIGURE 3 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Fig. 3 is based on $T_{J(pk)} = 150\,°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ 150 °C $T_{J(pk)}$ may be calculated from the data in Fig. . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (see AN-415A).

FIGURE 4 — SMALL-SIGNAL CURRENT GAIN

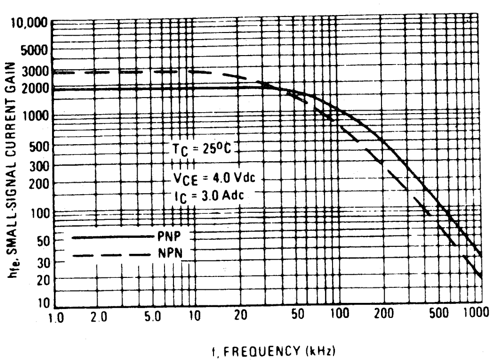
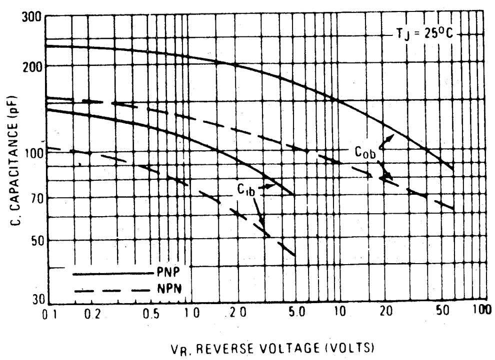


FIGURE 5 — CAPACITANCE



NPN — BDX33, 33A, 33B, 33C

PNP — BDX34, 34A, 34B, 34C

FIGURE 6 — DC CURRENT GAIN

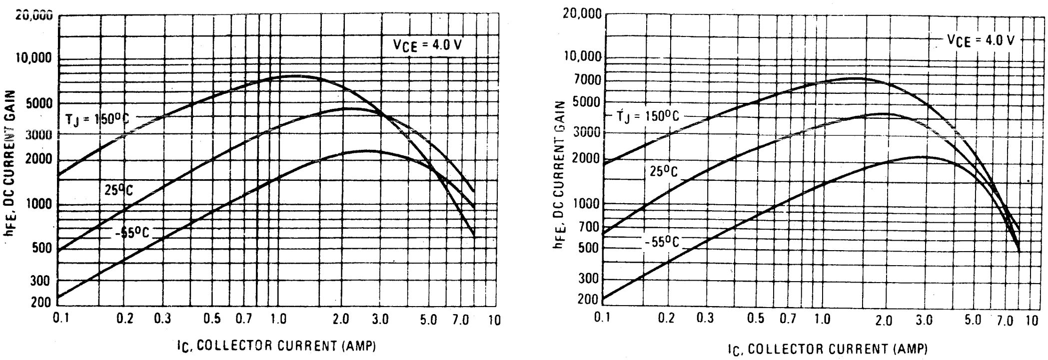


FIGURE 7 — COLLECTOR SATURATION REGION

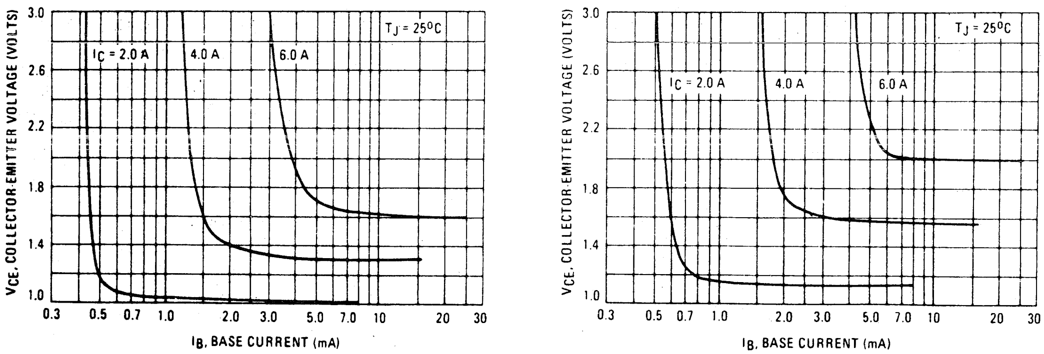
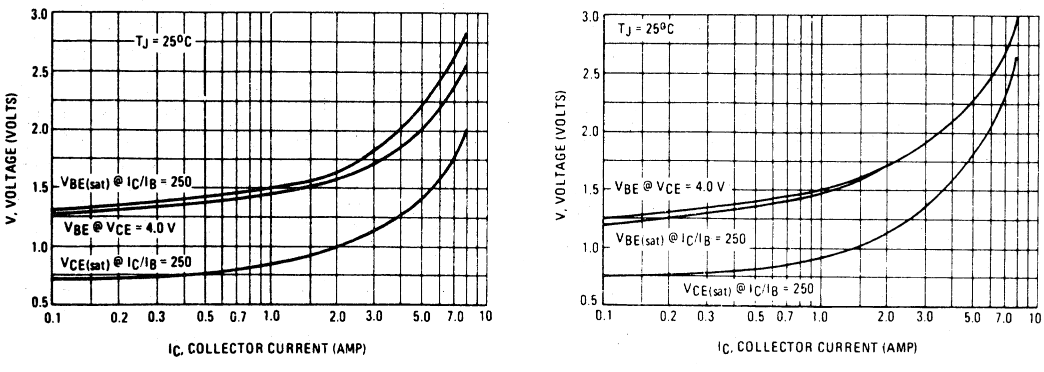


FIGURE 8 — "ON" VOLTAGES



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

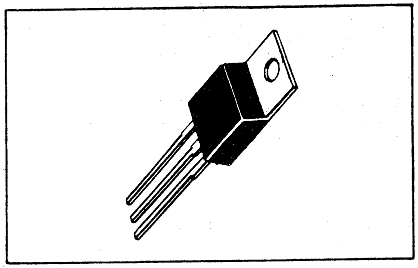
NPN	PNP
BDX53	**BDX54**
BDX53A	**BDX54A**
BDX53B	**BDX54B**
BDX53C	**BDX54C**

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 45 Vdc (Min) — BDX53, 54
  = 60 Vdc (Min) — BDX53A, 54A
  = 80 Vdc (Min) — BDX53B, 54B
  = 100 Vdc (Min) — BDX53C, 54C
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
65 WATTS



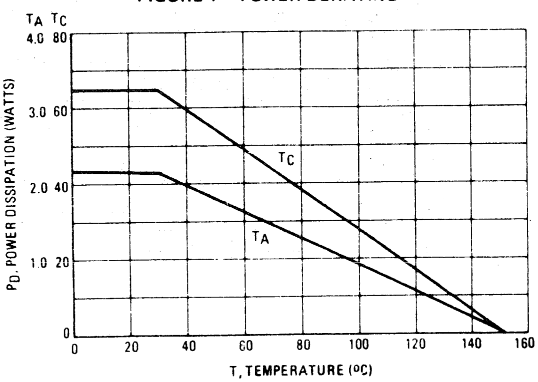
*MAXIMUM RATINGS

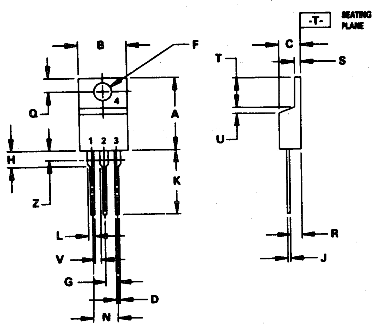
Rating	Symbol	BDX53 BDX54	BDX53A BDX54A	BDX53B BDX54B	BDX53C BDX54C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current Continuous Peak	I_C	8 12				Adc
Base Current	I_B	0.2				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 0.48				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	BDX53, BDX54	$V_{CEO(sus)}$	45		Vdc
	BDX53A, BDX54A		60	–	
	BDX53B, BDX54B		80	–	
	BDX53C, BDX54C		100	–	
Collector Cutoff Current (V_{CE} = 22 Vdc, I_B = 0)	BDX53, BDX54	I_{CEO}		0.5	mAdc
(V_{CE} = 30 Vdc, I_B = 0)	BDX53A, BDX54A		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	BDX53B, BDX54B		–	0.5	
(V_{CE} = 50 Vdc, I_B = 0)	BDX53C, BDX54C		–	0.5	
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0)	BDX53, BDX54	I_{CBO}		0.2	mAdc
(V_{CB} = 60 Vdc, I_E = 0)	BDX53A, BDX54A		–	0.2	
(V_{CB} = 80 Vdc, I_E = 0)	BDX53B, BDX54B		–	0.2	
(V_{CB} = 100 Vdc, I_E = 0)	BDX53C, BDX54C		–	0.2	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	750	–	–
				–	
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc)		$V_{CE(sat)}$	–	2.0	Vdc
			–	4.0	
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_C = 12 mA)		$V_{BE(sat)}$	–	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDX53, 53A, 53B, 53C	C_{ob}	–	300	pF
	BDX54, 54A, 54B, 54C		–	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

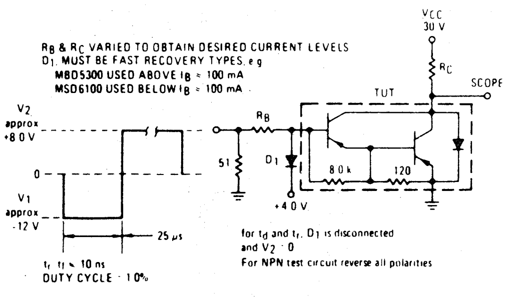


FIGURE 3 – SWITCHING TIMES

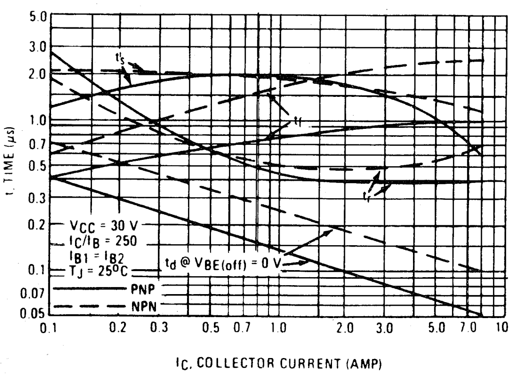


FIGURE 4 — THERMAL RESPONSE

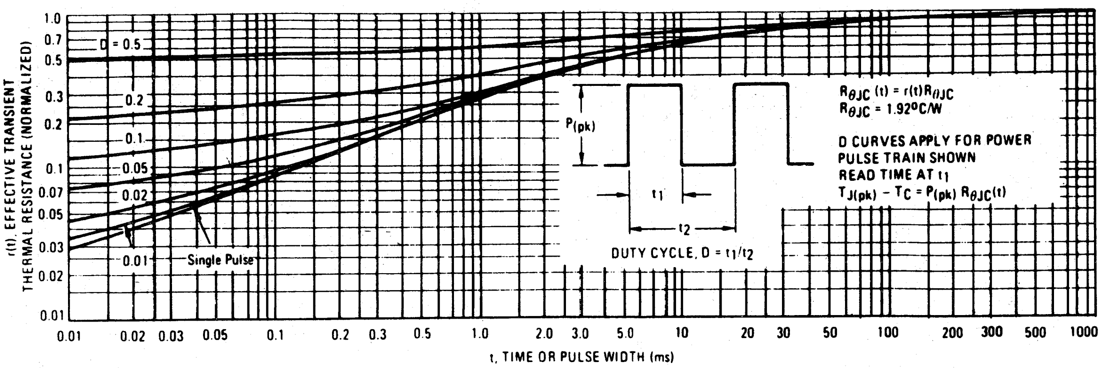
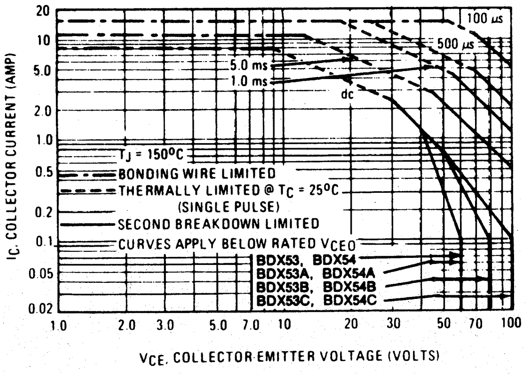


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (see AN-415A).

3

FIGURE 6 — SMALL-SIGNAL CURRENT GAIN

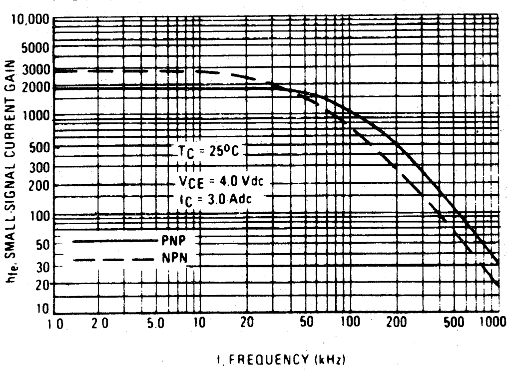
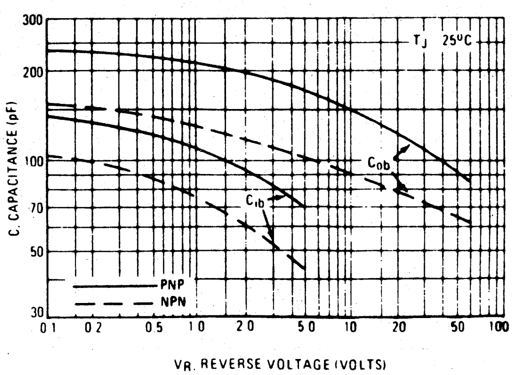


FIGURE 7 — CAPACITANCE



NPN — BDX53, BDX53A, BDX53B, BDX53C

PNP — BDX54, BDX54A, BDX54B, BDX54C

FIGURE 8 — DC CURRENT GAIN

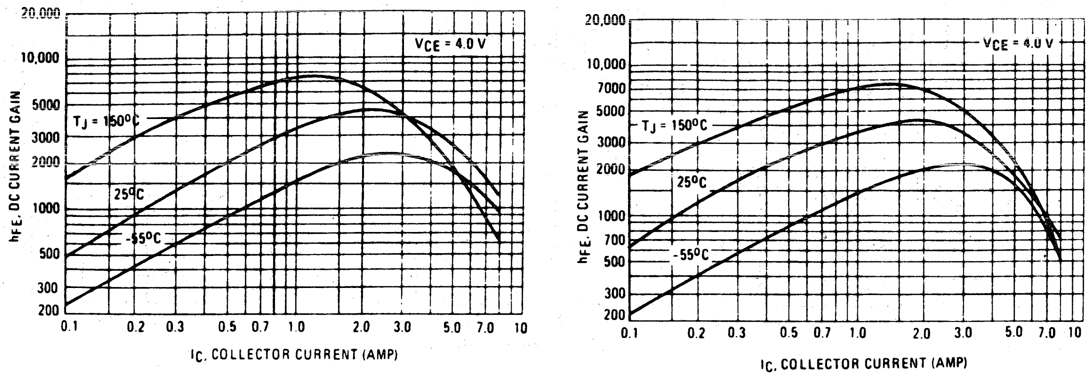


FIGURE 9 — COLLECTOR SATURATION REGION

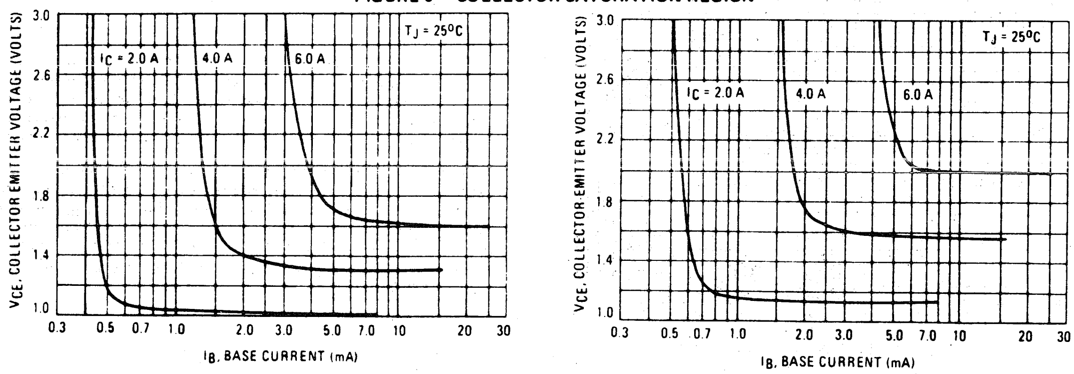
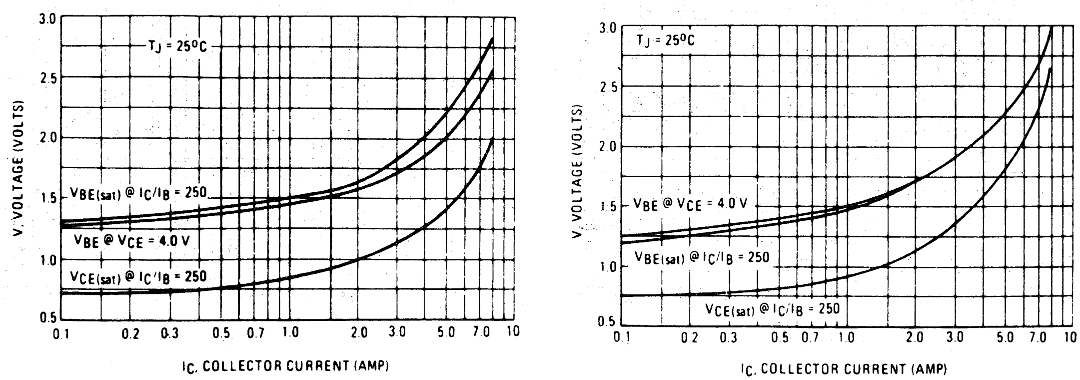


FIGURE 10 — "ON" VOLTAGES



3

NPN — **BDX53, BDX53A, BDX53B, BDX53C**

PNP — **BDX54, BDX54A, BDX54B, BDX54C**

FIGURE 11 – TEMPERATURE COEFFICIENTS

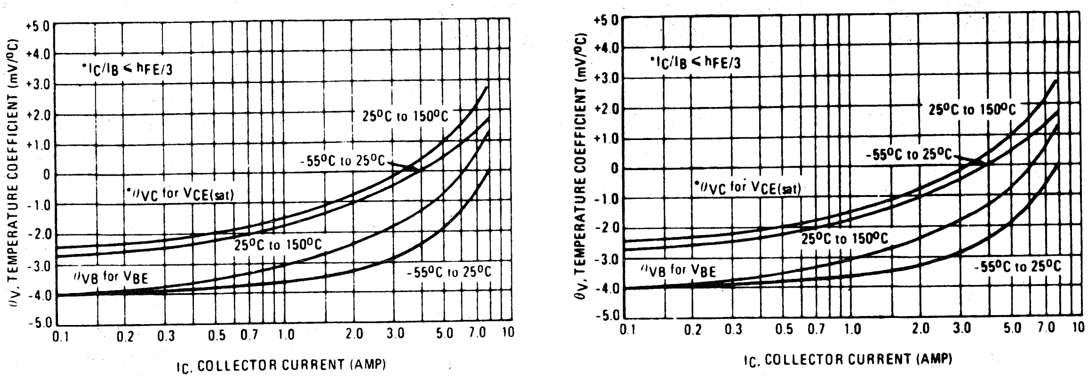


FIGURE 12 – COLLECTOR CUT-OFF REGION

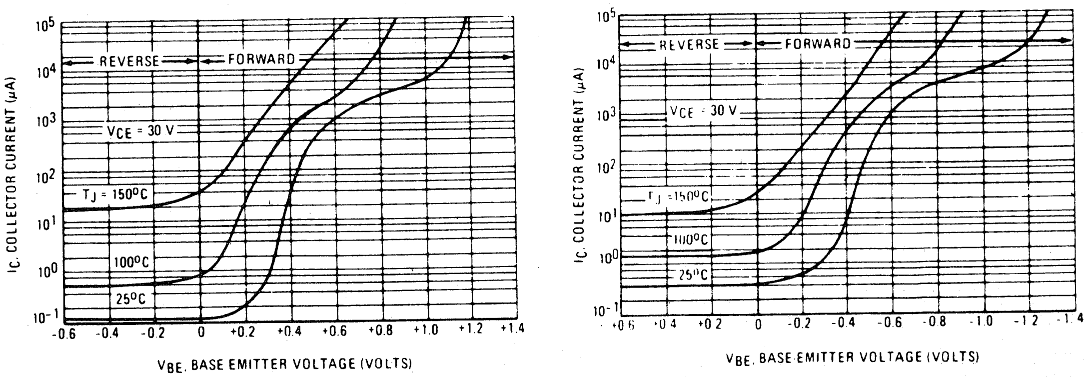
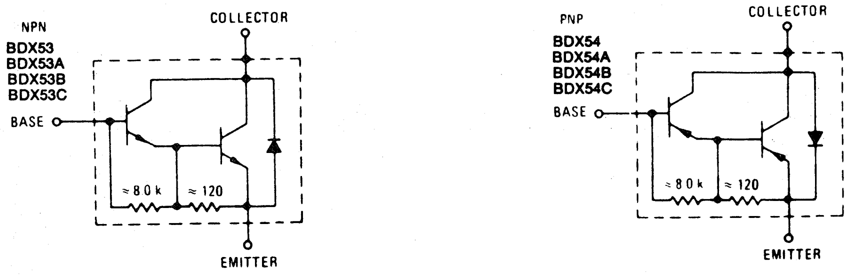


FIGURE 13 – DARLINGTON SCHEMATIC



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BU204
BU205

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage — V_{CEX} = 1300 Vdc — BU204
  1500 Vdc — BU205
- Glassivated Base-Collector Junction
- Switching Times with Inductive Loads —
  t_f = 0.65 μs (Typ) @ I_C = 2A

2.5 AMPERE

NPN SILICON POWER TRANSISTORS

1300 AND 1500 VOLTS
36 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

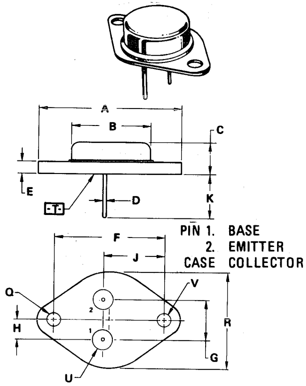
MAXIMUM RATINGS

Rating	Symbol	BU204	BU205	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	600	700	Vdc
Collector-Emitter Voltage	V_{CEX}	1300	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	2.5 3		Adc
Base Current — Peak (1)	I_{BM}	2.5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 90°C Derate above 25°C	P_D	36 10 0.4		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +115		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

   | ⌖ | ϕ.13 (0.005) Ⓜ | T | V Ⓜ |

   FOR LEADS:

   | ⌖ | ϕ.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

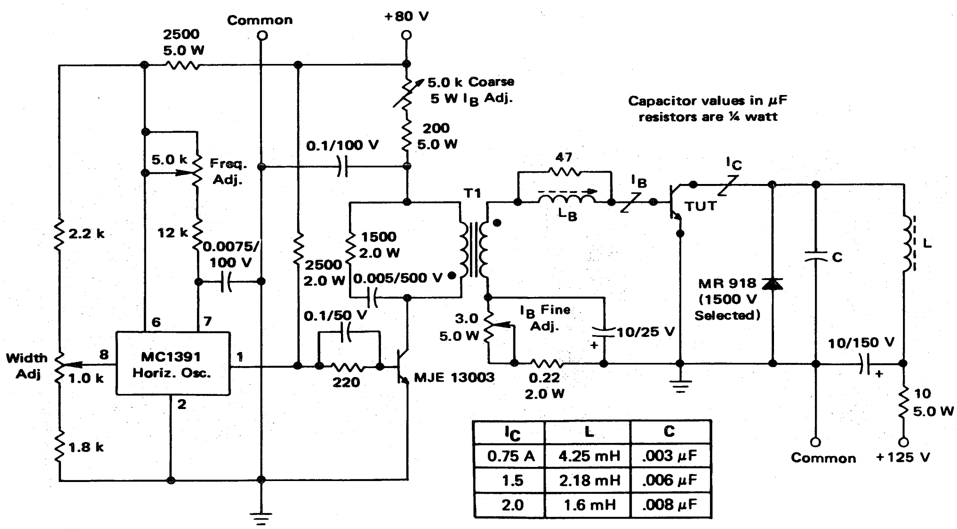
3

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	BU204 BU205	$V_{CEO(sus)}$	600 700	– –	– –	Vdc
Collector Cutoff Current (V_{CE} = 1300 Vdc, V_{BE} = 0) (V_{CE} = 1500 Vdc, V_{BE} = 0)	BU204 BU205	I_{CES}	– –	– –	1.0 1.0	mAdc
Emitter Base Voltage (I_E = 10 mA, I_C = 0)		V_{EBO}	5.0	–	–	Vdc
ON CHARACTERISTICS (1)						
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	–	–	5.0	Vdc
Base Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased		$I_{S/B}$	See Figure 14			
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (1) (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)		f_T	–	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	50	–	pF
SWITCHING CHARACTERISTICS						
Fall Time (I_C = 2.0 Adc, I_{B1} = 1.0 Adc, L_B = 25 μH) (See Figure 1)		t_f	–	0.65	–	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 1 — TEST CIRCUIT



I_C	L	C
0.75 A	4.25 mH	.003 μF
1.5	2.18 mH	.006 μF
2.0	1.6 mH	.008 μF

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance — 39 mH. Secondary Inductance — 22 mH, Leakage Inductance with primary shorted — 2.0 μH, Primary 260 turns #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst case component variations and maximum high voltage loading must also be taken into account.

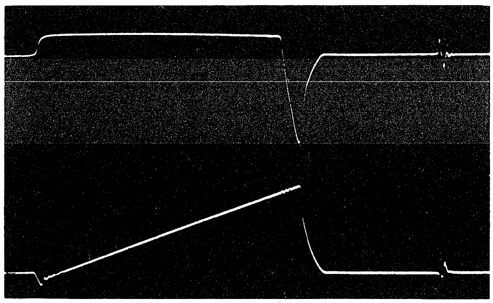
If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when I_{B1} h_{FE} = I_{CM}, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the I_{B1} h_{FE} = I_{CM} point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation I_{B1} h_{FE} = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

TEST CIRCUIT WAVEFORMS

FIGURE 2

I_B

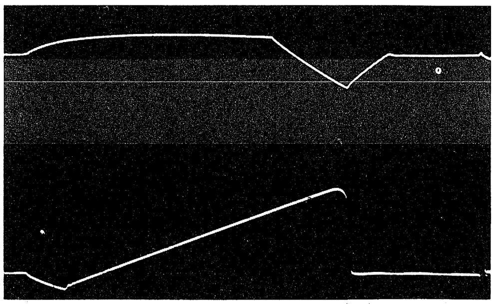


I_C

(time)

FIGURE 3

I_B



I_C

(time)

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 — OPTIMIZING DRIVE @ I_C = 0.75 A

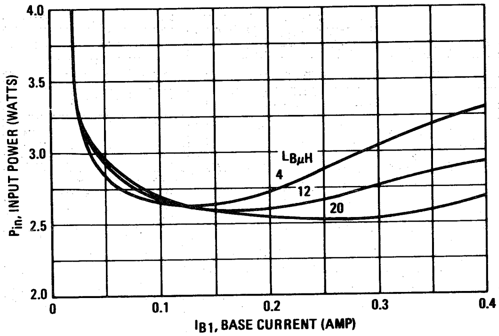


FIGURE 5 — OPTIMIZING DRIVE @ I_C 1.5 A

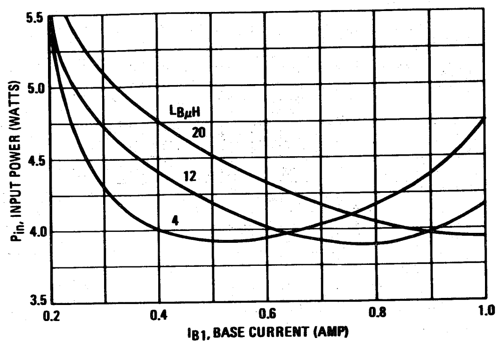


FIGURE 6 — OPTIMIZING DRIVE @ I_C = 2.0 A

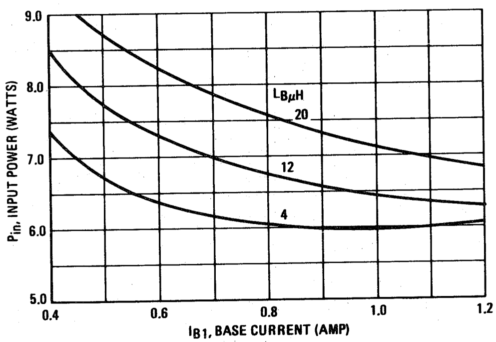


FIGURE 7 — SWITCHING BEHAVIOR versus TEMPERATURE

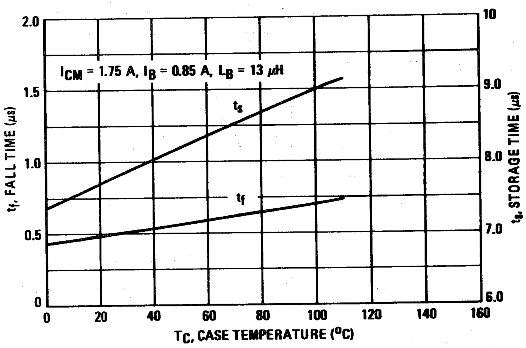


FIGURE 8 — OPTIMUM DRIVE CONDITIONS

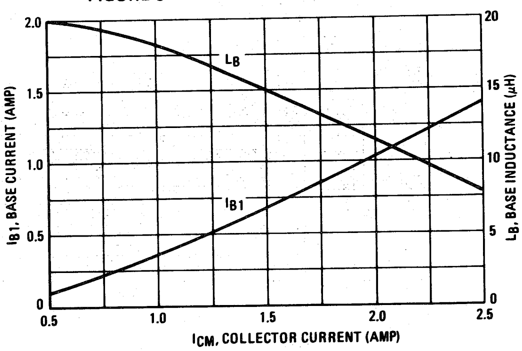
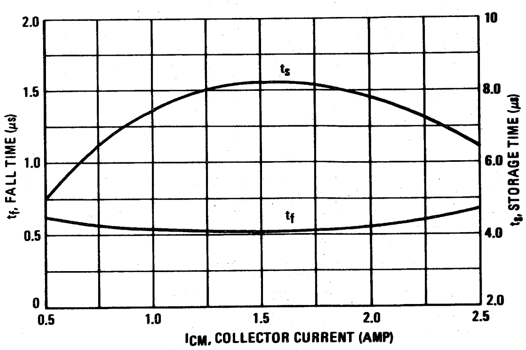


FIGURE 9 — SWITCHING BEHAVIOR versus I_{CM}



3

FIGURE 10 – THERMAL RESPONSE

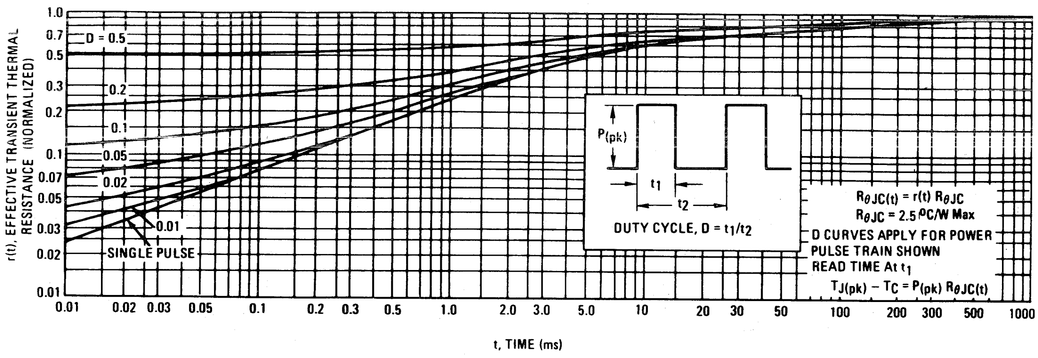


FIGURE 11 – COLLECTOR SATURATION REGION

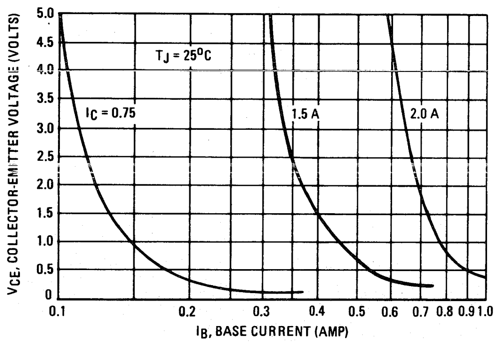


FIGURE 12 – DC CURRENT GAIN

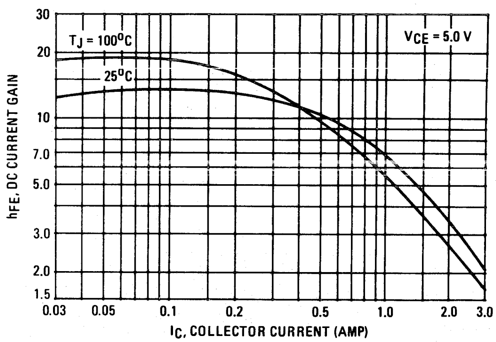


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FIGURE 13 – "ON" VOLTAGES

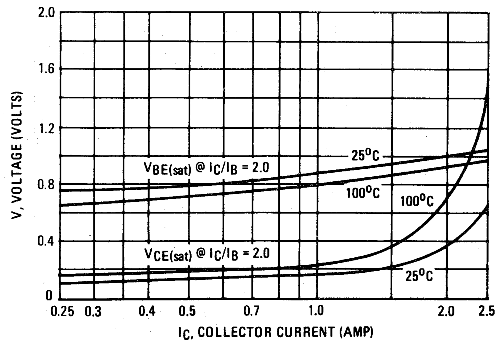
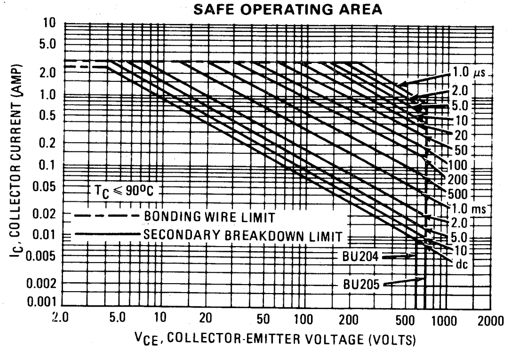


FIGURE 14-MAXIMUM FORWARD BIAS SAFE OPERATING AREA



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BU207
BU208

Designer's Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

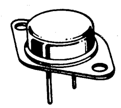
. . . specifically designed for use in large screen color deflection circuits.

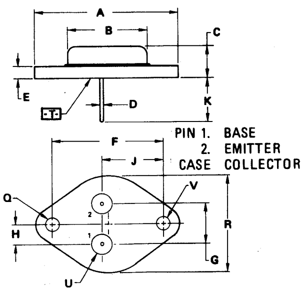
- Collector-Emitter Voltage —
  V_{CEX} = 1300 Vdc — BU207
  1500 Vdc — BU208
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 600 Vdc — BU207
  700 Vdc — BU208
- Switching Times with Inductive Loads, $t_f = 0.4\ \mu s$ (Typ) @ $I_C = 4.5$ A
- Optimum Drive Condition Curves
- Glass Base-Collector Junction

5 AMPERE
NPN SILICON
POWER TRANSISTORS
1300 AND 1500 VOLTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

*MAXIMUM RATINGS

Rating	Symbol	BU207	BU208	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	600	700	Vdc
Collector-Emitter Voltage	V_{CEX}	1300	1500	Vdc
Emitter Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	5 7.5		Adc
Base Current — Peak (1)	I_{BM}	4		Adc
Total Power Dissipation @ $T_C = 95°C$ Derate above 95°C	P_D	12.5 0.625		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +115		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.6	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

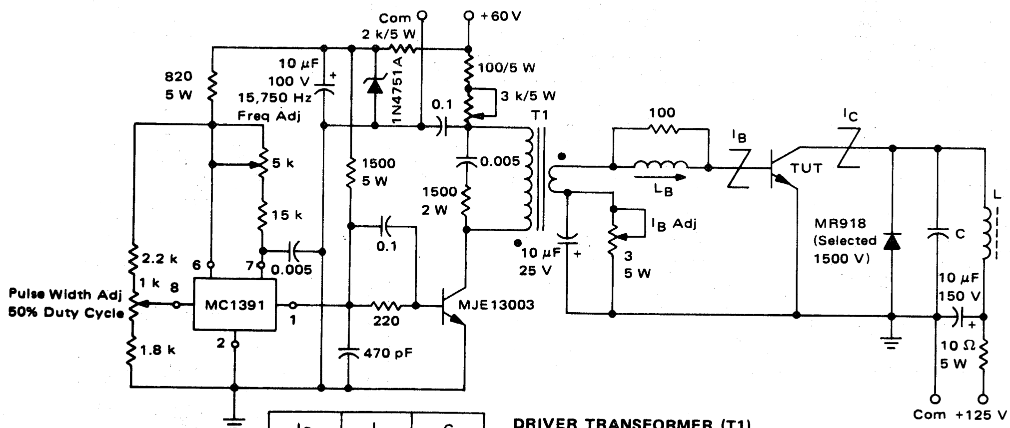
3

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	BU207	$V_{CEO(sus)}$	600	—	—	Vdc
	BU208		700	—	—	
Collector Cutoff Current (V_{CE} = 1300 Vdc, V_{BE} = 0)	BU207	I_{CES}	—	—	1.0	mAdc
(V_{CE} = 1500 Vdc, V_{BE} = 0)	BU208		—	—	1.0	
Emitter Base Voltage (I_E = 10 mA, I_C = 0)		V_{EBO}	5.0	—	—	Vdc
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 4.5 Adc, V_{CE} = 5 Vdc)		h_{FE}	2.25	—	—	—
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)		$V_{CE(sat)}$	—	—	5	Vdc
Base Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)		$V_{BE(sat)}$	—	—	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$		See Figure 14		
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1 MHz)		f_T	—	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	125	—	pF
SWITCHING CHARACTERISTICS						
Fall Time	(I_C = 4.5 Adc, I_B = 1.8 Adc, L_B = 10 μH, see Figure 1)	t_f	—	0.6	—	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



I_C A	L mH	C μF
3.5	0.87	0.013
4.5	0.67	0.017

DRIVER TRANSFORMER (T1)
Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance — 39 mH, Secondary Inductance — 0.22 mH, Leakage Inductance with primary shorted — 2.0 μH. Primary 260 turns, #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

BASE DRIVE: The Key to Performance

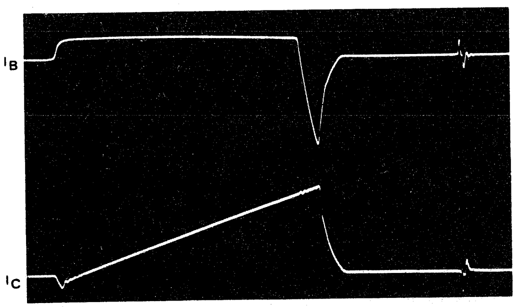
By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1}\ h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1}\ h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor *initiation* of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation $I_{B1}\ h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

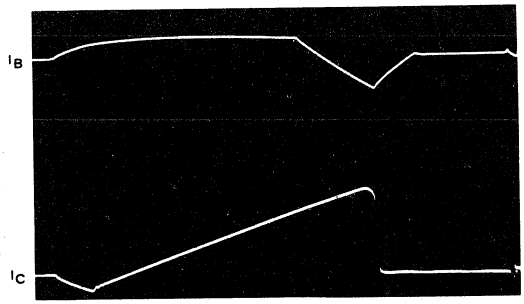
TEST CIRCUIT WAVEFORMS

FIGURE 2



(time)

FIGURE 3



(time)

3

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 – OPTIMIZING DRIVE @ I_C = 3.5 A

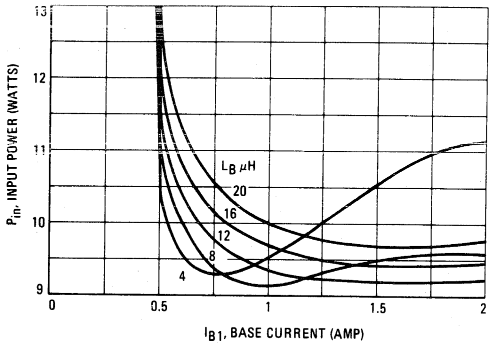


FIGURE 5 – OPTIMIZING DRIVE @ I_C = 4.5 A

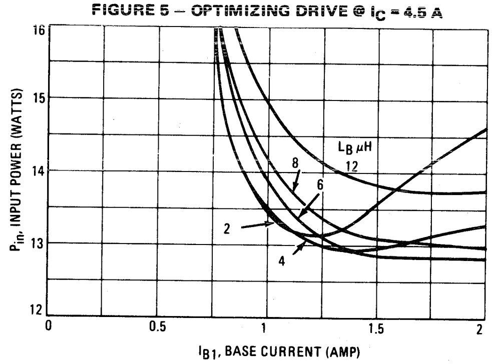


FIGURE 6 – SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 3.5 A, I_B = 1.5 A, L_B = 14 μH

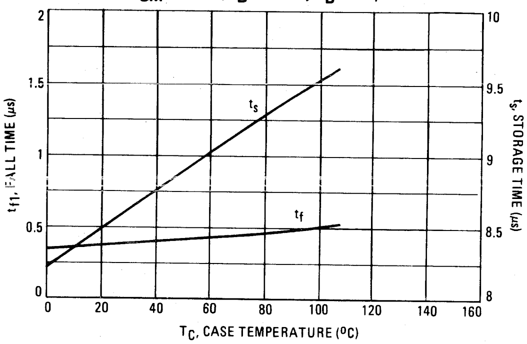


FIGURE 7 – SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 4.5 A, I_B = 1.75 A, L_B = 8 μH

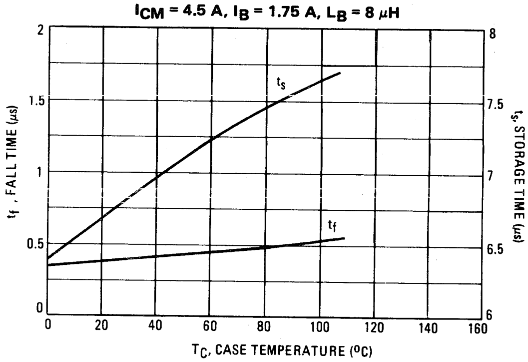


FIGURE 8 – OPTIMUM DRIVE CONDITIONS

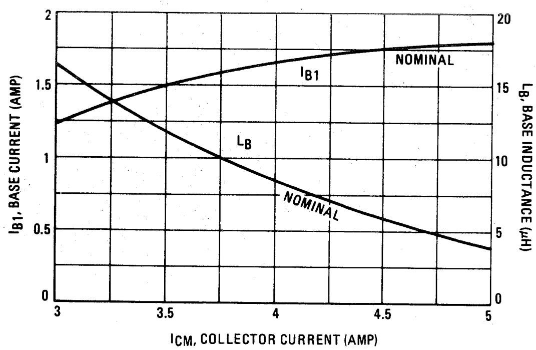


FIGURE 9 – SWITCHING BEHAVIOR versus I_{CM}

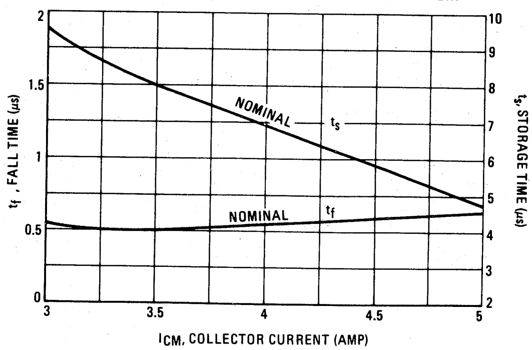


FIGURE 10 – THERMAL RESPONSE

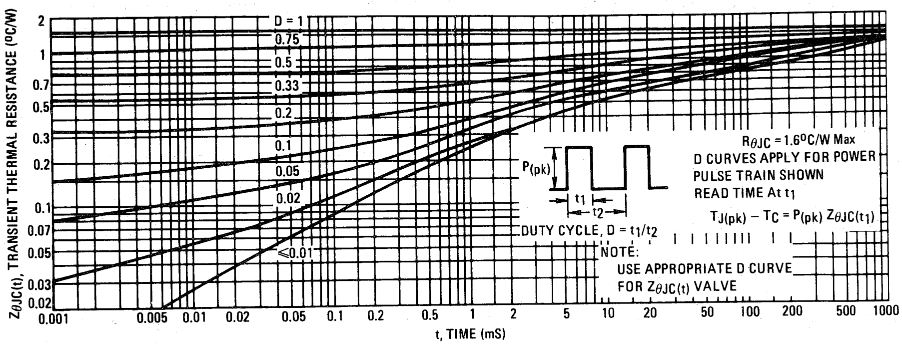


FIGURE 11 – COLLECTOR SATURATION REGION

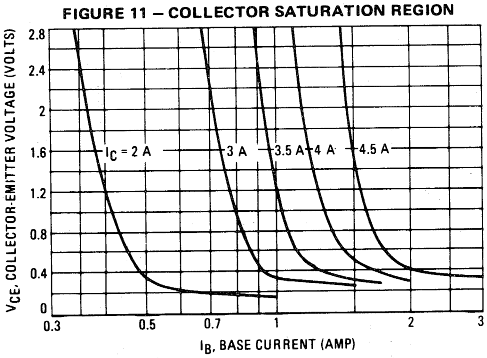


FIGURE 12 – DC CURRENT GAIN

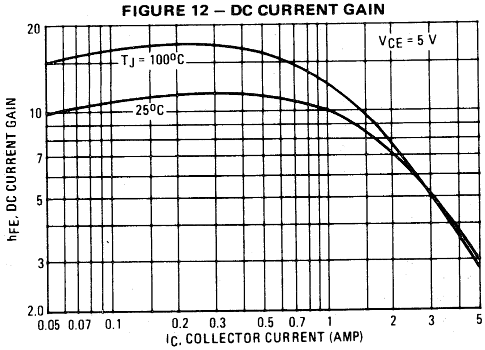


FIGURE 13 – "ON" VOLTAGES

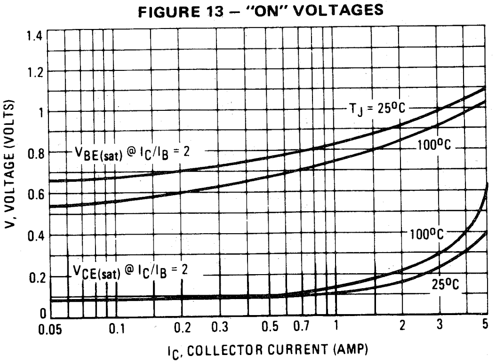


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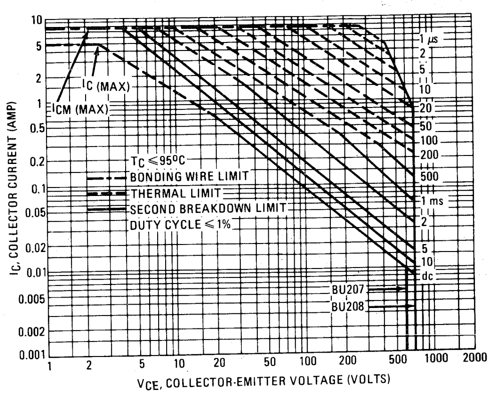
FIGURE 14-MAXIMUM FORWARD BIAS SAFE OPERATING AREA



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

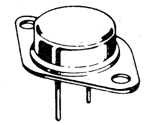
BU208A

HORIZONTAL DEFLECTION TRANSISTOR

. . . designed for use in televisions.

- Collector-Emitter Voltages V_{CES} 1500/1700 Volts
- Fast Switching – 400 ns Typical Fall Time
- Low $V_{CE(sat)}$ 0.3 Vdc Typical at 4.5 Adc/2.25 Adc (BU208A)
- Low thermal Resistance 1°C/W increased reliability
- Glass passivated (patented photoglass). Triple diffused Mesa Technology for long term stability.

6 AND 7 AMPERES
NPN SILICON POWER TRANSISTORS
1500 to 1700 VOLTS



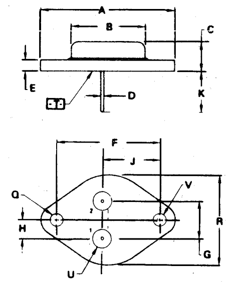
MAXIMUM RATINGS

Rating	Symbol	BU208A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector-Emitter Voltage	V_{CES}	1500	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current – Continuous – Peak	I_C I_{CM}	7 (5) 15 (7.5)	Vdc
Base Current – Continuous – Peak (Negative)	I_B I_{BM}	4 3.5	Adc
Total Power Dissipation at T_C = 95°C Derate above 95°C	P_D	20 (12.5) 1 (0.625)	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +115	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0 (1.6)	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8″ from Case for 5 Seconds	T_L	275	°C

NOTE: 1. Pulsed 5 ms, Duty Cycle ≤ 10%.
2. See page 3 for Additional Ratings on A Type.
3. Figures in ( ) are Standard Ratings Motorola Guarantees are Superior.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. T IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
⌖ ⌀0.13 (0.005) Ⓜ T V Ⓜ
FOR LEADS
⌖ ⌀0.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 (TO-3)

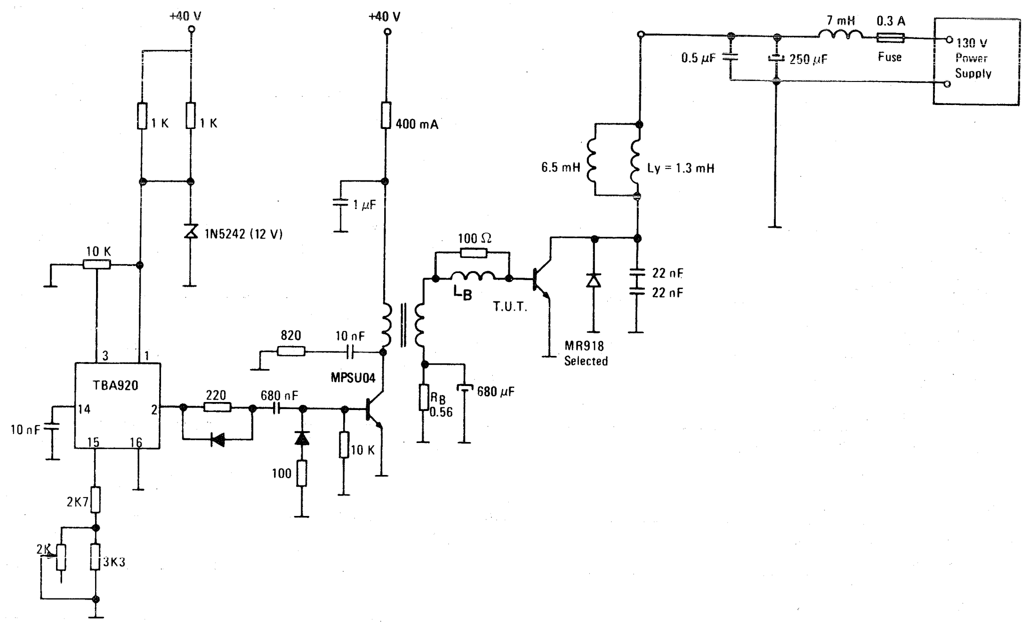
ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, L = 25 mH)	$V_{CEO(sus)}$	700			Vdc
Collector Cutoff Current[1] (V_{CE} = rated V_{CES}, V_{BE} = 0) ALL TYPES	I_{CES}			1.0	mAdc
Emitter Base Voltage[1] (I_C = 0, I_E = 10 mAdc) (I_C = 0, I_E = 100 mAdc)	V_{EBO}	5	7		Vdc
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 4.5 Adc, V_{CE} = 5 Vdc)	h_{FE}	2.25			
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc) (I_C = 4.5 Adc, I_B = 2 Adc)	$V_{CE(sat)}$			5 1	Vdc
Base-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)	$V_{BE(sat)}$			1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)	f_T		4		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0), f_{test} = 1 MHz)	C_{ob}		125		pF
SWITCHING CHARACTERISTICS					
Storage Time (see test circuit fig. 1) (I_C = 4.5 Adc, I_{B1} = 1.8 Adc, L_B = 10 μH)	t_s		8		μS
Fall time (see test circuit fig. 1) (I_C = 4.5 Adc, I_{B1} = 1.8 Adc, L_B = 10 μH)	t_f		0.4		μS

Pulse test: PW = 300 μS; Duty cycle ⩽ 2%.

3

FIGURE 1 — SWITCHING TIME TEST CIRCUIT



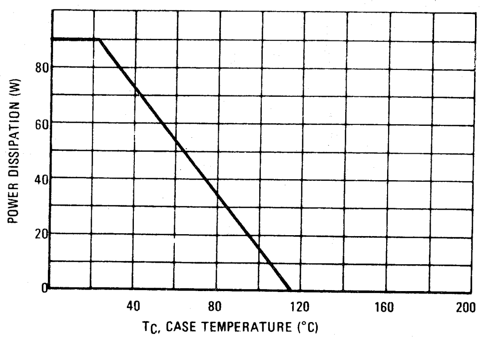
FLASHOVER PERFORMANCE

The BU208A is guaranteed to the following additional maximum ratings

I_C PEAK	10A	20 pulses maximum of Pulse Width ≤ 50 μS. Duty cycle ≤ 50%.
Followed by		
V_{CES} PEAK	1650V	

3

FIGURE 2 — POWER DERATING



BASE DRIVE
The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Fig. 3. This results in rapid, but only partial collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Fig. 4, thus allowing axcess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B.

This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. For very low L_B a very narrow optimum is obtained. This occurs when $I_{B1} \cdot h_{FE} \cong I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1} \cdot h_{FE} = I_{CM}$ point as the turn off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left, or right according to the relation $I_{B1} \cdot h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accomodate the lowest h_{FE} part specified. Neither L_B nor I_{B1} are absolutely critical. Due to the high gain of Motorola devices it is suggested that in general a low value of I_{B1} be used to obtain optimum efficiency– eg. for BU208A with I_{CM} = 4.5 A use $I_{B1} \approx 1.5$ A, at I_{CM} = 4 A use $I_{B1} \approx 1.2$ A. These values are lower than for most competition devices but practical tests have showed comparable efficiency for Motorola devices even at the higher level of I_{B1}.

An L_B of 10 uH to 12 uH should give satisfactory operation of BU208A with I_{CM} of 4 to 4.5 A and I_{B1} between 1.2 and 2 A.

TEST CIRCUIT WAVEFORMS

FIGURE 3

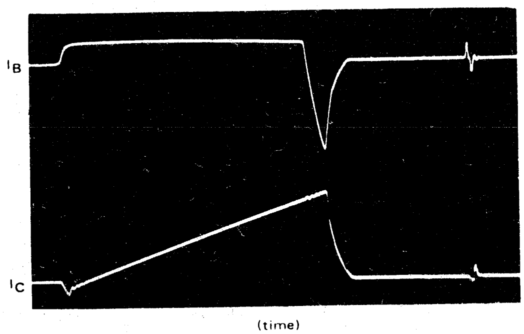
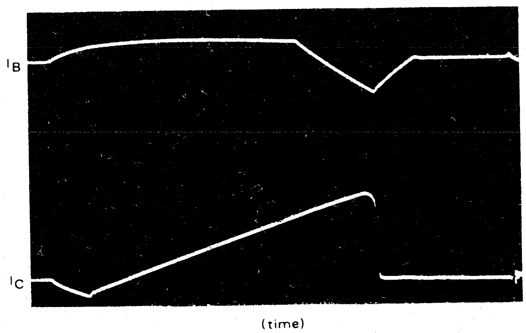


FIGURE 4



TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected.

FIGURE 5 — DC CURRENT GAIN

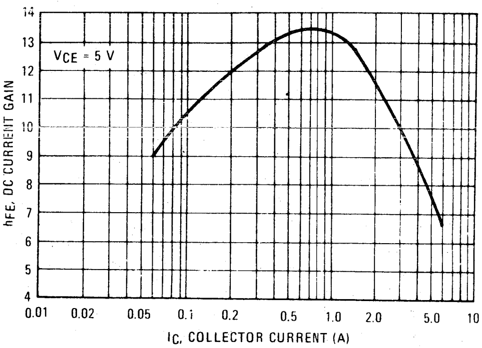


FIGURE 6 — COLLECTOR-EMITTER SATURATION VOLTAGE

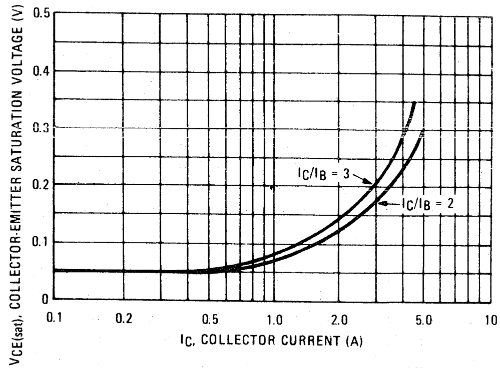


FIGURE 7 — BASE EMITTER SATURATION VOLTAGE

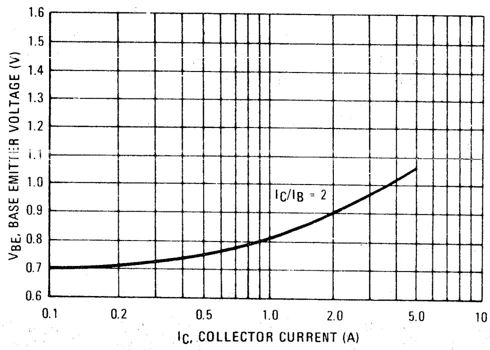


FIGURE 8 — COLLECTOR SATURATION REGION

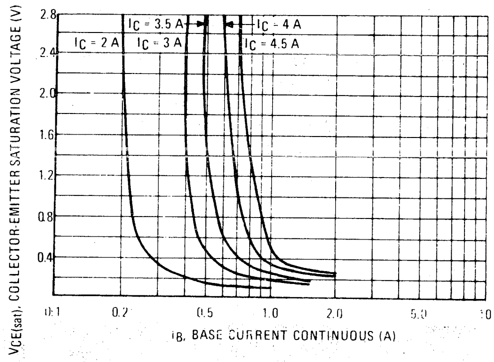
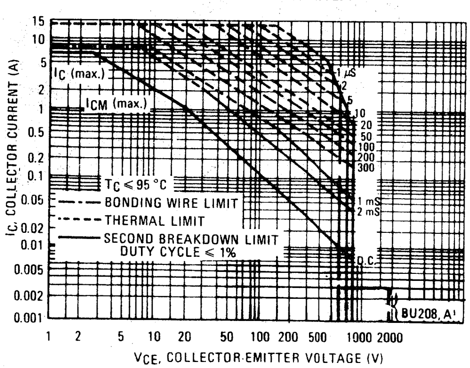


FIGURE 9 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



[1] Pulse width ≤ 20 μs. Duty cycle ≤ 0.25. R_{BE} ≤ 100 Ohms.

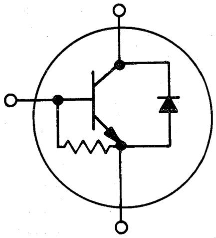
3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BU208D

NPN SILICON HORIZONTAL DEFLECTION TRANSISTOR WITH INTEGRATED DAMPER DIODE

. . . specifically designed for use in large screen color deflection circuits

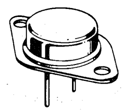


- V_{CES} = 1500 V;
  $V_{CEO(sus)}$ = 700 V (min)
- Low saturation:
  $V_{CE(sat)}$ = 1.0 V (max) @ I_C = 4.5 Adc

5 AMPERES

NPN SILICON POWER TRANSISTORS

1500 VOLTS
60 WATTS



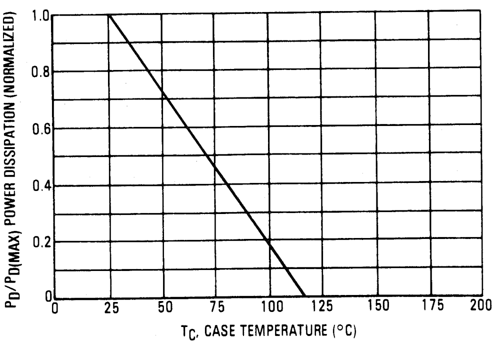
MAXIMUM RATINGS

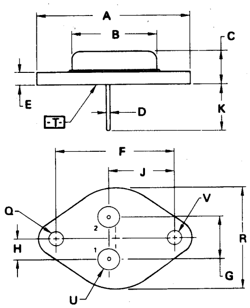
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	700	Vdc
Collector-Emitter Voltage (R_{BE} = 0)	V_{CES}	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C I_{CM}	5.0 7.5	Adc
Base Current — Peak	I_B	3.5	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	60 0.666	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 115	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA (Type)
(Formerly TO-3)

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (i_C = 100 mAdc, i_B = 0, L = 25 mH, V_{clamp} = 800 V)	$V_{CEO(sus)}$	700	—	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	—	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	300	mAdc
ON CHARACTERISTICS (1)				
Diode Forward Voltage (I_F = 4.0 A)	V_F	—	2.0	Vdc
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	—	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	—	1.5	Vdc
SWITCHING CHARACTERISTICS (Inductive Load)				
Fall Time (I_C (end) = 4.5 Adc, V_{CC} = 140 Vdc, I_B (end) = 1.8 A, L_C = 0.9 mH, L_B = 10 μH)	t_f	—	0.6 (typ)	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 3%.

3

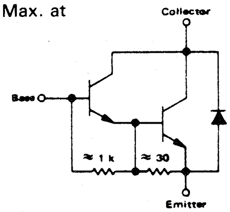
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BU323
BU323A

NPN SILICON POWER DARLINGTON TRANSISTOR

The BU323, BU323A are monolithic darlington transistors designed for automotive ignition, switching regulator and motor control applications.

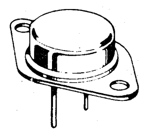
- V_{CE} Sat Specified at -40°C = 2 V Max. at I_C = 6 A.
- 550 mJ Energy Capability Tested in Automotive Ignition Circuit.
- Photoglass Passivation for Reliability and Stability.



16 AMPERE PEAK

POWER TRANSISTORS
DARLINGTON NPN SILICON

350 - 400 VOLTS
175 WATTS



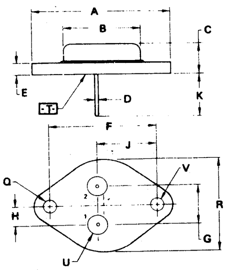
MAXIMUM RATINGS

Rating	Symbol	BU323	BU323A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Base Voltage	V_{CBO}	500	600	Vdc
Emitter-Base Voltage	V_{EBO}	8	8	Vdc
Collector Current — Continuous Peak (1)	I_C	10 16	10 16	Adc
Base Current — Continuous	I_B	3	3	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1	175 100 1	Watts Watts W/°C
Operating and Storage Junction	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES:
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2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	⌀.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	⌀.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS[1]						
Collector-Emitter Sustaining Voltage (Figure 1) L = 10 mH (I_C = 200 mAdc, I_B = 0, V_{clamp} = Rated V_{CEO})	BU323 BU323A	$V_{CEO(sus)}$	350 400			Vdc
Collector-Emitter sustaining Voltage (Figure 1) (I_C = 3 A, R_{BE} = 100 Ohms, L = 500 μH) Unclamped	BU323 BU323A	$V_{CER(sus)}$	400 475			Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 100 Ohms)		I_{CER}			1	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)		I_{CBO}			1	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)		I_{EBO}			40	mAdc
ON CHARACTERISTICS[1]						
DC Current Gain (I_C = 3 Adc, V_{CE} = 6 Vdc) (I_C = 6 Adc, V_{CE} = 6 Vdc) (I_C = 10 Adc, V_{CE} = 6 Vdc)		h_{FE}	300 150 50	550 350 150	 2000 	
Collector-Emitter Saturation Voltage (I_C = 3 Adc I_B = 60 mAdc) (I_C = 6 Adc, I_B = 120 mAdc) (I_C = 10 Adc, I_B = 300 mAdc) (I_C = 6 Adc, I_B = 120 mAdc, T_C = −40 °C)		$V_{CE(sat)}$			1.5 1.7 2.7 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 6 Adc, I_B = 120 mAdc) (I_C = 10 Adc, I_B = 300 mAdc) (I_C = 6 Adc, I_B = 120 mAdc, T_C = −40 °C)		$V_{BE(sat)}$			2.2 3 2.4	Vdc
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 6 Vdc)		$V_{BE(on)}$			2.5	Vdc
Diode Forward Voltage (I_F = 10 Adc)		V_f		2	3.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}		165	350	pF
SWITCHING CHARACTERISTICS						
Storage Time	(V_{CC} = 12 Vdc, I_C = 6 Adc, I_{B1} = I_{B2} = 0.3 Adc) Fig. 2	t_s		7.5	15	μs
Fall Time		t_f		5.2	15	μs
FUNCTIONAL TESTS						
Second Breakdown Collector Current with Base-Forward Biased		$I_{S/B}$		See Figure 10		
Pulsed Energy Test (See Figure 12)		$\frac{I_C^2 L}{2}$	550			mJ

1 Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 — SUSTAINING VOLTAGE TEST CIRCUIT

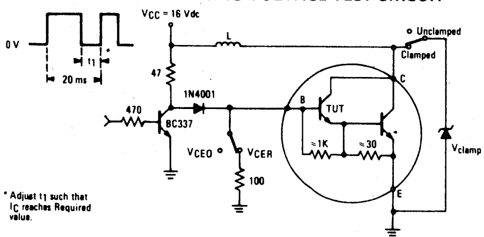

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT

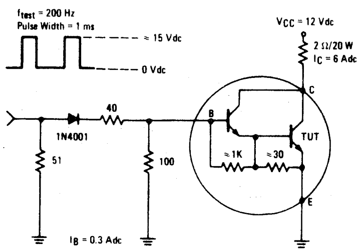

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FIGURE 3 — DC CURRENT GAIN

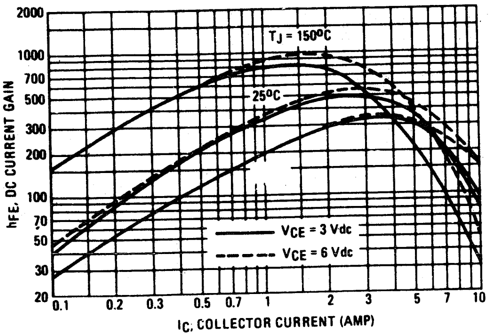


FIGURE 4 — COLLECTOR-SATURATION REGION

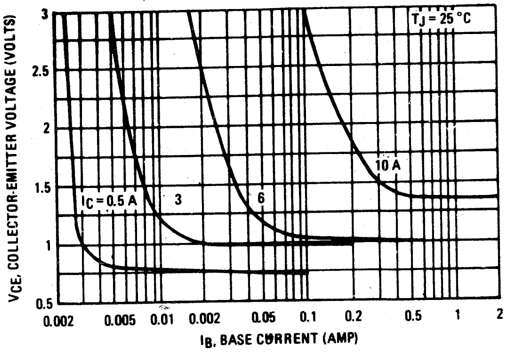


FIGURE 5 — COLLECTOR-EMITTER SATURATION VOLTAGE

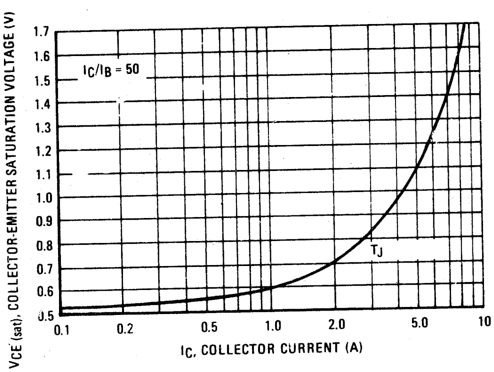


FIGURE 6 — BASE-EMITTER VOLTAGE

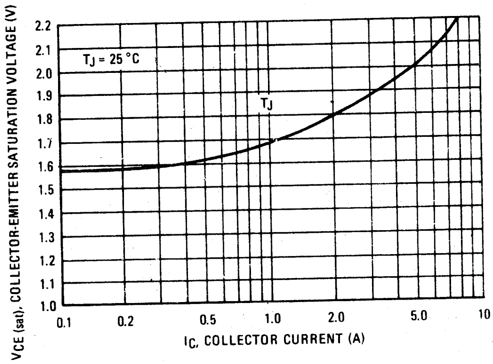


FIGURE 7 — TURN-OFF SWITCHING TIME

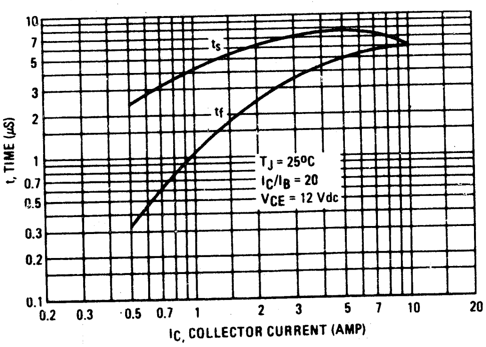
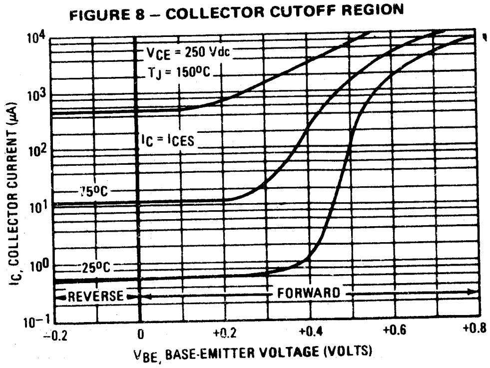


FIGURE 8 — COLLECTOR CUTOFF REGION



3

FIGURE 9 — THERMAL RESPONSE

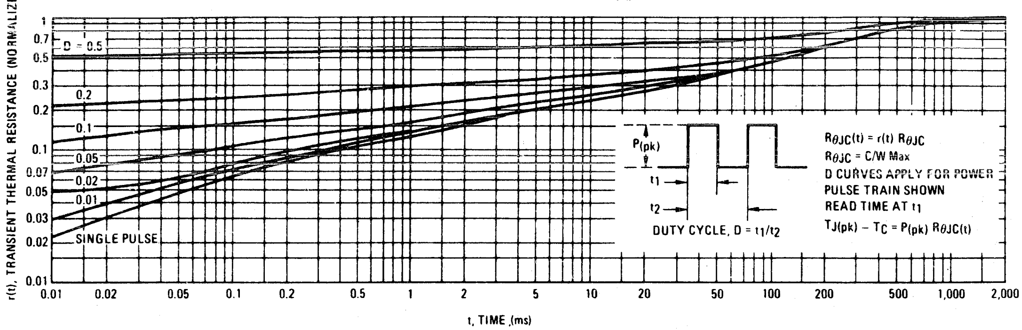
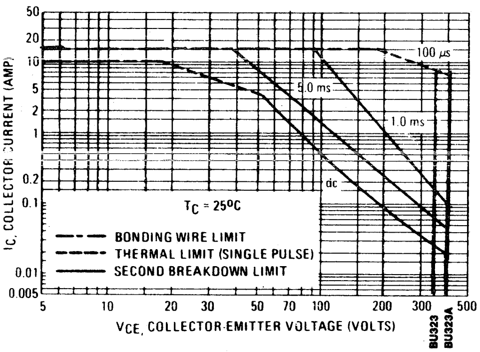


FIGURE 10 — FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^{\circ}C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 — POWER DERATING

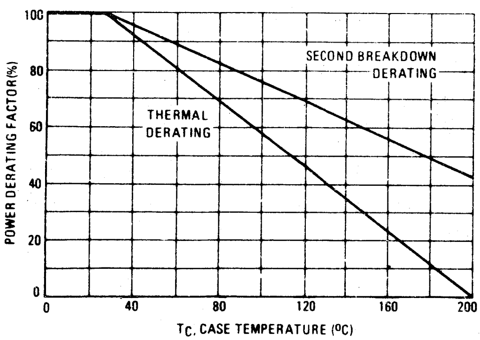
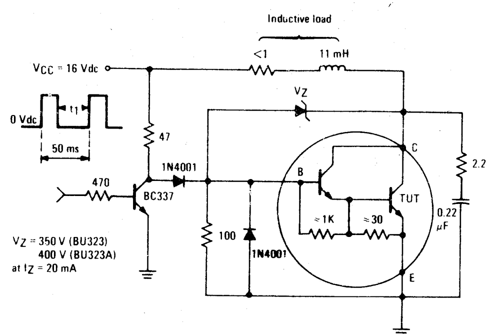


FIGURE 12 — IGNITION TEST CIRCUIT



t_1 to be selected such that I_C reaches 10 Adc before switch-off.

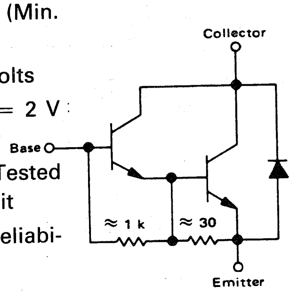
NOTE: Figure 12 specifies energy handling capabilities in an automotive ignition circuit.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BU323P
BU323AP

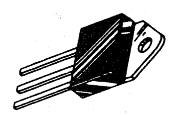
The BU323P, BU323APare monolithic darlington transistors designed for automotive ignition, switching regulator and motor control applications.

- Collector-Emitter Sustaining Voltage – $V_{CER\ (sus)}$ = 475 Vdc (Min. BU323AP)
- 125 Watts Capability at 50 Volts
- V_{CE} Sat Specified at −40°C = 2 V Max. at I_C = 6 A
- 550 mJ Energy Capability Tested in Automotive Ignition Circuit
- Photoglass Passivation for Reliability and Stability



DARLINGTON NPN SILICON POWER TRANSISTORS

350 & 400 VOLTS
125 WATTS



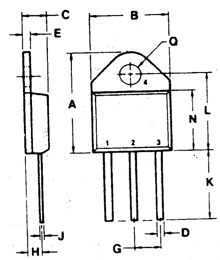
MAXIMUM RATINGS

Rating	Symbol	BU323P	BU323AP	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	200	250	Vdc
Collector-Emitter Voltage	V_{CEV}	300	350	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current – Continuous – Peak (1) – Overload	I_C I_{CM} I_{ol}	50 100	40 80	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	10	16	Adc
Total Power Dissipation – T_C = 25°C – T_C = 100°C Derate above 25°C	P_D	125 100 1		Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: ⅛″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦ 10%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
(TO-218AC)

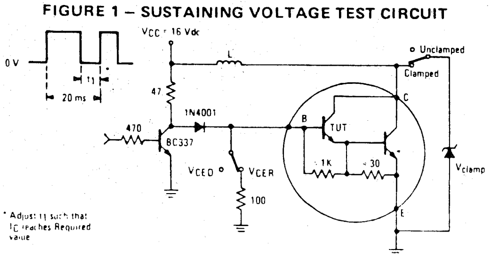
3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS[1]						
Collector-Emitter Sustaining Voltage (Figure 1) L = 10 mH (I_C = 200 mAdc, I_B = 0, V_{clamp} = Rated V_{CEO})	BU323P BU323AP	$V_{CEO(sus)}$	350 400			Vdc
Collector-Emitter sustaining Voltage (Figure 1) (I_C = 3 A, R_{BE} = 100 Ohms, L = 500 μH) Unclamped	BU323P BU323AP	$V_{CER(sus)}$	400 475			Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 100 Ohms)		I_{CER}			1	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)		I_{CBO}			1	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)		I_{EBO}			40	mAdc
ON CHARACTERISTICS[1]						
DC Current Gain (I_C = 3 Adc, V_{CE} = 6 Vdc) (I_C = 6 Adc, V_{CE} = 6 Vdc) (I_C = 10 Adc, V_{CE} = 6 Vdc)		h_{FE}	300 150 50	550 350 150	2000	
Collector-Emitter Saturation Voltage (I_C = 3 Adc I_B = 60 mAdc) (I_C = 6 Adc, I_B = 120 mAdc) (I_C = 10 Adc, I_B = 300 mAdc) (I_C = 6 Adc, I_B = 120 mAdc, T_C = −40 °C)		$V_{CE(sat)}$			1.5 1.7 2.7 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 6 Adc, I_B = 120 mAdc) (I_C = 10 Adc, I_B = 300 mAdc) (I_C = 6 Adc, I_B = 120 mAdc, T_C = −40 °C)		$V_{BE(sat)}$			2.2 3 2.4	Vdc
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 6 Vdc)		$V_{BE(on)}$			2.5	Vdc
Diode Forward Voltage (I_F = 10 Adc)		V_f		2	3.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}		165	350	pF
SWITCHING CHARACTERISTICS						
Storage Time	(V_{CC} = 12 Vdc, I_C = 6 Adc, I_{B1} = I_{B2} = 0.3 Adc) Fig. 2	t_s		7.5	15	μs
Fall Time		t_f		5.2	15	μs
FUNCTIONAL TESTS						
Second Breakdown Collector Current with Base-Forward Biased		$I_{S/B}$		See Figure 10		
Pulsed Energy Test (See Figure 12)		$\frac{I_C^2 L}{2}$	550			mJ

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 — SUSTAINING VOLTAGE TEST CIRCUIT



3-512

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT

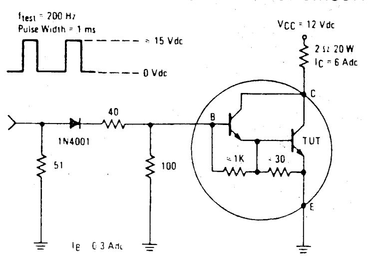


FIGURE 3 – DC CURRENT GAIN

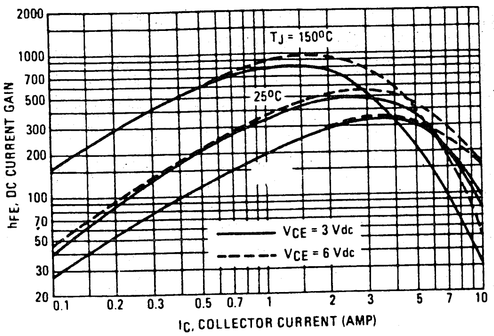


FIGURE 4 – COLLECTOR-SATURATION REGION

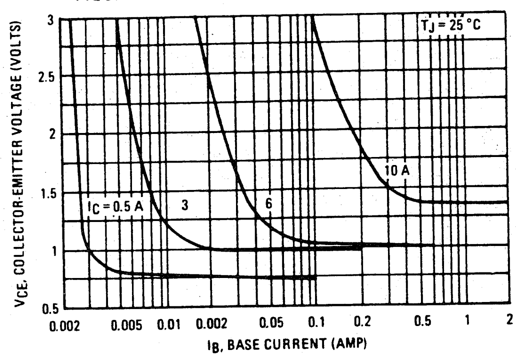


FIGURE 5 – COLLECTOR-EMITTER SATURATION VOLTAGE

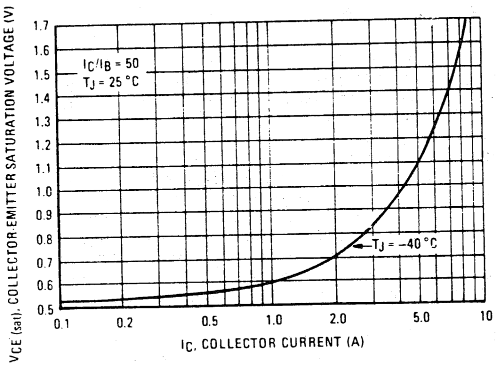


FIGURE 6 – BASE-EMITTER VOLTAGE

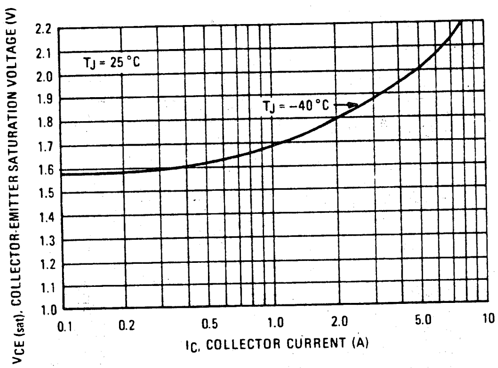


FIGURE 7 – TURN-OFF SWITCHING TIME

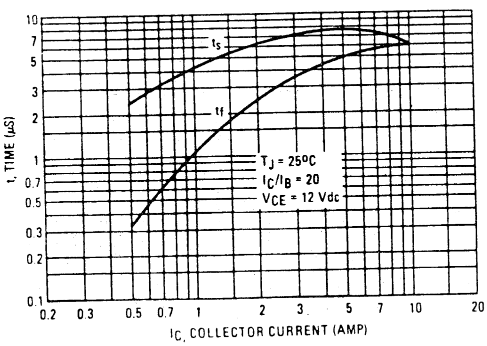


FIGURE 8 – COLLECTOR CUTOFF REGION

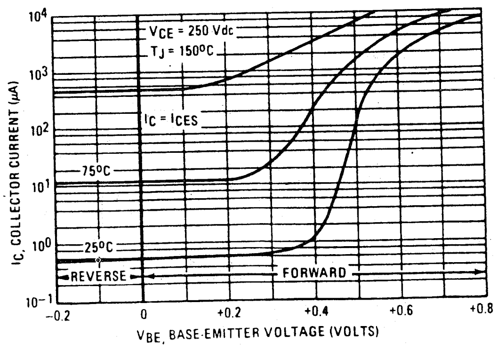


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FIGURE 9 – THERMAL RESPONSE

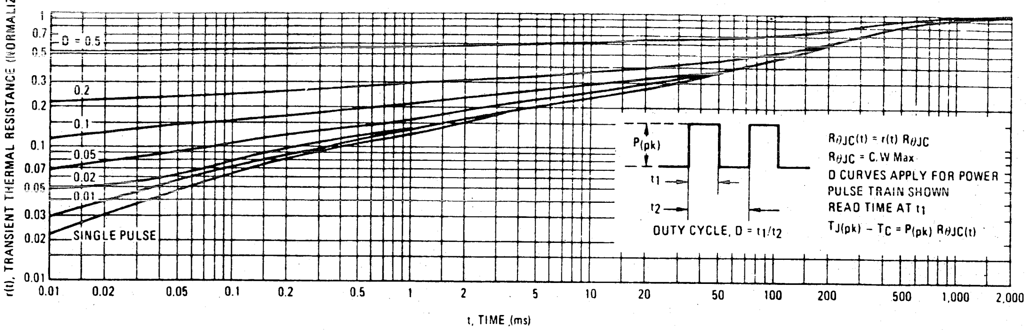
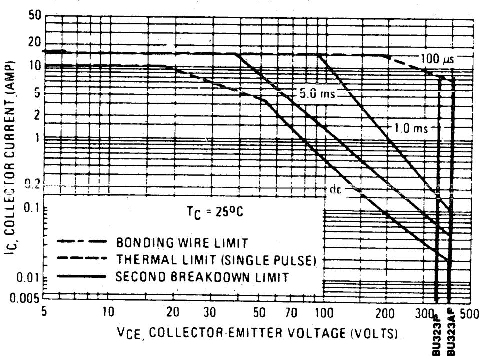


FIGURE 10 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING

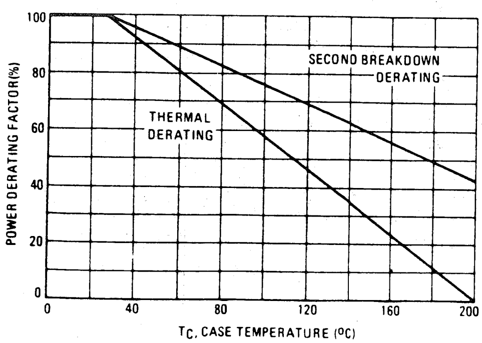
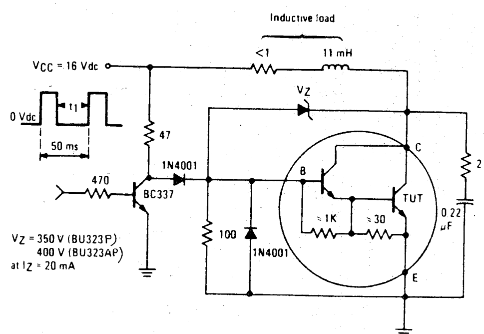


FIGURE 12 – IGNITION TEST CIRCUIT



t1 to be selected such that I_C reaches 10 Adc before switch-off

NOTE Figure 12 specifies energy handling capabilities in an automotive ignition circuit

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BU326
BU326A

6 AMPERES

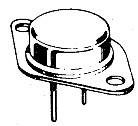
NPN SILICON POWER TRANSISTORS

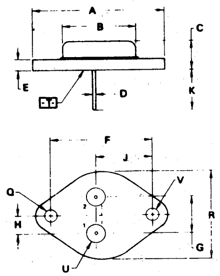
375, 400 VOLTS
90 WATTS

HIGH VOLTAGE NPN SILICON TRANSISTOR

. . . Designed for use in the switch-mode power supplies of colour television receivers.

- Collector-Emitter Voltage V_{CES} = 800 V and 900 V
- Collector-Current I_C = 6 A DC
- Low collector emitter saturation voltage
  $V_{CE\ (sat)}$ = 3 V max. at I_C = 4 A
- Fall time at I_C = 2.5 A
  T_F = 1 μs max. at T_C = 100 °C





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	⌀.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	⌀.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

MAXIMUM RATINGS

Rating	Symbol	BU326	BU326A	Unit
Collector-Emitter Voltage	$V_{CEO\ (sus)}$	375	400	Vdc
Collector-Emitter Voltage	V_{CES}	800	900	Vdc
Emitter Base Voltage	V_{EB}	10		Vdc
Collector Current – Continuous – Peak[1]	I_C I_{CM}	6 8		Adc
Base Current – Continuous – Peak[1]	I_B I_{BM}	2 3		Adc
Reverse Base Current 20 ms max. – Peak during turn off	I_B I_{BM}	100 3		mA A
Total Power Dissipation Derate above 25 °C	P_D	90 0.6		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.65	°C/W

[1] Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

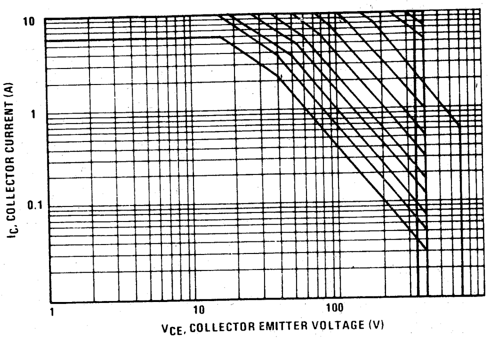
ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS[1]						
Collector-Emitter Sustaining Voltage (I_C = 100 mA, I_B = 0, L= 25 mH)	BU326 BU326A	$V_{CEO(sus)}$	375 400			Vdc
Collector-Cutoff Current (V_{CE} = 800 V, V_{BE} = 0) (V_{CE} = 900 V, V_{BE} = 0)	BU326 BU326A	I_{CES}			1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 800 V, V_{BE} = 0, T_J = 125 °C) (V_{CE} = 900 V, V_{BE} = 0, T_J = 125 °C)	BU326 BU326A	I_{CES}			2.0 2.0	mAdc
Emitter Cutoff Current (V_{EB} = 10 V, I_C = 0)		I_{EBO}			10	mAdc
ON CHARACTERISTICS[1]						
DC Current Gain (I_C = 0.6 A, V_{CE} = 5 V)		h_{FE}		30		–
Collector-Emitter Saturation Voltage (I_C = 2.5 A, I_B = 0.25 A) (I_C = 4.0 A, I_B = 1.25 A)		$V_{CE(sat)}$			10 3	Vdc
Base-Emitter Saturation Voltage (I_C = 2.5 A, I_B = 0.25 A) (I_C = 4.0 A, I_B = 1.25 A)		$V_{BE(sat)}$			1.4 1.6	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T		6		MHz
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Turn On Time	(I_C = 2.5 A, I_{B1} = 0.5 A) (I_{B2} = 1.0 A, V_{CC} = 250 V)	t_{on}			0.5	µs
Storage Time		t_s			3.5	µs
Fall Time		t_f		0.3		µs
Fall Time	(I_C = 2.5 A, I_{B1} = 0.5 A) (I_{B2} = 1.0 A, V_{CC} = 250 V, T_C = 100 °C)	t_f			1.0	µs

[1] Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2%.

3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data of figure 2 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.
At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 2 – "ON" VOLTAGES

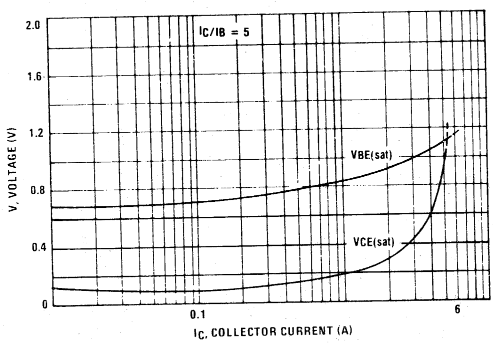


FIGURE 3 – DC CURRENT GAIN

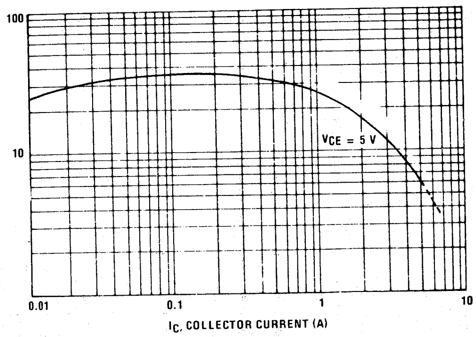


FIGURE 4 – RESISTIVE SWITCHING PERFORMANCE

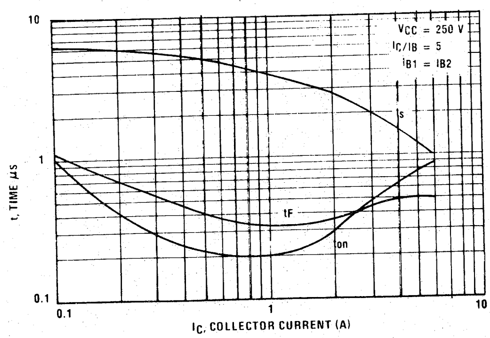
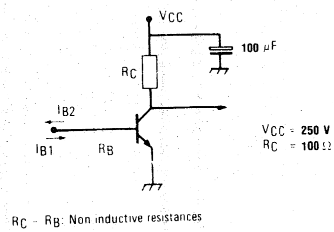


FIGURE 5 – SWITCHING TIMES TEST CIRCUIT



3

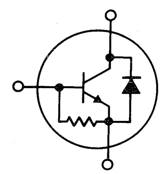
BU406,D
BU407,D

NPN Power Transistors

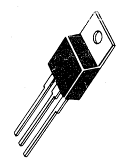
These devices are high voltage, high speed transistors for horizontal deflection output stages of TV's and CRT's.

- High Voltage: V_{CEV} = 330 or 400 V
- Fast Switching Speed: t_f = 750 ns (max)
- Low Saturation Voltage: $V_{CE(sat)}$ = 1 V (max) @ 5 A
- Packaged in Compact JEDEC TO-220AB
- "D" Suffix w/integral Damper Diode

7 AMPERES
NPN SILICON
POWER TRANSISTORS
60 WATTS
150 and 200 VOLTS



"D" SUFFIX ONLY



CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	BU406,D	BU407,D	Unit
Collector-Emitter Voltage	V_{CEO}	200	150	Vdc
Collector-Emitter Voltage	V_{CEV}	400	330	Vdc
Collector-Base Voltage	V_{CBO}	400	330	Vdc
Emitter Base Voltage	V_{EBO}	6		Vdc
Collector Current — Continuous Peak Repetitive Peak (10 ms)	I_C	7 10 15		Adc
Base Current	I_B	4		Adc
Total Device Dissipation, T_C = 25°C Derate above T_C = 25°C	P_D	60 0.48		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage(1) (I_C = 100 mAdc, I_B = 0)	BU406,D BU407,D	$V_{CEO(sus)}$	200 150	— —	— —	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, V_{BE} = 0) (V_{CE} = Rated V_{CEO} + 50 Vdc, V_{BE} = 0) (V_{CE} = Rated V_{CEO} + 50 Vdc, V_{BE} = 0, T_C = 150°C)		I_{CES}	— — —	— — —	5 0.1 1	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	BU406, BU407 BU406D, BU407D	I_{EBO}	— —	— —	1 400	mAdc
ON CHARACTERISTICS(1)						
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	—	—	1	Vdc
Base-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)		$V_{BE(sat)}$	—	—	1.2	Vdc
Forward Diode Voltage (I_{EC} = 5 Adc) "D" only		V_{EC}	—	—	2	Volts

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 1%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 20 MHz)	f_T	10	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	80	—	pF
SWITCHING CHARACTERISTICS					
Inductive Load Crossover Time (V_{CC} = 40 Vdc, I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc, L = 150 μH)	t_c	—	—	0.75	μs

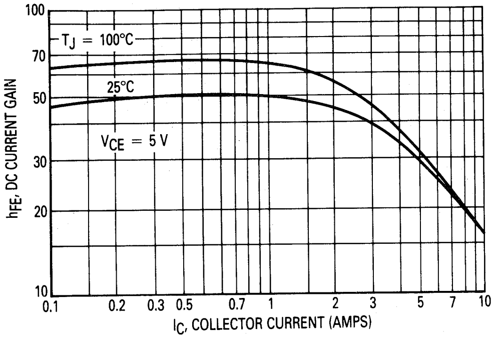


Figure 1. DC Current Gain

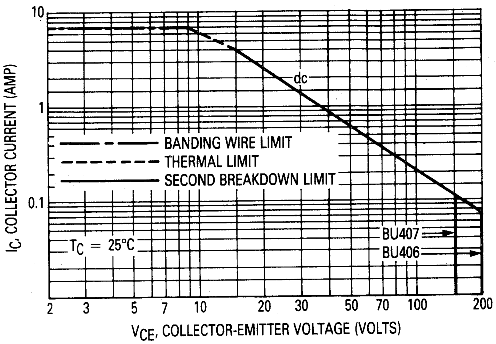
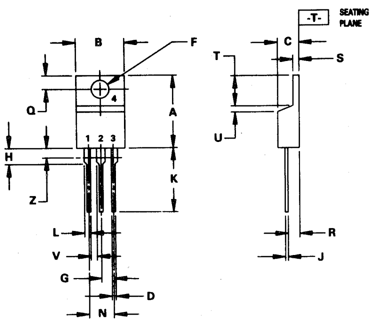


Figure 2. Maximum Rated Forward Bias Safe Operating Area

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BU426
BU426A

HIGH VOLTAGE NPN SILICON TRANSISTOR

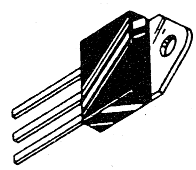
. . . designed for use in the switched mode power supply of 90° and 110° colour television receivers.

- High Collector-Emitter Voltage
  V_{CES} = 800 V, 900 V
- Collector Current
  I_C = 6 Adc
- Low Collector Emitter Saturation Voltage
  $V_{CE(sat)}$ = 3 Vdc, @ I_C = 4 A, I_B = 1.25 Adc
- Fall Time @ I_C = 2.5 A, $I_{B\,(end)}$ = 1 A
  t_f = 0,3 μsec (typ)

6 AMPERES

TRIPLE DIFFUSED NPN SILICON POWER TRANSISTORS

800, 900 VOLTS
113 WATTS



MAXIMUM RATINGS

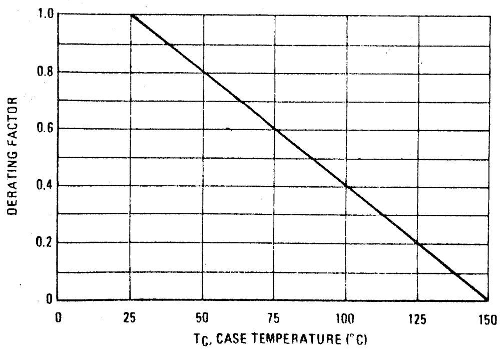
Rating	Symbol	BU426	BU426A	Unit
Collector-Emitter Voltage	V_{CEO}	375	400	Vdc
Collector-Emitter Voltage V_{BE} = 0	V_{CES}	800	900	Vdc
Emitter-Base Voltage	V_{EB}	10		Vdc
Collector Current — Continuous — Peak	I_C	6 12		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	113 0.90		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 150		°C

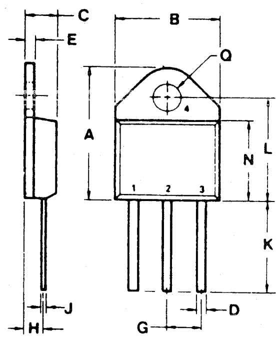
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.1	°C/W

3

FIGURE 1 — POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
(TO-218AC)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage See Figure 8 (I_C = 100 mA, L = 25 mH)	BU426	V_{CEO}	375	–	–	Vdc
	BU426A		400	–	–	
Collector-Cutoff Current (V_{CES} = Rated Value, T_C = 25°C)		I_{CES}	–	–	1.0	mAdc
(V_{CES} = Rated Value, T_C = 125°C)			–	–	2.0	
Emitter Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}	–	–	10	mAdc

ON CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
DC Current Gain (I_C = 0.6 Adc, V_{CE} = 5 Vdc)	h_{FE}		30	–	-
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 0.5 Adc)	$V_{CE(sat)}$	–	–	1.5	Vdc
(I_C = 4 Adc, I_B = 1.25 Adc)		–	–	3	
		–	–		
Base-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 1.25 Adc)	$V_{BE(sat)}$	–	–	1.6	Vdc
(I_C = 2.5 Adc, I_B = 0.5 Adc)		–	–	1.4	

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Current Gain – Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T		6		MHz

3

SWITCHING CHARACTERISTICS (Resistive Load)

	Conditions	Symbol	MIN.	TYP.	MAX.	Unit
Turn on Time	(I_C = 2.5 A, I_{B1} = 0.5 A) (I_{B2} = 1.0 A, V_{CC} = 250 V)	t_{on}		0.2	0.6	μs
Storage Time		t_s		2	3.5	
Fall Time		t_f		0.5		
Fall Time	(I_C = 2.5 A, I_{B1} = 0.5 A) (I_{B2} = 1.0 A, V_{CC} = 250 V, T_C = 95°C)	t_f			0.75	μs
		t_f				

FIGURE 2 – DC CURRENT GAIN

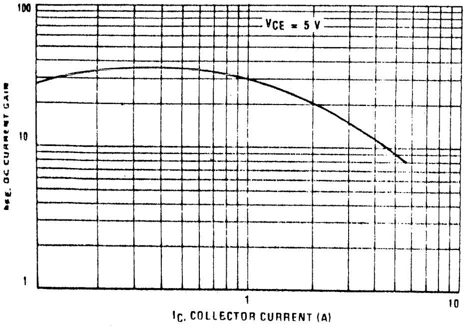


FIGURE 3 – "ON VOLTAGE"

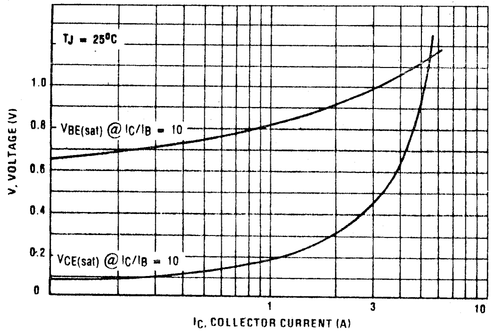


FIGURE 4 – TURN ON TIMES

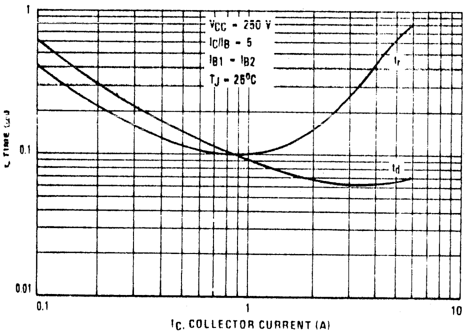


FIGURE 5 – TURN OFF TIMES

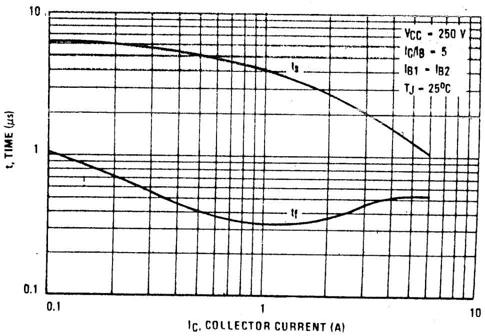
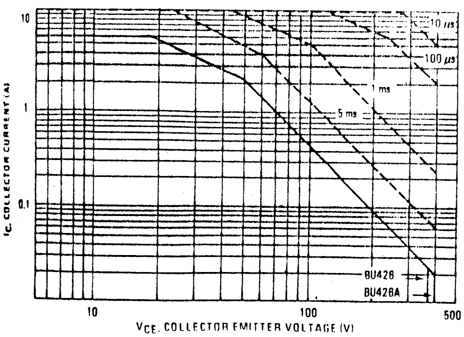


FIGURE 6 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C \cdot V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 6 is based on $T_{J(pk)}$ 150°C, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN 415A)

FIGURE 7 – THERMAL RESPONSE

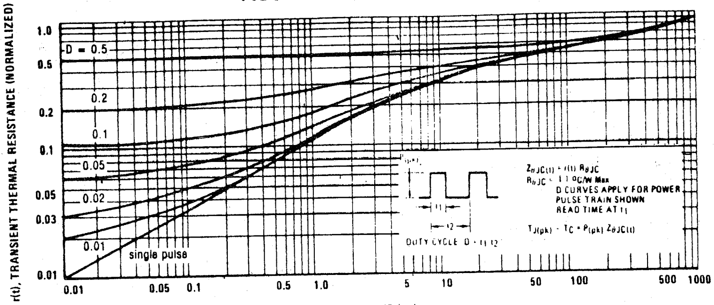
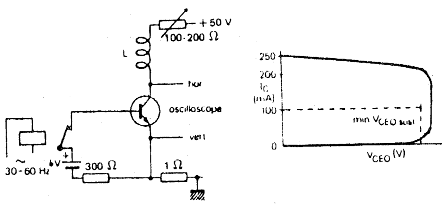


FIGURE 8 – SUSTAINING VOLTAGE TEST CIRCUIT



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BU500

HORIZONTAL DEFLECTION TRANSISTOR

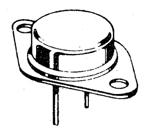
. . . specifically designed for use in large screen color deflection circuits

- V_{CEX} = 1500 V;
  $V_{CEO(sus)}$ = 700 V (min.)
- Low saturation:
  $V_{CE(sat)}$ = 1 V (max.) @ Ic = 4.5 Adc

6 AMPERES

NPN SILICON POWER METAL TRANSISTOR

1500 VOLTS
75 WATTS



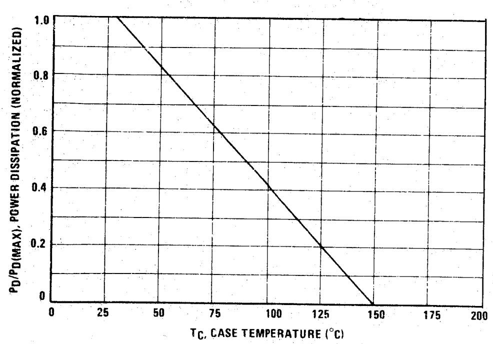
MAXIMUM RATINGS

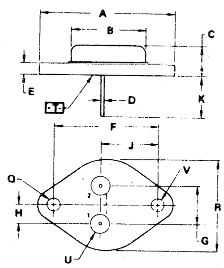
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector-Base Voltage	V_{CBO}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector-Emitter Voltage (V_{BE} = −2.0 V)	V_{CEX}	1500	Vdc
Collector-Current — continuous — peak (pw ⩽ 300 μs)	I_C I_{CM}	6 16	Adc Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ T_C = 25°C	P_D	75	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.66	°C/W

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ ⌀0.13 (0.005) Ⓜ T V Ⓜ
   FOR LEADS:
   ⌖ ⌀0.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS (1)				
Collector-Emitter Sustaining Voltage ($I_C = 500$ mAdc, $I_B = 0$) L = 10 mH	$V_{CEO(sus)}$	700		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 1000$ V, $I_E = 0$) ($V_{CE} = 1500$ V, $I_E = 0$)	I_{CBO}		0.02 1.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 1500$ V, $V_{BE} = -2$ V)	I_{CEX}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 100$ mA)	V_{EBO}	5		V
Emitter Cutoff Current ($V_{EB} = 4$ V)	I_{EBO}		10	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 4.5$ Adc, $V_{CE} = 5$ V)	h_{FE}	3.0		–
Collector-Emitter Saturation Voltage ($I_C = 4.5$ Adc, $I_B = 2$ A)	$V_{CE(sat)}$		1.0	Vdc
Base-Emitter On Voltage ($I_C = 4.5$Adc, $V_{CE} = 2$ A)	$V_{BE(on)}$		1.3	Vdc

SWITCHING CHARACTERISTICS (Resistive Load)

	Conditions	Symbol	Min.	Max.	Unit
	($V_{CC} = 100$ Vdc, $I_C = 4.5$ A, $I_{B1} = 1.5$ A, $I_{B2} = 1.5$ A)		–		μs
Storage Time		t_s	–	1.2	
Fall Time		t_f	–	1.0	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

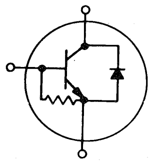
3

BU508
BU508D
BU508A
BU508AD

NPN Silicon Power Transistors
Horizontal Deflection

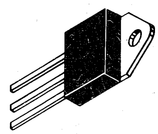
. . . specifically designed for use in large screen color deflection circuits.

- Glass Passivated (Patented Photoglass)
- Triple Diffused Mesa Technology for Long Term Stability
- Collector-Emitter Voltage — V_{CE} = 1500 Vdc
- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 700 Vdc
- Switching Times with Inductive Loads, t_f = 0.5 μs (Typ) @ I_C = 4.5 A
- Optimum Drive Condition Curves
- Glass Base-Collector Junction
- TO-218 Package for Low Cost Mounting
- Available with Internal Flyback Diode, "D" Suffix



"D" SUFFIX

POWER TRANSISTORS
8 AMPERES
1500 VOLTS



CASE 340-01
TO-218 AC

MAXIMUM RATINGS

Rating	Symbol	All Parts	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector-Emmiter Voltage	V_{CES}	1500	Vdc
Emitter Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak(1)	I_C I_{CM}	8 15	Adc
Base Current — Continuous Peak(1)	I_B I_{BM}	4 6	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 seconds	T_L	275	°C

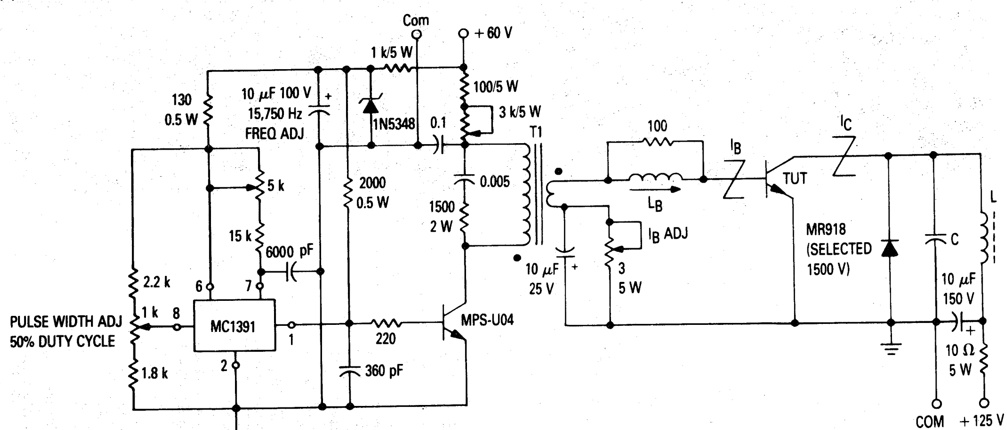
(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)						
Collector-Emitter sustaining voltage (I_C = 100 mAdc, I_B = 0)		$V_{CEO(sus)}$	700	—	—	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0, T_C = 25°C) (V_{CE} = 1500 Vdc, V_{BE} = 0, T_C = 125°C)		I_{CES}	— —	— —	0.1 2	mAdc
Emitter Base Leakage (V_{EB} = 6 V, I_C = 0)	BU508, A BU508D, AD	I_{EBO}		—	10 300	mAdc
ON CHARACTERISTICS(1)						
DC Current Gain (I_C = 4.5 Adc, V_{CE} = Vdc)		h_{FE}	2.25	—	—	—
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)	BU508, D BU508A, AD	$V_{CE(sat)}$	—	—	3 1	Vdc
Base Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)		$V_{BE(sat)}$	—	—	1.3	Vdc
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$		See Figure 11		
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)		f_T	—	7	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	125	—	pF
SWITCHING CHARACTERISTICS						
Fall Time	(I_C = 4.5 Adc, I_B = 1.8 Adc, dI_B/dt = 1 A/µs, LB = 10 µH, see Figure 1)	t_s t_f		8 0.5		µs

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



I_C A	L mH	C µF
3.5	0.87	0.013
4.5	0.67	0.017

DRIVER TRANSFORMER (T1)

- Ferrox cube pot core #4229P-L00-3C8
- Adjust gap for primary inductance Lp = 70 mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than 3 µH
- Use 3 mil mylar tape between each winding layer

Figure 1. Switching Times Test Circuit

3

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B. This kind of analysis shows the parameter which really matters is dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. For very low L_B a very narrow optimum is obtained. This occurs when I_{B1} h_{FE} = I_{CM}, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the I_{B1} h_{FE} = I_{CM} point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor *initiation* of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation I_{B1} h_{FE} = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Neither L_B nor I_{B1} are absolutely critical, and should be selected for the specific required condition. Similar curves relating to this discussion can be found on Motorola's data sheet for the BU207.

TEST CIRCUIT WAVEFORMS

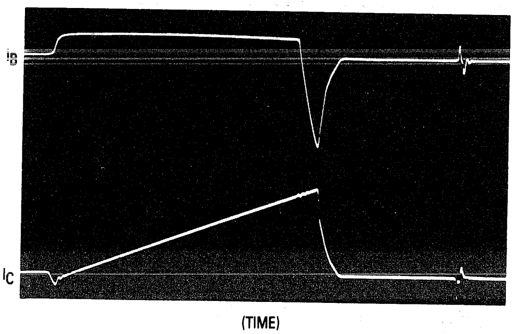


Figure 2.

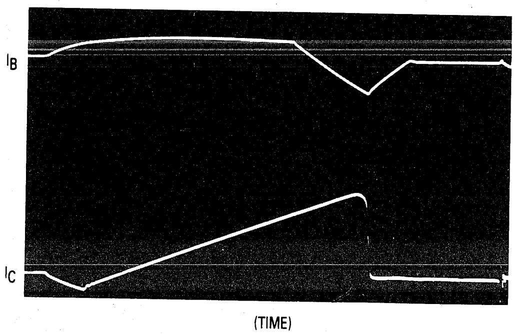


Figure 3.

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

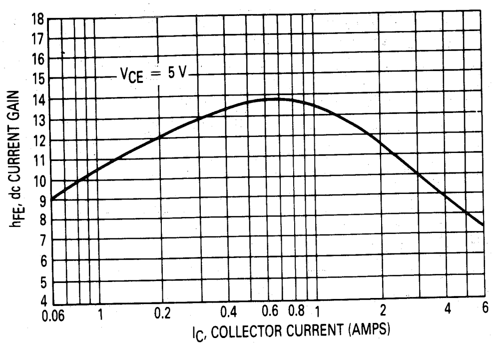


Figure 4. Typical dc Current Gain

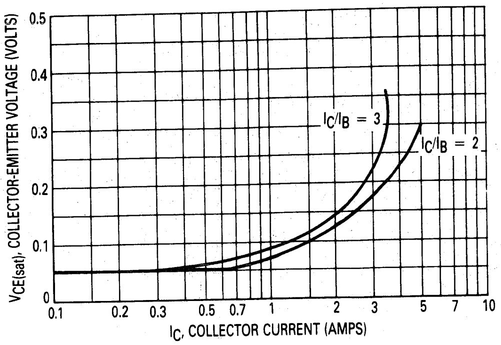


Figure 5. Typical Collector Saturation Voltage

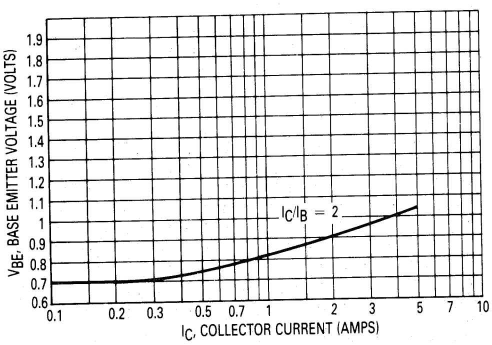


Figure 6. Typical Base Emitter Saturation Voltage

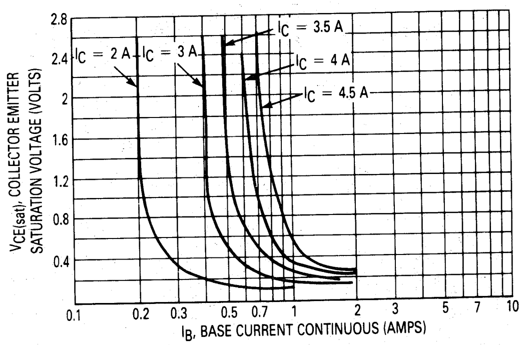


Figure 7. Typical Collector Saturation Region

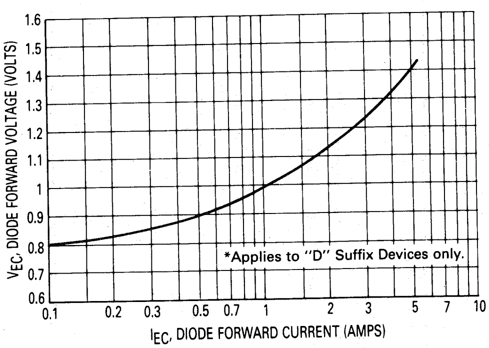


Figure 8. Typical Damper Diode Forward Voltage*

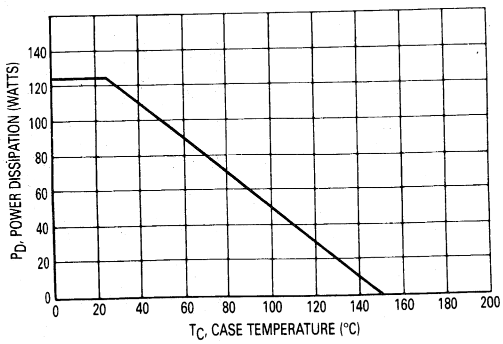


Figure 9. Power-Temperature Derating Curve

3

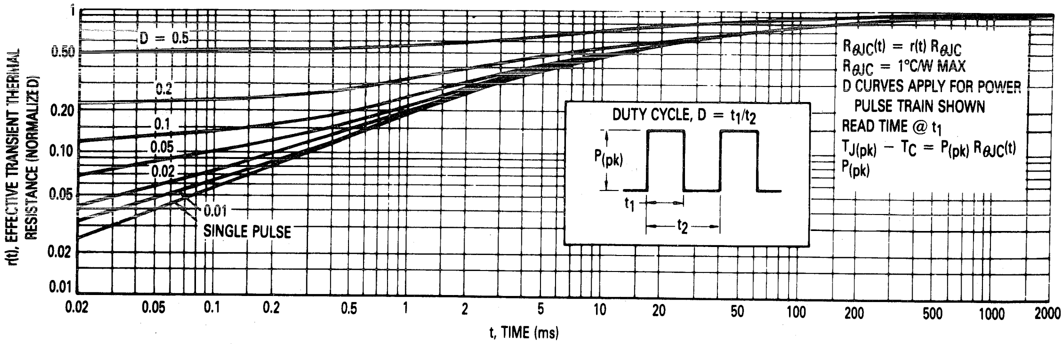


Figure 10. Thermal Response

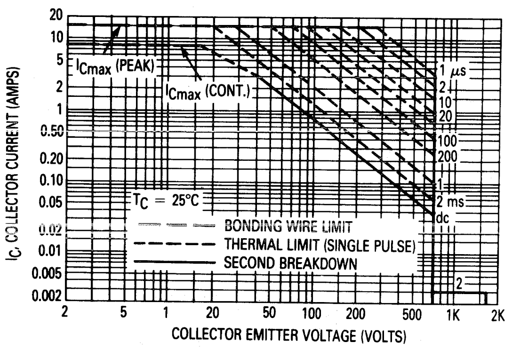
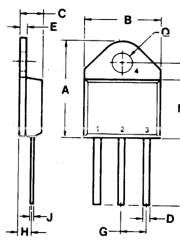


Figure 11. Maximum Forward Biased Safe Operating Area

Note (2) Operation in this area limited to Pulse Width < 20 μs, Duty Cycle < 0.25, R_{BE} < 100 ohms

CASE 340-01
TO-218 AC

STYLE 1:
PIN 1. BASE 3. EMITTER
2. COLLECTOR 4. COLLECTOR



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BU522
BU522A
BU522B

HIGH VOLTAGE SILICON POWER DARLINGTONS

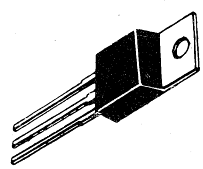
Power Transistor mainly intended for use as ignition circuit output transistor.

- Specified minimum sustaining voltage:
  $V_{CER(sus)}$ = 350 V (BU522)
  at I_C = 1 A 400 V (BU522A)
  425 V (BU522B)
- High S.O.A. capability:
  V_{CE} = 350 V (BU522) at I_C = 5 A
  400 V (BU522A, BU522B)
- Low $V_{CE(sat)}$ = 2.0 V max. at I_C = 4 A (BU522A, BU522B)

7 AMPERES

DARLINGTON TRIPLE DIFFUSED POWER TRANSISTORS NPN SILICON

375, 425, 450 VOLTS
75 WATTS

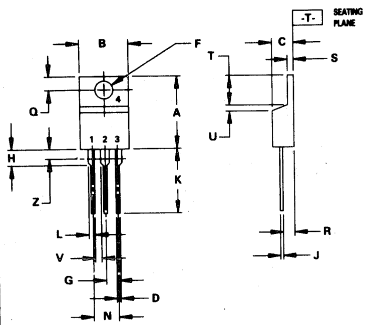


MAXIMUM RATINGS

Rating	Symbol	BU522	BU522A	BU522B	Unit
Collector-Emitter Voltage Sust.	$V_{CER(sus)}$	350	400	425	Vdc
Collector-Emitter Voltage	V_{CER}	375	425	450	Vdc
Collector-Base Voltage	V_{CBO}	400	450	475	Vdc
Emitter-Base Voltage	V_{EBO}		5.0		Vdc
Collector Current - Continuous	I_C		7.0		Adc
Base Current	I_B		2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		75 0.60		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W



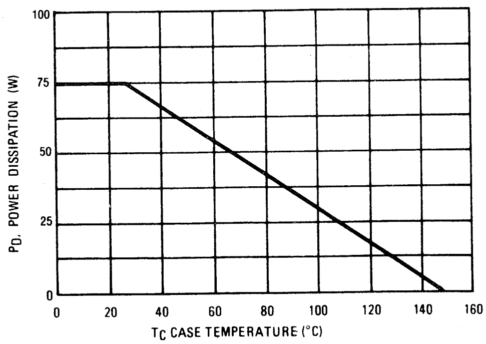
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

FIGURE 1 — POWER DERATING



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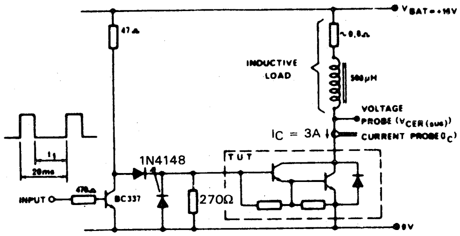
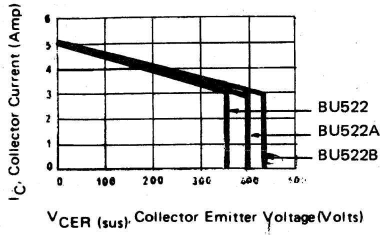
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (See Figure 2) (I_C = 1.0 A) See Figure 2 BU522 / BU522A / BU522B	$V_{CER(sus)}$	350 / 400 / 425			Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 270 Ω)	I_{CER}			1.0	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)	I_{CBO}			1.0	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}			40	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 5 Vdc)	h_{FE}	250			–
Collector-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 80 mAdc) BU522 / BU522A, BU522B	$V_{CE(sat)}$			2.5 / 2	Vdc
Base-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 80 mAdc)	$V_{BE(sat)}$			2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (I_C = 0.3 mAdc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T		7.5		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}		150		pF

3

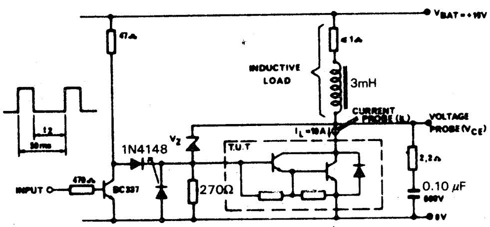
FIGURE 2 – SUSTAINING VOLTAGE TEST $V_{CER\ (sus)}$





t_1 to be selected that I_C reaches 3 Adc before switch-off
Case temperature of the power transistor: $T_C = 25^oC$

Test conditions of the Collector-Base Clamping Circuit:



Clamping device characteristics:

V_Z = 350 V (BU522) / 400 V (BU522A/B) ± 1% at I_Z = 20 mA

Clamping duration is around 45 μsec (BU522) / 40 μsec (BU522A/B)

t_2 to be selected that I_L reaches 5 Adc before switch-off

Case temperature of the power transistor: $T_C = 25^oC$.

FIGURE 3 – S.O.A. TEST

3

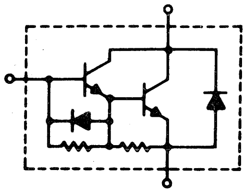
BU806
BU807

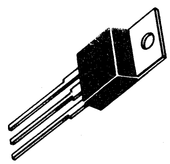
8.0 AMPERE
DARLINGTON NPN POWER TRANSISTORS
60 WATTS
150 and 200 VOLTS

NPN DARLINGTON POWER TRANSISTORS

These Darlington transistors are high voltage, high speed devices for horizontal deflection circuits in TV's and CRT's.

- High Voltage: V_{CEV} = 330 or 400 V
- Fast Switching Speed: t_c = 1.0 μs (max)
- Low Saturation Voltage: $V_{CE(sat)}$ = 1.5 V (max)
- Packaged in JEDEC TO-220AB
- Damper Diode V_F is specified. V_F = 2.0 V (max)



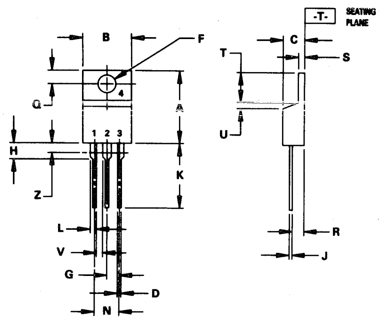


MAXIMUM RATINGS

Rating	Symbol	BU806	BU807	Unit
Collector-Emitter Voltage	V_{CEO}	200	150	Vdc
Collector-Emitter Voltage	V_{CEV}	400	330	Vdc
Collector-Base Voltage	V_{CBO}	400	330	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current — Continuous — Peak	I_C	8.0 15		Adc
Emitter-Collector Diode Current	I_F	10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation, T_C = 25°C Derate above T_C = 25°C	P_D	60 0.48		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Lead Temperature for Soldering Purposes, 1/8" from Case for 5.0 Seconds	T_L	275	°C



NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	BU806 BU807	$V_{CEO(sus)}$	200 150	— —	— —	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CBO}, V_{BE} = 0)		I_{CES}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 6.0 Vdc)		I_{CEV}	—	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	3.0	mAdc
ON CHARACTERISTICS (1)						
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 50 mAdc)		$V_{CE(sat)}$	—	—	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 50 mAdc)		$V_{BE(sat)}$	—	—	2.4	Vdc
Emitter-Collector Diode Forward Voltage (I_F = 4.0 Adc)		V_F	—	—	2.0	Vdc
SWITCHING CHARACTERISTICS						
Turn-On Time	(Resistive Load, V_{CC} = 100 Vdc, I_C = 5.0 Adc, I_{B1} = 50 mAdc, I_{B2} = 500 mAdc)	t_{on}	—	0.35	—	μs
Storage Time		t_s	—	0.55	—	μs
Fall Time		t_f	—	0.20	—	μs
Crossover Time (I_C = 5.0 Adc, I_{B1} = 50 mAdc, $V_{BE(off)}$ = 4.0 Vdc, V_{clamp} = 200 Vdc, L = 500 μH)		t_c	—	0.40	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 1%.

3

FIGURE 1 — DC CURRENT GAIN

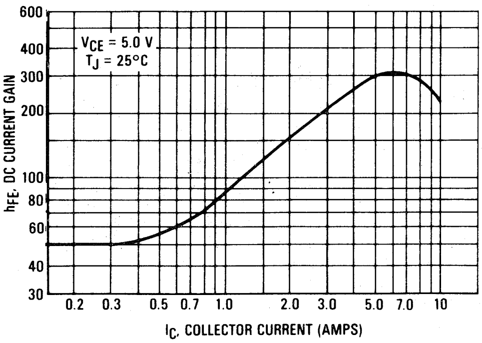
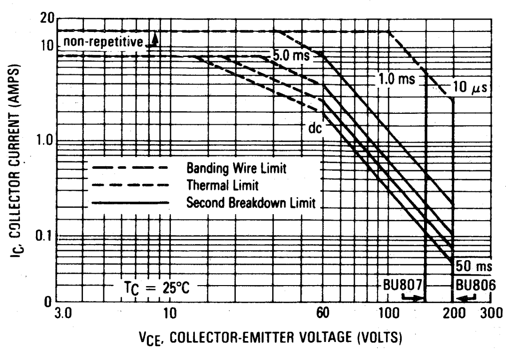


FIGURE 2 — SAFE OPERATING AREA (FBSOA)



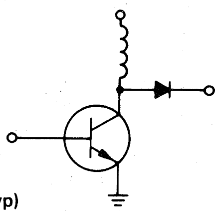
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUS36
BUS37

SWITCHMODE II▲ SERIES
NPN SILICON POWER TRANSISTORS

The BUS36 and BUS37 transistors are designed for low voltage, high speed, power switching in inductive and resistive circuits where turn-off times are critical. They are particularly suited for battery-operated Switchmode applications and driver applications such as :

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls



Fast Turn-Off Times
 60 ns Inductive Fall Time — 25°C (Typ)
 110 ns Inductive Crossover Time — 25°C (Typ)

Operating Temperature Range — 65 to + 175°C

100°C Performance Specified for :
 Reverse-Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents (125°C)

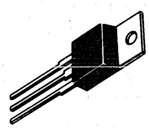
12 AMPERES

NPN SILICON POWER TRANSISTORS

120 & 150 VOLTS
107 WATTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



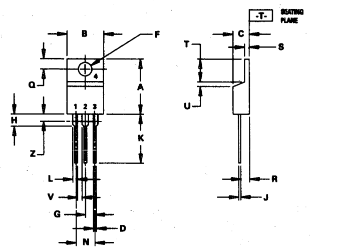
MAXIMUM RATINGS

Rating	Symbol	BUS36	BUS37	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	120	150	Vdc
Collector-Emitter Voltage	V_{CEV}	250	300	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous — Peak(1) — Overload	I_C I_{OL}	12 25 40		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	7 15		Adc
Total Power Dissipation — T_C = 25°C — T_C = 100°C Derate above 25°C	P_D	107 53 0.71		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 65 to + 175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 50 mA, I_B = 0) L = 25 mH BUS36	$V_{CEO(sus)}$	120	–		Vdc
BUS37		150	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	0.1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		–	–	1.0	
Collector Cutoff Current BUS36 : V_{CE} = 60 V	I_{CEO}	–	–	0.05	mAdc
BUS37 : V_{CE} = 75 V		–	–	0.05	
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	I_{EBO}			0.1	mAdc
Emitter-base breakdown Voltage (I_E = 50 mA - I_C = 0)	BV_{EBO}	8.0			Vdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 12		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 2 Vdc)	h_{FE}	30	–	–	–
(I_C = 0.5 Amp, V_{CE} = 2 V)		50	–	–	
Collector-Emitter Saturation Voltage (I_C = 12 Amp, I_B = 1.2 Amp)	$V_{CE(sat)}$	–	–	0.8	Vdc
(I_C = 12 Amp, I_B = 1.2 Amp, T_c = 100°C)		–	–	1.0	
Base-Emitter Saturation Voltage (I_C = 12 Amp, I_B = 1.2 Amp)	$V_{BE(sat)}$	–	–	1.8	Vdc
(I_C = 12 Amp, I_B = 1.2 Amp, T_c = 100°C)		–	–	1.8	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 khz)	C_{ob}	–	–	300	pF
Current Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz	f_T	30	–	–	MHz

SWITCHING CHARACTERISTICS
Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	(V_{CC} = 100 Vdc, I_C = 12 A, I_{B1} = 1.2 A, t_p = 30 μs, Duty Cycle ≤ 2%, $V_{BE(off)}$ = 5 V)	t_d	–	0.07	0.15	μs
Rise Time		t_r	–	0.15	0.3	
Storage Time		t_s	–	0.5	1.0	
Fall Time		t_f	–	0.12	0.25	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)}$ = 12 A, I_{B1} = 1.2 A, $V_{BE(off)}$ = 5 V, $V_{CE(c1)}$ = 100 V)	(T_C = 25°C)	t_{sv}	–	0.5	–	μs
Fall Time			t_{fi}	–	0.06	–	
Storage Time		(T_C = 100°C)	t_{sv}	–	0.6	1.0	
Fall Time			t_{fi}	–	0.15	0.30	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

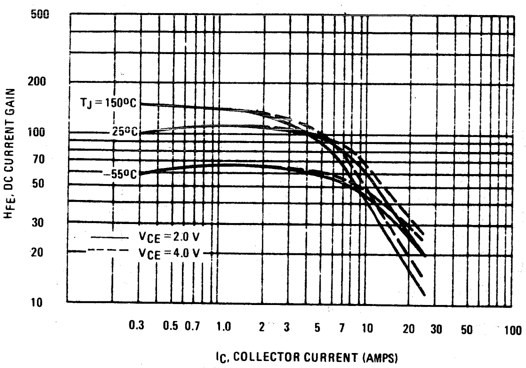


FIGURE 2 – COLLECTOR SATURATION REGION

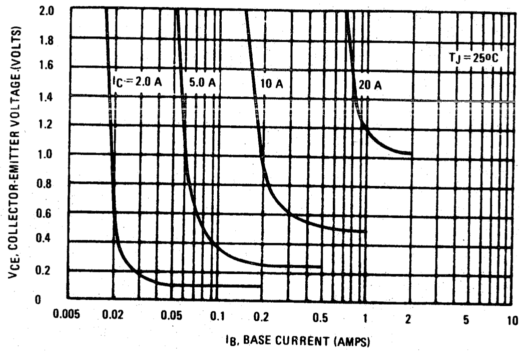


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

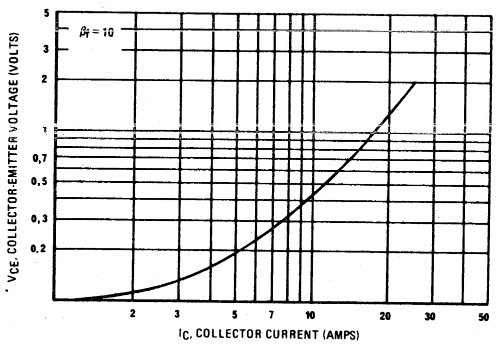


FIGURE 4 – BASE-EMITTER VOLTAGE

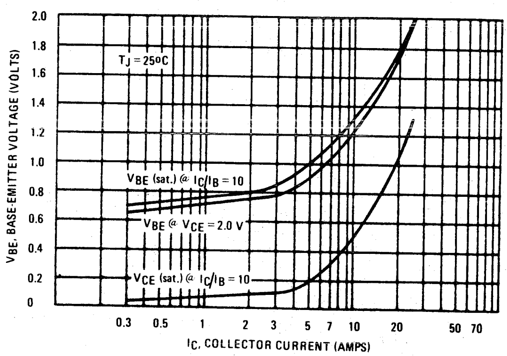


FIGURE 5 – COLLECTOR CUTOFF REGION

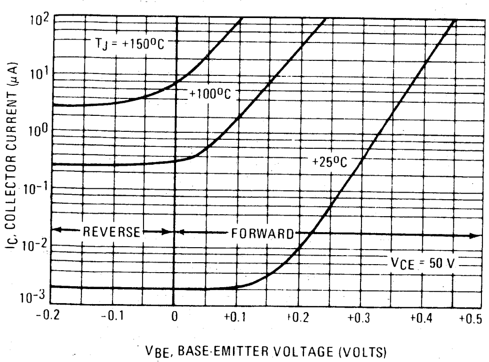


FIGURE 6 – CAPACITANCE

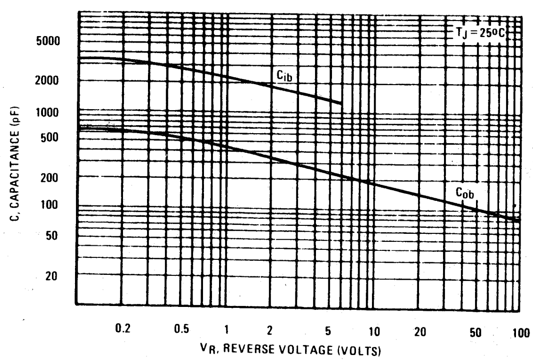


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TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

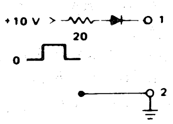
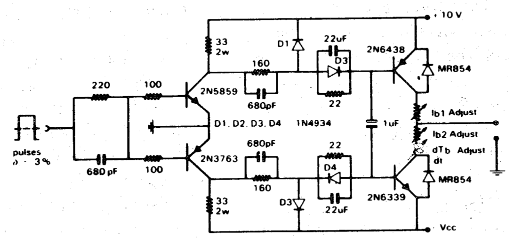
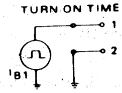
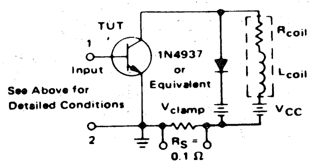
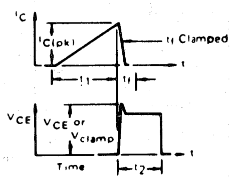
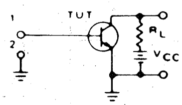
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

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FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

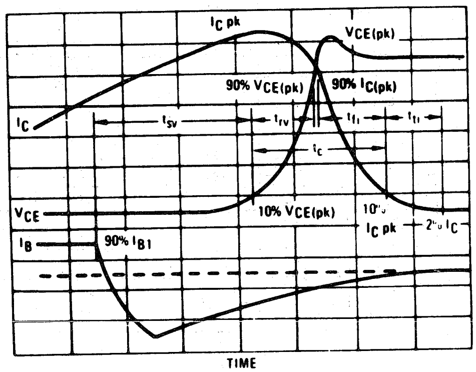
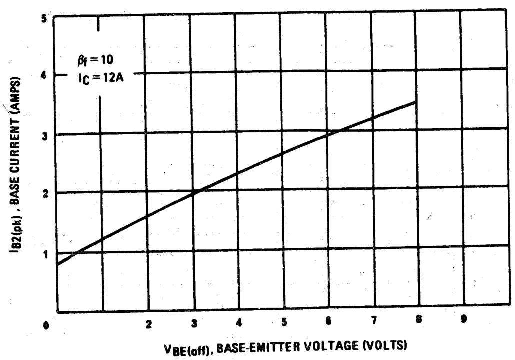


FIGURE 8 – PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME, Tsv

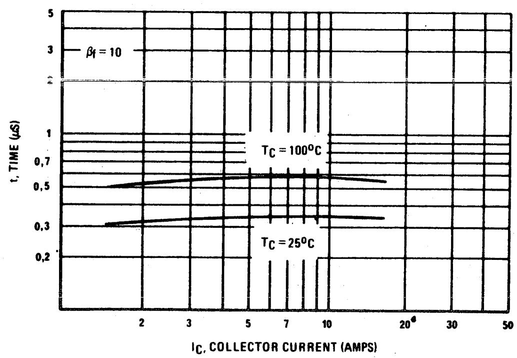


FIGURE 10 – FALL TIMES

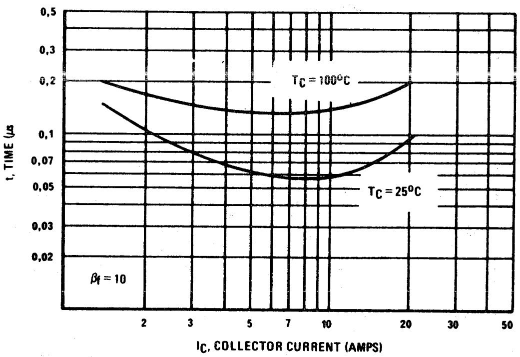


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

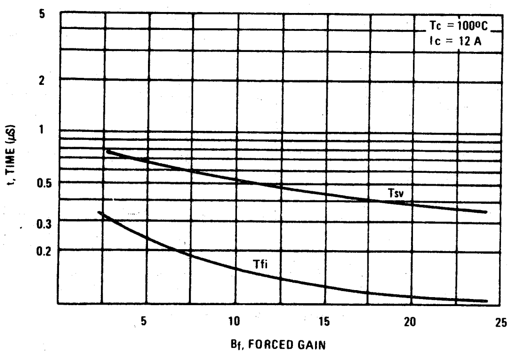
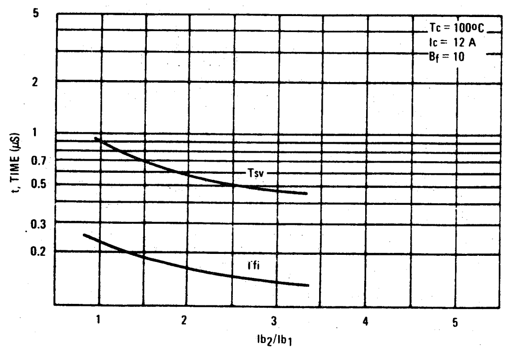


FIGURE 11b – TURN-OFF TIMES vs I_{b2}/I_{b1}



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The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

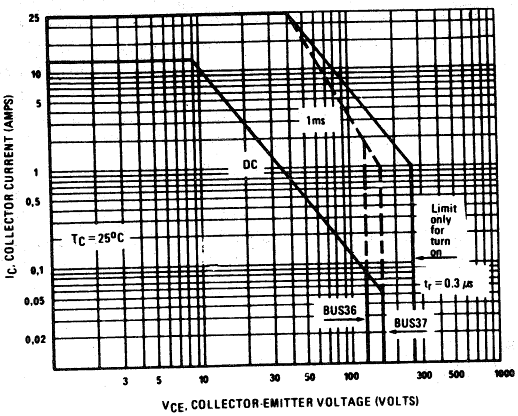


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

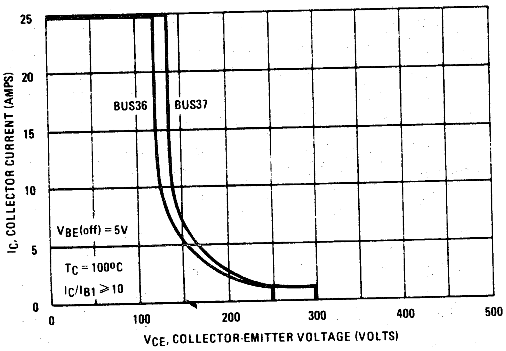
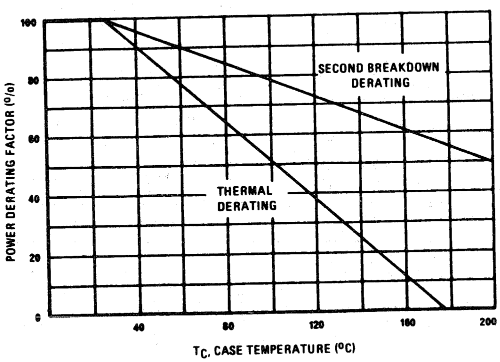


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

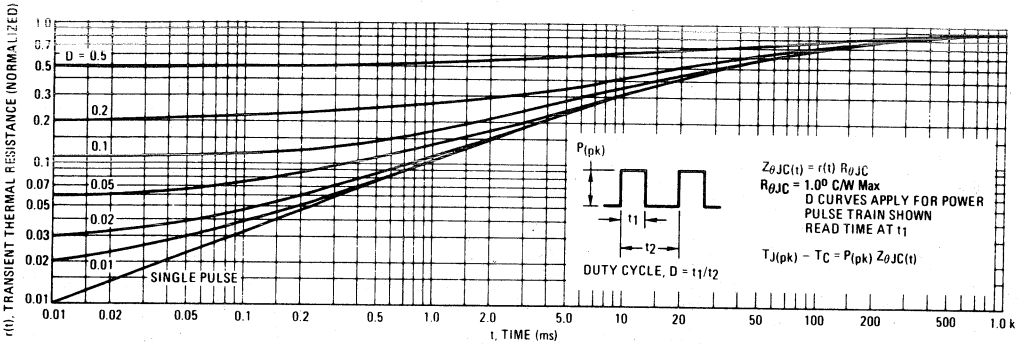
$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

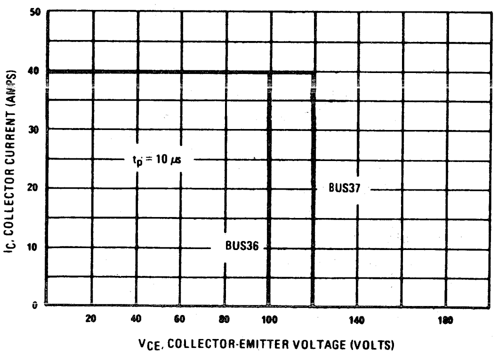
3

FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

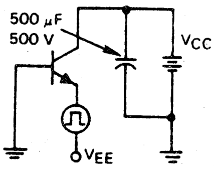
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 17) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 17 – OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

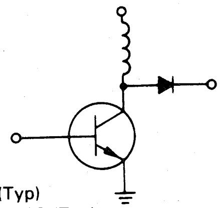


MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUS45P

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The BUS 45P transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:



- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
 100 ns Inductive Fall Time — 25°C (Typ)
 150 ns Inductive Crossover Time — 25°C (Typ)
 400 ns Inductive Storage Time — 25°C (Typ)

Operating Temperature Range −65 to +150°C

100°C Performance Specified for:
 Reverse-Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents

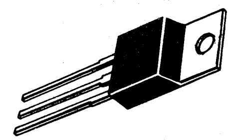
3 AMPERES

NPN SILICON POWER TRANSISTORS

450 VOLTS
75 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



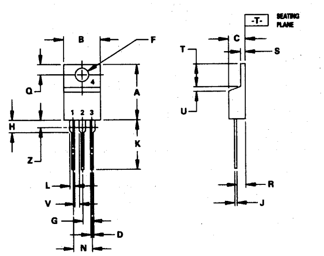
MAXIMUM RATINGS

Rating	Symbol	BUS 45P	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6	Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	3 5	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	1.5 3	Adc
Total Power Dissipation – T_C = 25°C – T_C = 100°C Derate above 25°C	P_D	75	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦ 10%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = 850 V, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 V, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	– –	– –	0.5 2.5	mAdc
Collector Cutoff Current (V_{CE} = 850 V, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc

ON CHARACTERISTICS (1)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Current Gain (I_C = 2 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	6	–	–	–
Collector-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.5 Adc) (I_C = 3 Adc, I_B = 0.75 Adc) (I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)	$V_{CE(sat)}$	– – –	– – –	1.0 3.0 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.5 Adc) (I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)	$V_{BE(sat)}$	– –	– –	1.5 1.5	Vdc

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	(V_{CC} = 250 Adc, I_C = 2 A, I_{B1} = 0.5 Adc, t_p = 30 μs, Duty Cycle ≤ 2%, $V_{BE(off)}$ = 5.0 Vdc)	t_d	–	0.03	0.05	μs
Rise Time		t_r	–	0.10	0.40	
Storage Time		t_s	–	0.40	1.50	
Fall Time		t_f	–	0.175	0.50	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)}$ = 2 A, I_{B1} = 0.5 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V)	(T_J = 100°C)	t_{sv}	–	0.70	2.0	μs
Crossover Time			t_c	–	0.28	0.50	
Fall Time			t_{fi}	–	0.15	0.35	
Storage Time		(T_J = 25°C)	t_{sv}	–	0.40	–	
Crossover Time			t_c	–	0.15	–	
Fall Time			t_{fi}	–	0.10	–	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

$$\beta_f = \frac{I_C}{I_B}$$

3

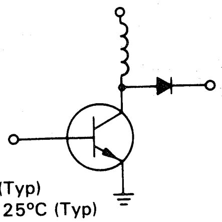
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUS46P

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The BUS 46P transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
  100 ns Inductive Fall Time — 25°C (Typ)
  150 ns Inductive Crossover Time — 25°C (Typ)
  400 ns Inductive Storage Time — 25°C (Typ)

Operating Temperature Range −65 to +150°C

100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents

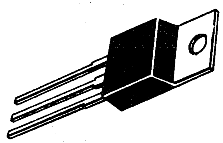
5 AMPERES

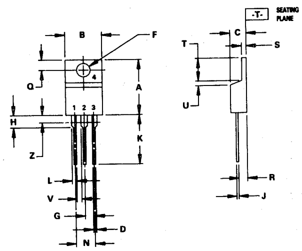
NPN SILICON POWER TRANSISTORS

450 VOLTS
80 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	BUS 46P	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6	Vdc
Collector Current − Continuous − Peak (1)	I_C I_{CM}	5 8	Adc
Base Current − Continuous − Peak (1)	I_B I_{BM}	2 4	Adc
Total Power Dissipation − T_C = 25°C − T_C = 100°C Derate above 25°C	P_D	80	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = 850 V, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 V, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	 – –	 – –	 0.5 2.5	mAdc
Collector Cutoff Current (V_{CE} = 850 V, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 12		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	7.0	–	–	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)	$V_{CE(sat)}$	 – – –	 – – –	 1.0 3.0 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)	$V_{BE(sat)}$	 – –	 – –	 1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 Khz)	C_{ob}	–	–	250	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	(V_{CC} = 250 Adc, I_C = 3.0 Adc, I_{B1} = 0.4 Adc, t_p = 30 μs, Duty Cycle ≦ 2%, $V_{BE(off)}$ = 5.0 Vdc)	t_d	–	0.03	0.05	μs
Rise Time		t_r	–	0.10	0.40	
Storage Time		t_s	–	0.40	1.50	
Fall Time		t_f	–	0.175	0.50	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)}$ = 3.0 A, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V)	(T_J = 100°C)	t_{sv}	–	0.70	2.0	μs
Crossover Time			t_c	–	0.28	0.50	
Fall Time			t_{fi}	–	0.15	0.30	
Storage Time		(T_J = 25°C)	t_{sv}	–	0.40	–	
Crossover Time			t_c	–	0.15	–	
Fall Time			t_{fi}	–	0.10	–	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

$\beta_f = \frac{I_C}{I_B}$

3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

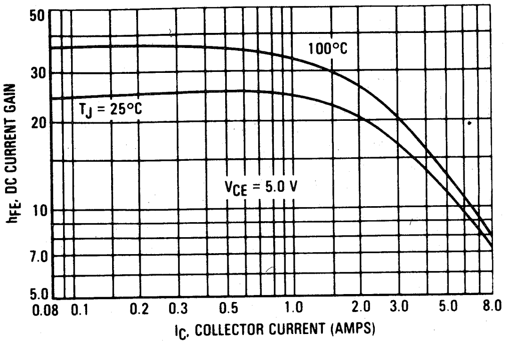


FIGURE 2 — COLLECTOR SATURATION REGION

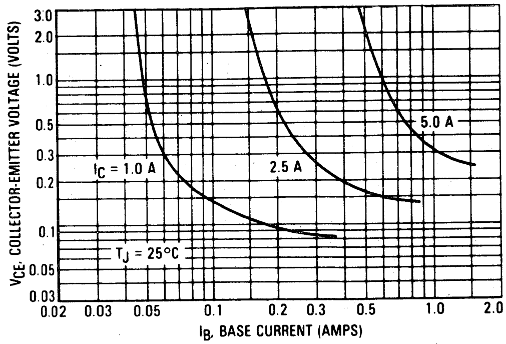


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

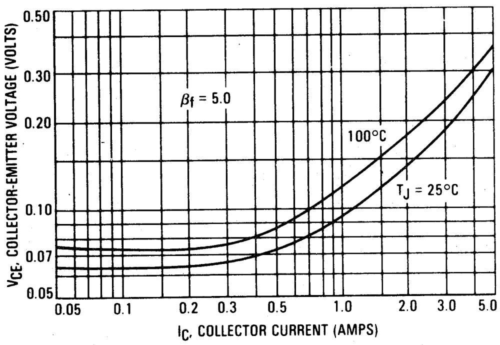


FIGURE 4 — BASE-EMITTER VOLTAGE

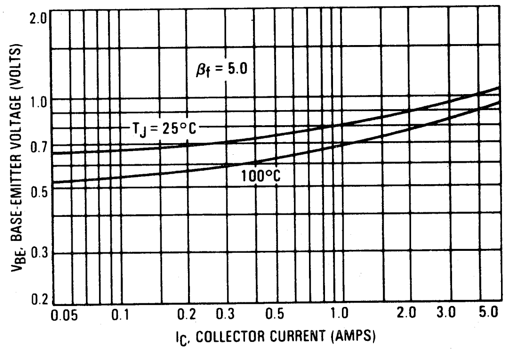


FIGURE 5 — COLLECTOR CUTOFF REGION

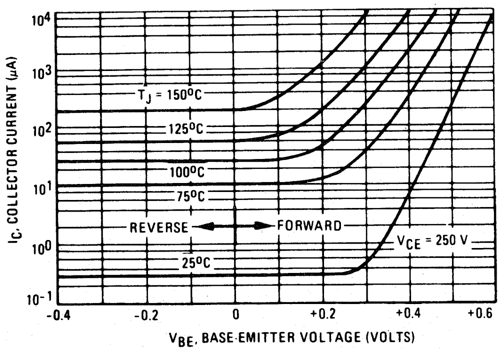


FIGURE 6 — CAPACITANCE

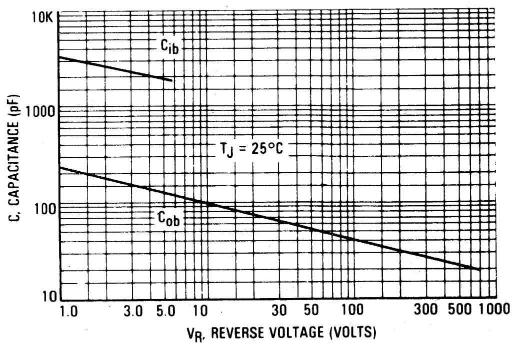


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

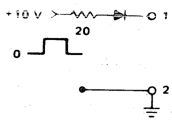
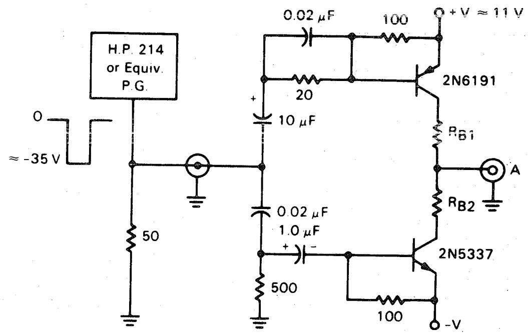
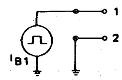
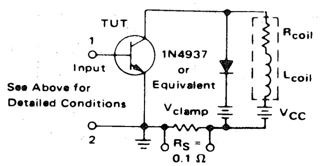
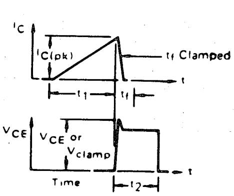
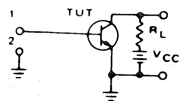
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

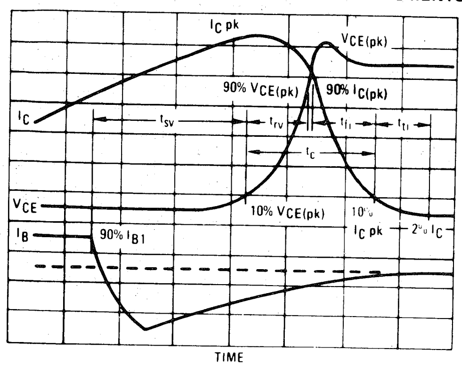
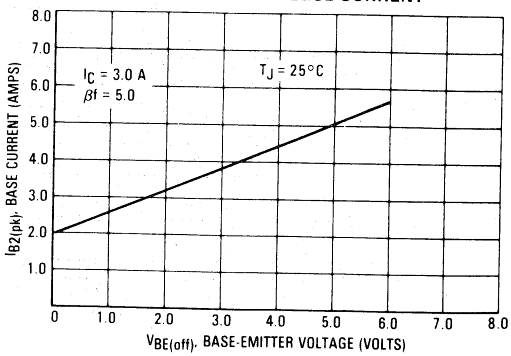


FIGURE 8 — PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

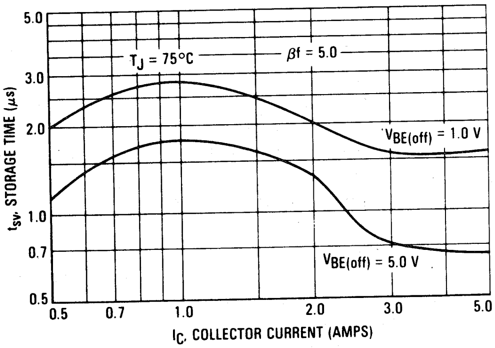
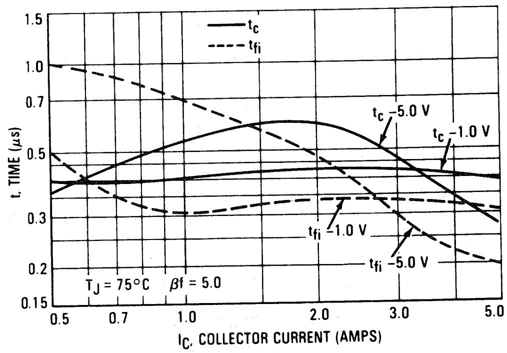
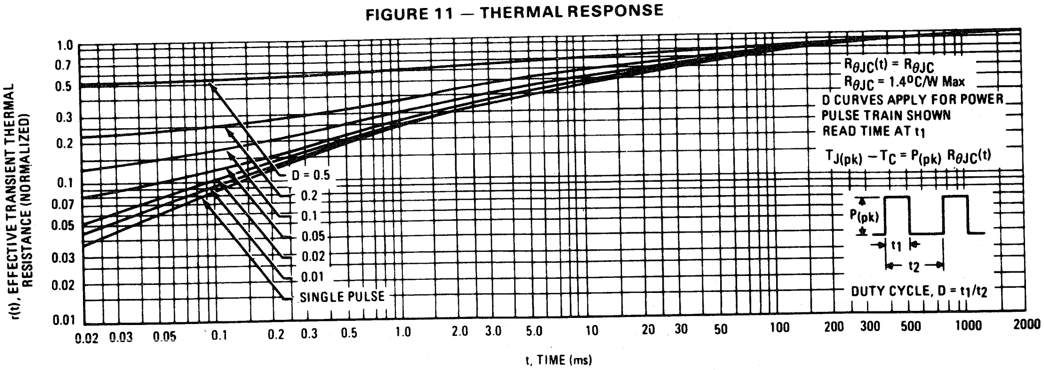


FIGURE 10 — CROSSOVER AND FALL TIMES



3

FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices nder the test conditions shown.

FIGURE 12 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

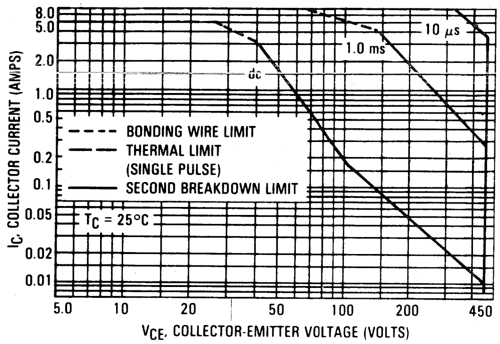


FIGURE 13 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

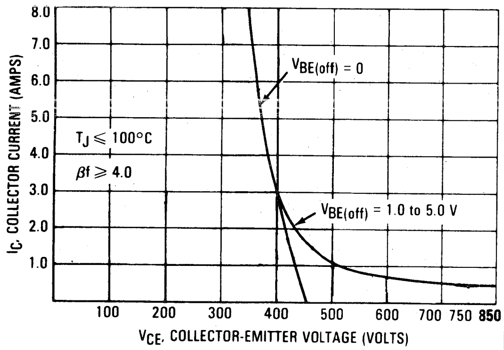
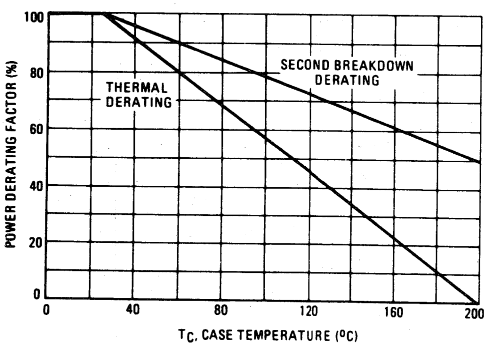


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

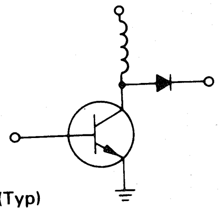
3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUS47
BUS47A

SWITCHMODE II▲ SERIES
NPN SILICON POWER TRANSISTORS

The BUS 47 and BUS 47A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:



- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

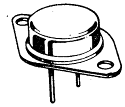
Fast Turn-Off Times
  60 ns Inductive Fall Time — 25°C (Typ)
  120 ns Inductive Crossover Time — 25°C (Typ)

Operating Temperature Range −65 to +200°C
100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents (125°C)

9 AMPERES
NPN SILICON POWER TRANSISTORS
400 AND 450 VOLTS (BVCEO)
150 WATTS
850 – 1000 V (BVCES)

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



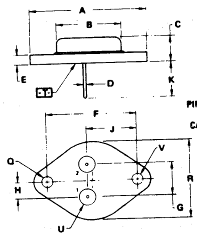
MAXIMUM RATINGS

Rating	Symbol	BUS 47	BUS 47A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current – Continuous – Peak (1) – Overload	I_C I_{CM} I_{OI}	9 18 36		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	5 10		Adc
Total Power Dissipation – T_C = 25°C – T_C = 100°C Derate above 25°C	P_D	150 85.5 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   | ⌖ | ⌀ 0.13 (0.005) Ⓜ | T | V Ⓜ |
   FOR LEADS:
   | ⌖ | ⌀ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3 TYPE

3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 200$ mA, $I_B = 0$) L = 25 mH	BUS47 BUS47A	$V_{CEO(sus)}$	400 450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc) (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc, $T_C = 125°C$)		I_{CEV}	– –	– –	0.15 1.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $R_{BE} = 10\ \Omega$)	$T_C = 25°C$ $T_C = 125°C$	I_{CER}	–	–	0.4 3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 5$ Vdc, $I_C = 0$)		I_{EBO}	–	–	0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50$ mA - $I_C = 0$)		BV_{EBO}	7.0	–	–	Vdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain ($I_C = 6$ Adc, $V_{CE} = 5$ Vdc) ($I_C = 5$ Adc, $V_{CE} = 5$ V)	BUS47 BUS47A	h_{FE}	7	–	–	
Collector-Emitter Saturation Voltage ($I_C = 6$ Adc, $I_B = 1.2$ Adc) ($I_C = 9$ Adc, $I_B = 1.8$ Adc) ($I_C = 6$ Adc, $I_B = 1.2$ Adc, $T_C = 100°C$)	BUS47	$V_{CE(sat)}$	– – –	– – –	1.5 5.0 2.5	Vdc
($I_C = 5$ Adc, $I_B = 1$ Adc) ($I_C = 8$ Adc, $I_B = 1.6$ Adc) ($I_C = 5$ Adc, $I_B = 1$ Adc, $T_C = 100°C$)	BUS47A		– – –	– – –	1.5 5.0 2.5	
Base-Emitter Saturation Voltage ($I_C = 6$ Adc, $I_B = 1.2$ Adc) ($I_C = 6$ Adc, $I_B = 1.2$ Adc, $T_C = 100°C$)	BUS47	$V_{BE(sat)}$	– –	– –	1.6 1.6	Vdc
($I_C = 5$ Adc, $I_B = 1$ Adc) ($I_C = 5$ Adc, $I_B = 1$ Adc, $T_C = 100°C$)	BUS47A		– –	– –	1.6 1.6	
DYNAMIC CHARACTERISTICS						
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f_{test} = 100$ Khz)		C_{ob}	–	–	300	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	($V_{CC} = 250$ Vdc, $I_C = 6$ A, $I_{B1} = 1.2$ A, $t_p = 30\ \mu s$, Duty Cycle 2 , $V_{BE(off)} = 5$ V)	t_d	–	0.05	0.2	μs
Rise Time		t_r	–	0.5	0.8	
Storage Time		t_s	–	1	2.0	
Fall Time		t_f	–	0.2	0.4	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions	Device	Temperature	Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)} = 6$ A, $I_{B1} = 1.2$ A,	BUS47	($T_C = 25°C$)	t_{sv}	–	0.9	–	μs
Fall Time	$V_{BE(off)} = 5$ V,			t_{fi}	–	0.06	–	
Storage Time	$V_{CE(c1)} = 250$ V)	BUS47A	($T_C = 100°C$)	t_{sv}	–	1.0	2.5	
Crossover Time	$I_{C(pk)} = 5$ A			t_c	–	0.2	0.5	
Fall Time	$I_{B1} = 1$ A			t_{fi}	–	0.1	0.3	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

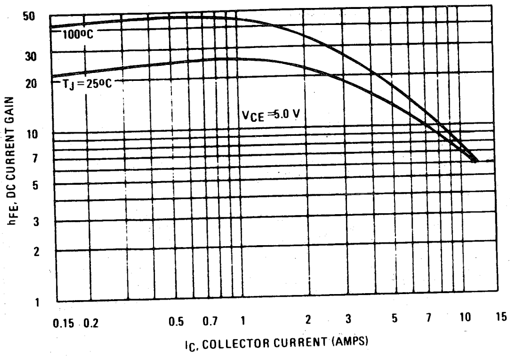


FIGURE 2 – COLLECTOR SATURATION REGION

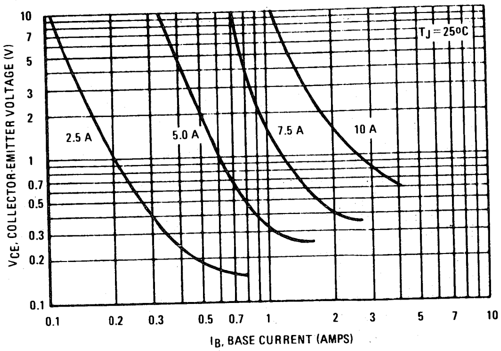


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

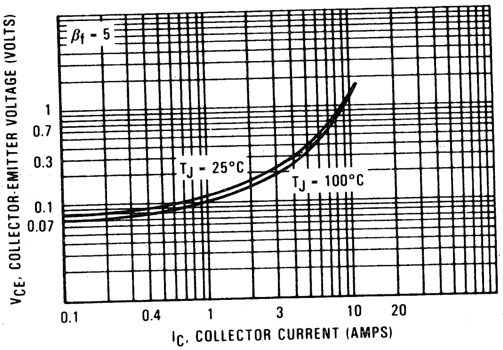


FIGURE 4 – BASE-EMITTER VOLTAGE

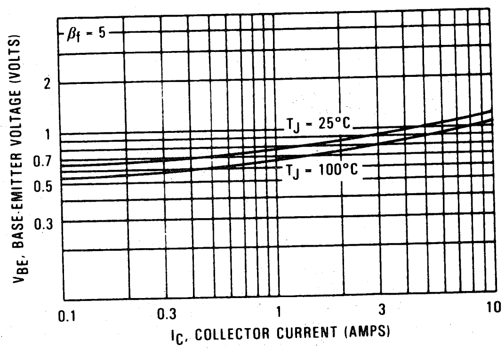


FIGURE 5 – COLLECTOR CUTOFF REGION

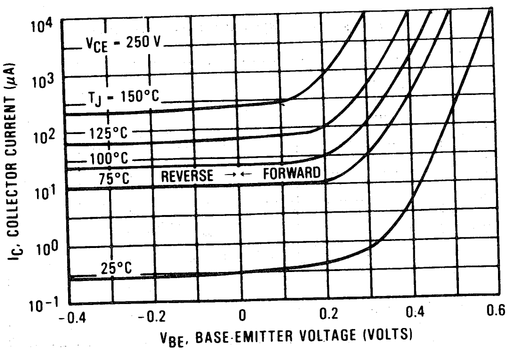


FIGURE 6 – CAPACITANCE

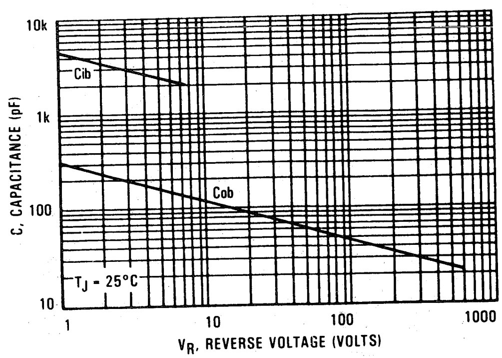


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TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

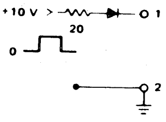
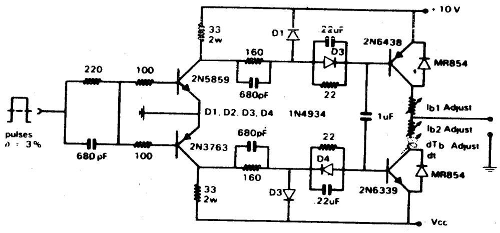
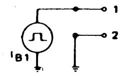
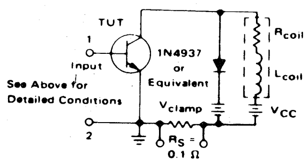
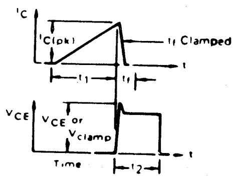
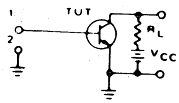
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired. TURN OFF TIME: Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} 180 μH R_{coil} 0.05 Ω V_{CC} 20 V V_{clamp} 250 V R_B adjusted to attain desired I_{B1}	V_{CC} 250 V R_L 83 Ω Pulse Width 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

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FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

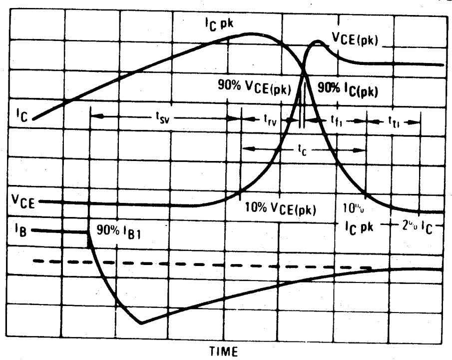
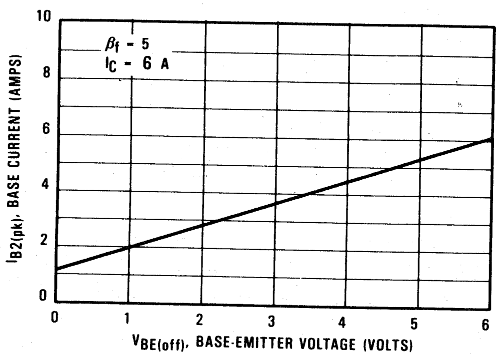


FIGURE 8 – PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10−90% V_{clamp}
t_{fi} = Current Fall Time, 90−10% I_C
t_{ti} = Current Tail, 10−2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME

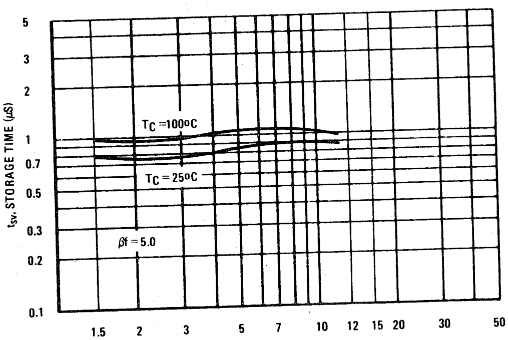


FIGURE 10 – CROSSOVER AND FALL TIMES

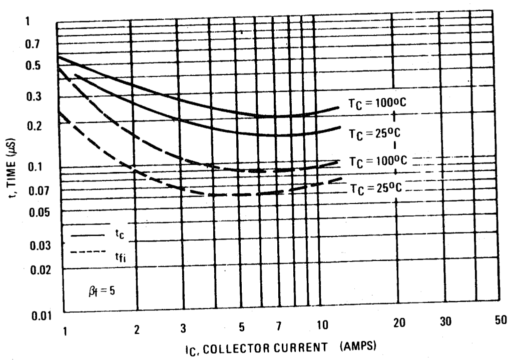


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

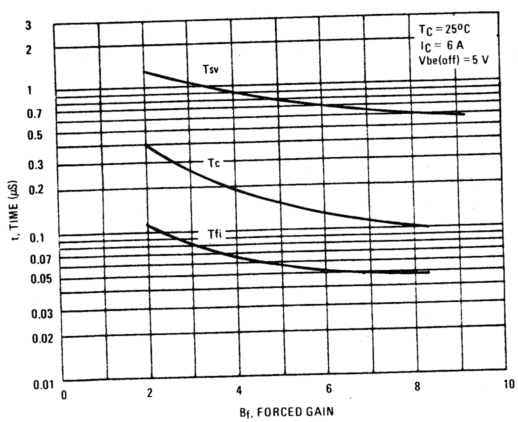
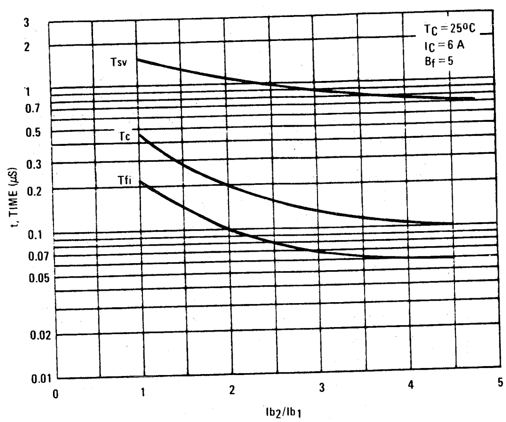


FIGURE 11b – TURN-OFF TIMES vs Ib2/Ib1



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The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

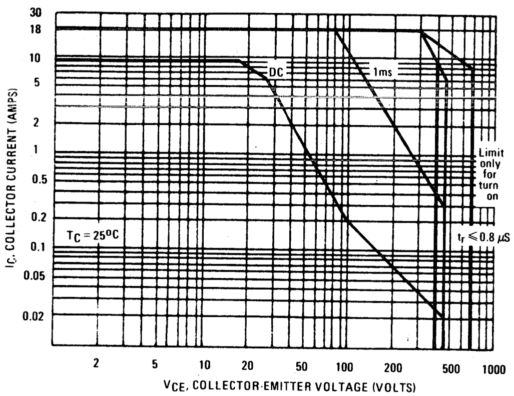


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

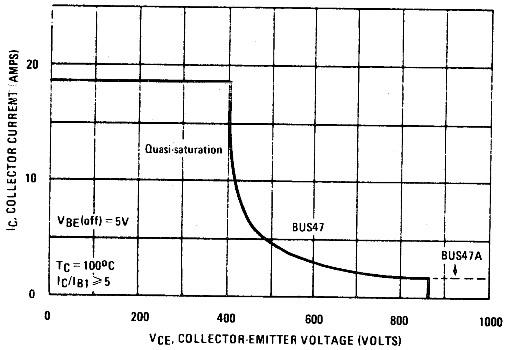
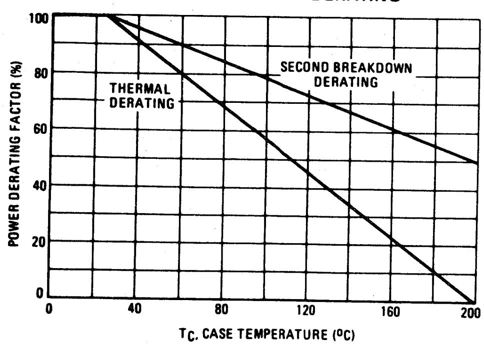


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

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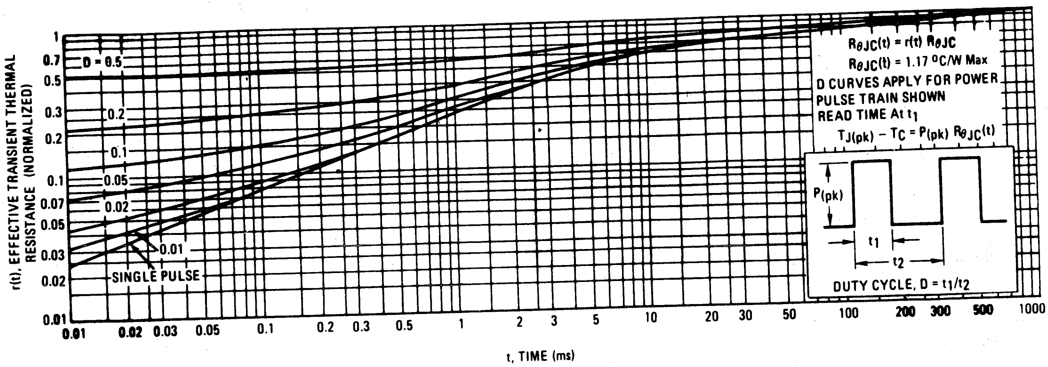
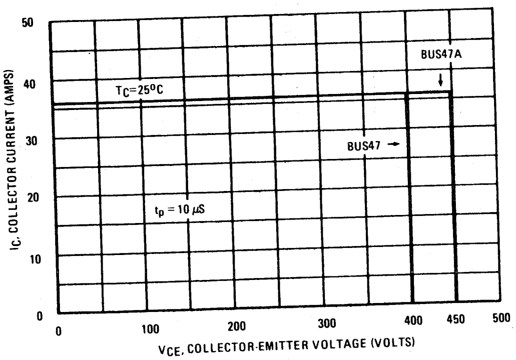
FIGURE 15 —THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 — RATED OVERLOAD SAFE OPERATING AREA (OLSOA)



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

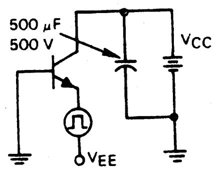
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 17) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 17 -- OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p



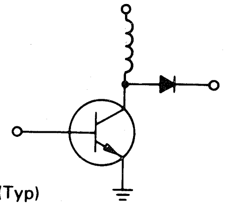
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUS47P
BUS47AP

SWITCHMODE II[▲] SERIES
NPN SILICON POWER TRANSISTORS

The BUS 47P/BUS 47AP transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

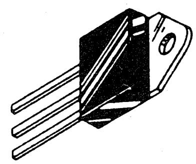
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

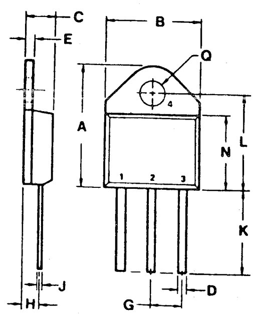


Fast Turn-Off Times
 60 ns Inductive Fall Time—25°C (Typ)
 120 ns Inductive Crossover Time—25°C (Typ)

Operating Temperature Range −65 to +175°C
100°C Performance Specified for:
 Reverse-Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents (125°C)

9 AMPERES
NPN SILICON POWER TRANSISTORS
400 AND 450 VOLTS (BVCEO)
128 WATTS
850 – 1000 V (BVCES)





STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	BUS 47P	BUS 47AP	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous — Peak (1) — Overload	I_C I_{CM}	9 18 36		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	5 10		Adc
Total Power Dissipation — T_C = 25°C — T_C = 100°C Derate above 25°C	P_D	128 64.5 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

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ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 200$ mA, $I_B = 0$) L = 25 mH	BUS47P BUS47AP	$V_{CEO(sus)}$	400 450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc) (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc, $T_C = 125°C$)		I_{CEV}	– –	– –	0.15 1.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $R_{BE} = 10\ \Omega$)	$T_C = 25°C$ $T_C = 125°C$	I_{CER}	–	–	0.4 3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 5$ Vdc, $I_C = 0$)		I_{EBO}	–	–	0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50$ mA - $I_C = 0$)		BV_{EBO}	7.0	–	–	Vdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain ($I_C = 6$ Adc, $V_{CE} = 5$ Vdc) ($I_C = 5$ Adc, $V_{CE} = 5$ V)	BUS47P BUS47AP	h_{FE}	7	–	–	
Collector-Emitter Saturation Voltage ($I_C = 6$ Adc, $I_B = 1.2$ Adc) ($I_C = 9$ Adc, $I_B = 1.8$ Adc) ($I_C = 6$ Adc, $I_B = 1.2$ Adc, $T_C = 100°C$) ($I_C = 5$ Adc, $I_B = 1$ Adc) ($I_C = 8$ Adc, $I_B = 1.6$ Adc) ($I_C = 5$ Adc, $I_B = 1$ Adc, $T_C = 100°C$)	BUS47P BUS47AP	$V_{CE(sat)}$	– – – – – –	– – – – – –	1.5 5.0 2.5 1.5 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 6$ Adc, $I_B = 1.2$ Adc) ($I_C = 6$ Adc, $I_B = 1.2$ Adc, $T_C = 100°C$) ($I_C = 5$ Adc, $I_B = 1$ Adc) ($I_C = 5$ Adc, $I_B = 1$ Adc, $T_C = 100°C$)	BUS47P BUS47AP	$V_{BE(sat)}$	– – – –	– – – –	1.6 1.6 1.6 1.6	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f_{test} = 100$ Khz)		C_{ob}	–	–	300	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	($V_{CC} = 250$ Vdc, $I_C = 6$ A, $I_{B1} = 1.2$ A, $t_p = 30\ \mu s$, Duty Cycle ≦ 2%, $V_{BE(off)} = 5$ V)	t_d	–	0.05	0.2	μs
Rise Time		t_r	–	0.5	0.8	
Storage Time		t_s	–	1	2.0	
Fall Time		t_f	–	0.2	0.4	
Inductive Load, Clamped (Table 1)						
Storage Time	($I_{C(pk)} = 6$ A, $I_{B1} = 1.2$ A, BUS47P, $T_C = 25°C$)	t_{sv}	–	0.9	–	μs
Fall Time		t_{fi}	–	0.06	–	
Storage Time	$V_{BE(off)} = 5$ V, $V_{CE(c1)} = 250$ V, ($T_C = 100°C$)	t_{sv}	–	1.0	2.5	
Crossover Time	$I_{C(pk)} = 5$ A, $I_{B1} = 1$ A, BUS47AP	t_c	–	0.2	0.5	
Fall Time		t_{fi}	–	0.1	0.3	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

3

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

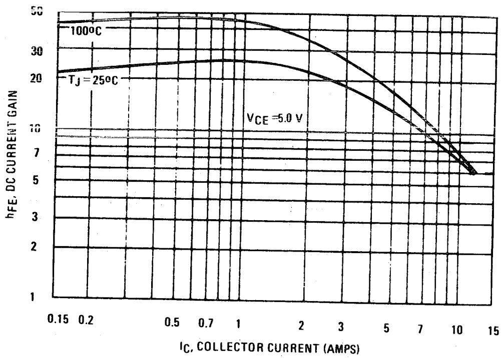


FIGURE 2 — COLLECTOR SATURATION REGION

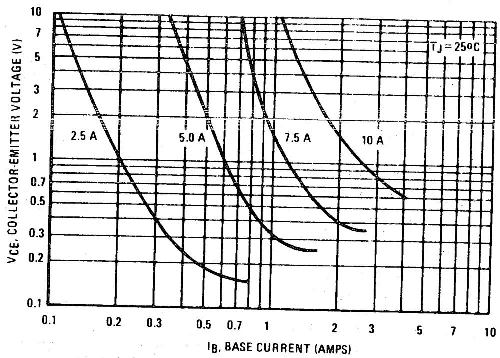


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

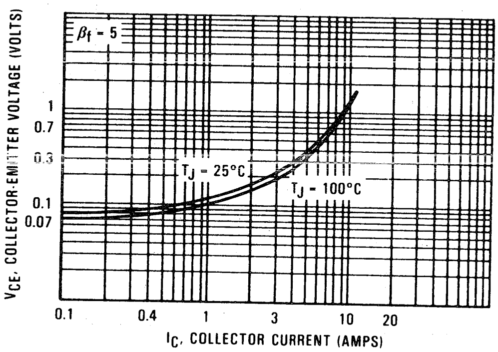


FIGURE 4 — BASE-EMITTER VOLTAGE

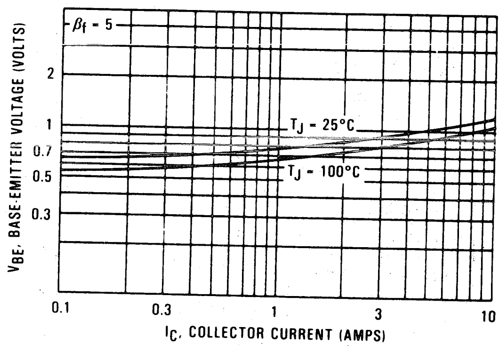


FIGURE 5 — COLLECTOR CUTOFF REGION

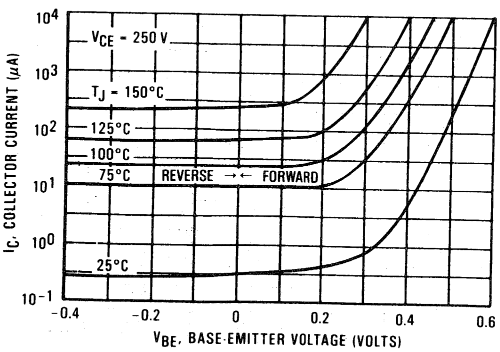


FIGURE 6 — CAPACITANCE

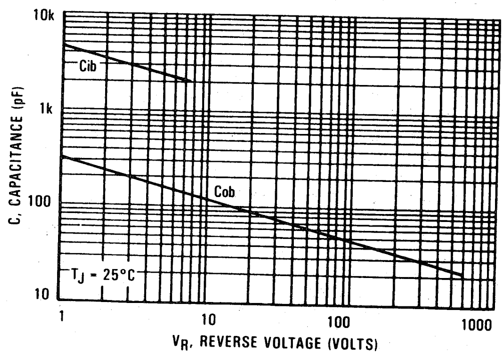


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

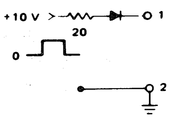
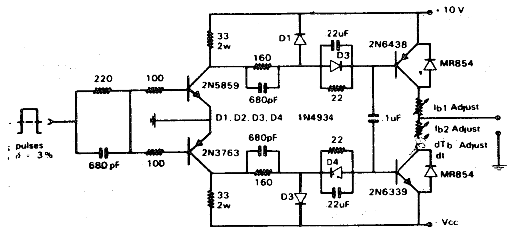
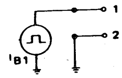
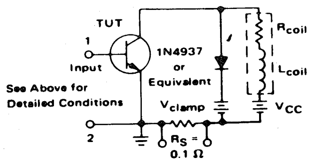
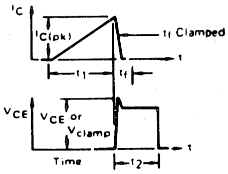
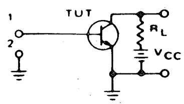
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

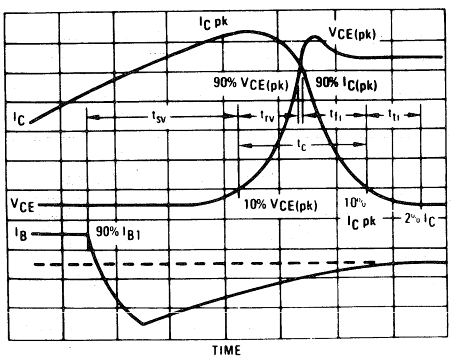
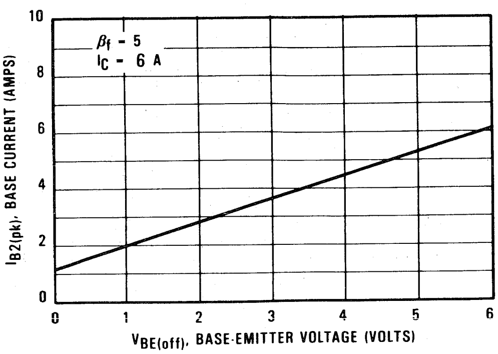


FIGURE 8 – PEAK-REVERSE CURRENT



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SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME

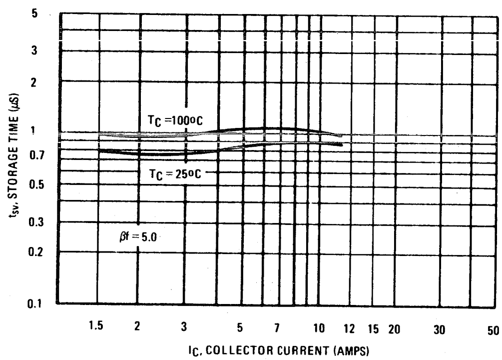


FIGURE 10 – CROSSOVER AND FALL TIMES

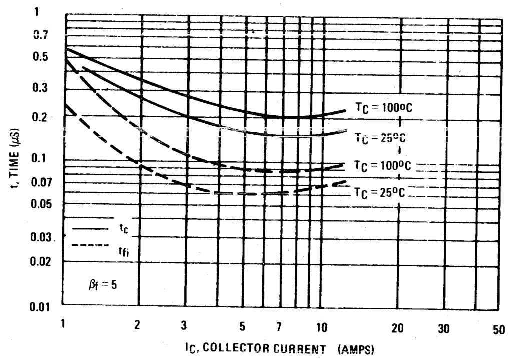


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

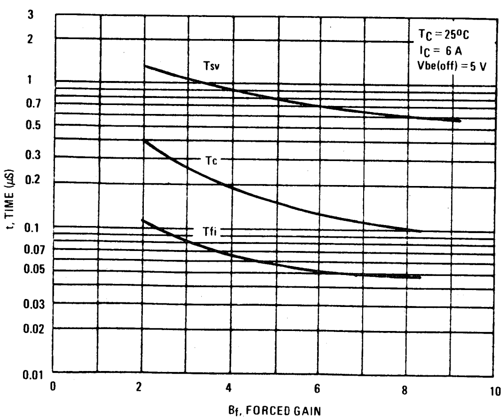
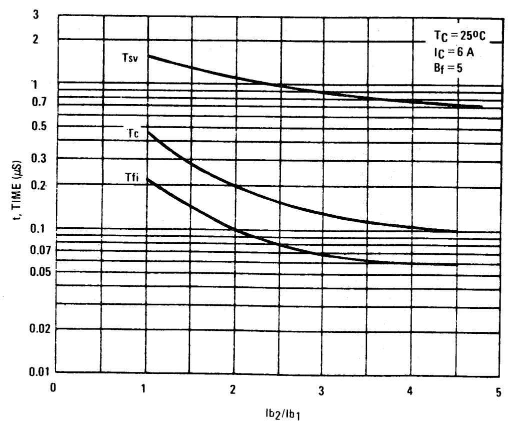


FIGURE 11b – TURN-OFF TIMES vs I_{b2}/I_{b1}



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The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

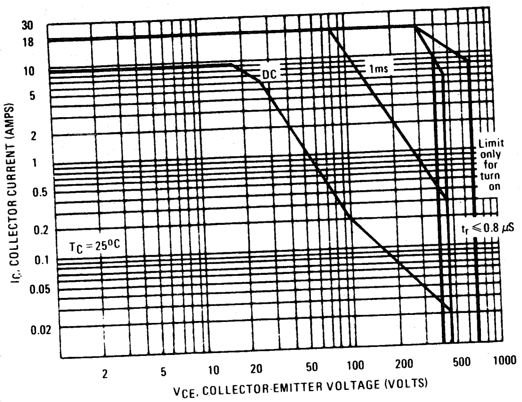


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

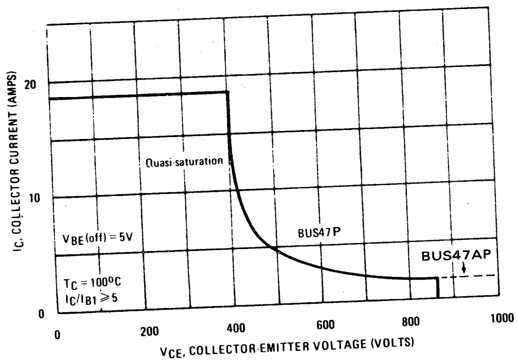
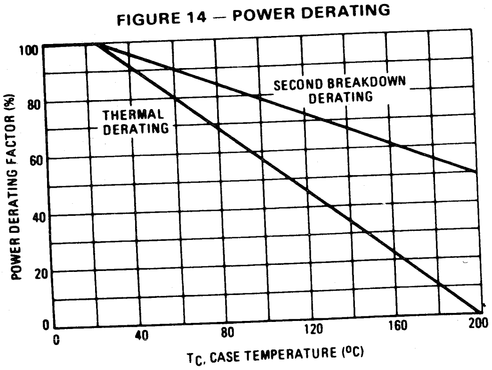


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

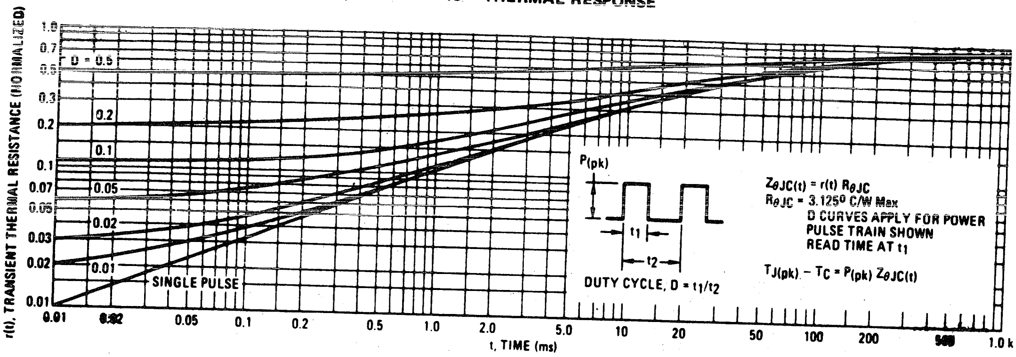
$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

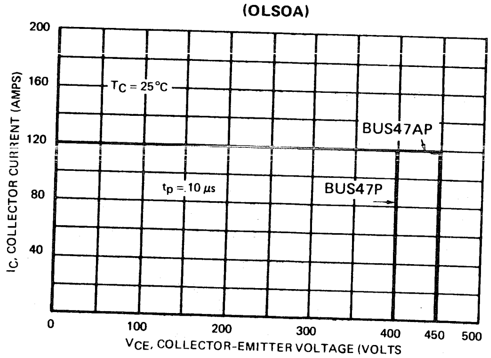
3

FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

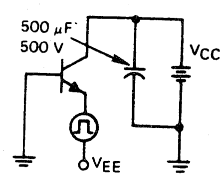
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 17) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 17 – OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

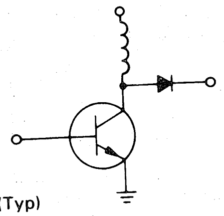


MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUS48
BUS48A

SWITCHMODE II▲ SERIES
NPN SILICON POWER TRANSISTORS

The BUS 48 and BUS 48A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:



- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

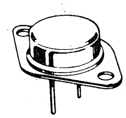
Fast Turn-Off Times
60 ns Inductive Fall Time — 25°C (Typ)
120 ns Inductive Crossover Time — 25°C (Typ)

Operating Temperature Range −65 to +200°C
100°C Performance Specified for:
Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents (125°C)

15 AMPERES
NPN SILICON
POWER TRANSISTORS
400 and 450 VOLTS (BV_{CEO})
850 — 1000 VOLTS (BV_{CES})
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



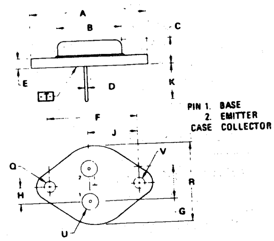
MAXIMUM RATINGS

Rating	Symbol	BUS 48	BUS 48A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous — Peak(1) — Overload	I_C I_{CM} I_{OL}	15 30 60		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	5 20		Adc
Total Power Dissipation — T_C = 25°C — T_C = 100°C Derate above 25°C	P_D	175 100 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦ 10%.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
⌖ Ø 0.13 (0.005) Ⓜ | T | V Ⓜ
FOR LEADS
⌖ Ø 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 200$ mA, $I_B = 0$) L = 25 mH — BUS48 BUS48A	$V_{CEO(sus)}$	400 450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc) (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc, $T_C = 125°C$)	I_{CEV}	– –	– –	0.2 2.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $R_{BE} = 10\ \Omega$) — $T_C = 25°C$ $T_C = 125°C$	I_{CER}	–	–	0.5 3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 5$ Vdc, $I_C = 0$)	I_{EBO}	–	–	0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50$ mA - $I_C = 0$)	BV_{EBO}	7.0	–	–	Vdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 10$ Adc, $V_{CE} = 5$ Vdc) — BUS48 ($I_C = 8$ Adc, $V_{CE} = 5$ V) — BUS48A	h_{FE}	8	–	–	
Collector-Emitter Saturation Voltage ($I_C = 10$ Adc, $I_B = 2$ Adc) ($I_C = 15$ Adc, $I_B = 3$ Adc) — BUS48 ($I_C = 10$ Adc, $I_B = 2$ Adc, $T_C = 100°C$) ($I_C = 8$ Adc, $I_B = 1.6$ Adc) ($I_C = 12$ Adc, $I_B = 2.4$ Adc) — BUS48A ($I_C = 8$ Adc, $I_B = 1.6$ Adc, $T_C = 100°C$)	$V_{CE(sat)}$	– – – – – –	– – – – – –	1.5 5.0 2.0 1.5 5.0 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10$ Adc, $I_B = 2$ Adc) ($I_C = 10$ Adc, $I_B = 2$ Adc, $T_C = 100°C$) — BUS48 ($I_C = 8$ Adc, $I_B = 1.6$ Adc) ($I_C = 8$ Adc, $I_B = 1.6$ Adc, $T_C = 100°C$) — BUS48A	$V_{BE(sat)}$	– – – –	– – – –	1.6 1.6 1.6 1.6	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f_{test} = 100$ Khz)	C_{ob}	–	–	350	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — ($V_{CC} = 250$ Vdc, $I_C = 10$ A, $I_{B1} = 2.0$ A, $t_p = 30\ \mu s$, Duty Cycle ≤ 2%, $V_{BE(off)} = 5$ V)	t_d	–	0.1	0.2	μs
Rise Time	t_r	–	0.4	0.7	
Storage Time	t_s	–	1.3	2.0	
Fall Time	t_f	–	0.2	0.4	
Inductive Load, Clamped (Table 1)					
Storage Time — ($I_{C(pk)} = 10$ A, $I_{B1} = 2.0$ A, $V_{BE(off)} = 5$ V, $V_{CE(c1)} = 250$ V) ($T_C = 25°C$)	t_{sv}	–	1.3	–	μs
Fall Time ($T_C = 25°C$)	t_{fi}	–	0.06	–	
Storage Time ($T_C = 100°C$)	t_{sv}	–	1.5	2.5	
Crossover Time ($T_C = 100°C$)	t_c	–	0.3	0.6	
Fall Time ($T_C = 100°C$)	t_{fi}	–	0.17	0.35	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

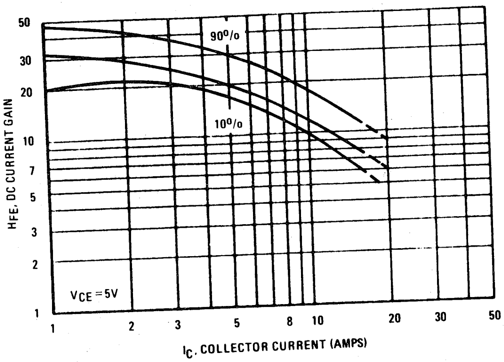


FIGURE 2 – COLLECTOR SATURATION REGION

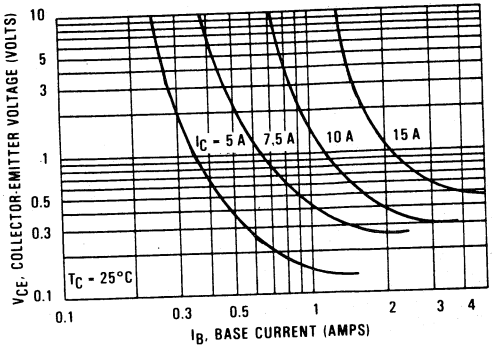


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

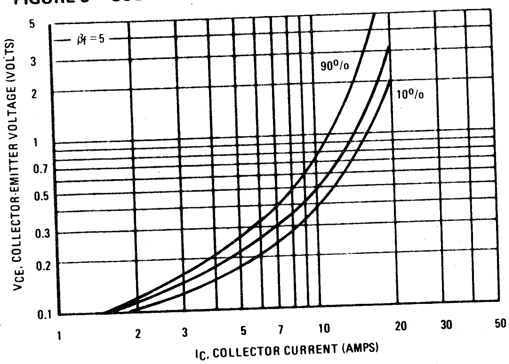


FIGURE 4 – BASE-EMITTER VOLTAGE

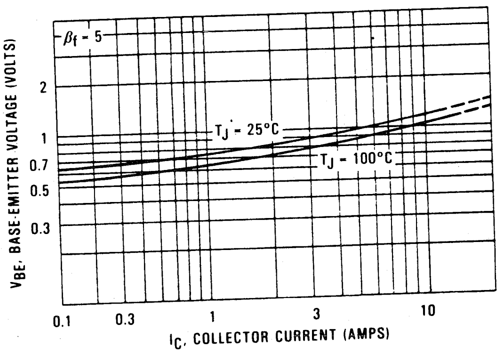


FIGURE 5 – COLLECTOR CUTOFF REGION

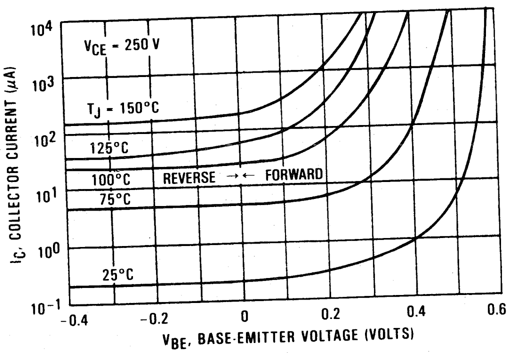


FIGURE 6 – CAPACITANCE

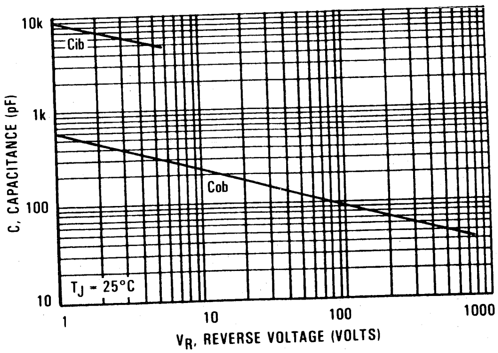


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TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

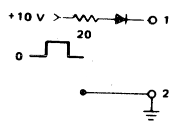
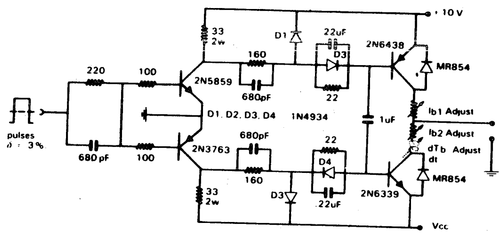
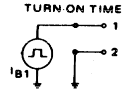
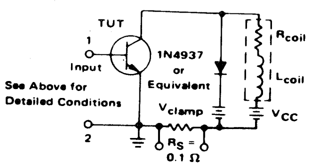
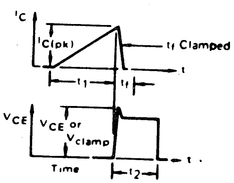
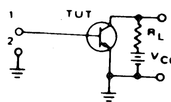
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired. TURN-OFF TIME: Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V, R_{coil} = 0.7 Ω	L_{coil} = 180 μH, R_{coil} = 0.05 Ω, V_{CC} = 20 V; V_{clamp} = 250 V, R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V, R_L = 83 Ω, Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C; $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$; $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$; Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

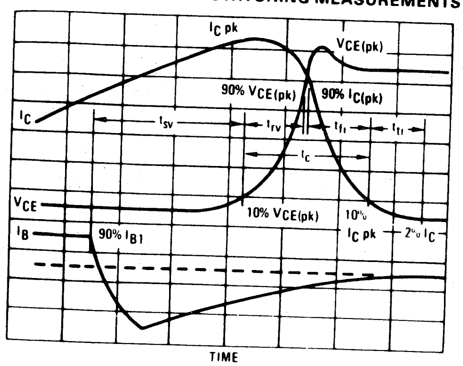
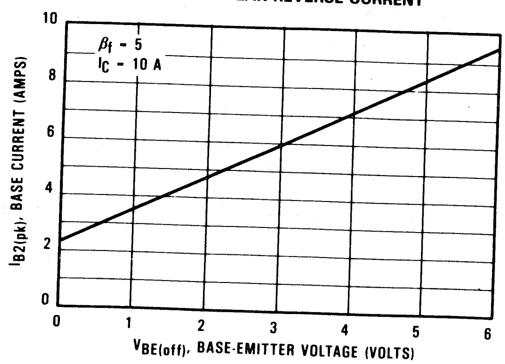


FIGURE 8 — PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10−90% V_{clamp}
t_{fi} = Current Fall Time, 90−10% I_C
t_{ti} = Current Tail, 10−2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME, Tsv

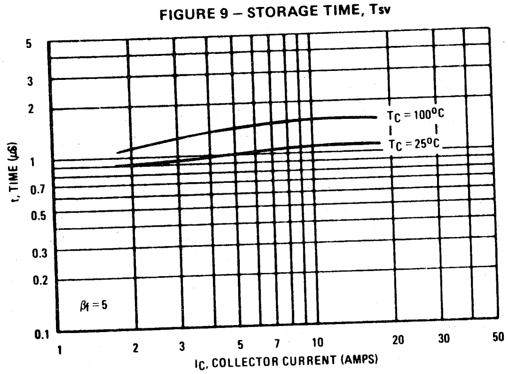


FIGURE 10 – CROSSOVER AND FALL TIMES

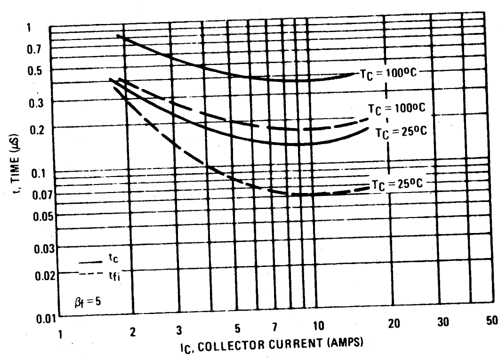


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

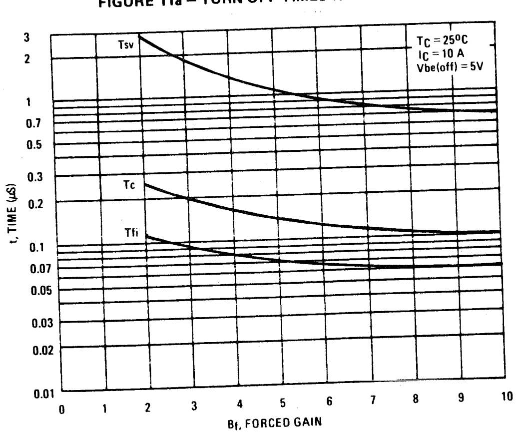
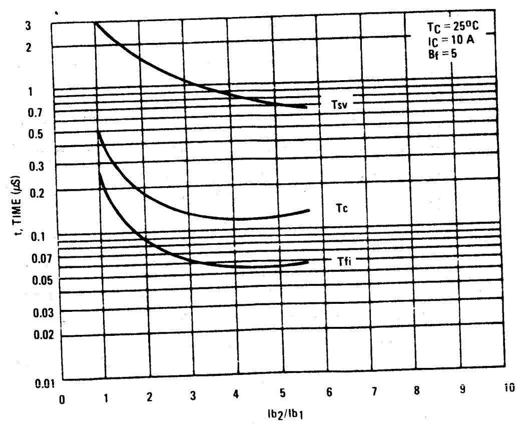


FIGURE 11b – TURN-OFF TIMES vs I_{b2}/I_{b1}



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

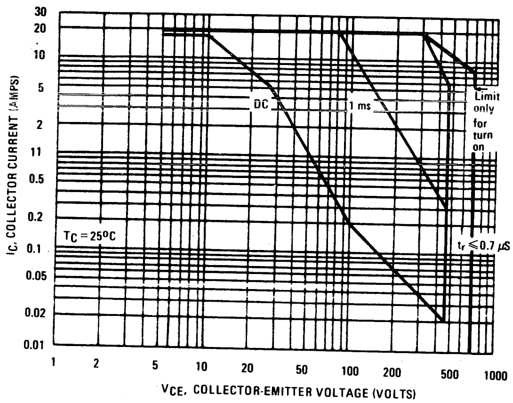


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

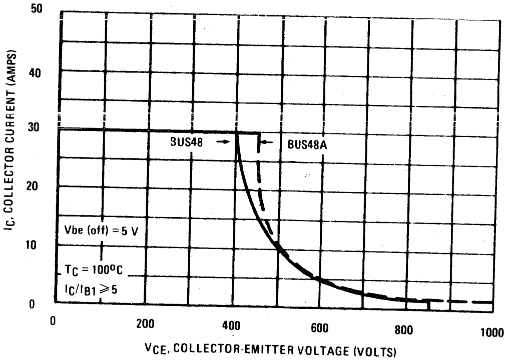
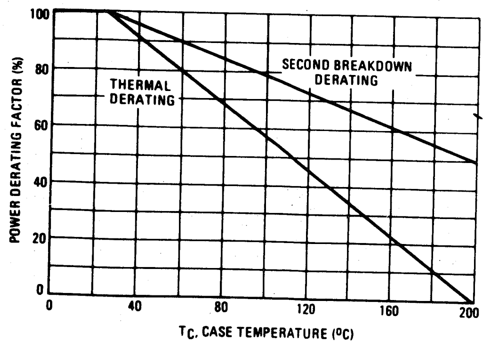


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

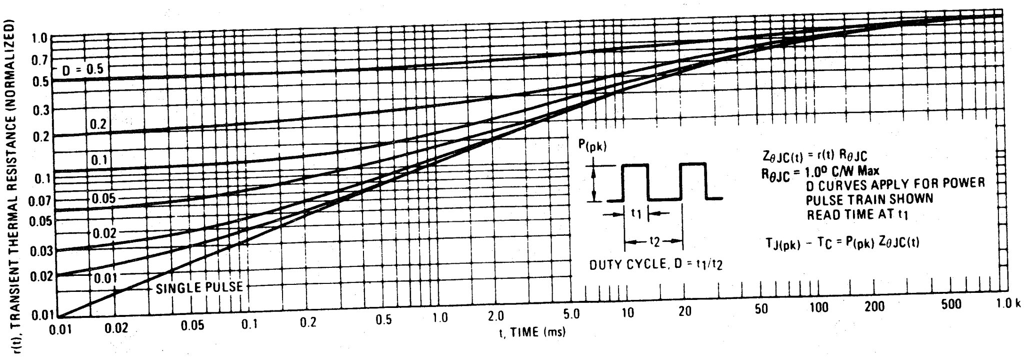
$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

3

FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)

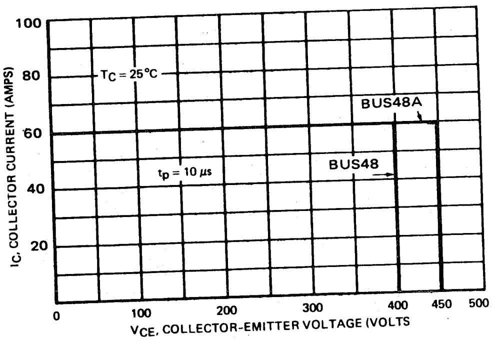
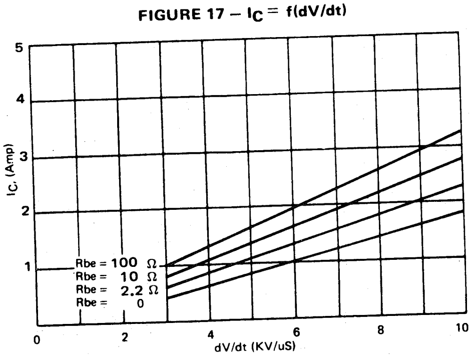


FIGURE 17 – $I_C = f(dV/dt)$



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

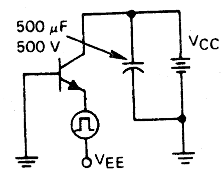
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 18 – OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p



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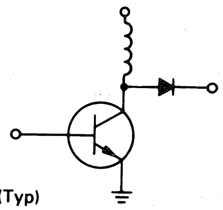
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUS48P
BUS48AP

SWITCHMODE II▲ SERIES
NPN SILICON POWER TRANSISTORS

The BUS 48P/BUS 48AP transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



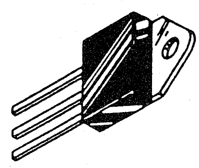
Fast Turn-Off Times
60 ns Inductive Fall Time—25°C (Typ)
120 ns Inductive Crossover Time—25°C (Typ)

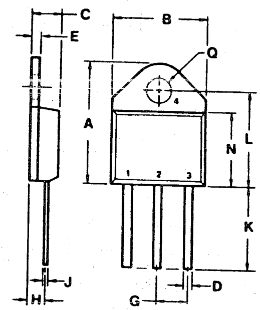
Operating Temperature Range −65 to +175°C
100°C Performance Specified for:
Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents (125°C)

15 AMPERES

NPN SILICON POWER TRANSISTORS

400 and 450 VOLTS (BVCEO)
850 — 1000 VOLTS (BVCES)
150 WATTS





STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	BUS 48P	BUS 48AP	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous — Peak(1) — Overload	I_C I_{CM} I_{OI}	15 30 60		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	5 20		Adc
Total Power Dissipation — $T_C = 25°C$ — $T_C = 100°C$ Derate above 25°C	P_D	150 75 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 200$ mA, $I_B = 0$) L = 25 mH — BUS48P BUS48AP	$V_{CEO(sus)}$	400 450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc) (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc, $T_C = 125°C$)	I_{CEV}	— —	— —	0.2 2.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $R_{BE} = 10\ \Omega$) — $T_C = 25°C$ $T_C = 125°C$	I_{CER}	—	—	0.5 3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 5$ Vdc, $I_C = 0$)	I_{EBO}	—	—	0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50$ mA - $I_C = 0$)	B_{VEBO}	7.0	—	—	Vdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 10$ Adc, $V_{CE} = 5$ Vdc) — BUS48 ($I_C = 8$ Adc, $V_{CE} = 5$ V) — BUS48A	h_{FE}	8	—	—	
Collector-Emitter Saturation Voltage BUS48P: ($I_C = 10$ Adc, $I_B = 2$ Adc) ($I_C = 15$ Adc, $I_B = 3$ Adc) ($I_C = 10$ Adc, $I_B = 2$ Adc, $T_C = 100°C$) BUS48AP: ($I_C = 8$ Adc, $I_B = 1.6$ Adc) ($I_C = 12$ Adc, $I_B = 2.4$ Adc) ($I_C = 8$ Adc, $I_B = 1.6$ Adc, $T_C = 100°C$)	$V_{CE(sat)}$	 — — — — — —	 — — — — — —	 1.5 5.0 2.0 1.5 5.0 2.0	Vdc
Base-Emitter Saturation Voltage BUS48P: ($I_C = 10$ Adc, $I_B = 2$ Adc) ($I_C = 10$ Adc, $I_B = 2$ Adc, $T_C = 100°C$) BUS48AP: ($I_C = 8$ Adc, $I_B = 1.6$ Adc) ($I_C = 8$ Adc, $I_B = 1.6$ Adc, $T_C = 100°C$)	$V_{BE(sat)}$	 — — — —	 — — — —	 1.6 1.6 1.6 1.6	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f_{test} = 100$ Khz)	C_{ob}	—	—	350	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1) ($V_{CC} = 250$ Vdc, $I_C = 10$ A, $I_{B1} = 2.0$ A, $t_p = 30\ \mu s$, Duty Cycle 2 , $V_{BE(off)} = 5$ V)					
Delay Time	t_d	—	0.1	0.2	μs
Rise Time	t_r	—	0.4	0.7	
Storage Time	t_s	—	1.3	2.0	
Fall Time	t_f	—	0.2	0.4	
Inductive Load, Clamped (Table 1) ($I_{C(pk)} = 10$ A, $I_{B1} = 2.0$ A, $V_{BE(off)} = 5$ V, $V_{CE(c1)} = 250$ V)					
Storage Time ($T_C = 25°C$)	t_{sv}	—	1.3	—	μs
Fall Time ($T_C = 25°C$)	t_{fi}	—	0.06	—	
Storage Time ($T_C = 100°C$)	t_{sv}	—	1.5	2.5	
Crossover Time ($T_C = 100°C$)	t_c	—	0.3	0.6	
Fall Time ($T_C = 100°C$)	t_{fi}	—	0.17	0.35	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

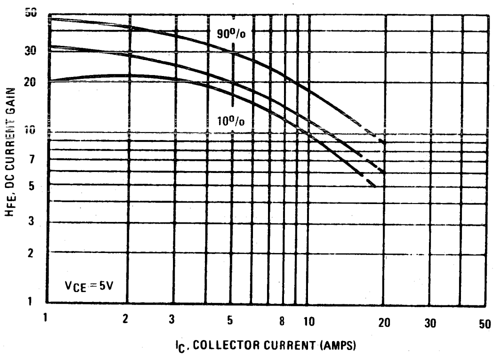


FIGURE 2 — COLLECTOR SATURATION REGION

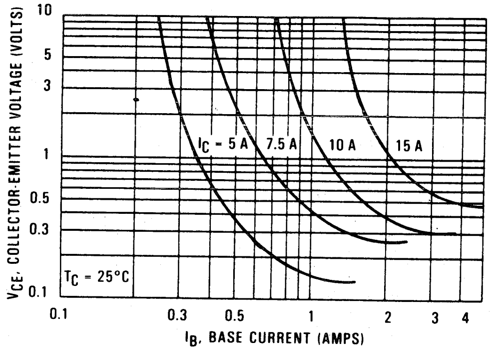


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

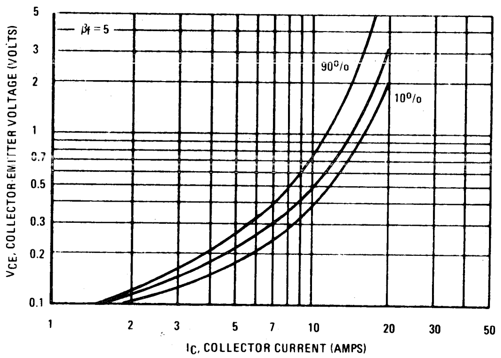


FIGURE 4 — BASE-EMITTER VOLTAGE

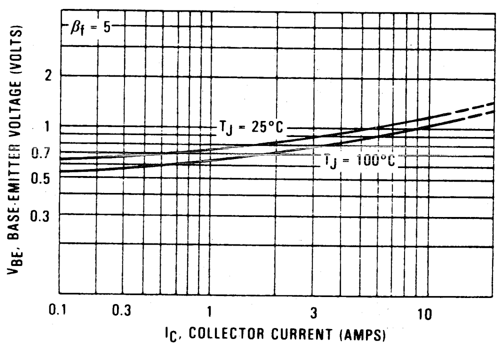


FIGURE 5 — COLLECTOR CUTOFF REGION

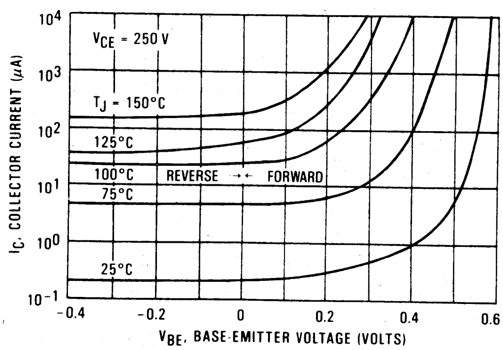


FIGURE 6 — CAPACITANCE

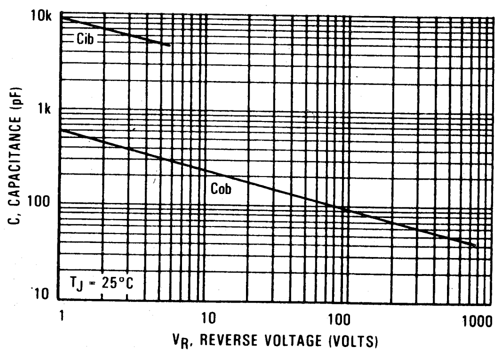


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

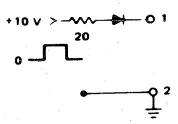
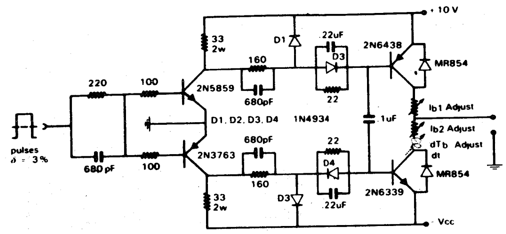
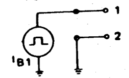
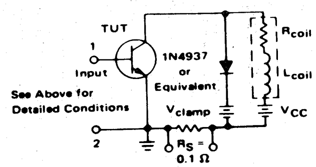
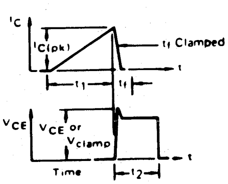
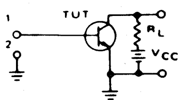
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

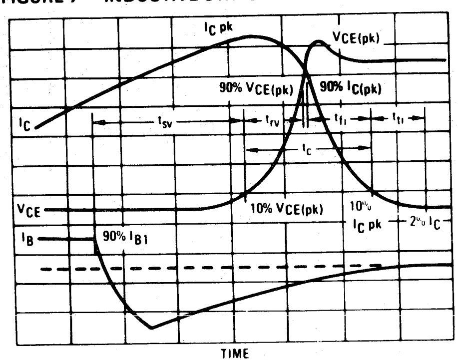
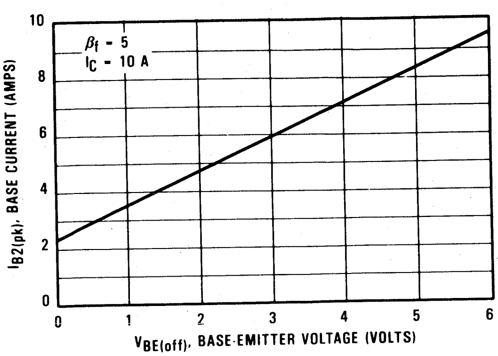


FIGURE 8 – PEAK-REVERSE CURRENT



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SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME, Tsv

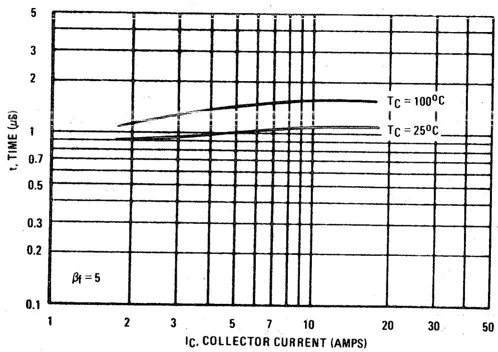

FIGURE 10 – CROSSOVER AND FALL TIMES

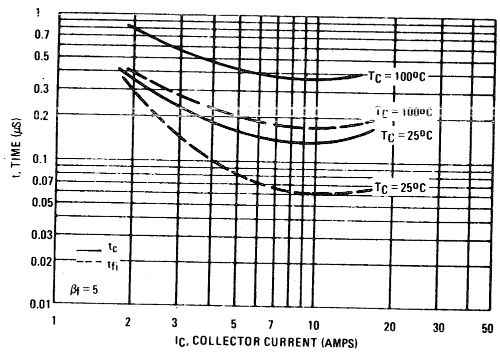

FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

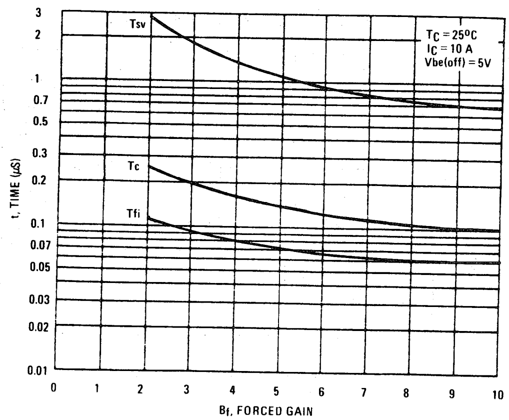

FIGURE 11b – TURN-OFF TIMES vs I_{b2}/I_{b1}

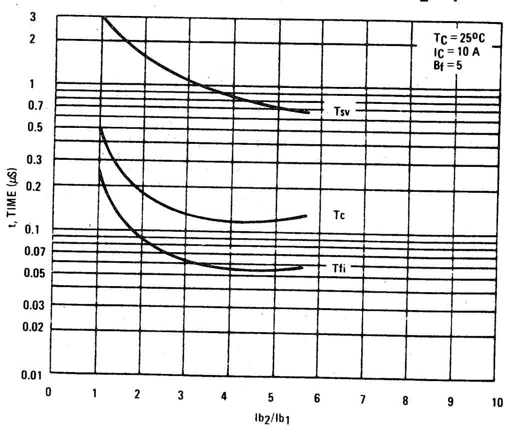

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FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

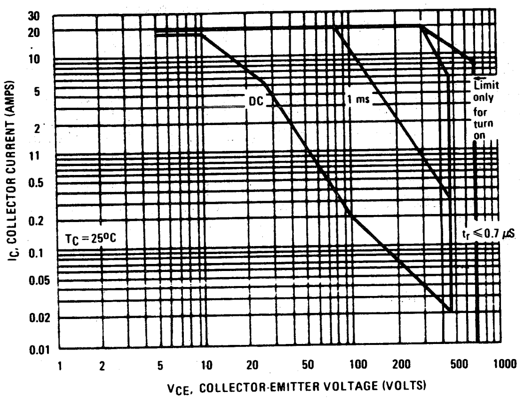


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

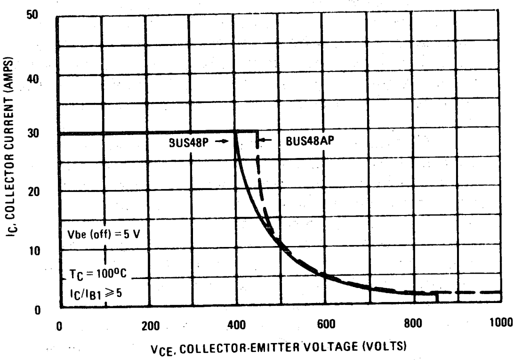
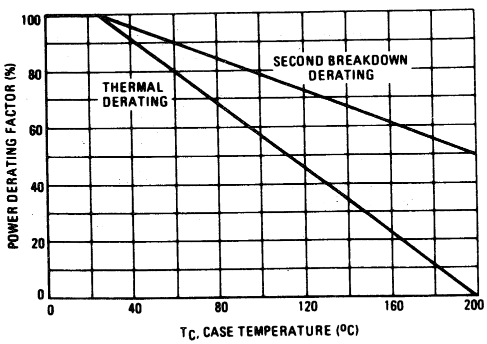


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

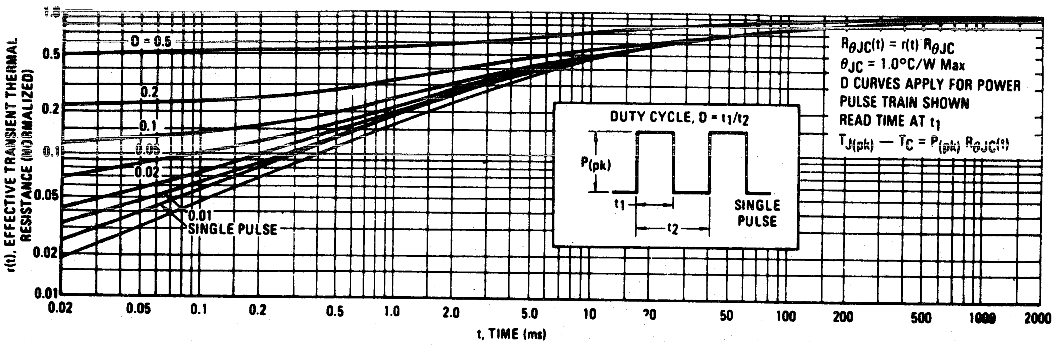
$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

3

FIGURE 15 — THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 — RATED OVERLOAD SAFE OPERATING AREA (OLSOA)

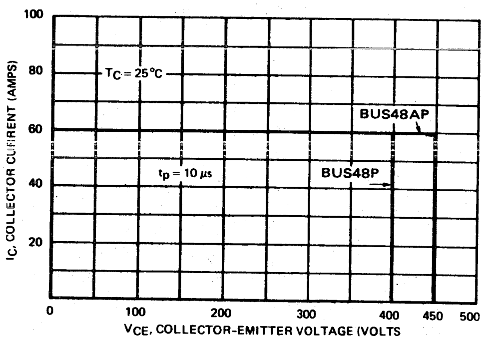
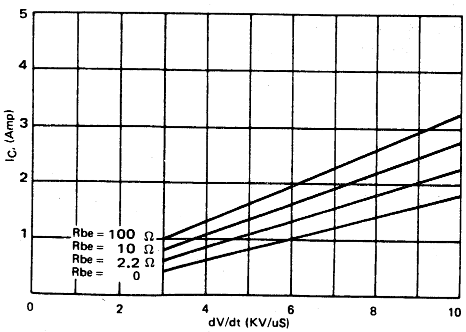


FIGURE 17 — $I_C = f(dV/dt)$



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

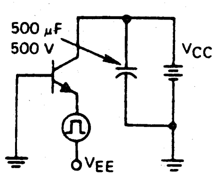
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 18 — OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

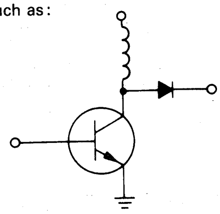
BUS50

70 AMPERES
NPN SILICON
POWER TRANSISTORS
125 VOLTS (BVCEO)
350 WATTS
200 V (BVCES)

ADVANCED INFORMATION
SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The BUS50 transistor is designed for low voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for battery switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

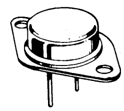


Fast Turn-Off Times
300 ns Inductive Fall Time –25°C (Typ)

Operating Temperature Range –65 to +200°C
100°C Performance Specified for:
Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents (125°C)

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



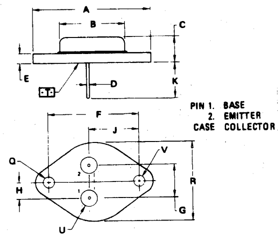
MAXIMUM RATINGS

Rating	Symbol	BUS50	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	125	Vdc
Collector-Emitter Voltage	V_{CEV}	200	Vdc
Emitter Base Voltage	V_{EB}	7	Vdc
Collector Current – Continuous – Peak (1) – Overload	I_C I_{CM} I_{ol}	70 140	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	20	Adc
Total Power Dissipation – T_C = 25°C – T_C = 100°C Derate above 25°C	P_D	350 200 2	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.5	°C/W
Maximum Lead Temperature for Soldering Purposes: ⅛″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦ 10%.



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 1-05 TO-3 TYPE

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit.
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Bias: (V_{CE} = 200 V, V_{BE} = −1.5 V) (V_{CE} = 200 V, V_{BE} = −1.5 V, T_C = 125°C)	I_{CEX}		.2 2	mAdc
Collector-Emitter Cutoff Current (V_{CE} = 125 V)	I_{CEO}		1	mAdc
Emitter Cutoff Current (V_{EB} = 7 V)	I_{EBO}		.2	mAdc

ON CHARACTERISTICS[1]

Characteristic	Symbol	Min.	Max.	Unit.
DC Current Gain (I_C = 5 A, V_{CE} = 4 V) (I_C = 50 A, V_{CE} = 4 V)	h_{FE}	20 15		
Collector-Emitter Saturation Voltage (I_C = 35 A, I_B = 2 A) (I_C = 70 A, I_B = 7 A)	$V_{CE(sat)}$		1 1.2	V_{dc}
Base-Emitter Saturation Voltage (I_C = 35 A, I_B = 2 A) (I_C = 70 A, I_B = 7 A)	$V_{BE(sat)}$		1.8 2	V_{dc}

SWITCHING CHARACTERISTICS (Resistive Load) t_{on} and (Inductive Load) t_{sv}, t_{fi}

Characteristic	Conditions	Symbol	Min.	Max.	Unit
Turn-on Time	I_C = 70 A, I_{B1} = 7 A VBEoff = −5 V (V_{CC} = 125 V)	t_{on}		1.2	μs
Storage Time		t_{sv}		1.5	
Fall Time		t_{fi}		.3	

3

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

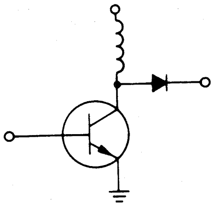
BUS51
BUS52

ADVANCED INFORMATION

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The BUS51 and BUS52 transistors are designed for low voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for battery switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls



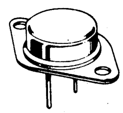
Fast Turn-Off Times
300 ns Inductive Fall Time −25°C (Typ)

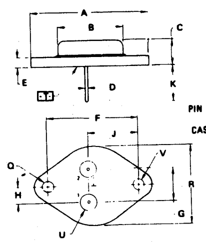
Operating Temperature Range −65 to +200°C
100°C Performance Specified for:
Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents (125°C)

50 & 40 AMPERES
NPN SILICON POWER TRANSISTORS
200 and 250 VOLTS (BVCEO)
350 WATTS
300-350 (BVCES)

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.





PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
| ⌖ | ⌀ 0.13 (0.005) Ⓜ | T | V Ⓜ |

FOR LEADS:
| ⌖ | ⌀ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 1-05 TO-3

MAXIMUM RATINGS

Rating	Symbol	BUS51	BUS52	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	200	250	Vdc
Collector-Emitter Voltage	V_{CEV}	300	350	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current – Continuous – Peak (1) – Overload	I_C I_{CM} I_{ol}	50 100	40 80	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	10	16	Adc
Total Power Dissipation – T_C = 25°C – T_C = 100°C Derate above 25°C	P_D	350 200 2		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.5	°C/W
Maximum Lead Temperature for Soldering Purposes: ⅛" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS[1]						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 200 mA, I_B = 0, L = 25 mH)	BUS51 BUS52	$V_{CEO(sus)}$	200 250			Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEV}			0.2 2.0	mAdc
Collector Cutoff Current (V_{CEO} = Rated Value)		I_{CEO}			1	mA
Emitter Cutoff Current (V_{EB} = 7 Vdc, I_C = 0)		I_{EBO}			2	mAdc

ON CHARACTERISTICS[1]

Characteristic		Symbol	Min	Typ	Max	Unit
DC Current Gain (I_C = 5 Adc, V_{CE} = 4 Vdc) (I_C = 50 Adc, V_{CE} = 4 V)	BUS51	h_{FE}	20 15			
DC Current Gain (I_C = 5 Adc, V_{CE} = 4 Vdc) (I_C = 40 Adc, V_{CE} = 4 V)	BUS52	h_{FE}	20 15			
Collector-Emitter Saturation Voltage (I_C = 30 Adc, I_B = 2 Adc) (I_C = 50 Adc, I_B = 5 Adc)	BUS51	$V_{CE(sat)}$			1 1.5	V_{dc}
(I_C = 25 Adc, I_B = 2 Adc) (I_C = 40 Adc, I_B = 4 Adc)	BUS52				1 1.5	
Base-Emitter Saturation Voltage (I_C = 30 Adc, I_B = 2 Adc) (I_C = 50 Adc, I_B = 5 Adc)	BUS51	$V_{BE(sat)}$			1.8 2	V_{dc}
(I_C = 25 Adc, I_B = 2 Adc) (I_C = 40 Adc, I_B = 4 Adc)	BUS52				1.8 2	

SWITCHING CHARACTERISTICS
Resistive Load (Table 1)

Characteristic	Conditions	Device	Temp	Symbol	Min	Typ	Max	Unit
Turn-on Time	$I_{C(pk)}$ = 50 A, I_{b1} = 5 A, $V_{BE(off)}$ = 5 V, $V_{CE(c1)}$ = 150 V	BUS51	(T_C = 25°C)	t_{on}			1	µs
	$I_{C(pk)}$ = 40 A, I_{B1} = 4 A	BUS52	(T_C = 100°C)					

Inductive Load, Clamped (Table 1)

Characteristic	Conditions	Device	Temp	Symbol	Min	Typ	Max	Unit
Storage Time	$I_{C(pk)}$ = 50 A, I_{b1} = 5 A, $V_{BE(off)}$ = 5 V, $V_{CE(c1)}$ = 150 V	BUS51	(T_C = 25°C)	t_{sv}			2	µs
Fall Time				t_{fi}			.3	
Storage Time	$I_{C(pk)}$ = 40 A, I_{B1} = 4 A	BUS52	(T_C = 100°C)	t_{sv}				
Crossover Time				t_c				
Fall Time				t_{fi}				

[1] Pulse Test: PW = 300 µs, Duty Cycle ≤ 2%.

3

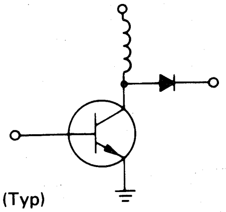
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUS97
BUS97A

SWITCHMODE II▲ SERIES
NPN SILICON POWER TRANSISTORS

The BUS97 and BUS97A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



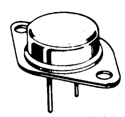
Fast Turn-Off Times
60 ns Inductive Fall Time—25°C (Typ)
120 ns Inductive Crossover Time—25°C (Typ)

Operating Temperature Range −65 to +200°C
100°C Performance Specified for:
Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents (125°C)

18 AMPERES
NPN SILICON
POWER TRANSISTORS
450 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



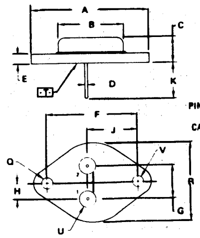
MAXIMUM RATINGS

Rating	Symbol	BUS97	BUS97A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous — Peak(1) — Overload	I_C I_{CM} I_{OL}	18 30 60		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	5 20		Adc
Total Power Dissipation — T_C = 25°C — T_C = 100°C Derate above 25°C	P_D	175 100 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES
1 DIMENSIONS Q AND V ARE DATUMS
2 [T] IS SEATING PLANE AND DATUM
3 POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
| ⌖ | ⌀ 0.13 (0.005) Ⓜ | T | V Ⓜ |
FOR LEADS
| ⌖ | ⌀ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 200 mA, I_B = 0) L = 25 mH	BUS97 BUS97A	$V_{CEO(sus)}$	400 450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEV}	– –	– –	0.2 2.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 10 Ω)	T_C = 25°C T_C = 125°C	I_{CER}	–	–	0.5 3.0	mAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)		I_{EBO}	–	–	0.1	mAdc
Emitter-base breakdown Voltage (I_E = 50 mA - I_C = 0)			7			Vdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 12Adc, V_{CE} = 5Vdc) (I_C = 10A, V_{CE} = 5V)	BUS97 BUS97A	h_{FE}	7	–	–	
Collector-Emitter Saturation Voltage (I_C = 12A, I_B = 2.4A) (I_C = 18A, I_B = 6A) (I_C = 12A, I_B = 2.4A, T_C = 100°C)	BUS97	$V_{CE(sat)}$	– – –	– – –	1.5 3 2.5	Vdc
(I_C = 10A, I_B = 2A) (I_C = 15A, I_B = 3A) (I_C = 10A, I_B = 2A, T_C = 100°C)	BUS97A		– – –	– – –	1.5 5.0 2.5	
Base-Emitter Saturation Voltage (I_C = 12Adc, I_B = 2.4Adc) (I_C = 12Adc, I_B = 2.4Adc, T_C = 100°C)	BUS97	$V_{BE(sat)}$	– –	– –	1.6 1.6	Vdc
(I_C = 10A, I_B = 2Adc) (I_C = 10A, I_B = 2Adc, T_C = 100°C)	BUS97A				1.6 1.6	
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 Khz)		C_{ob}	–	–	350	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	(V_{CC} = 250 Vdc, I_C = 12A, I_{B1} = 2.4A, t_p = 30 ès, Duty Cycle ≦ 2%, $V_{BE(off)}$ = 5 V)	t_d	–	0.1	0.2	μs
Rise Time		t_r	–	0.4	0.7	
Storage Time		t_s	–	1.3	2.0	
Fall Time		t_f	–	0.2	0.4	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)}$ = 12A, I_{B1} = 2.4A) BUS97	(T_C = 25°C)	t_{sv}	–	1.3	–	μs
Fall Time	$V_{BE(off)}$ = 5 V, $V_{CE(C1)}$ = 250 V)		t_{fi}	–	0.06	–	
Storage Time	$I_{C(PK)}$ = 10A, I_{B1} = 2A BUS97A	(T_C = 100°C)	t_{sv}	–	1.5	2.5	
Crossover Time			t_c	–	0.3	0.6	
Fall Time			t_{fi}	–	0.17	0.35	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

3

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

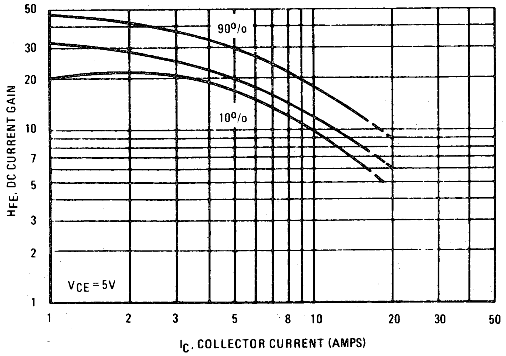


FIGURE 2 — COLLECTOR SATURATION REGION

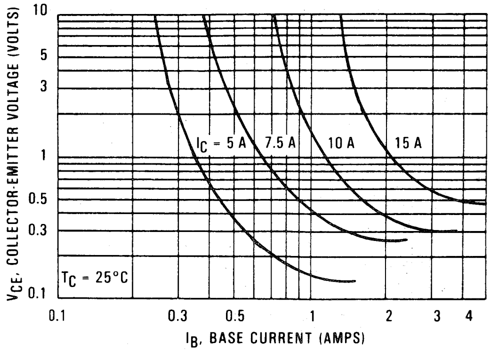


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

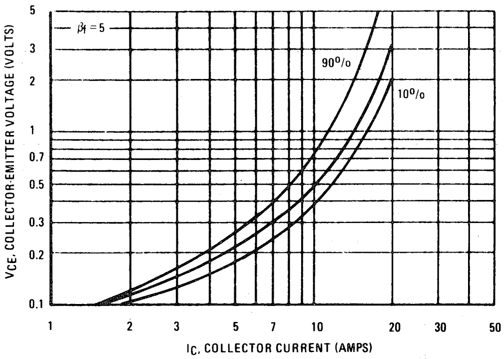


FIGURE 4 — BASE-EMITTER VOLTAGE

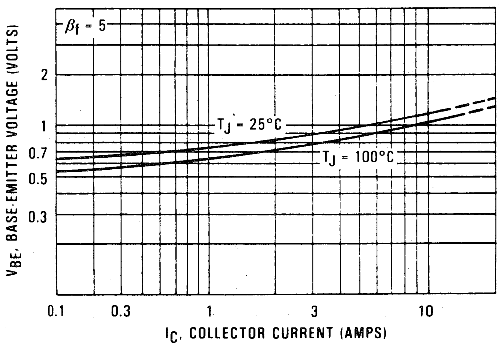


FIGURE 5 — COLLECTOR CUTOFF REGION

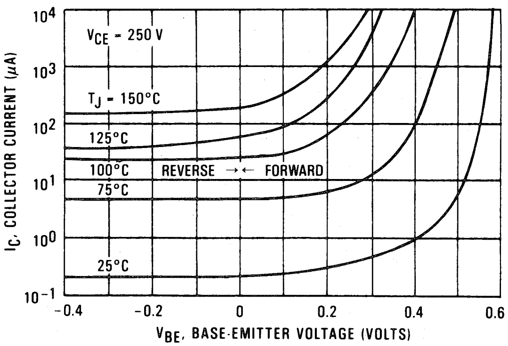


FIGURE 6 — CAPACITANCE

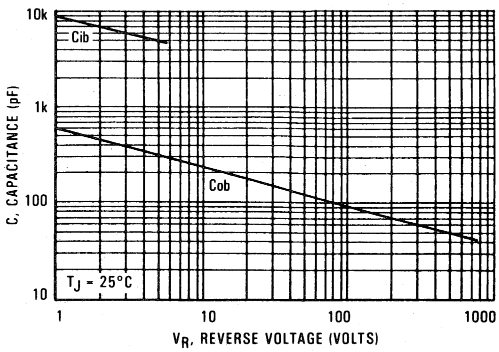


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TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

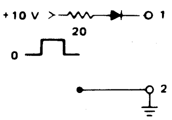
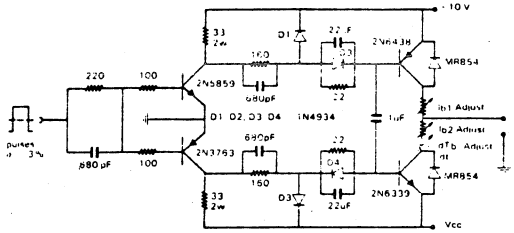
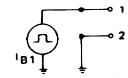
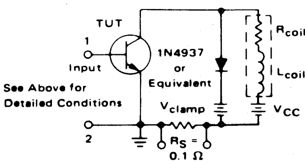
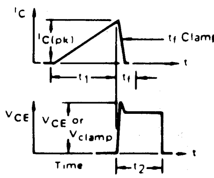
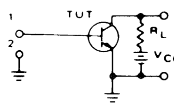
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA		TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 50 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

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FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

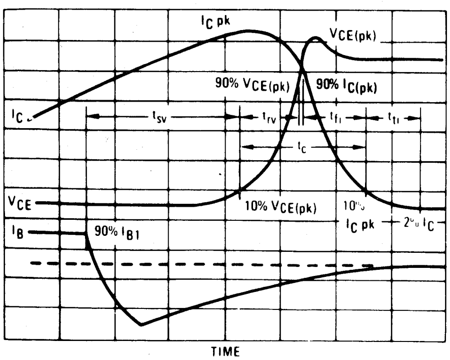
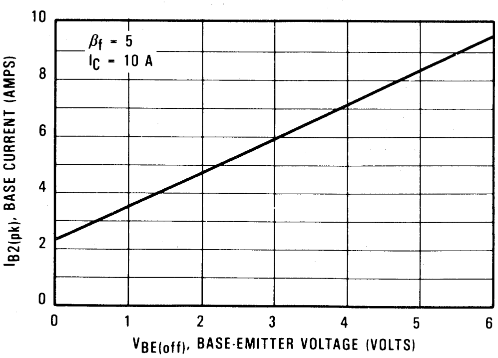


FIGURE 8 – PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME, Tsv

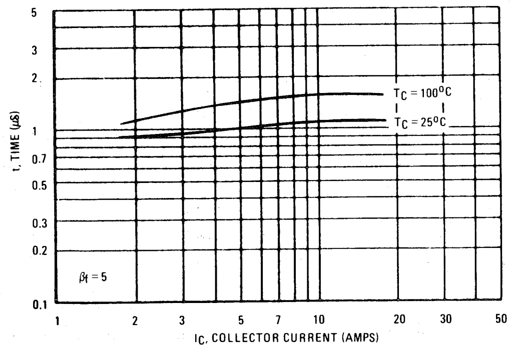


FIGURE 10 — CROSSOVER AND FALL TIMES

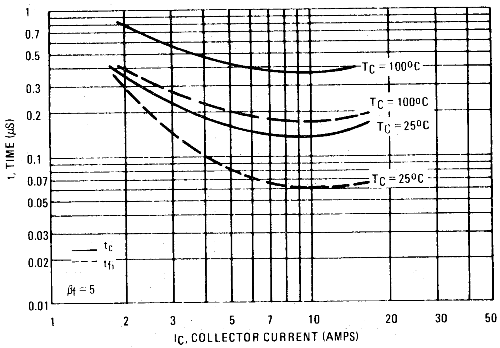


FIGURE 11a — TURN-OFF TIMES vs FORCED GAIN

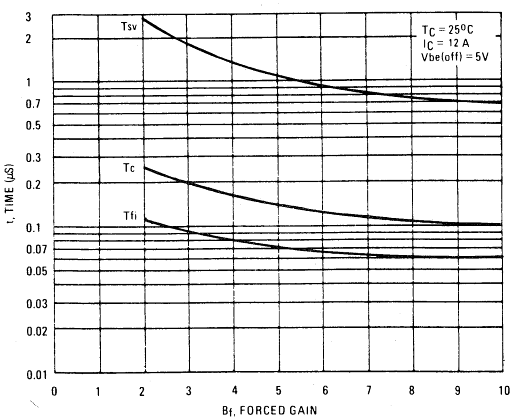
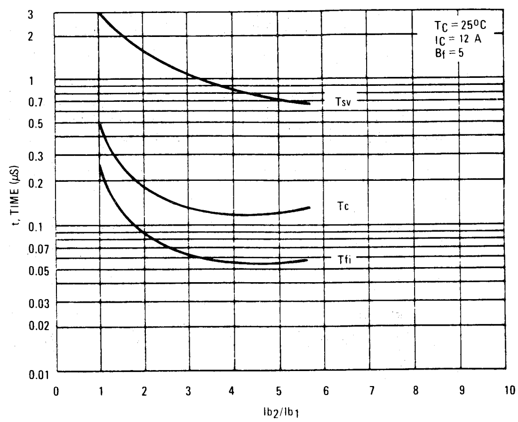


FIGURE 11b — TURN-OFF TIMES vs I_{b2}/I_{b1}



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The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

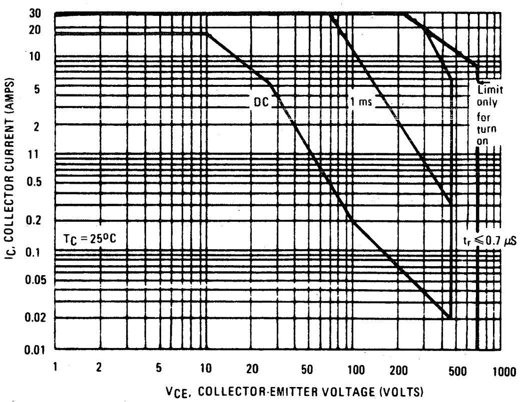


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

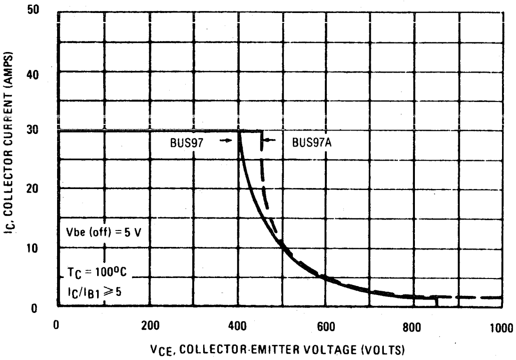
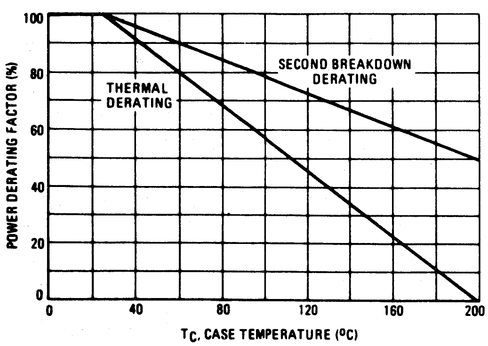


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

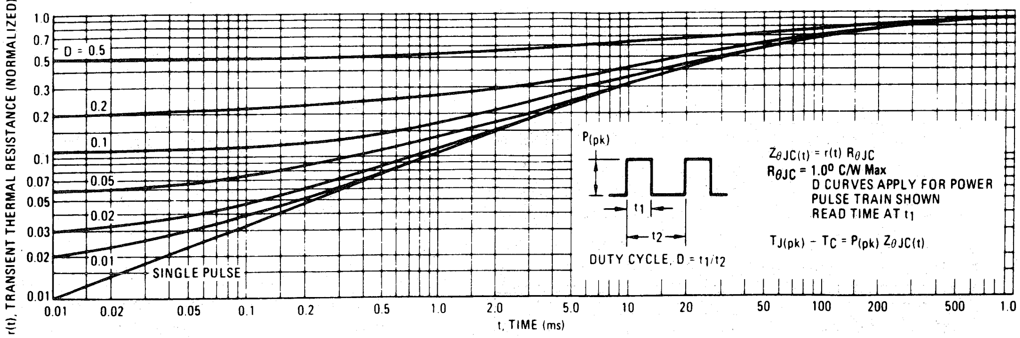
$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

3

FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)

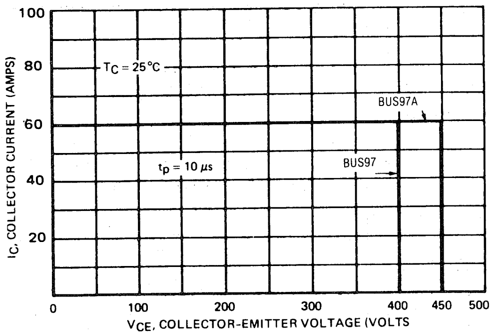
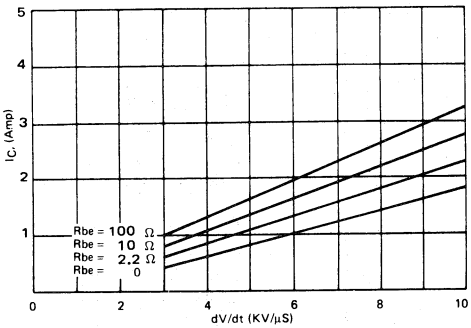


FIGURE 17 – $I_C = f(dV/dt)$



OLSOA

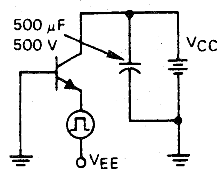
OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

3

FIGURE 18 – OVERLOAD SOA TEST CIRCUIT



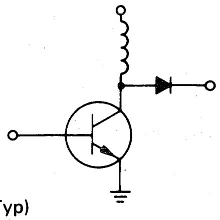
Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

BUS98
BUS98A

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The BUS 98 and BUS 98A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:



- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
60 ns Inductive Fall Time – 25°C (Typ)
120 ns Inductive Crossover Time – 25°C (Typ)

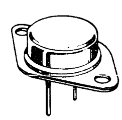
Operating Temperature Range – 65 to + 200°C

100°C Performance Specified for :
Reverse-Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents (125°C)

30 AMPERES
NPN SILICON POWER TRANSISTORS
400 AND 450 VOLTS (BVCEO)
250 WATTS
850 – 1000 V (BVCES)

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



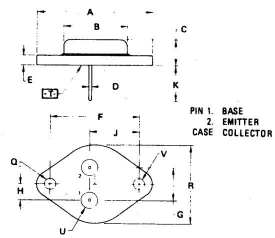
MAXIMUM RATINGS

Rating	Symbol	BUS 98	BUS98A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current – Continuous – Peak (1) – Overload	I_C I_{CM} I_{ol}	30 60 120		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	10 30		Adc
Total Power Dissipation – T_C = 25°C – T_C = 100°C Derate above 25°C	P_D	250 142 1.42		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to + 200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
⌖ ∅ 0.13 (0.005) Ⓜ | T | V Ⓜ
FOR LEADS:
⌖ ∅ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 200 mA, I_B = 0) L = 25 mH — BUS98 / BUS98A	$V_{CEO(sus)}$	400 / 450	– / –	– / –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) / (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEV}	– / –	– / –	0.4 / 4.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 10 Ω) T_C = 25°C / T_C = 125°C	I_{CER}	– / –	– / –	1.0 / 6.0	mAdc
Emitter Cutoff Current (V_{EB} = 7 Vdc, I_C = 0)	I_{EBO}			0.2	mAdc
Emitter-base breakdown Voltage (I_E = 100 mA - I_C = 0)	V_{EBO}	7.0			Vdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 12		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 20 Adc, V_{CE} = 5 Vdc) BUS98 / (I_C = 16 Adc, V_{CE} = 5 V) BUS98A	h_{FE}	8	–	–	–
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
BUS98: (I_C = 20 Adc, I_B = 4 Adc)		–	–	1.5	
(I_C = 30 Adc, I_B = 8 Adc)		–	–	3.5	
(I_C = 20 Adc, I_B = 4 Adc, T_c = 100°C)		–	–	2.0	
BUS98A: (I_C = 16 Adc, I_B = 3.2 Adc)		–	–	1.5	
(I_C = 24 Adc, I_B = 5 Adc)		–	–	5.0	
(I_C = 16 Adc, I_B = 3.2 Adc, T_c = 100°C)		–	–	2.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
BUS98: (I_C = 20 Adc, I_B = 4 Adc)		–	–	1.6	
(I_C = 20 Adc, I_B = 4 Adc, T_c = 100°C)		–	–	1.6	
BUS98A: (I_C = 16 Adc, I_B = 3.2 Adc)		–	–	1.6	
(I_C = 16 Adc, I_B = 3.2 Adc, T_c = 100°C)		–	–	1.6	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 khz)	C_{ob}	–	–	700	pF

SWITCHING CHARACTERISTICS
Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	(V_{CC} = 250 Vdc, I_C = 20A, I_{B1} = 4.0 A, tp = 30 μs, Duty Cycle ≤ 2%, $V_{BE(off)}$ = 5 V) (for BUS98A : I_C = 16A, Ib_1 = 3.2A)	t_d	–	0.1	0.2	μs
Rise Time		t_r	–	0.4	0.7	
Storage Time		t_s	–	1.55	2.3	
Fall Time		t_f	–	0.2	0.4	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	$I_{C(pk)}$ = 20A, I_{b1} = 4A (BUS98)	(T_C = 25°C)	t_{sv}	–	1.55	–	μs
Fall Time			t_{fi}	–	0.06	–	
Storage Time	$V_{BE(off)}$ = 5 V, $V_{CE(c1)}$ = 250 V) $I_{C(pk)}$ = 16A, I_{B1} = 3.2A (BUS98A)	(T_C = 100°C)	t_{sv}	–	1.8	2.8	
Crossover Time			t_c	–	0.3	0.6	
Fall Time			t_{fi}	–	0.17	0.35	

(1) Pulse Test : PW = 300 μs, Duty Cycle ≤ 2%.

3

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

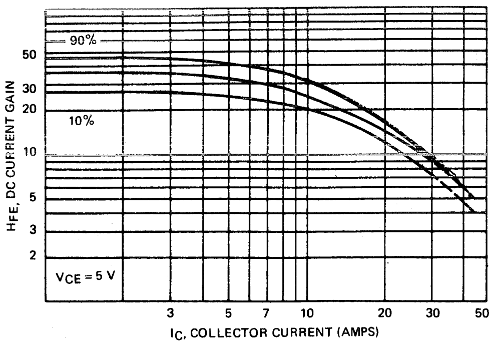


FIGURE 2 — COLLECTOR SATURATION REGION

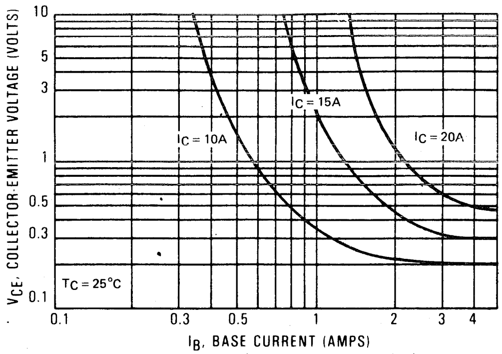


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

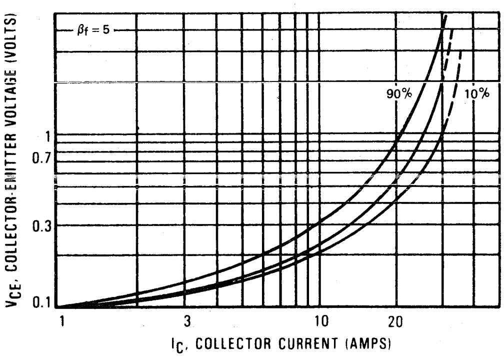


FIGURE 4 — BASE-EMITTER VOLTAGE

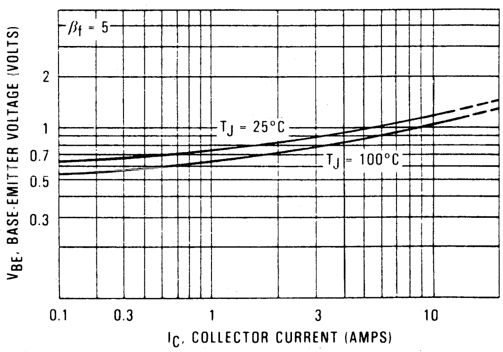


FIGURE 5 — COLLECTOR CUTOFF REGION

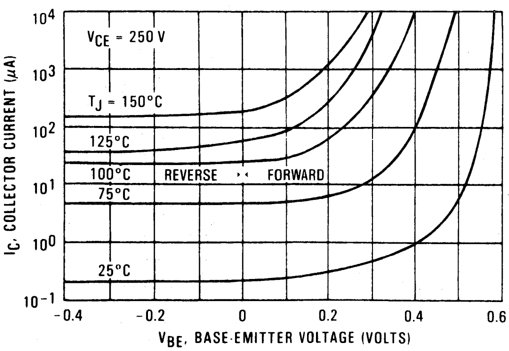


FIGURE 6 — CAPACITANCE

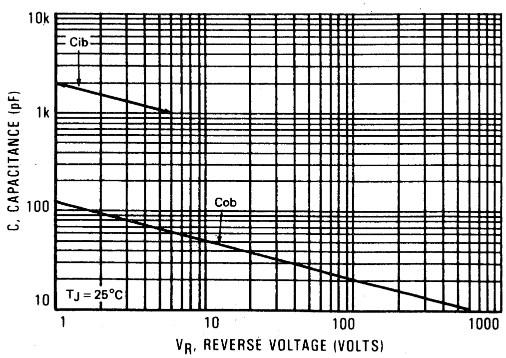


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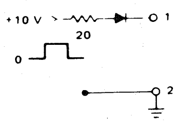
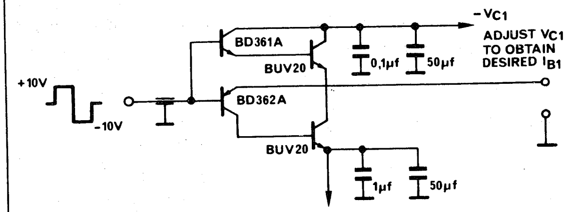
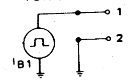
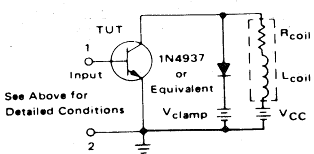
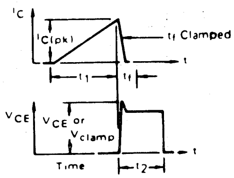
TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

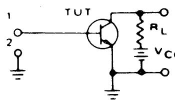
<table>
<tr><th></th><th>$V_{CEO(sus)}$</th><th>RBSOA AND INDUCTIVE SWITCHING</th><th>RESISTIVE SWITCHING</th></tr>
<tr><td>INPUT CONDITIONS</td><td>


PW Varied to Attain I_C = 100 mA</td><td>


</td><td>TURN ON TIME


I_{B1} adjusted to obtain the forced h_{FE} desired
TURN OFF TIME
Use inductive switching driver as the input to the resistive test circuit.</td></tr>
<tr><td>CIRCUIT VALUES</td><td>L_{coil} = 25 mH V_{CC} = 10 V
R_{coil} = 0.7 Ω</td><td>L_{coil} 180 µH
R_{coil} 0.05 Ω
V_{CC} 20 V
V_{clamp} 250 V</td><td>V_{CC} 250 V
Pulse Width 10 µs</td></tr>
<tr><td>TEST CIRCUITS</td><td colspan="2">INDUCTIVE TEST CIRCUIT


OUTPUT WAVEFORMS


t_1 Adjusted to Obtain I_C
$t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$
$t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$
Test Equipment
Scope – Tektronix
475 or Equivalent</td><td>RESISTIVE TEST CIRCUIT


</td></tr>
</table>

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

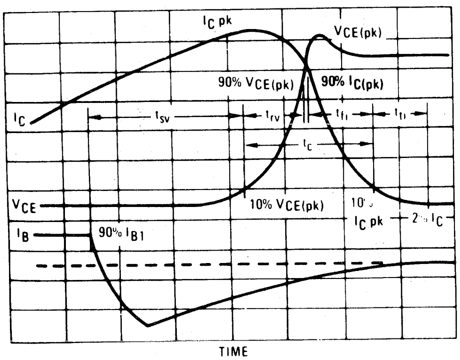
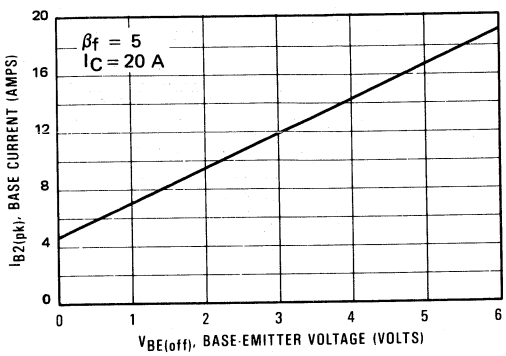


FIGURE 8 – PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME, Tsv

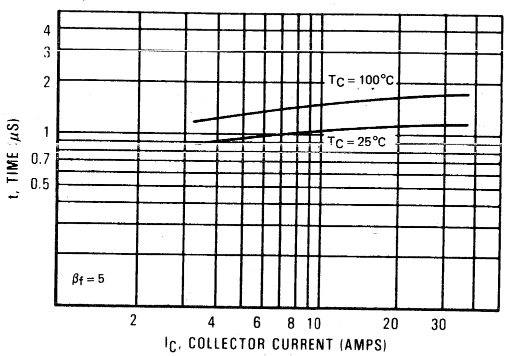


FIGURE 10 — CROSSOVER AND FALL TIMES

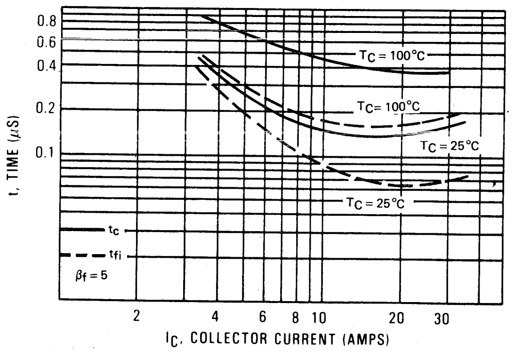


FIGURE 11a — TURN-OFF TIMES vs FORCED GAIN

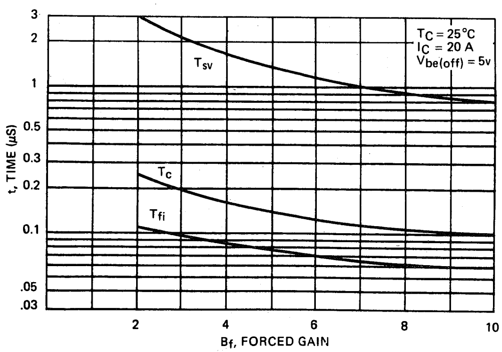
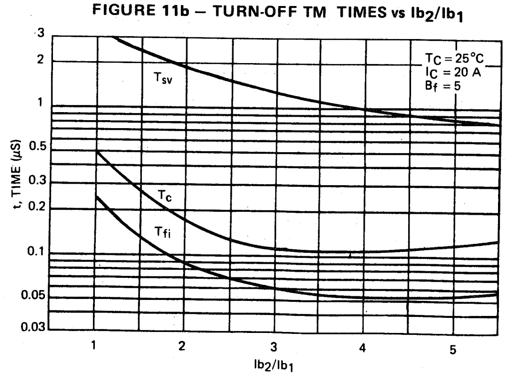


FIGURE 11b — TURN-OFF TM TIMES vs Ib2/Ib1



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

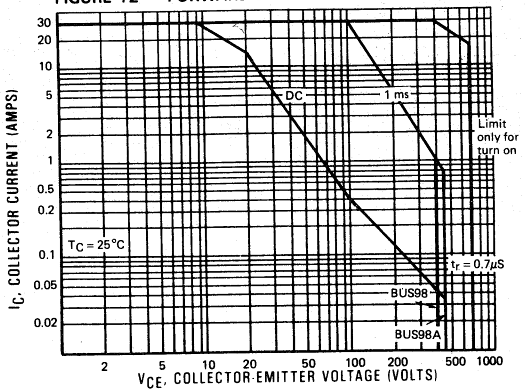


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

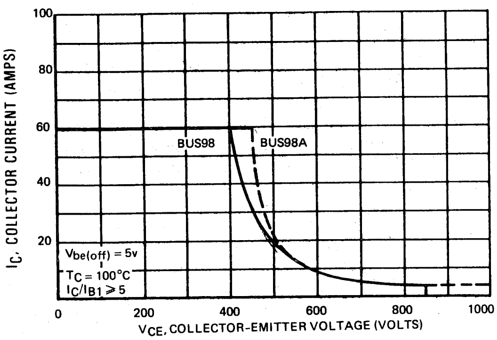
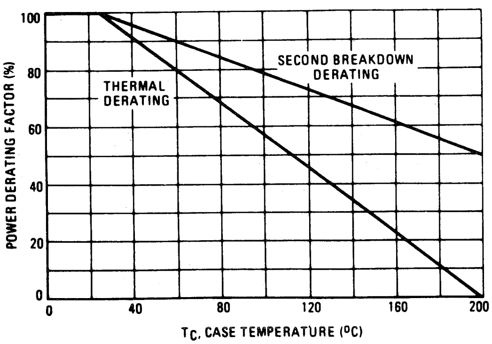


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

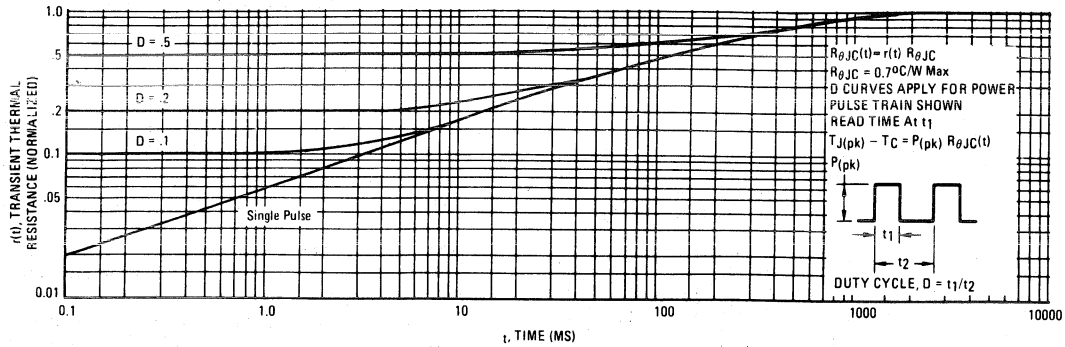
$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

3

FIGURE 15 — THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 — RATED OVERLOAD SAFE OPERATING AREA (OLSOA)

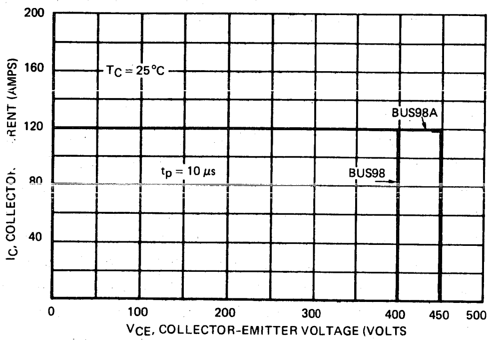
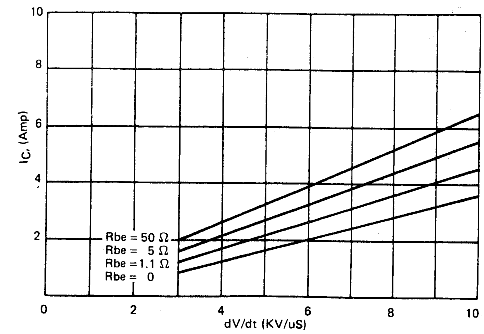


FIGURE 17 — $I_C = f$ (dV/dt)



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OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

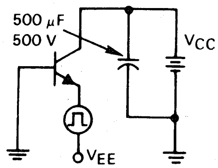
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 18 - OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p



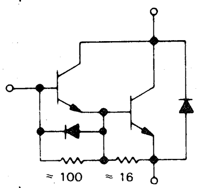
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUT13

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The BUT 13 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

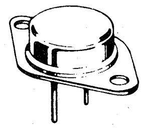
- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  300 nS Inductive Fall Time at 25°C (Typ)
  1.1 μS Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range −65 to 200°C



28 AMPERES
NPN SILICON POWER DARLINGTON TRANSISTORS
600 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



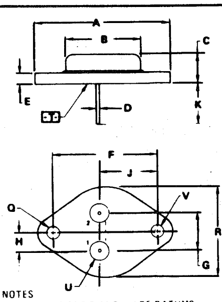
MAXIMUM RATINGS

Rating	Symbol	BUT13	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	28 35	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	6 7.5	Adc
Free Wheel Diode: Forward current – Continuous – Peak	I_F I_{FM}	28 35	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≦ 10%.



NOTES
1 DIMENSIONS Q AND V ARE DATUMS
2 [T] IS SEATING PLANE AND DATUM
3 POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
| ⌖ | ∅ 0.13 (0.005) Ⓜ | T | V Ⓜ |
FOR LEADS
| ⌖ | ∅ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	-	39.37		1.550
B		21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67		1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	400	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100 °C	I_{CEV}	 – –	 – –	 0.1 2.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 A, V_{CE} = 5 V) (I_C = 18 A, V_{CE} = 5 V)	h_{FE}	 30 20	 – –	 – –	
Collector-Emitter Saturation Voltage (I_C = 10 A, I_B = 0.5 A) (I_C = 18 A, I_B = 1.8 A) (I_C = 22 A, I_B = 2.2 A) (I_C = 28 A, I_B = 5.6 A)	$V_{CE(sat)}$	 – – – –	 – – – –	 2.0 2.5 3.0 5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 A, I_B = 0.5 A) (I_C = 18 A, I_B = 1.8 A) (I_C = 22 A, I_B = 2.2 A)	$V_{BE(sat)}$	 – – –	 – – –	 2.5 3.0 3.3	Vdc
Diode Forward Voltage (I_F = 22 A)	V_f	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS
Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	T_C = 25°C	See Table 1	t_s	–	1.1	2.6	μs
Fall Time		I_C = 18 A	t_f	–	0.3	0.8	μs
Storage Time	T_C = 100°C	I_{B1} = 1.8 A	t_s	–	1.4	–	μs
Fall Time		$V_{BE(off)}$ = 5 V	t_f	–	0.33	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

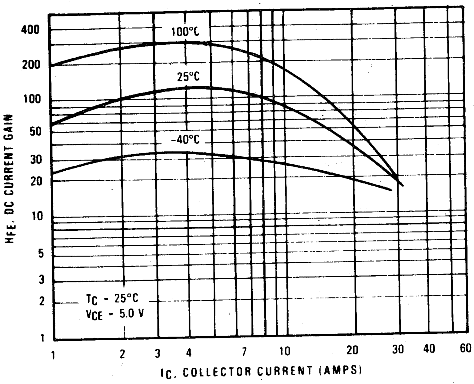


FIGURE 2 — COLLECTOR SATURATION REGION

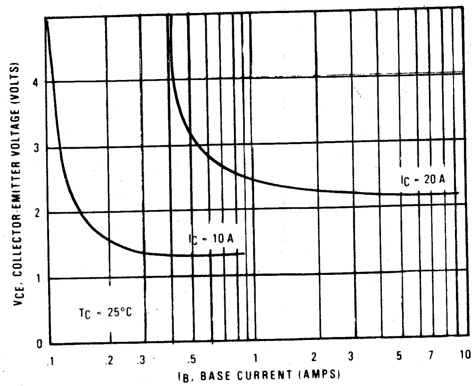


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

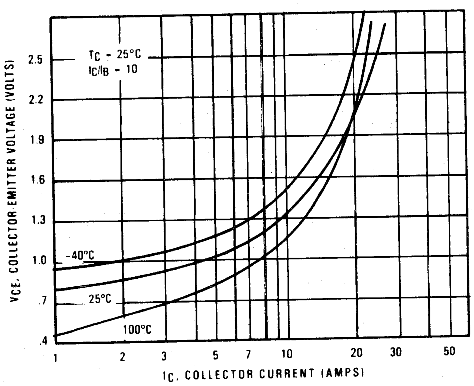


FIGURE 4 — BASE-EMITTER VOLTAGE

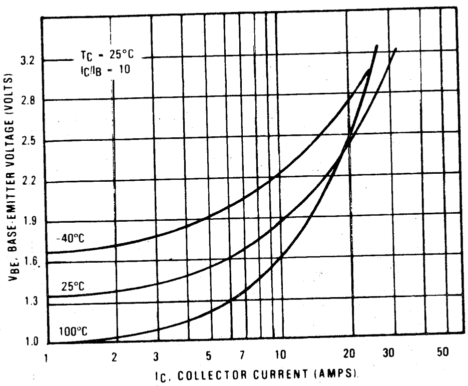


FIGURE 5 — THERMAL RESPONSE

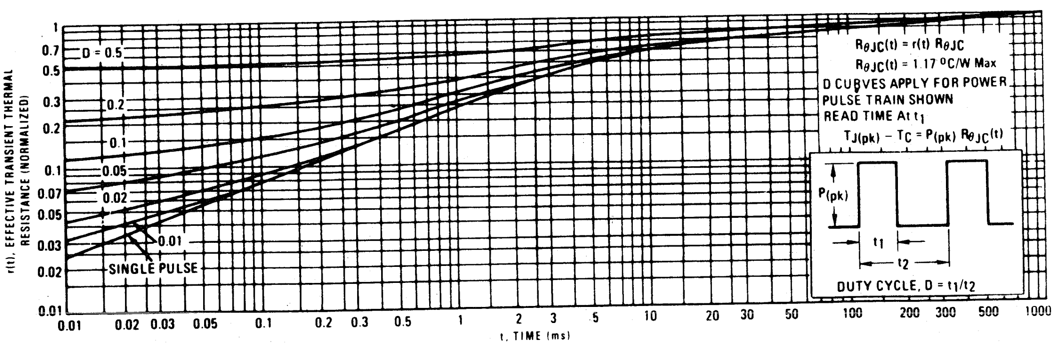


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TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

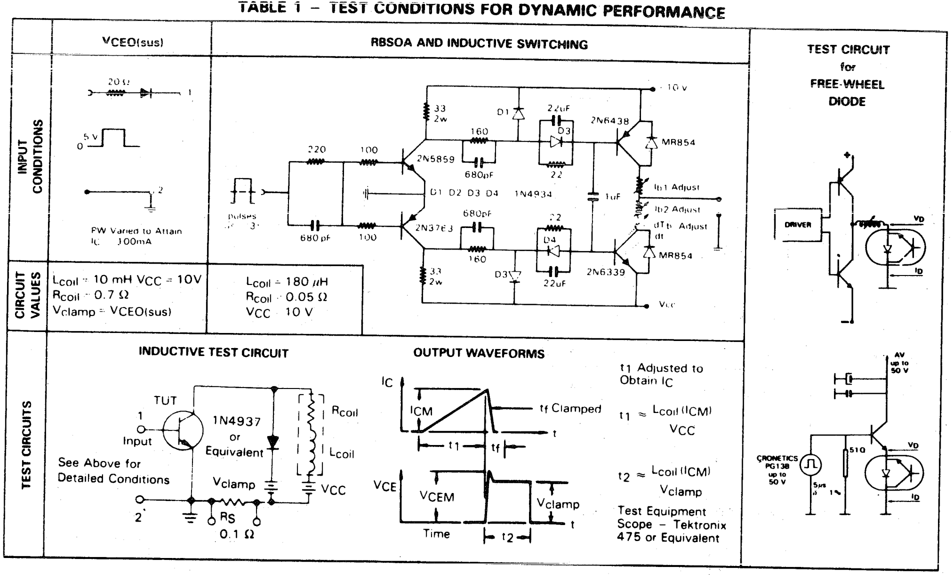


FIGURE 6 — FALL TIME vs IB2/IB1

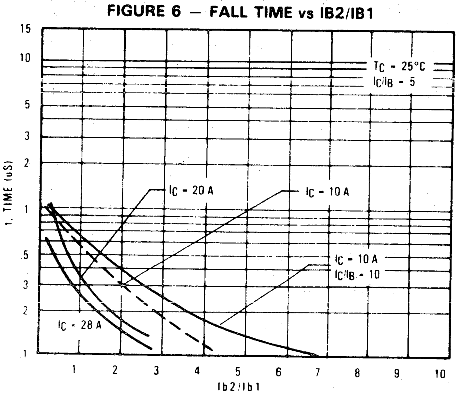


FIGURE 7 — TURN-OFF TIME vs Ic

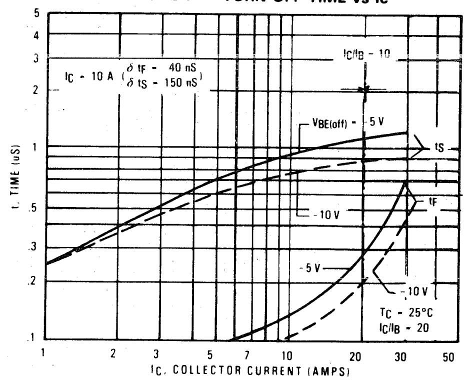


FIGURE 8 — STORAGE TIME vs FORCED GAIN

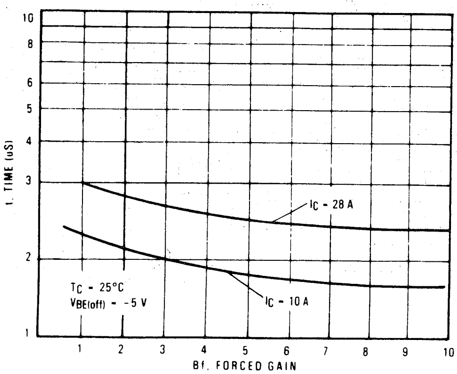
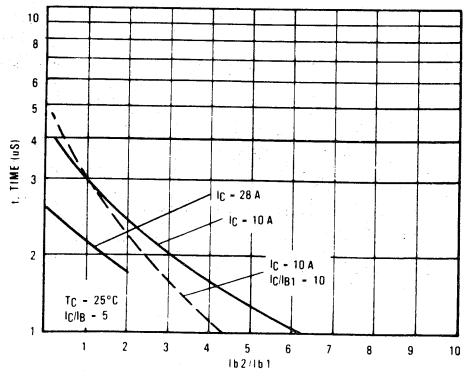


FIGURE 9 — STORAGE TIME vs Ib2/Ib1



FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

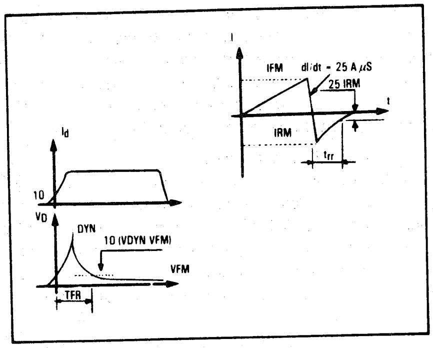


FIGURE 11 — FORWARD VOLTAGE

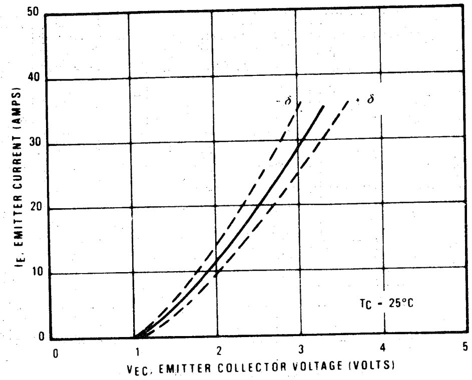


FIGURE 12 — FORWARD MODULATION VOLTAGE

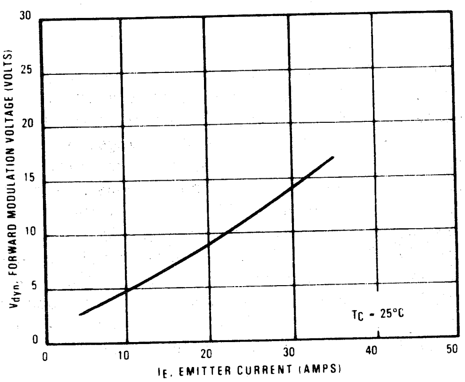


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

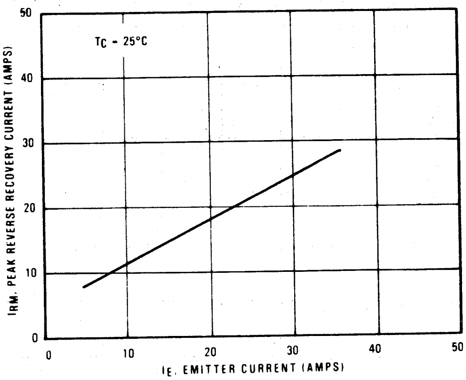


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FIGURE 14 — FORWARD RECOVERY TIME

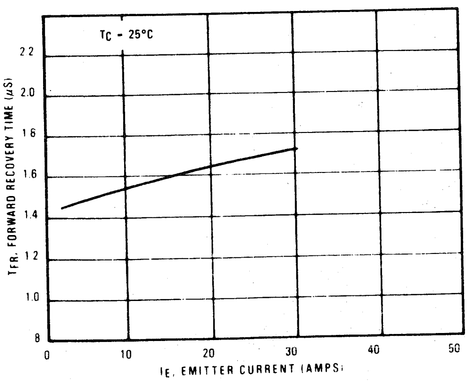
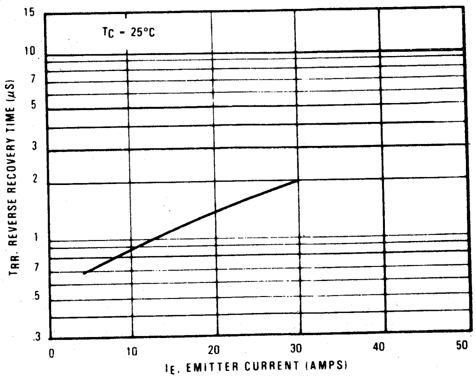


FIGURE 15 — REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specifed for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

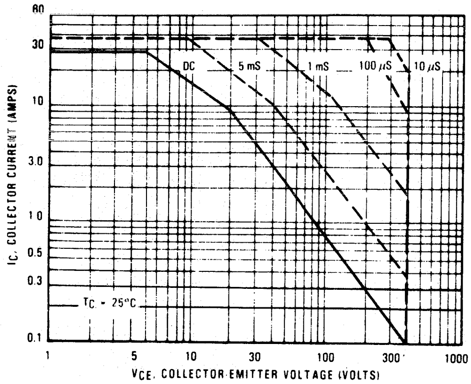
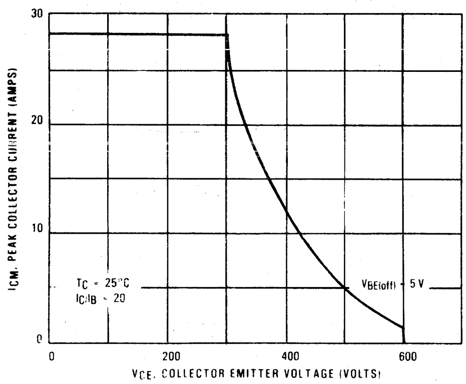


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to grater dissipation than the curves indicate.

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$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

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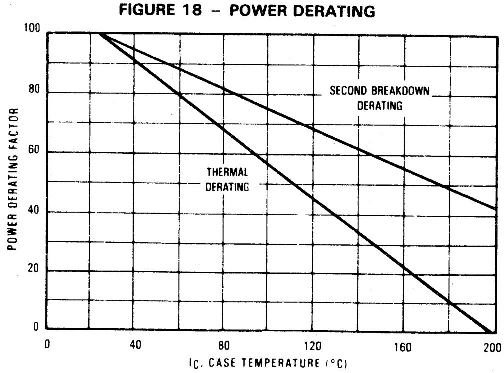
FIGURE 18 — POWER DERATING



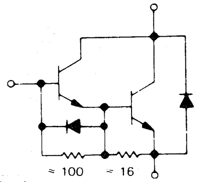
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUT14

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The BUT14 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

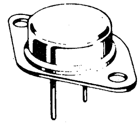
- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  300 nS Inductive Fall Time at 25°C (Typ)
  1.3 μS Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range −65 to 200°C



25 AMPERES
NPN SILICON POWER DARLINGTON TRANSISTORS
850 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



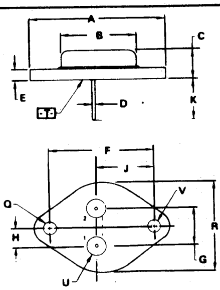
MAXIMUM RATINGS

Rating	Symbol	BUT14	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	500	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	25 35	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	5 7.5	Adc
Free Wheel Diode: Forward current – Continuous – Peak	I_F I_{FM}	25 35	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≦ 10%.



NOTES
1 DIMENSIONS Q AND V ARE DATUMS
2 [T] IS SEATING PLANE AND DATUM
3 POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
[⌖ | ⌀ 13 (0 005) Ⓤ | T | V Ⓤ]
FOR LEADS
[⌖ | ⌀ 13 (0 005) Ⓜ T | V Ⓜ | Q Ⓜ]
4 DIMENSIONS AND TOLERANCES PER ANSI Y14 5, 1973

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39 37		1 550
B		21 08		0 830
C	6 35	7 62	0 250	0 300
D	0 97	1 09	0 038	0 043
E		3 43		0 135
F	30 15 BSC		1 187 BSC	
G	10 92 BSC		0 430 BSC	
H	5 46 BSC		0 215 BSC	
J	16 89 BSC		0 665 BSC	
K	11 18	12 19	0 440	0 480
Q	3 81	4 19	0 150	0 165
R		26 67		1 050
U	4 83	5 33	0 190	0 210
V	3 81	4 19	0 150	0 165

CASE 1-05 TO-3

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	500	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	0.2	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	2.0	
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 8 A, V_{CE} = 5 V)	h_{FE}	30	–	–	
(I_C = 16 A, V_{CE} = 5 V)		15	–	–	
Collector-Emitter Saturation Voltage (I_C = 8 A, I_B = 0.4 A)	$V_{CE(sat)}$	–	–	2.0	Vdc
(I_C = 16 A, I_B = 1.6 A)		–	–	3.0	
(I_C = 20 A, I_B = 2.0 A)		–	–	3.5	
(I_C = 25 A, I_B = 5 A)		–	–	5.0	
Base-Emitter Saturation Voltage (I_C = 8 A, I_B = 0.4 A)	$V_{BE(sat)}$	–	–	2.5	Vdc
(I_C = 16 A, I_B = 1.6 A)		–	–	2.9	
(I_C = 20 A, I_B = 2 A)		–	–	3.3	
Diode Forward Voltage (I_F = 20 A)	V_f	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS
Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	T_C = 25°C	See Table 1	t_s	–	1.3	2.8	μs
Fall Time		I_C = 16 A	t_f	–	0.3	0.8	μs
Storage Time	T_C = 100°C	I_{B1} = 1.6 A	t_s	–	1.5	–	μs
Fall Time		$V_{BE(off)}$ = 5 V	t_f	–	0.35	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

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TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

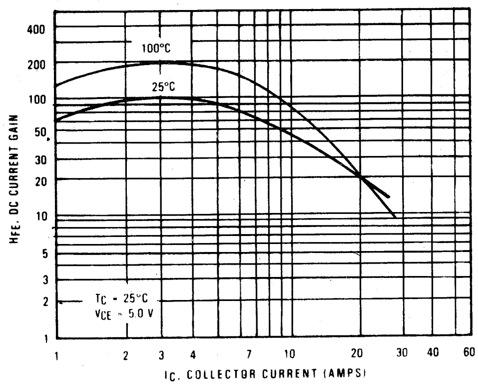

FIGURE 2 — COLLECTOR SATURATION REGION

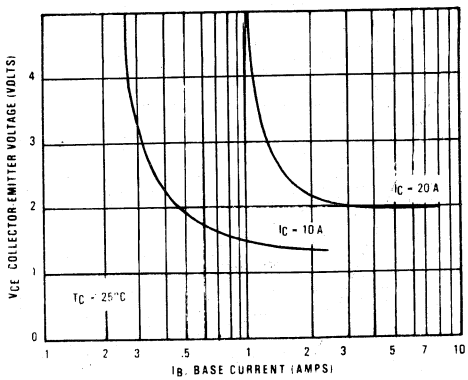

FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

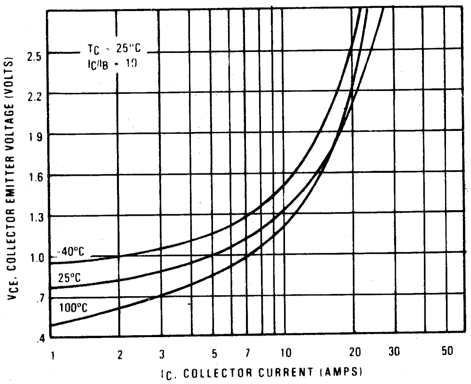

FIGURE 4 — BASE-EMITTER VOLTAGE

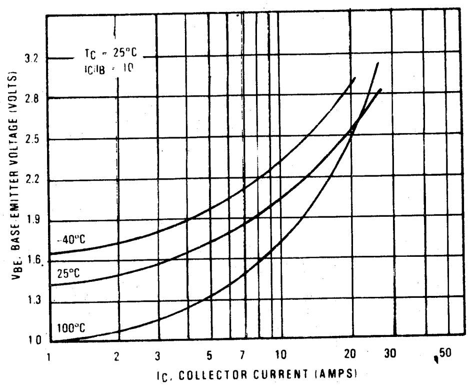

FIGURE 5 — THERMAL RESPONSE

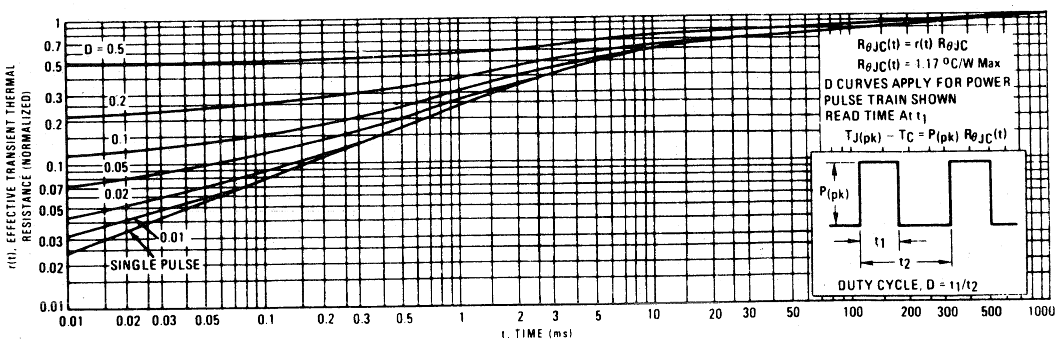

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TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

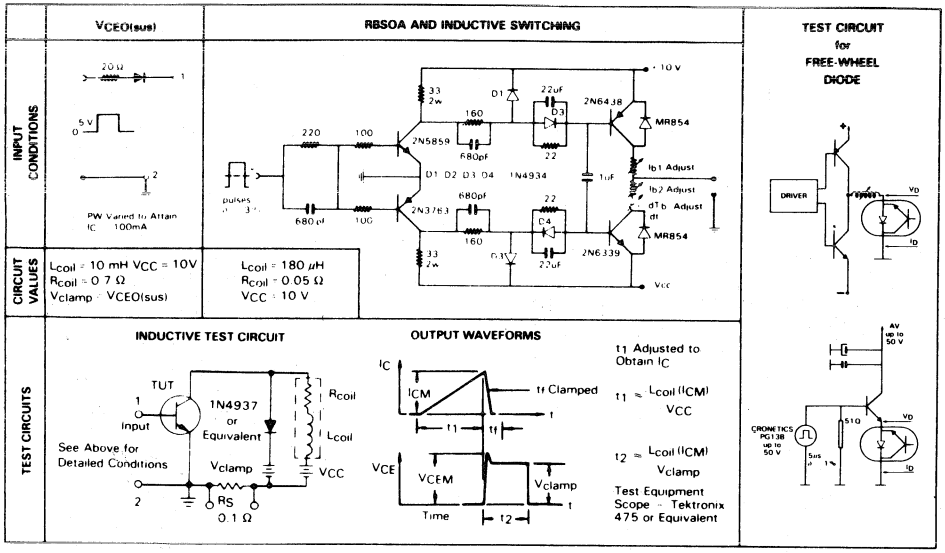

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FIGURE 6 — FALL TIME vs IB2/IB1

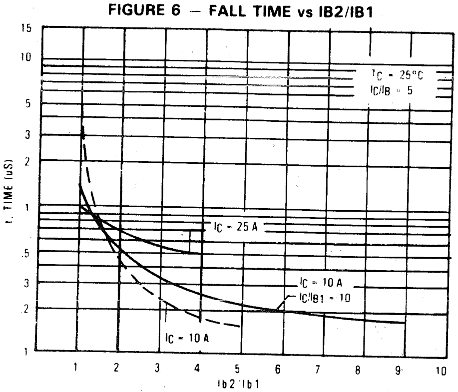


FIGURE 7 — TURN-OFF TIME vs Ic

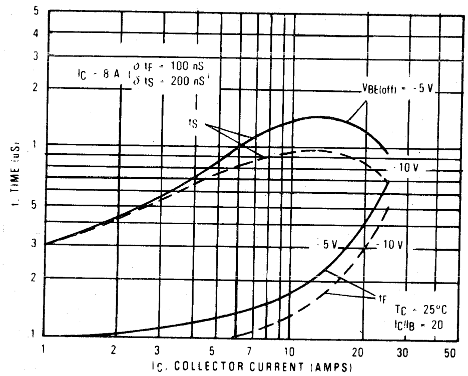


FIGURE 8 — STORAGE TIME vs FORCED GAIN

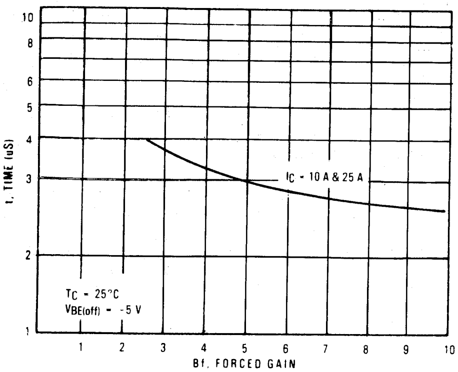
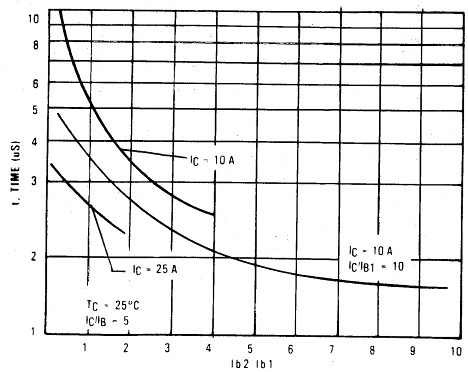


FIGURE 9 — STORAGE TIME vs Ib2/Ib1



FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

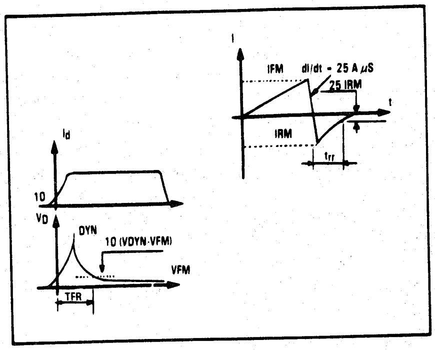


FIGURE 11 — FORWARD VOLTAGE

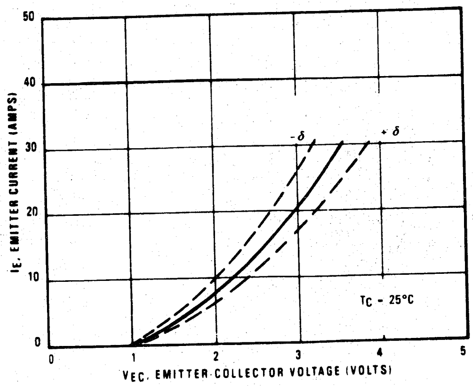


FIGURE 12 — FORWARD MODULATION VOLTAGE

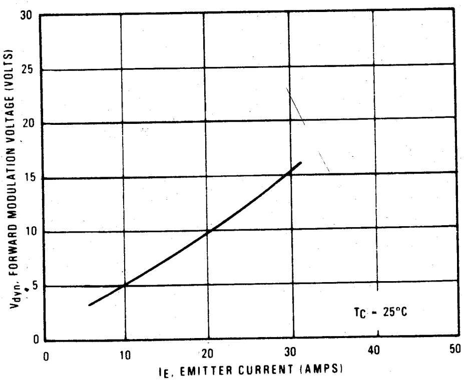


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

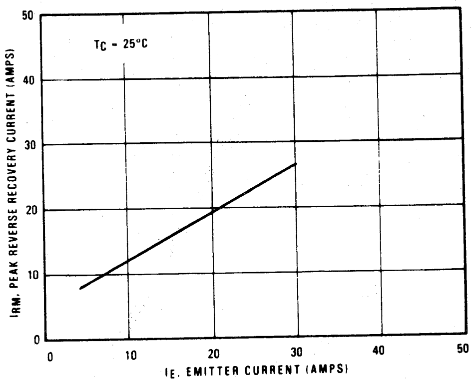


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FIGURE 14 — FORWARD RECOVERY TIME

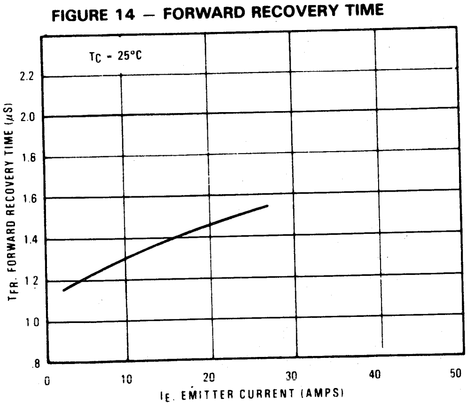
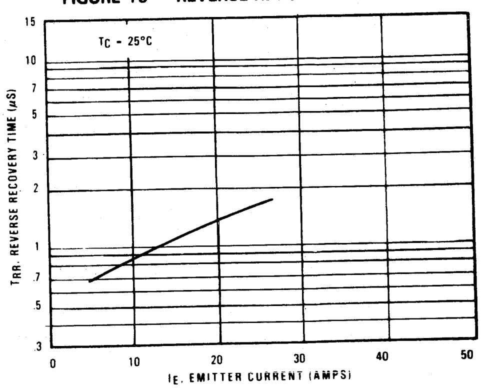


FIGURE 15 — REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

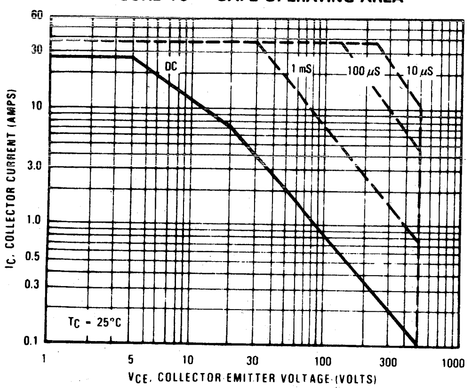
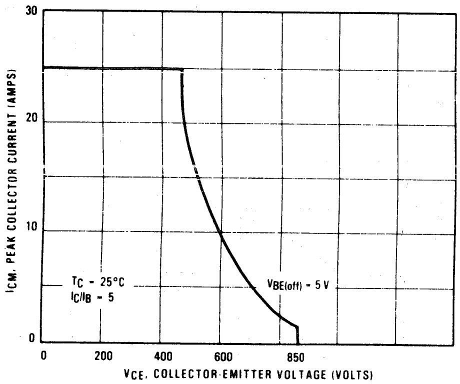


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to grater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

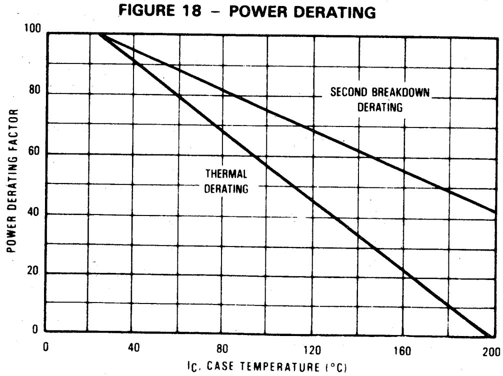
$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

3

FIGURE 18 — POWER DERATING



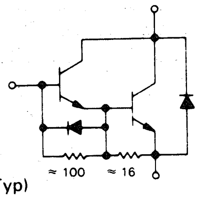
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUT15

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The BUT 15 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

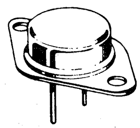
- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  300 nS Inductive Fall Time at 25°C (Typ)
  1.2 μS Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range −65 to 200°C



20 AMPERES
NPN SILICON POWER DARLINGTON TRANSISTORS
1000 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data − representing device characteristics boundaries − are given to facilitate "worst case" design.



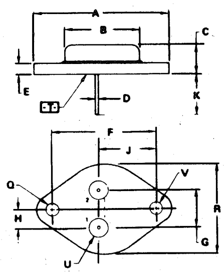
MAXIMUM RATINGS

Rating	Symbol	BUT15	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector-Emitter Voltage	V_{CEV}	1000	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current − Continuous − Peak (1)	I_C I_{CM}	20 25	Adc
Base Current − Continuous − Peak (1)	I_B I_{BM}	5 10	Adc
Free Wheel Diode: Forward current − Continuous − Peak	I_F I_{FM}	20 25	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≦ 10%.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. [T] IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
   | ⌖ | ⌀ 0.13 (0.005) Ⓜ | T | V Ⓜ |
   FOR LEADS
   | ⌖ | ⌀ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	700	–	–	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	0.1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100 °C)		–	–	2.0	
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17		
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				
(I_C = 6 A, V_{CE} = 5 V)		30	–	–	
(I_C = 12 A, V_{CE} = 5 V)		15	–	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 6 A, I_B = 0.3 A)		–	–	2.0	
(I_C = 12 A, I_B = 1.2 A)		–	–	3.0	
(I_C = 16 A, I_B = 1.6 A)		–	–	3.5	
(I_C = 20 A, I_B = 4 A)		–	–	5.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 6 A, I_B = 0.3 A)		–	–	2.5	
(I_C = 12 A, I_B = 1.2 A)		–	–	2.9	
(I_C = 16 A, I_B = 1.6 A)		–	–	3.3	
Diode Forward Voltage (I_F = 16 A)	V_f	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS
Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	T_C = 25°C	See Table 1	t_s	–	1.2	2.5	μs
Fall Time		I_C = 12 A	t_f	–	0.3	0.8	μs
Storage Time	T_C = 100°C	I_{B1} = 1.2 A	t_s	–	1.4	–	μs
Fall Time		$V_{BE(off)}$ = 5 V	t_f	–	0.35	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

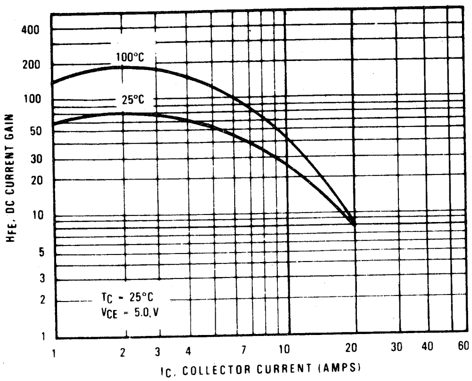


FIGURE 2 — COLLECTOR SATURATION REGION

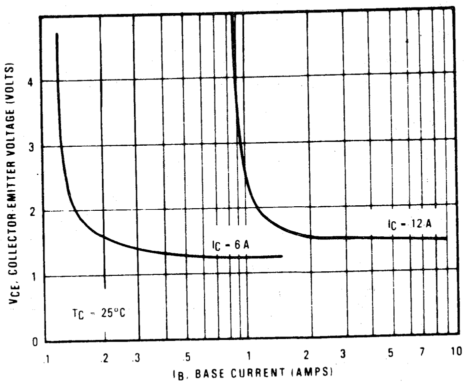


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

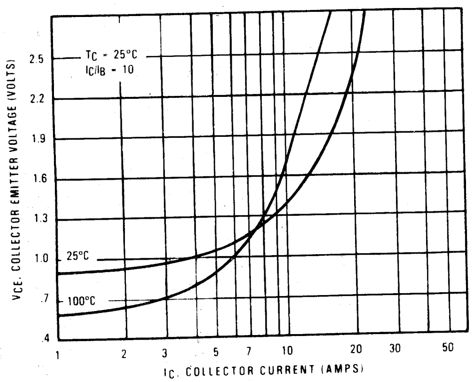


FIGURE 4 — BASE-EMITTER VOLTAGE

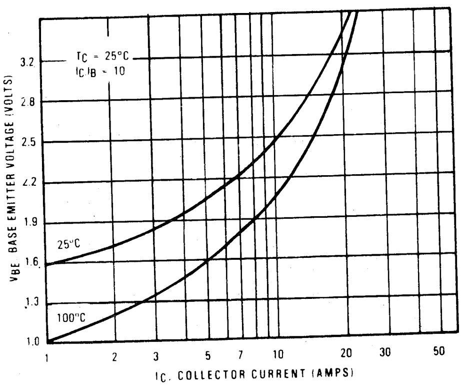


FIGURE 5 — THERMAL RESPONSE

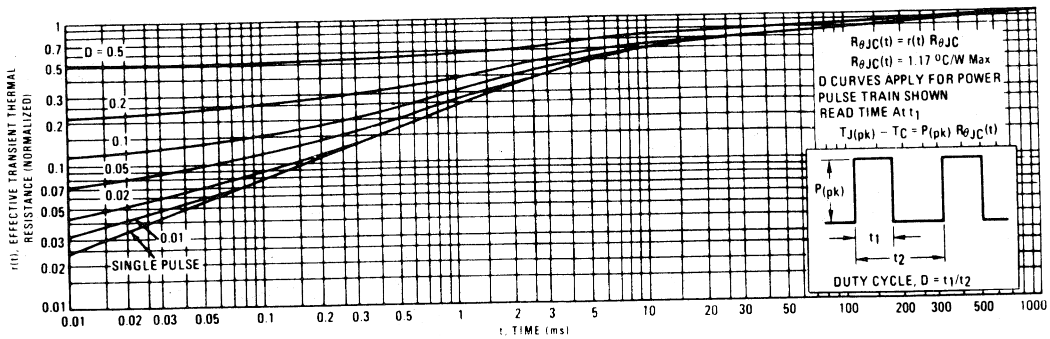


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TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

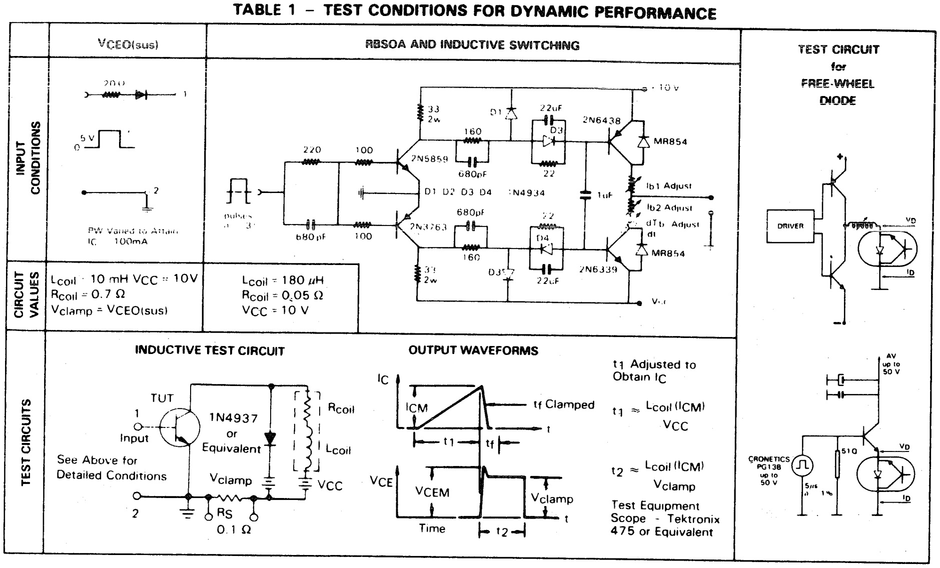


FIGURE 6 – FALL TIME vs IB2/IB1

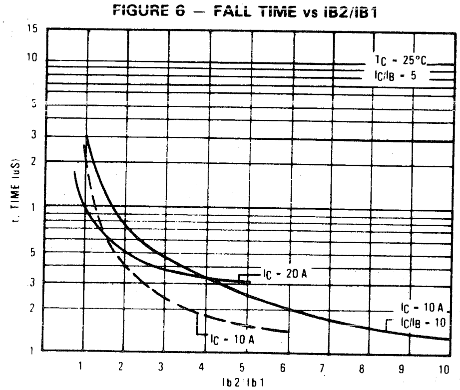


FIGURE 7 – TURN-OFF TIME vs Ic

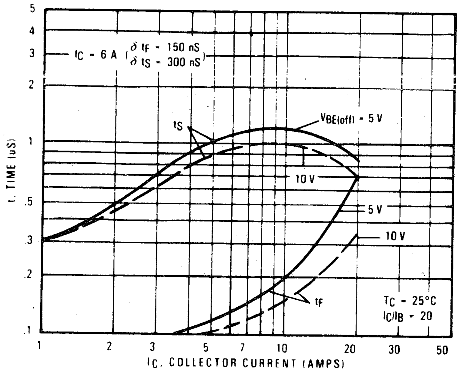


FIGURE 8 – STORAGE TIME vs FORCED GAIN

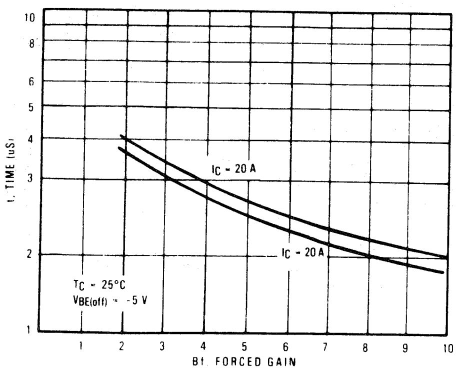
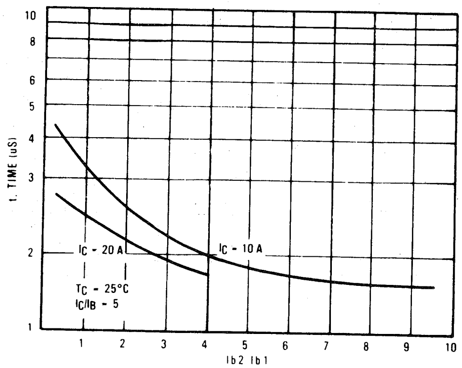


FIGURE 9 – STORAGE TIME vs Ib2/Ib1



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FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

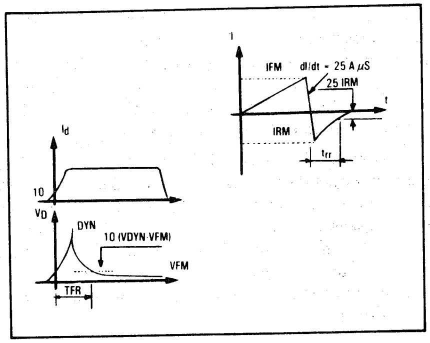


FIGURE 11 — FORWARD VOLTAGE

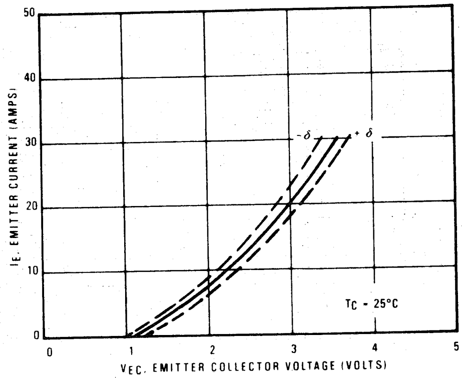


FIGURE 12 — FORWARD MODULATION VOLTAGE

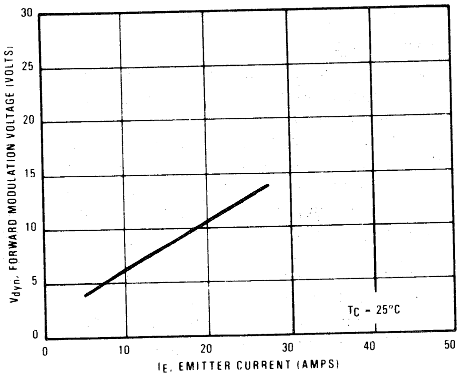


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

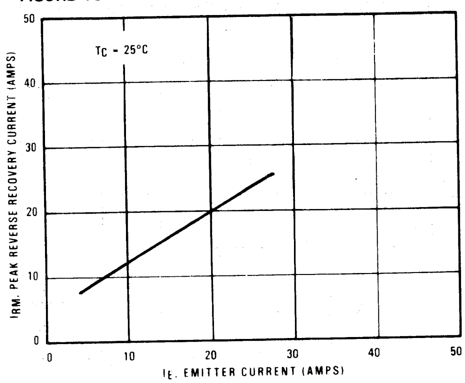


FIGURE 14 — FORWARD RECOVERY TIME

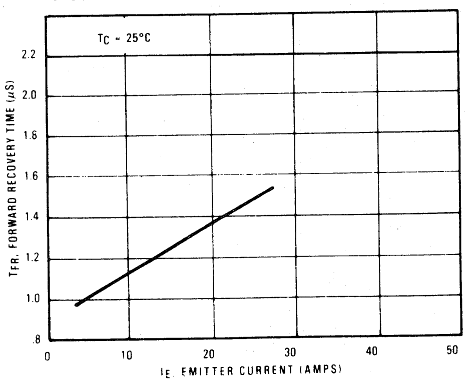
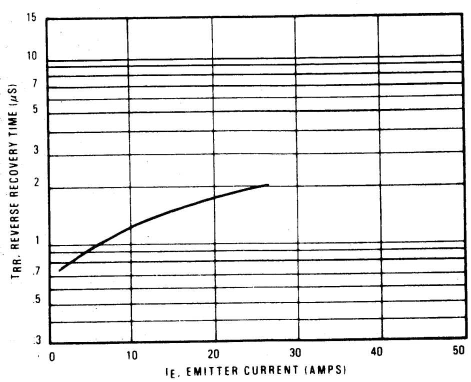


FIGURE 15 — REVERSE RECOVERY TIME



3

The Safe Operating Area figures shown in Figures 16 and 17 are specifed for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

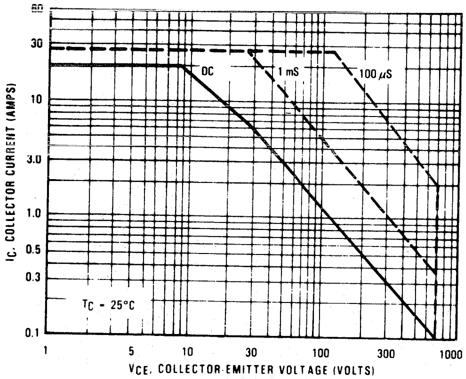
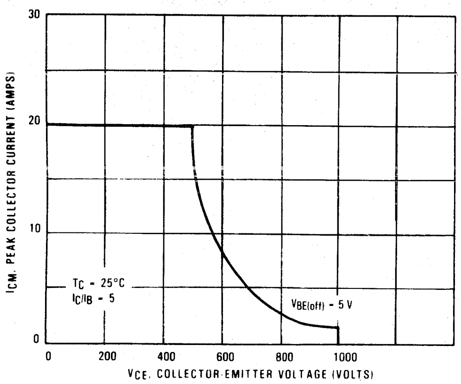


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to grater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

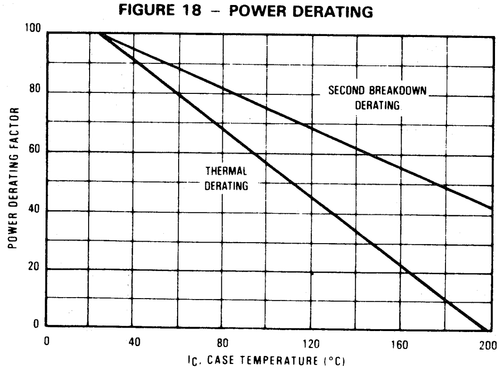
$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

3

FIGURE 18 — POWER DERATING



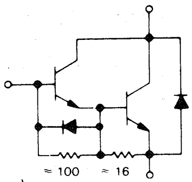
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUT16

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The BUT 16 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  - 2.0 uS Inductive Fall Time at 100°C (Typ)
  - 0.8 uS Inductive Storage Time at 100°C (Typ)
- Operating Temperature Range − 65 to 175°C



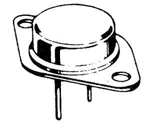
12 AMPERES

NPN SILICON POWER DARLINGTON TRANSISTORS

1400 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data − representing device characteristics boundaries − are given to facilitate "worst case" design.



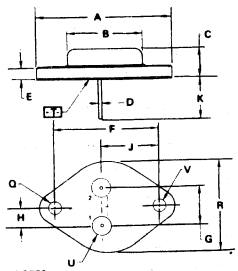
MAXIMUM RATINGS

Rating	Symbol	BUT16	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	1000	Vdc
Collector-Emitter Voltage	V_{CEV}	1400	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	12 20	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	8 10	Adc
Free Wheel Diode: Forward current – Continuous – Peak	I_F I_{FM}	12 20	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 75	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to + 175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≦ 10%.



NOTES
1 DIMENSIONS Q AND V ARE DATUMS
2 [T] IS SEATING PLANE AND DATUM
3 POSITIONAL TOLERANCE FOR MOUNTING HOLE Q

⌖	⌀ 0.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS

⌖	⌀ 0.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	1000	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	0.1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100 °C)		–	–	2.0	
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 4 A, V_{CE} = 5 V)	h_{FE}	20	–	–	
(I_C = 8 A, V_{CE} = 5 V)		5	–	–	
Collector-Emitter Saturation Voltage (I_C = 12 A, I_B = 6 A)	$V_{CE(sat)}$	–	–	5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 8 A, I_B = 1.6 A)	$V_{BE(sat)}$	–	–	3.3	Vdc
Diode Forward Voltage (I_F = 12 A)	V_f	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS
Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	T_C = 25°C	See Table 1	t_s	–	–	3.3	μs
Fall Time		I_C = 8 A	t_f	–	–	1.5	μs
Storage Time	T_C = 100°C	I_{B1} = 1.6 A	t_s	–	2.0	–	μs
Fall Time		$V_{BE(off)}$ = 5 V	t_f	–	0.8	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

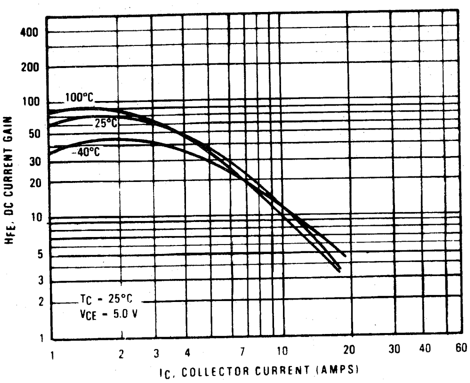


FIGURE 2 — COLLECTOR SATURATION REGION

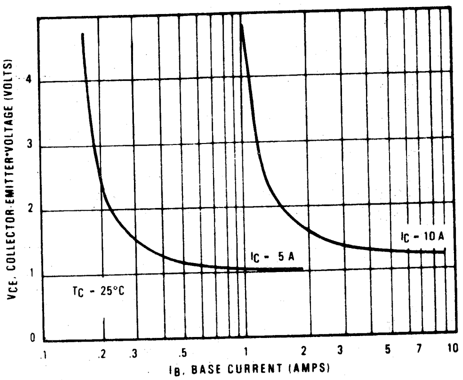


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

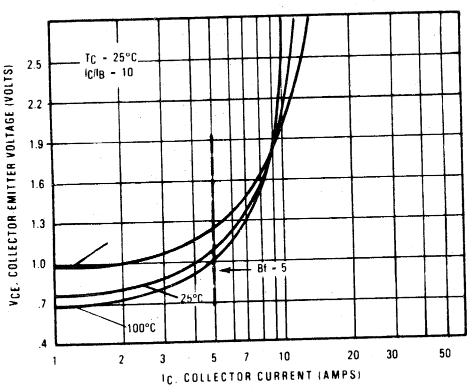


FIGURE 4 — BASE-EMITTER VOLTAGE

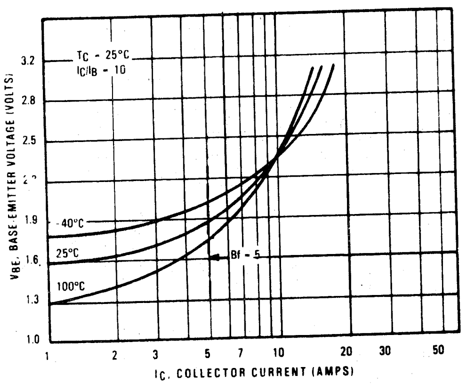
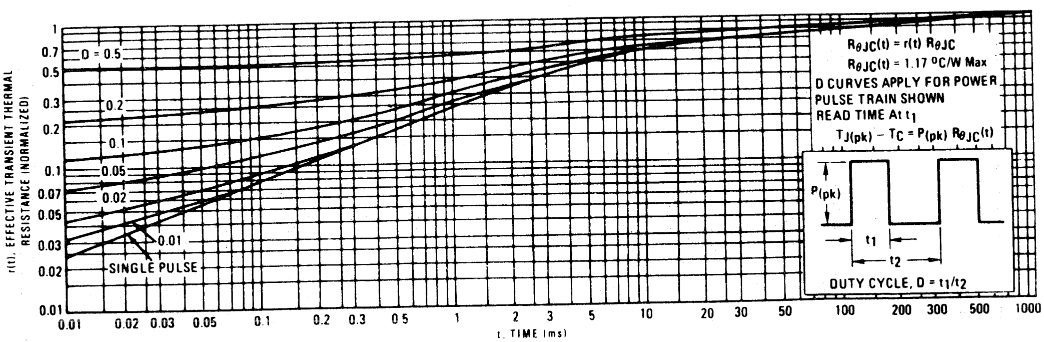


FIGURE 5 — THERMAL RESPONSE



3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

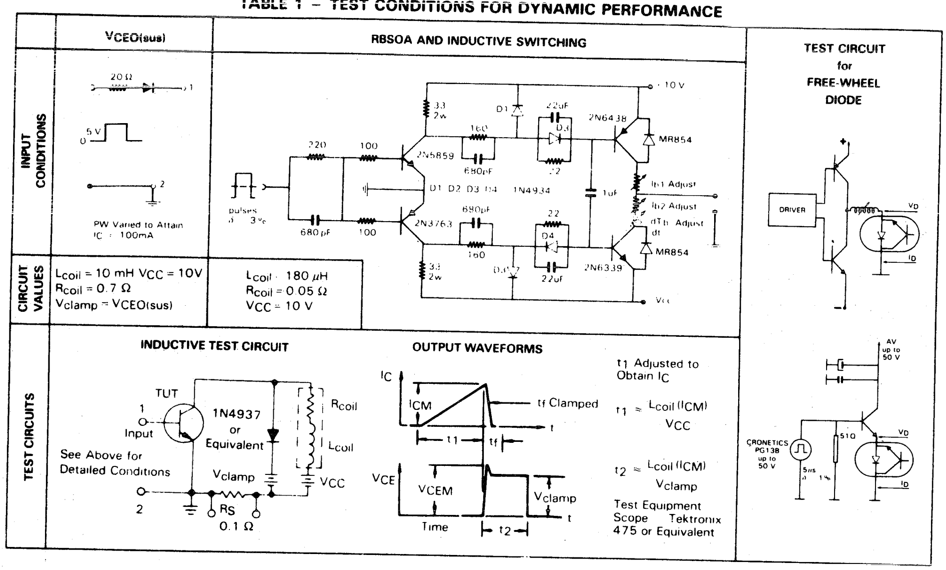


FIGURE 6 — FALL TIME vs IB2/IB1

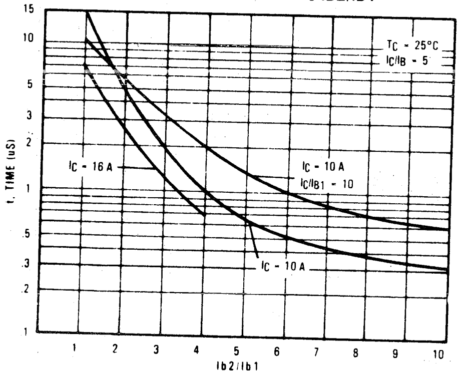


FIGURE 7 — TURN-OFF TIME vs Ic

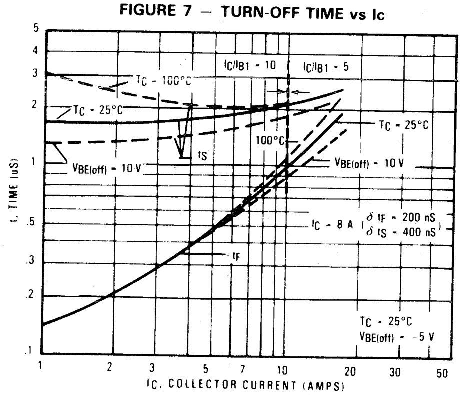


FIGURE 8 — STORAGE TIME vs FORCED GAIN

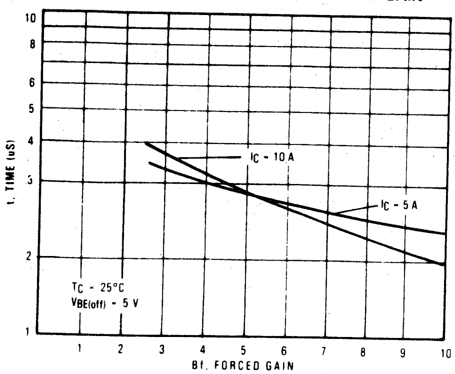
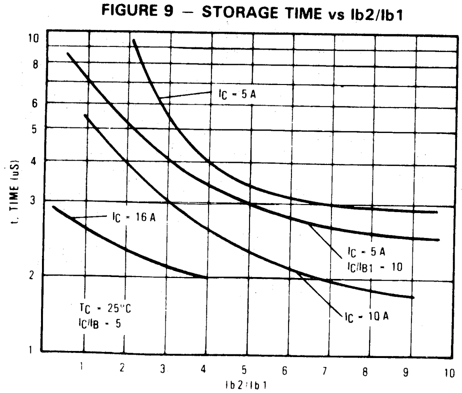


FIGURE 9 — STORAGE TIME vs Ib2/Ib1



FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

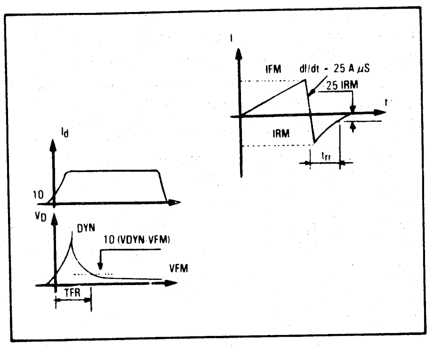


FIGURE 11 — FORWARD VOLTAGE

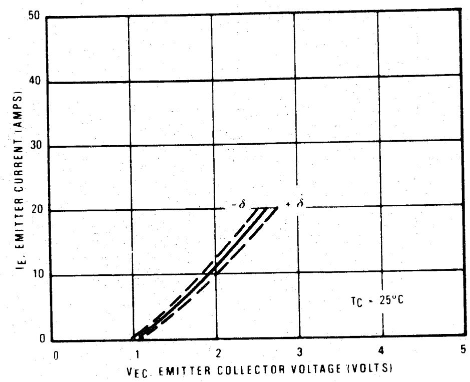


FIGURE 12 — FORWARD MODULATION VOLTAGE

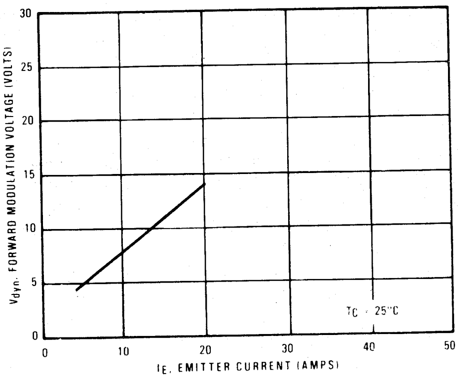


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

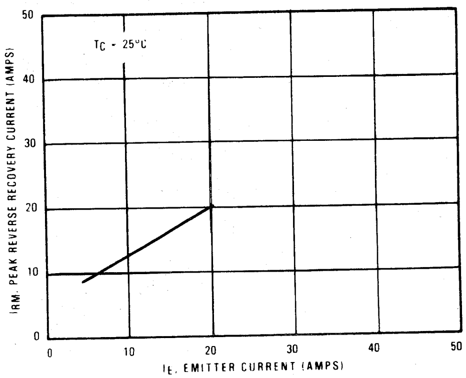


FIGURE 14 — FORWARD RECOVERY TIME

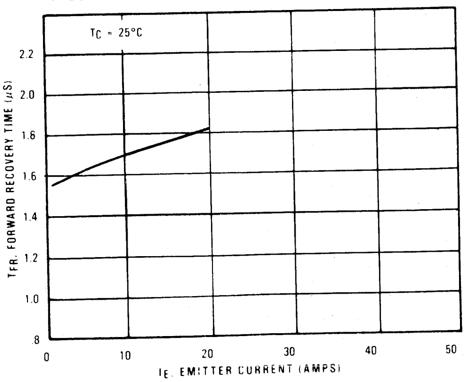
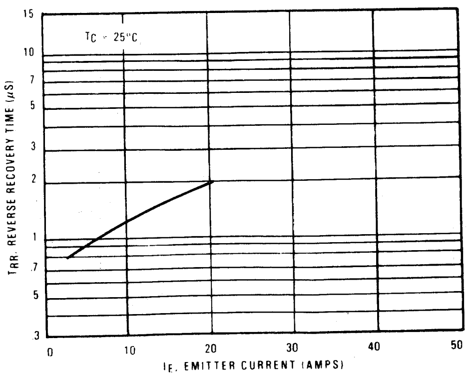


FIGURE 15 — REVERSE RECOVERY TIME



3

The Safe Operating Area figures shown in Figures 16 and 17 are specifed for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

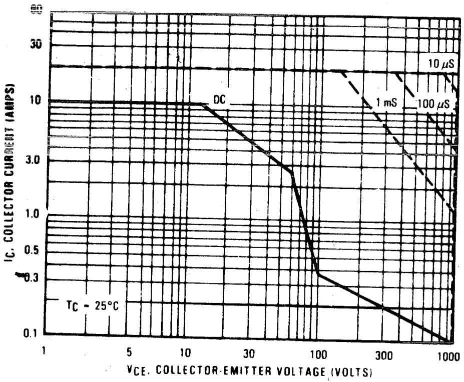
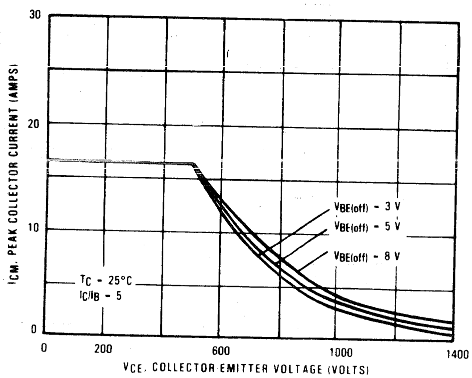


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to grater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

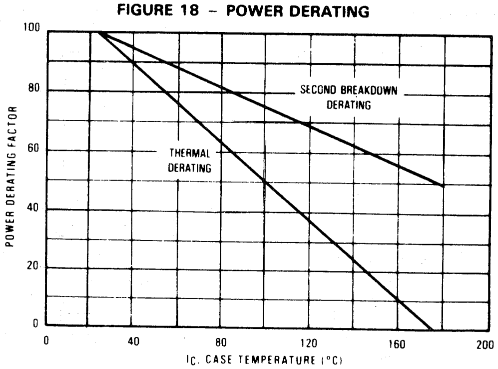
$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

3

FIGURE 18 — POWER DERATING



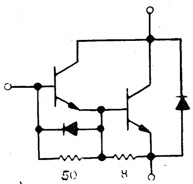
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUT33

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The BUT33 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

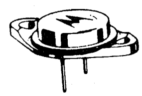
- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  800 nS Inductive Fall Time at 25°C (Typ)
  2.0 μS Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range − 65 to 200°C



56 AMPERES
NPN SILICON POWER DARLINGTON TRANSISTORS
600 VOLTS
250 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



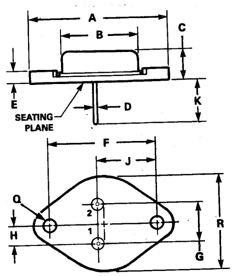
MAXIMUM RATINGS

Rating	Symbol	BUT33	Unit
Collector Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current — Continuous / — Peak (1)	I_C / I_{CM}	56 / 75	Adc
Base Current — Continuous / — Peak (1)	I_B / I_{BM}	12 / 15	Adc
Free Wheel Diode Forward current — Continuous / — Peak	I_F / I_{FM}	56 / 75	Adc
Total Power Dissipation @ T_C = 25°C / @ T_C = 100°C / Derate above 25°C	P_D	250 / 140	Watts / W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO-3

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	400	–	–	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	0.2	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100 °C)		–	–	4.0	
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	–	–	350	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17		
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				
(I_C = 20 A, V_{CE} = 5 V)		30	–	–	
(I_C = 36 A, V_{CE} = 5 V)		20	–	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 20 A, I_B = 1 A)		–	–	2.0	
(I_C = 36 A, I_B = 3.6 A)		–	–	2.5	
(I_C = 44 A, I_B = 4.4 A)		–	–	3.0	
(I_C = 56 A, I_B = 11.2 A)		–	–	5.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 20 A, I_B = 1 A)		–	–	2.5	
(I_C = 36 A, I_B = 3.6 A)		–	–	2.9	
(I_C = 44 A, I_B = 4.4 A)		–	–	3.3	
Diode Forward Voltage (I_F = 44 A)	V_f	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS
Inductive Load, Clamped (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Storage Time	T_C = 25°C; See Table 1; I_C = 36 A, I_B = 3.6 A, $V_{BE(off)}$ = 5 V	t_s	–	2.0	3.3	μs
Fall Time	T_C = 25°C	t_f	–	0.8	1.6	μs
Storage Time	T_C = 100°C	t_s	–	2.2	–	μs
Fall Time	T_C = 100°C	t_f	–	0.8	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

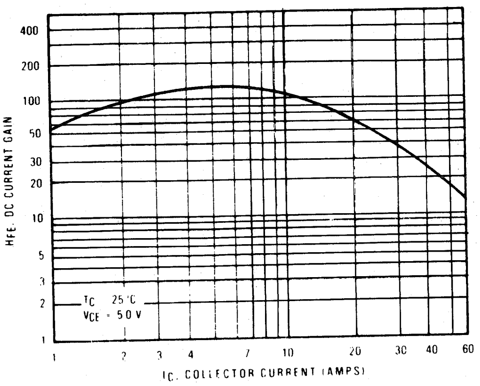


FIGURE 2 — COLLECTOR SATURATION REGION

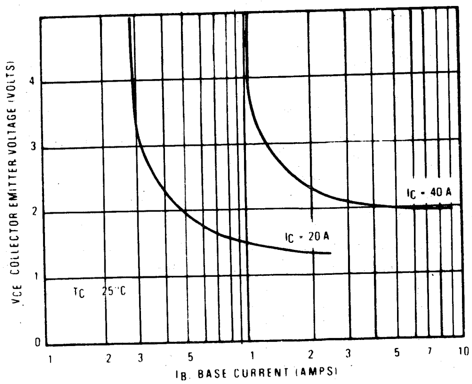


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

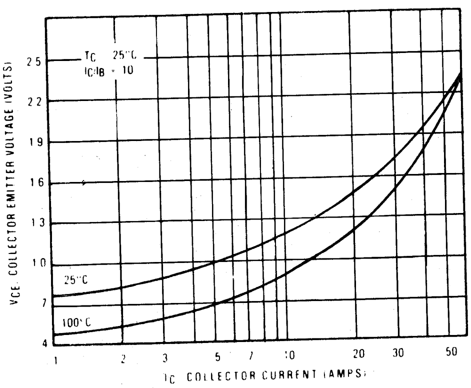


FIGURE 4 — BASE-EMITTER VOLTAGE

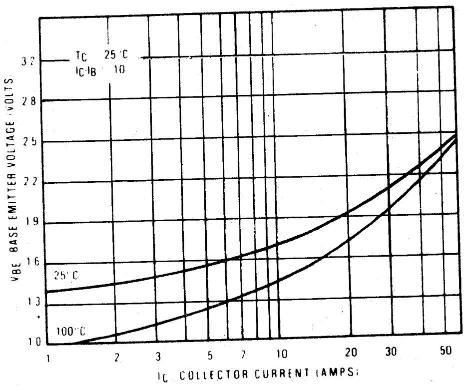


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FIGURE 5 — THERMAL RESPONSE

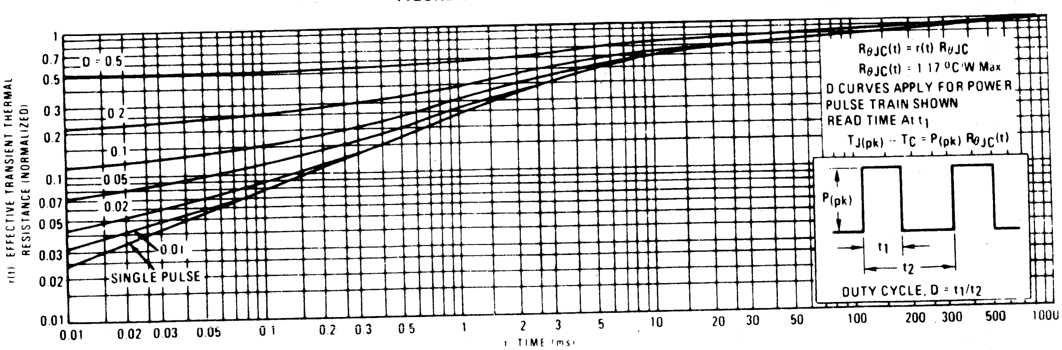


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

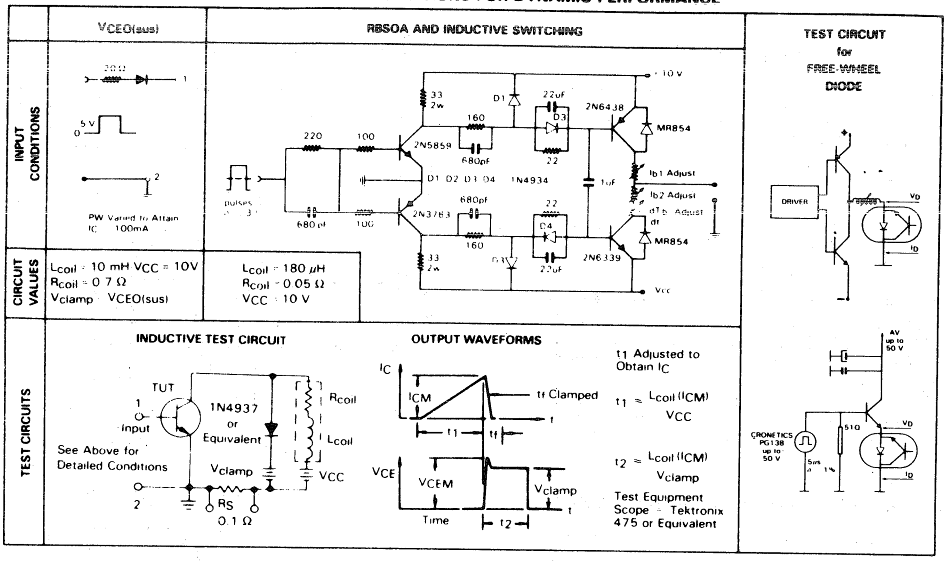


FIGURE 6 – FALL TIME vs IB2/IB1

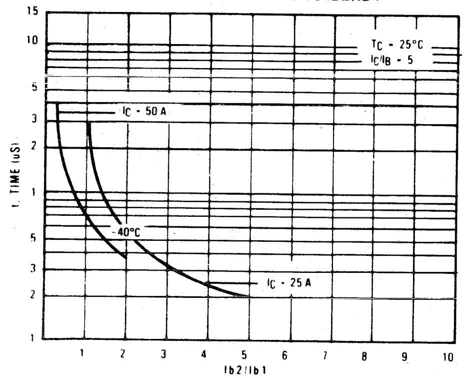


FIGURE 7 – TURN-OFF TIME vs Ic

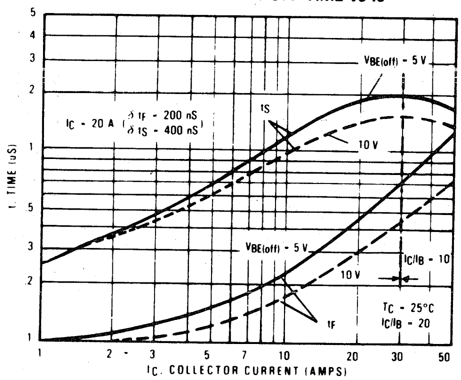


FIGURE 8 – STORAGE TIME vs FORCED GAIN

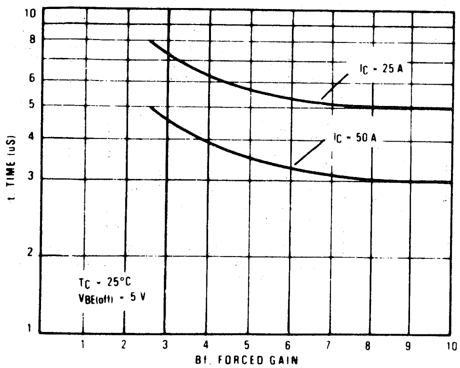
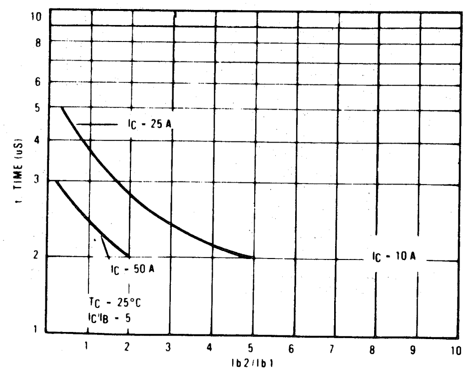


FIGURE 9 – STORAGE TIME vs Ib2/Ib1



FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

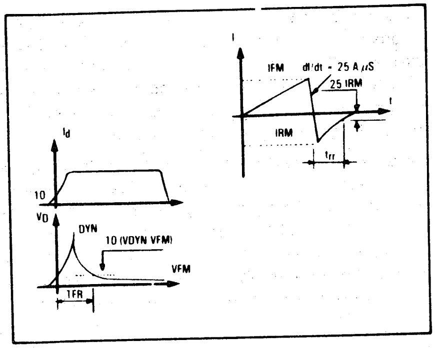


FIGURE 11 — FORWARD VOLTAGE

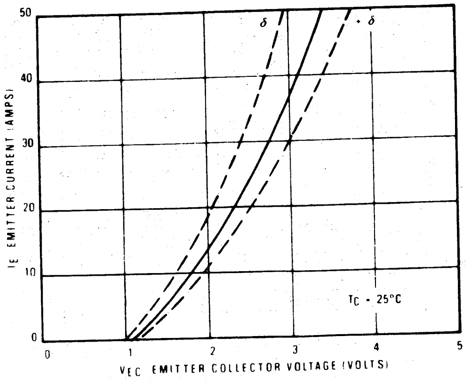


FIGURE 12 — FORWARD MODULATION VOLTAGE

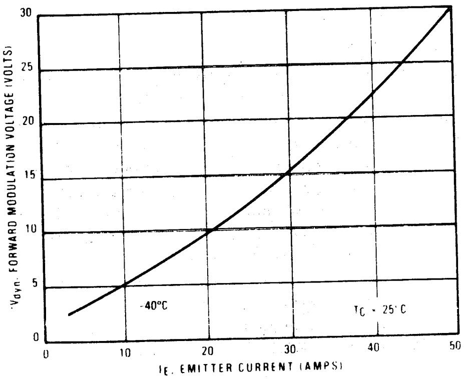


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

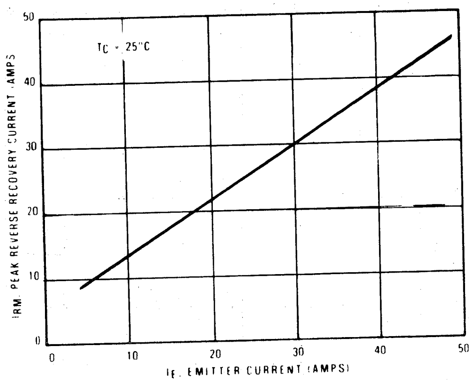


FIGURE 14 — FORWARD RECOVERY TIME

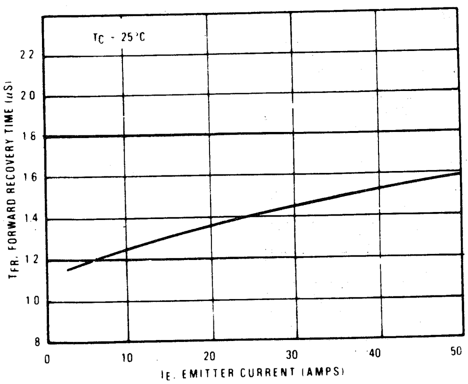
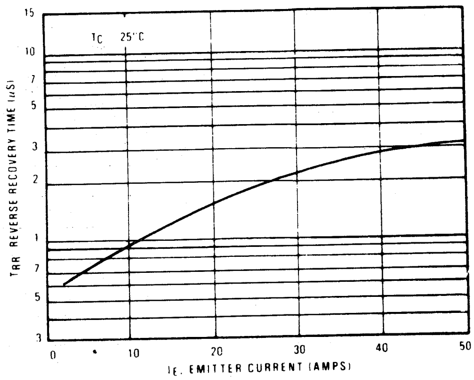


FIGURE 15 — REVERSE RECOVERY TIME



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The Safe Operating Area figures shown in Figures 16 and 17 are specifed for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

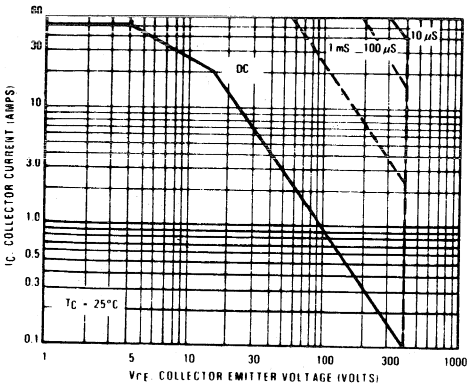
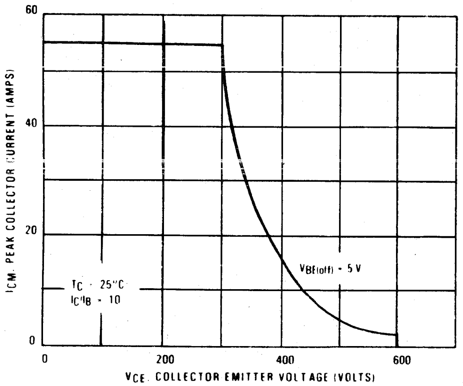


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to grater dissipation than the curves indicate.

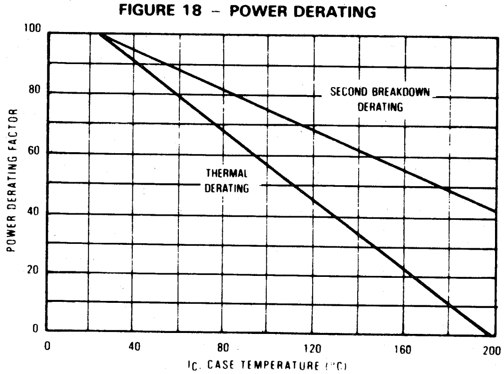
The data of Figure 16 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

FIGURE 18 — POWER DERATING



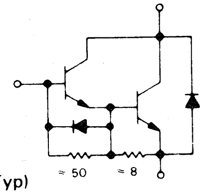
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUT34

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The BUT34 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  - 0.7 uS Inductive Fall Time at 25°C (Typ)
  - 1.8 uS Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range −65 to 200°C



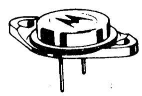
50 AMPERES

NPN SILICON POWER DARLINGTON TRANSISTORS

850 VOLTS
250 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



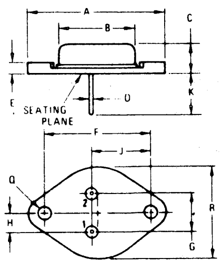
MAXIMUM RATINGS

Rating	Symbol	BUT34	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	500	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	50 75	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	10 15	Adc
Free Wheel Diode: Forward current – Continuous – Peak	I_F I_{FM}	50 75	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 140	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	-	39.37	–	1 550
B	-	21.08		0.830
C	6.35	7 62	0.250	0.300
D	0.99	1 09	0.039	0.043
E	–	3.43		0.135
F	29 90	30.40	1 177	1.197
G	10.67	11 18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17 15	0.655	0.675
K	11.18	12.19	0 440	0 480
Q	3.84	4.09	0 151	0.161
R		26.67	-	1 050

CASE 197-01
MODIFIED TO-3

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	500	–	–	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	0.2	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	4.0	
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	–	–	350	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17		
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				
(I_C = 16 A, V_{CE} = 5 V)		30	–	–	
(I_C = 32 A, V_{CE} = 5 V)		15	–	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 16 A, I_B = 0.8 A)		–	–	2.0	
(I_C = 32 A, I_B = 3.2 A)		–	–	3.0	
(I_C = 40 A, I_B = 4 A)		–	–	3.5	
(I_C = 50 A, I_B = 10 A)		–	–	5.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 16 A, I_B = 0.8 A)		–	–	2.5	
(I_C = 32 A, I_B = 3.2 A)		–	–	2.9	
(I_C = 40 A, I_B = 4 A)		–	–	3.3	
Diode Forward Voltage (I_F = 40 A)	V_f	–	–	4.0	Vdc

40°C

SWITCHING CHARACTERISTICS
Inductive Load, Clamped (Table 1)

Characteristic	Temperature	Conditions	Symbol	Min	Typ	Max	Unit
Storage Time	T_C = 25°C	See Table 1	t_s	–	1.8	3.0	µs
Fall Time		I_C = 32 A	t_f	–	0.7	1.5	µs
Storage Time	T_C = 100°C	I_{B1} = 3.2 A	t_s	–	2.2	–	µs
Fall Time		$V_{BE(off)}$ = 5 V	t_f	–	0.8	–	µs

(1) Pulse Test: PW = 300 µs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

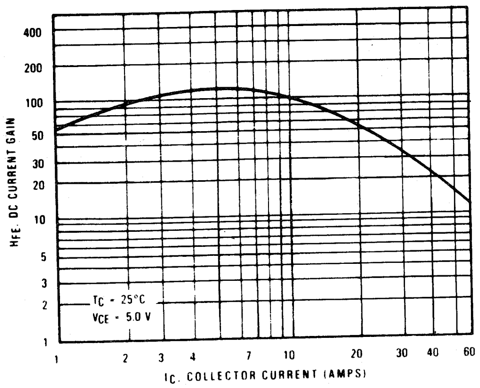


FIGURE 2 — COLLECTOR SATURATION REGION

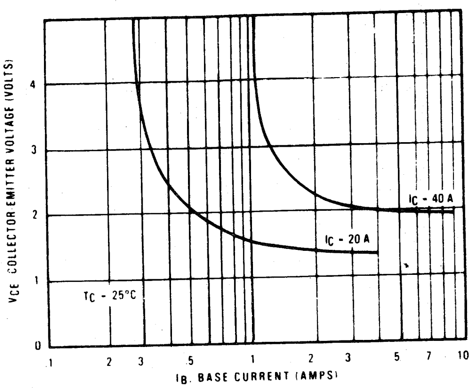


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

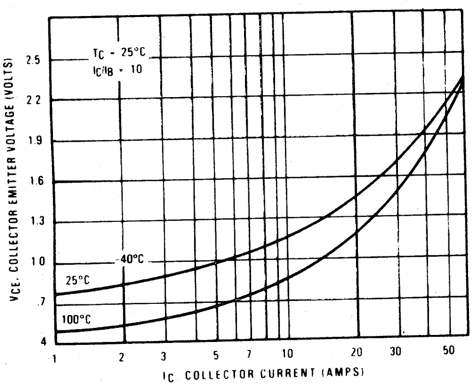


FIGURE 4 — BASE-EMITTER VOLTAGE

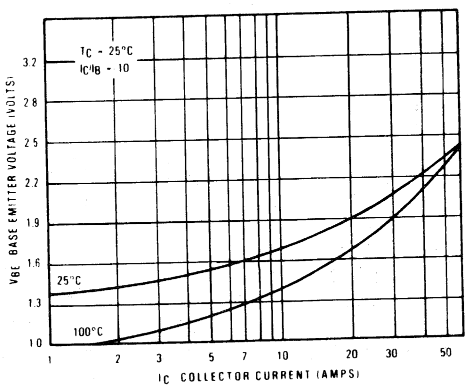


FIGURE 5 — THERMAL RESPONSE

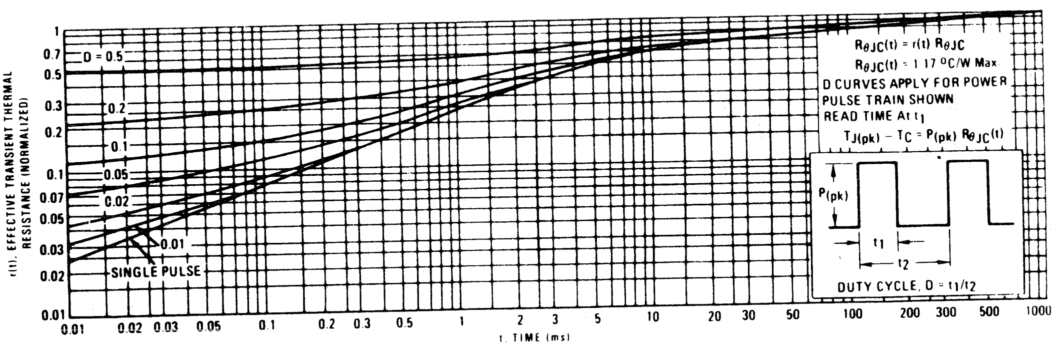


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TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

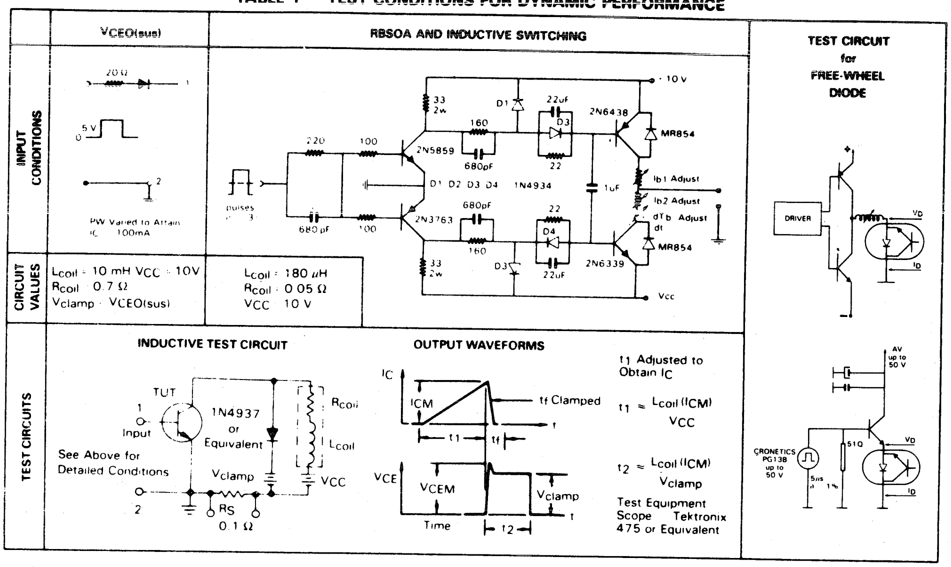


FIGURE 6 – FALL TIME vs IB2/IB1

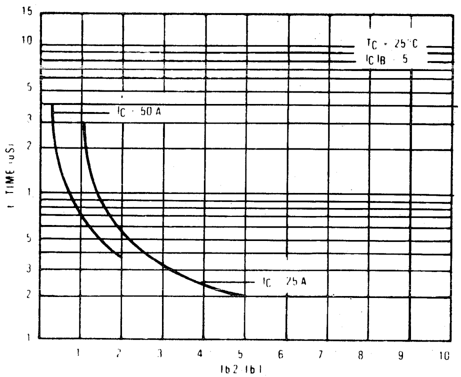


FIGURE 7 – TURN-OFF TIME vs Ic

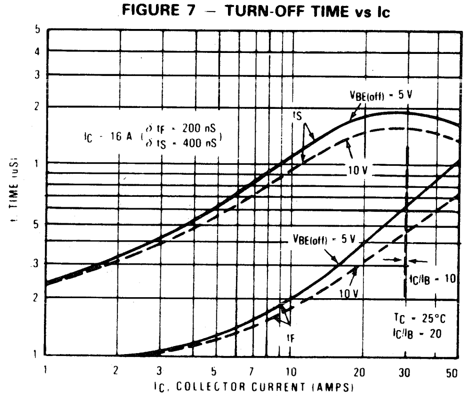


FIGURE 8 – STORAGE TIME vs FORCED GAIN

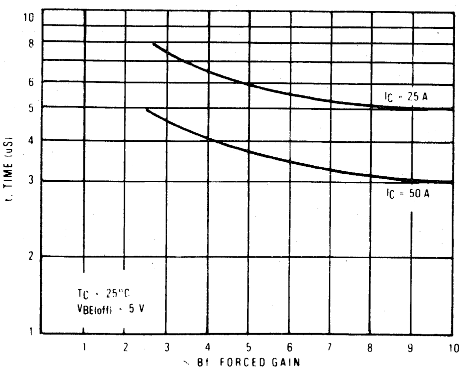
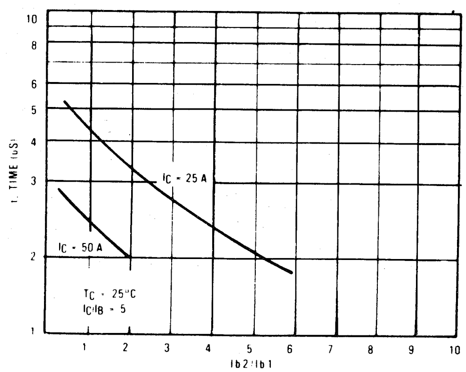


FIGURE 9 – STORAGE TIME vs Ib2/Ib1



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FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

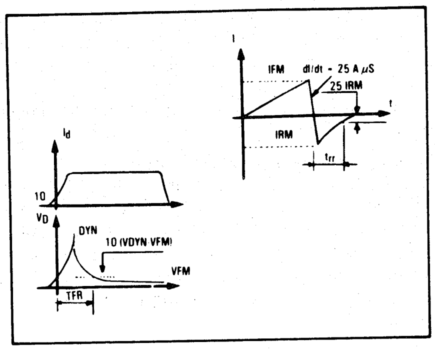


FIGURE 11 — FORWARD VOLTAGE

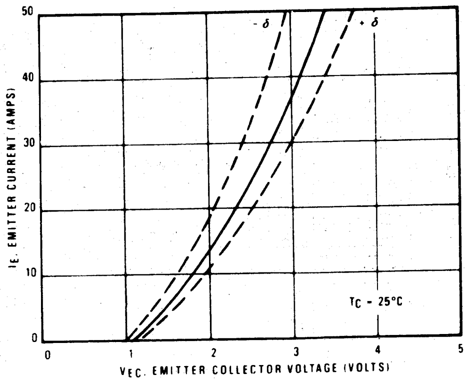


FIGURE 12 — FORWARD MODULATION VOLTAGE

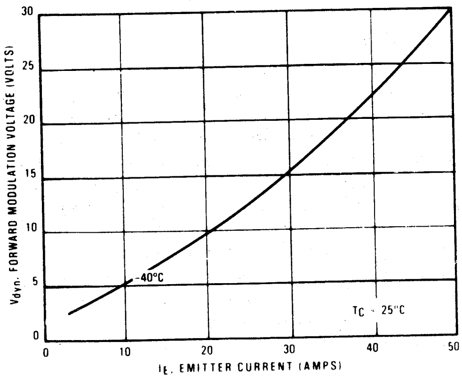


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

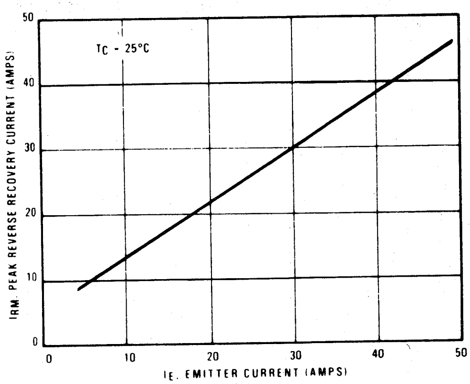


FIGURE 14 — FORWARD RECOVERY TIME

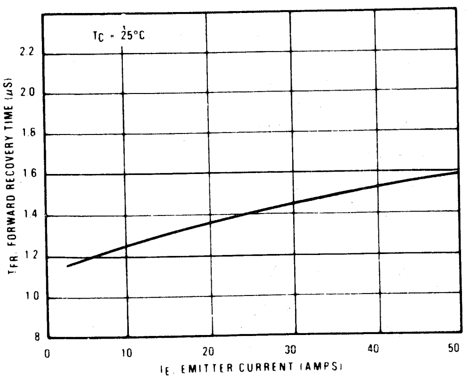
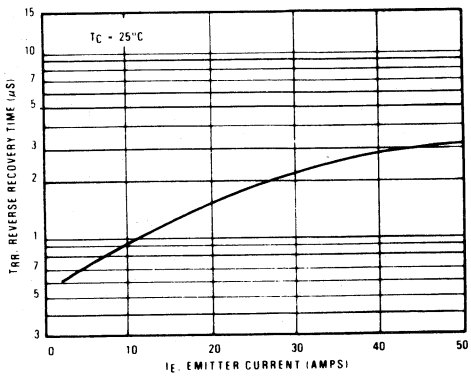


FIGURE 15 — REVERSE RECOVERY TIME



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The Safe Operating Area figures shown in Figures 16 and 17 are specifed for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

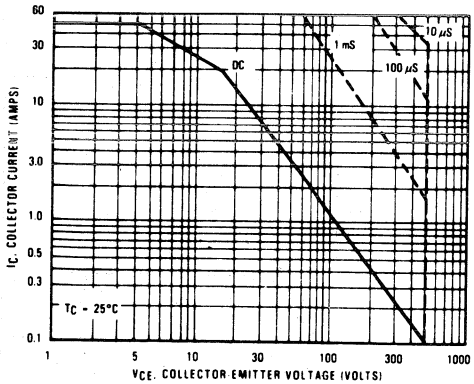
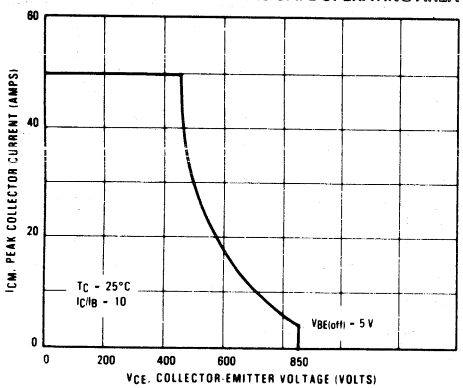


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to grater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

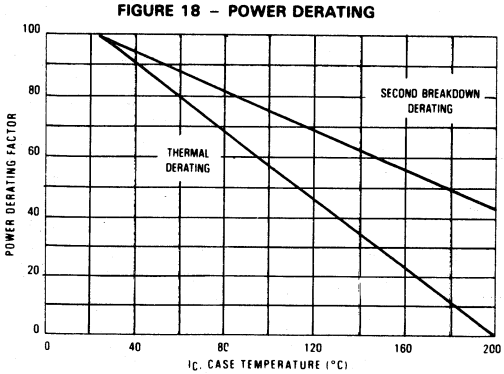
$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

3

FIGURE 18 — POWER DERATING



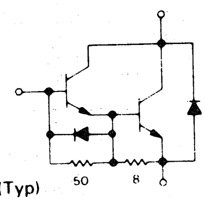
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUT35

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The BUT35 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

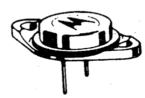
- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  - 550 nS Inductive Fall Time at 25°C (Typ)
  - 2.5 uS Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range −65 to 200°C



40 AMPERES
NPN SILICON POWER DARLINGTON TRANSISTORS
1000 VOLTS
250 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



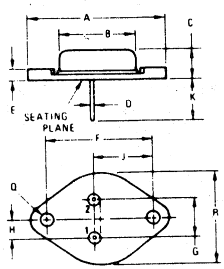
MAXIMUM RATINGS

Rating	Symbol	BUT35	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector-Emitter Voltage 40°C	V_{CEV}	1000	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	40 50	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	10 20	Adc
Free Wheel Diode: Forward current Continuous Peak	I_F I_{FM}	40 50	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 140	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	·	21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	·	3.43		0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R		26.67		1.050

CASE 197-01
MODIFIED TO-3

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	700	–	–	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	0.2	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	4.0	
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	–	–	350	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17		
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				
(I_C = 12 A, V_{CE} = 5 V)		30	–	–	
(I_C = 24 A, V_{CE} = 5 V)		15	–	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 12 A, I_B = 0.6 A)		–	–	2.0	
(I_C = 24 A, I_B = 2.4 A)		–	–	3.0	
(I_C = 32 A, I_B = 3.2 A)		–	–	3.5	
(I_C = 40 A, I_B = 8 A)		–	–	5.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 12 A, I_B = 0.6 A)		–	–	2.5	
(I_C = 24 A, I_B = 2.4 A)		–	–	2.9	
(I_C = 32 A, I_B = 3.2 A)		–	–	3.3	
Diode Forward Voltage (I_F = 32 A)	V_f	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS
Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	T_C = 25°C	See Table 1	t_s	–	–	4.0	μs
Fall Time		I_C = 24 A	t_f	–	–	1.2	μs
Storage Time	T_C = 100°C	I_{B1} = 2.4 A	t_s	–	2.8	–	μs
Fall Time		$V_{BE(off)}$ = 5 V	t_f	–	0.65	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

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TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

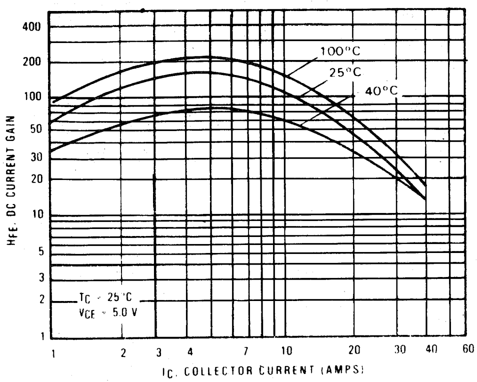

FIGURE 2 — COLLECTOR SATURATION REGION

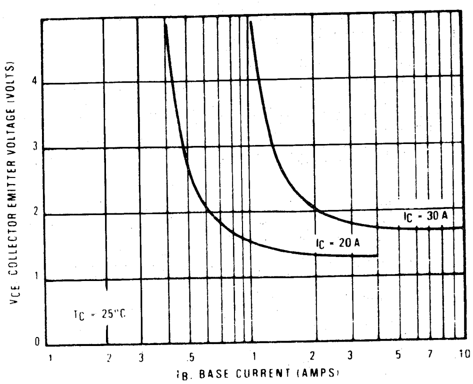

FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

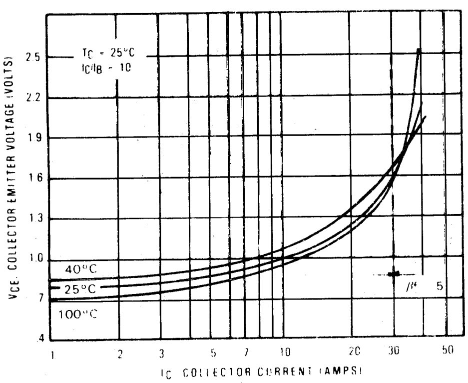

FIGURE 4 — BASE-EMITTER VOLTAGE

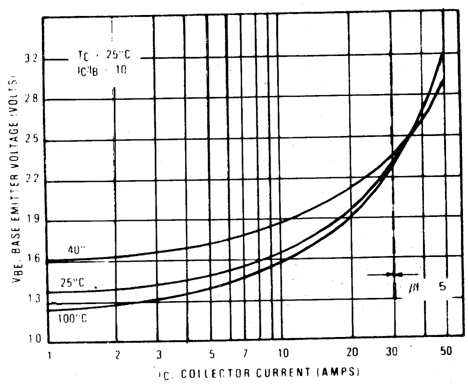

FIGURE 5 — THERMAL RESPONSE

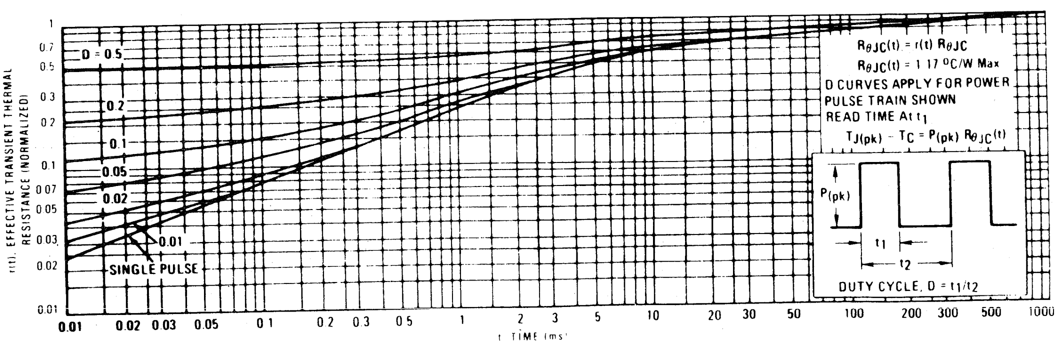

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TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

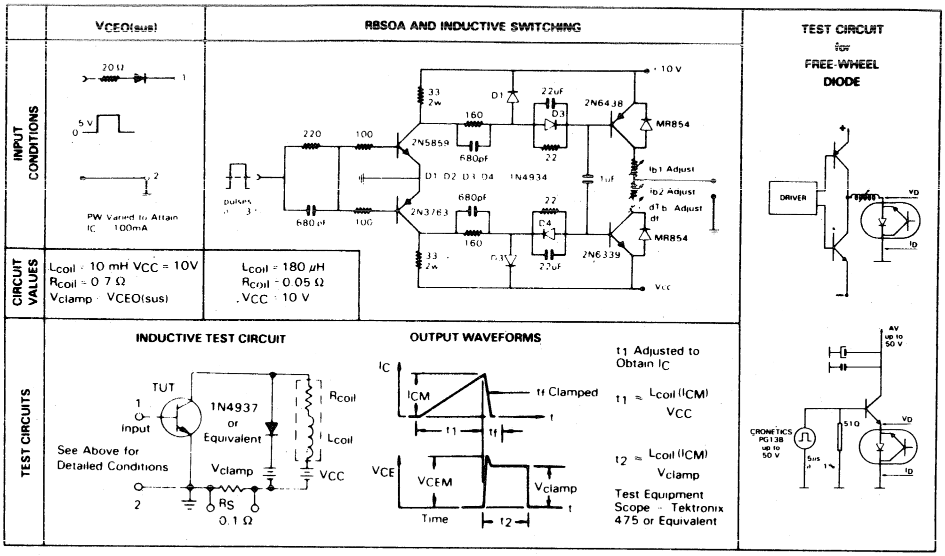


FIGURE 6 – FALL TIME vs IB2/IB1

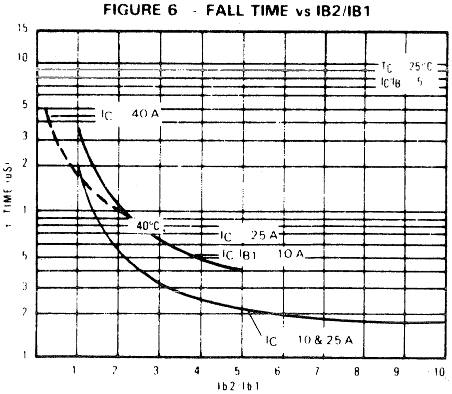


FIGURE 7 – TURN-OFF TIME vs Ic

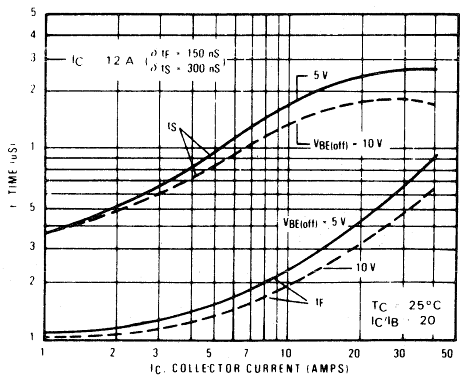


FIGURE 8 – STORAGE TIME vs FORCED GAIN

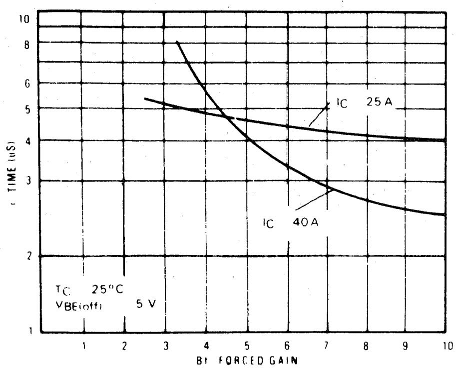
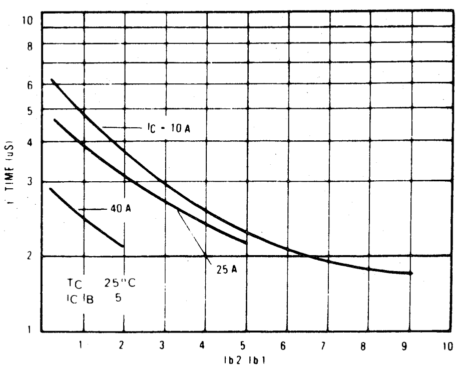


FIGURE 9 – STORAGE TIME vs Ib2/Ib1



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FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

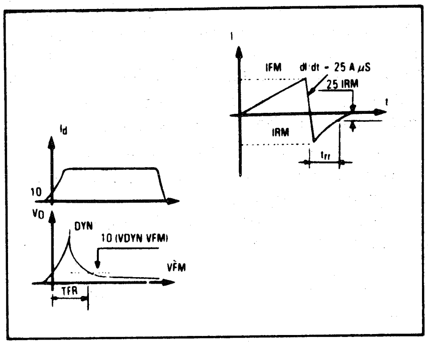


FIGURE 11 — FORWARD VOLTAGE

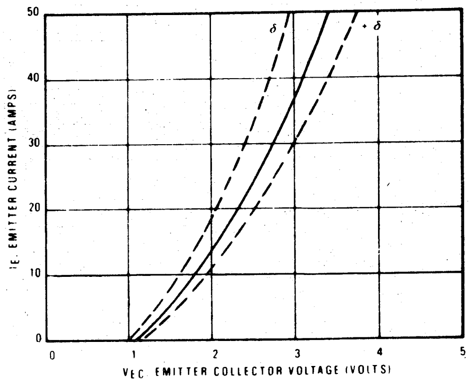


FIGURE 12 — FORWARD MODULATION VOLTAGE

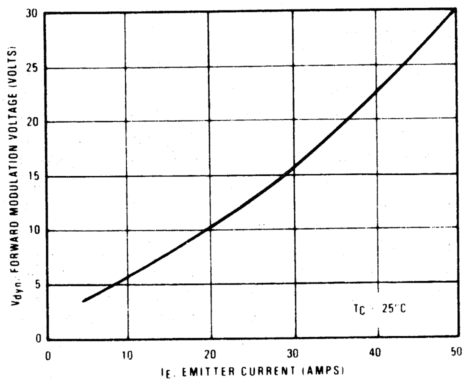


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

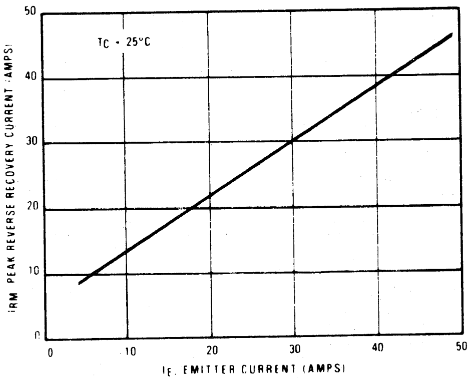


FIGURE 14 — FORWARD RECOVERY TIME

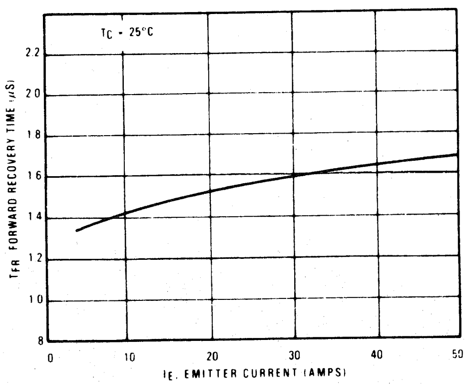
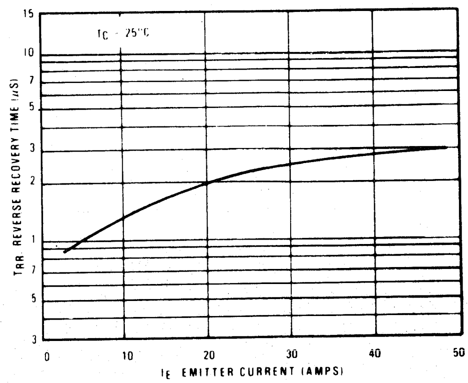


FIGURE 15 — REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specifed for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

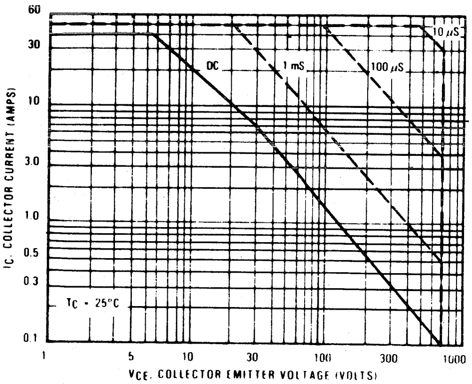
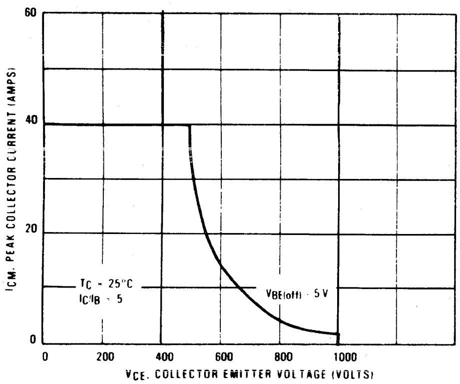


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to grater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

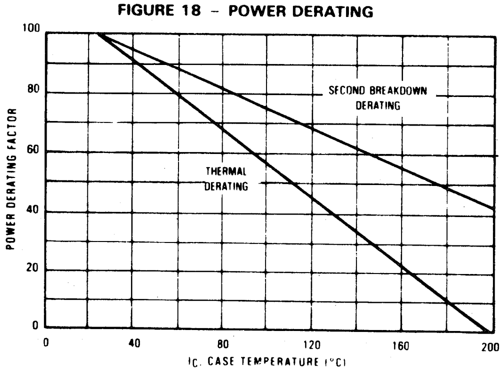
$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

3

FIGURE 18 – POWER DERATING



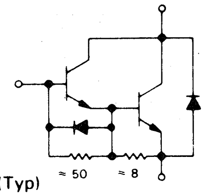
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUT36

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The BUT36 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  1.7 uS Inductive Fall Time at 100°C (Typ)
  4.5 uS Inductive Storage Time at 100°C (Typ)
- Operating Temperature Range −65 to 175°C



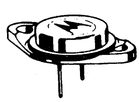
24 AMPERES

NPN SILICON POWER DARLINGTON TRANSISTORS

1400 VOLTS
250 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data − representing device characteristics boundaries − are given to facilitate "worst case" design.



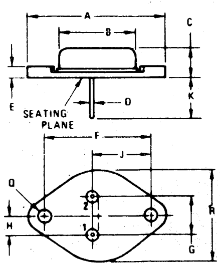
MAXIMUM RATINGS

Rating	Symbol	BUT36	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	1000	Vdc
Collector-Emitter Voltage	V_{CEV}	1400	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current − Continuous − Peak (1)	 I_C I_{CM}	 24 40	Adc
Base Current − Continuous − Peak (1)	 I_B I_{BM}	 15 20	Adc
Free Wheel Diode: Forward current − Continuous − Peak	 I_F I_{FM}	 24 40	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 125	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≦ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	−	39.37	−	1.550
B	−	21.08	−	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	−	3.43	−	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R		26.67	−	1.050

CASE 197-01
MODIFIED TO-3

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	1000	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	0.2	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100 °C)		–	–	4.0	
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	–	–	350	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 8 A, V_{CE} = 5 V)	h_{FE}	20	–	–	
(I_C = 16 A, V_{CE} = 5 V)		5	–	–	
Collector-Emitter Saturation Voltage (I_C = 24 A, I_B = 12 A)	$V_{CE(sat)}$	–	–	5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 16 A, I_B = 3.2 A)	$V_{BE(sat)}$	–	–	3.3	Vdc
Diode Forward Voltage (I_F = 24 A)	V_f	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS
Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	T_C = 25°C	See Table 1	t_s	–	–	6.0	μs
Fall Time		I_C = 16 A	t_f	–	–	2.5	μs
Storage Time	T_C = 100°C	I_{B1} = 3.2 A	t_s	–	4.5	–	μs
Fall Time		$V_{BE(off)}$ = 5 V	t_f	–	1.7	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

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TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

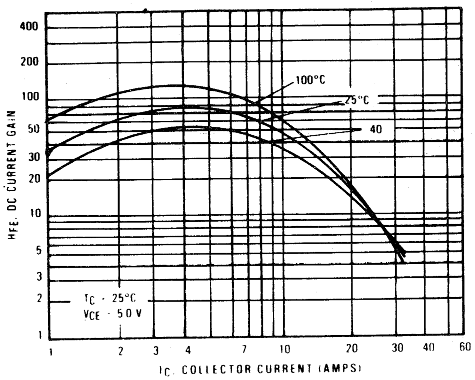

FIGURE 2 — COLLECTOR SATURATION REGION

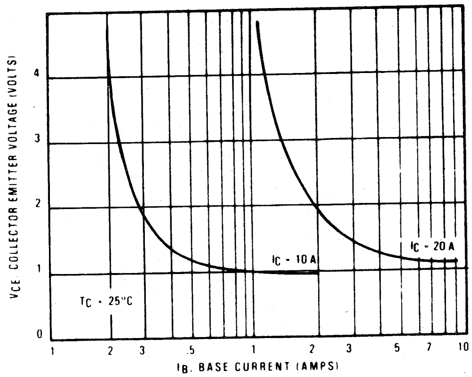

FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

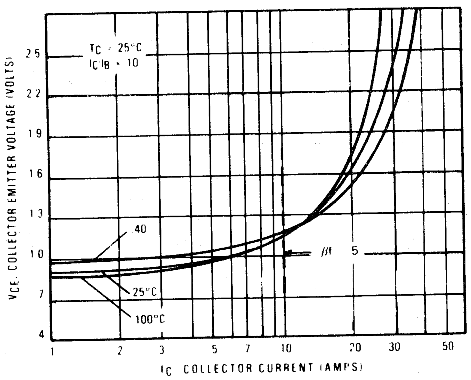

FIGURE 4 — BASE-EMITTER VOLTAGE

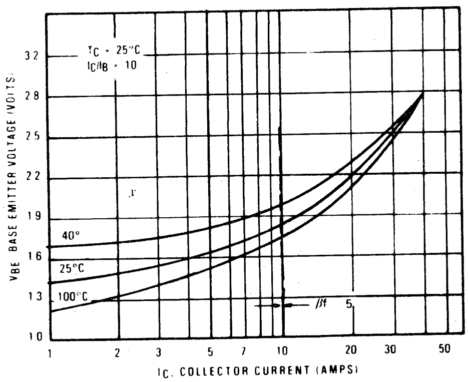

FIGURE 5 — THERMAL RESPONSE

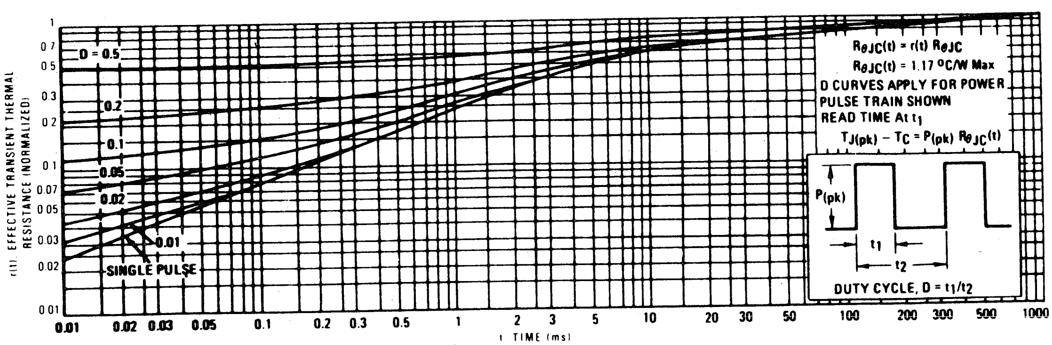

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TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

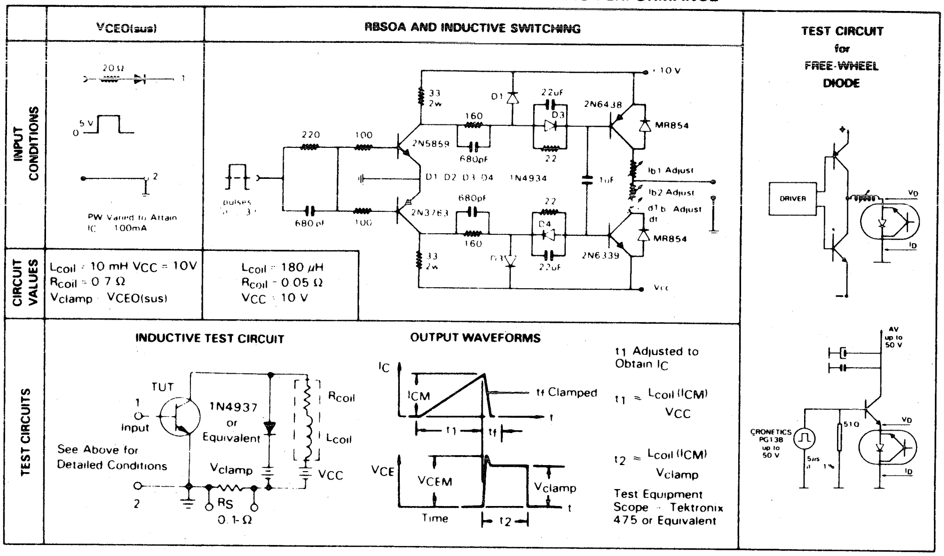


FIGURE 6 — FALL TIME vs IB2/IB1

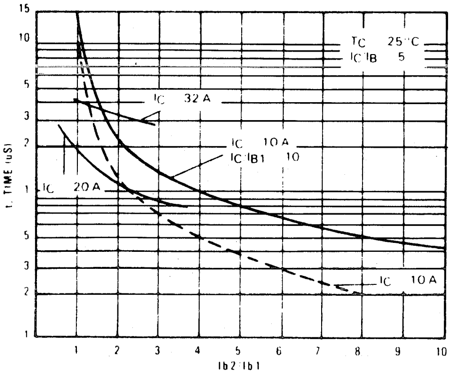


FIGURE 7 — TURN-OFF TIME vs Ic

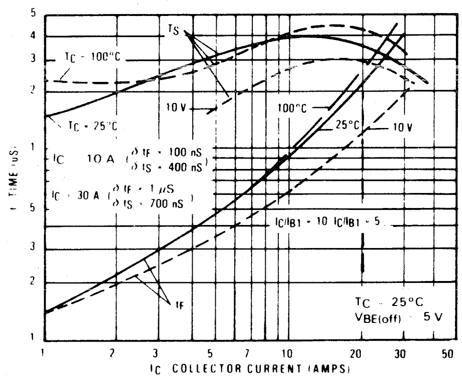


FIGURE 8 — STORAGE TIME vs FORCED GAIN

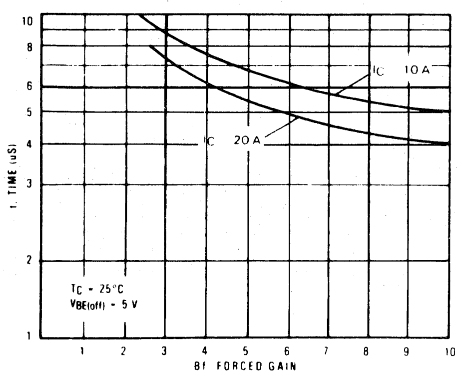
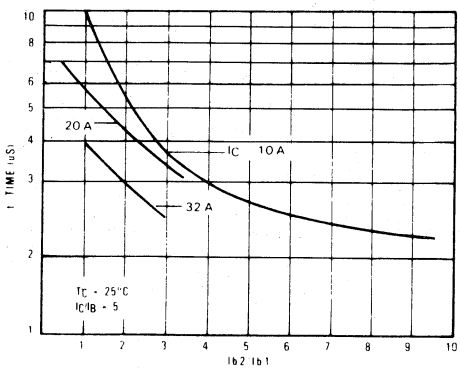


FIGURE 9 — STORAGE TIME vs Ib2/Ib1



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FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

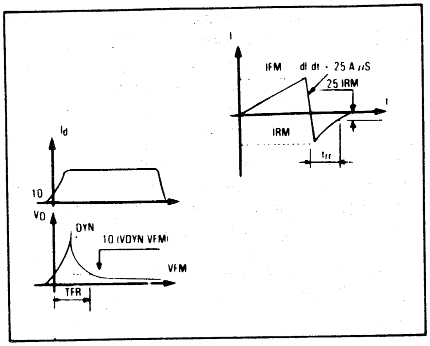


FIGURE 11 — FORWARD VOLTAGE

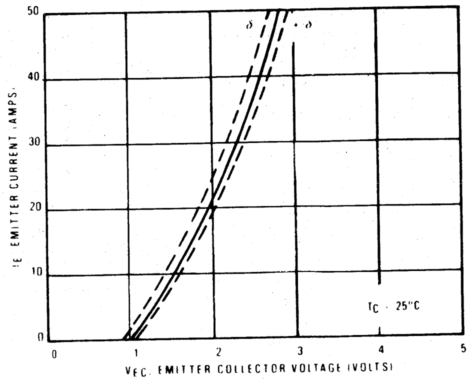


FIGURE 12 — FORWARD MODULATION VOLTAGE

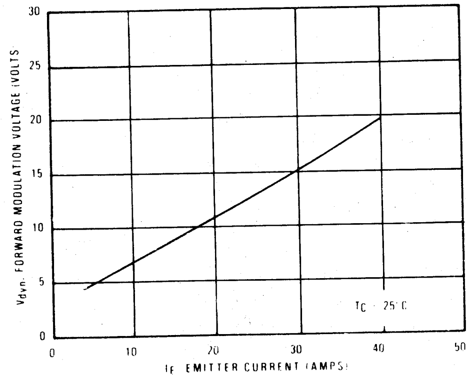


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

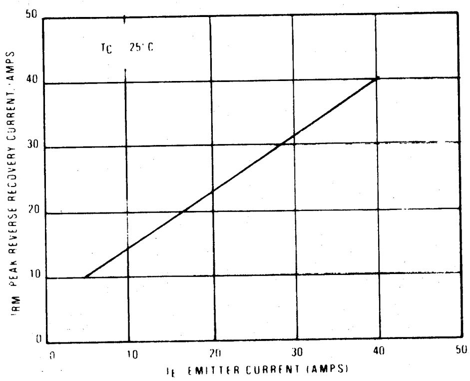


FIGURE 14 — FORWARD RECOVERY TIME

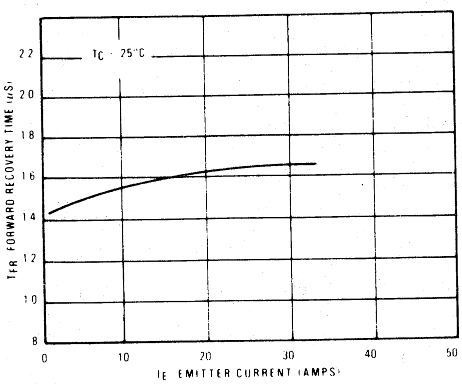
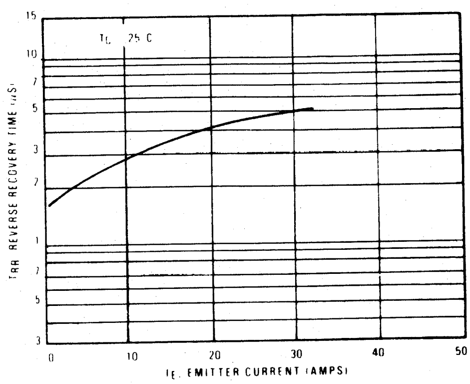


FIGURE 15 — REVERSE RECOVERY TIME



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The Safe Operating Area figures shown in Figures 16 and 17 are specifed for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

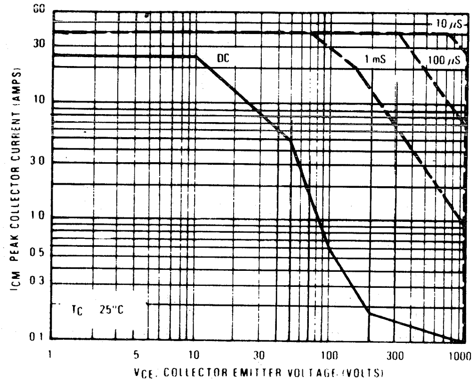
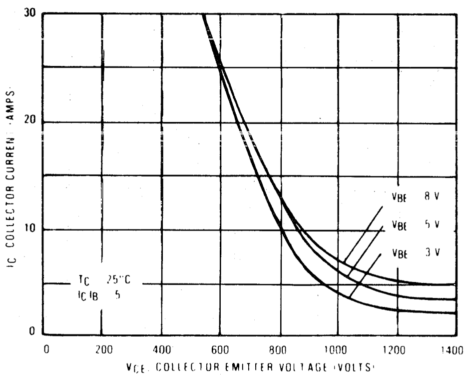


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to grater dissipation than the curves indicate.

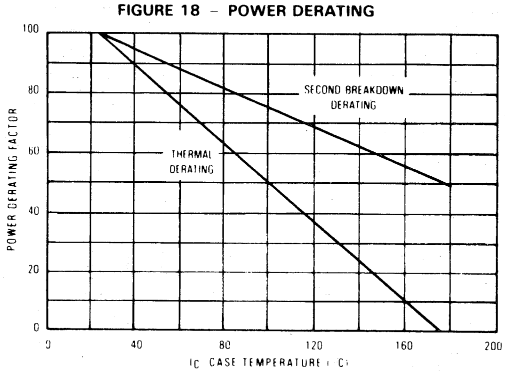
The data of Figure 16 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

FIGURE 18 — POWER DERATING



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUT50P

ADVANCE INFORMATION

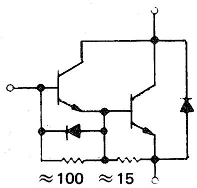
8 AMPERES
NPN SILICON
POWER DARLINGTON TRANSISTORS

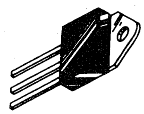
500 VOLTS – $V_{ceo(sus)}$
100 WATTS
850 VOLTS – V_{ces}

SWITCHMODE▲ SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The BUT50P darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switch-mode applications such as :

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits





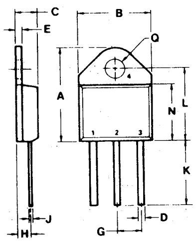
MAXIMUM RATINGS

Rating	Symbol	BUT50P	Unit
Collector-Emiter Voltage	$V_{CEO(sus)}$	500	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	850	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	8	Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	8 16	Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2 4	Adc
Free Wheel Diode : Forward Current – continous – peak	I_F I_{FM}	8 16	Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	100 40 .8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1.
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.156	0.165

Case 340-01
TO-218AC

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	500	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C	I_{CEV}	– –	– –	0.25 2.5	mAdc
Emitter Cutoff Current (V_{EB} = 8.0 V, I_C = 0)	I_{EBO}	–	–	175	mAdc

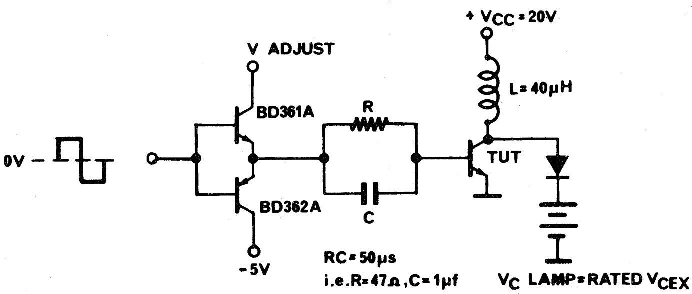
ON CHARACTERISTICS (1)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Current Gain (I_c = 2 Adc, V_{ce} = 5 V)	h_{FE}	30	–	–	–
Collector-Emitter Saturation Voltage (I_c = 5 Adc, I_b = 0.25 Adc) (I_c = 8 Adc, I_b = 1 Adc) (I_c = 5 Adc, I_b = 0.25 Adc, T_c = 100°C)	$V_{CE(sat)}$	– – –	– – –	2.0 3.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_c = 5 Adc, I_b = 0.25 Adc) (I_c = 5 Adc, I_b = 0.25 Adc, T_c = 100°C)	$V_{BE(sat)}$	– –	– –	2.5 2.5	Vdc
Diode Forward Voltage (I_F = 5 Adc)	V_f	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS
Inductive Load, Clamped

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Storage Time	(I_c = 5 A, Ib_1 = 0.25 A, Vbe(off) = 5 V)	t_s	–	0.75	–	μs
Fall Time		t_f	–	0.10	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%



SWITCHING TIMES TEST CIRCUIT

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

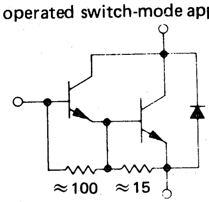
BUT51P

ADVANCE INFORMATION

SWITCHMODE▲ SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

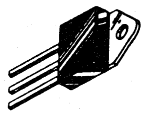
The BUT51P darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switch-mode applications such as :

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



15 AMPERES
NPN SILICON
POWER DARLINGTON TRANSISTORS

500 VOLTS-$V_{ceo(sus)}$
100 WATTS
850 VOLTS—V_{ces}



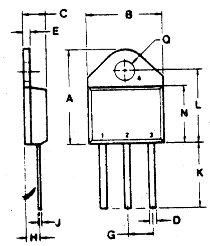
MAXIMUM RATINGS

Rating	Symbol	BUT51P	Unit
Collector-Emiter Voltage	$V_{CEO(sus)}$	500	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	850	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	8	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 25	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5	Adc
Free Wheel Diode : Forward Current — continous — peak	 I_F I_{FM}	 15 25	Adc
Total Power Dissipation @ T_C=25°C @ T_C=100°C Derate above 25°C	P_D	125 50 1	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

Case 340-01
TO-218AC

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUV10N

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

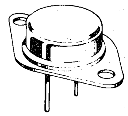
. . . designed for high current, high speed, high power applications.

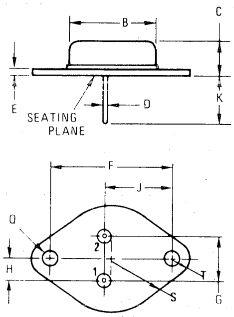
- HFe min.: 20 at Ic = 10 A
- T_F max. = 0.45 μs at Ic = 15 A
- Equivalent to BDY58

25 AMPERES

NPN SILICON POWER METAL TRANSISTOR

125 VOLTS
175 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E		3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

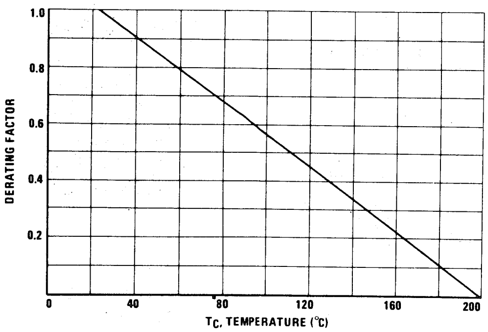
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	125	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	160	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	140	Vdc
Collector-Current — continuous — peak (pw ⩽ 10 ms)	I_C I_{CM}	25 30	Adc Apk
Base-Current continuous	I_B	6	Adc
Total Power Dissipation @ $T_C = 25°C$	P_D	175	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W

FIGURE 1 — POWER DERATING



3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, L = 25 mH)	$V_{CEO(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Biais: ($V_{CE} = 160$ V, $V_{BE} = -1.5$ V) ($V_{CE} = 160$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)	I_{CEX}		1.5 6	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 100$ V)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		0.5	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 20$ V, t = 0.5 s) ($V_{CE} = 48$ V, t = 0.5 s)	$I_{S/b}$	8.75 1.0		Adc
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 10$ A, $V_{CE} = 4$ V) ($I_C = 20$ A, $V_{CE} = 4$ V)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 10$ A, $I_B = 1$ A) ($I_C = 20$ A, $I_B = 2$ A)	$V_{CE(sat)}$		1 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10$ A, $I_B = 1$ A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product ($V_{CE} = 15$ V, $I_C = 1$ A, f = 4 MHz)	f_T	10.0		MHz

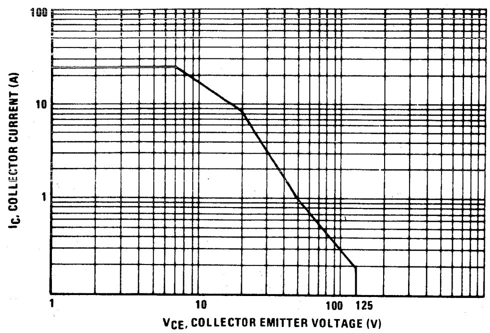
SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 15$ A, $I_{B1} = I_{B2} = 1.5$ A, ($V_{CC} = 75$ V, RC = 5 Ω)	t_{on}		1.0	μs
Storage Time		t_s		1.55	
Fall Time		t_f		0.45	

3

1 Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩽2%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data of figure 2 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.
At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

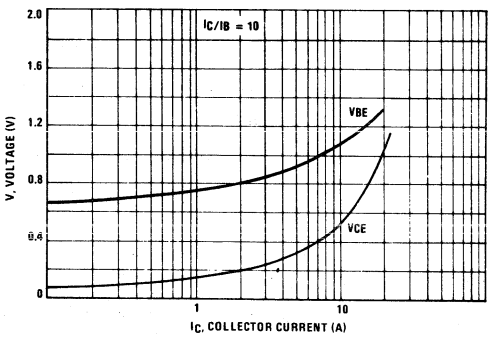


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

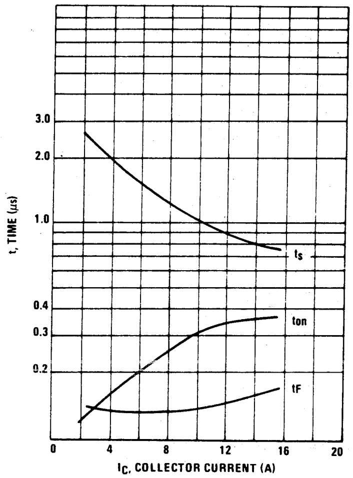


FIGURE 4 – DC CURRENT GAIN

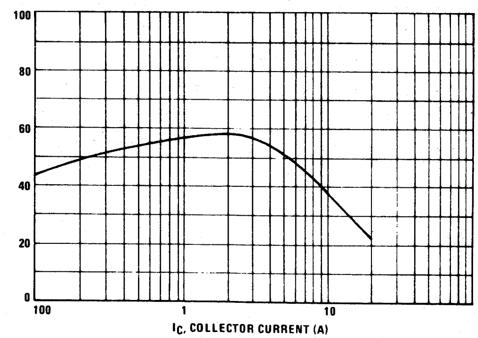
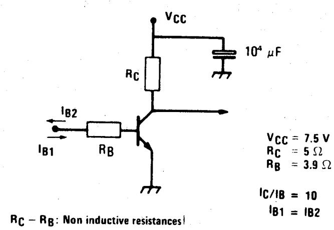


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUV11

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

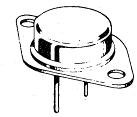
. . . designed for high current, high speed, high power applications.

- High DC current gain: HFE min. = 20 at Ic = 6 A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 0.6 V at Ic = 6 A
- Very fast switching times:
  T_F max. = 0.8 μs at Ic = 12 A

20 AMPERES

NPN SILICON POWER METAL TRANSISTOR

200 VOLTS
150 WATTS



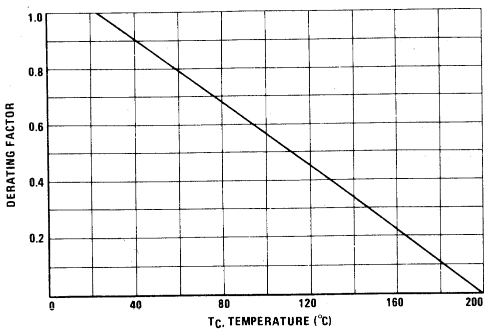
MAXIMUM RATINGS

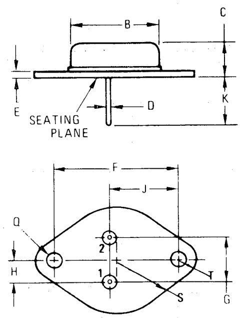
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector-Base Voltage	V_{CBO}	250	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	250	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	240	Vdc
Collector-Current — continuous — peak (pw ≤ 10 ms)	I_C I_{CM}	20 25	Adc Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ $T_C = 25°C$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR
STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE-EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, $L = 25$ mH)	$V_{CEO(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Biais: ($V_{CE} = 250$ V, $V_{BE} = -1.5$ V)	I_{CEX}		1.5	mAdc
($V_{CE} = 250$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)			6	
Collector-Emitter Cutoff Current ($V_{CE} = 160$ V)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 30$ V, $t = 1$ s)	$I_{S/b}$	5.0		Adc
($V_{CE} = 140$ V, $t = 1$ s)		0.15		
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 6$ A, $V_{CE} = 2$ V)	h_{FE}	20	60	
($I_C = 12$ A, $V_{CE} = 4$ V)		10		
Collector-Emitter Saturation Voltage ($I_C = 6$ A, $I_B = 0.6$ A)	$V_{CE(sat)}$		0.6	Vdc
($I_C = 12$ A, $I_B = 1.5$ A)			1.5	
Base-Emitter Saturation Voltage ($I_C = 12$ A, $I_B = 1.5$ A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product ($V_{CE} = 15$ V, $I_C = 1$ A, $f = 4$ MHz)	f_T	8.0		MHz

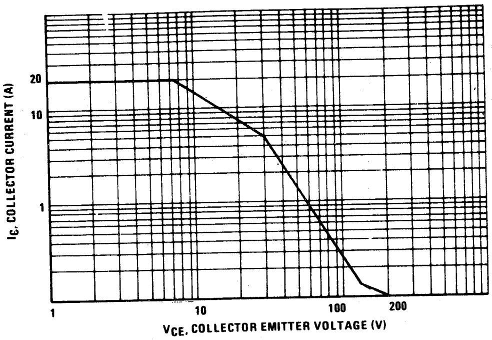
3

SWITCHING CHARACTERISTICS (Resistive Load)

		Symbol	Min.	Max.	Unit
Turn on Time	$I_C = 12$ A, $I_{B1} = I_{B2} = 1.5$ A, ($V_{CC} = 150$ V, $R_C = 12.5\ \Omega$)	t_{on}		0.8	μs
Storage Time		t_s		1.8	
Fall Time		t_f		0.4	

[1] Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩽2%.

FIG'IRE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

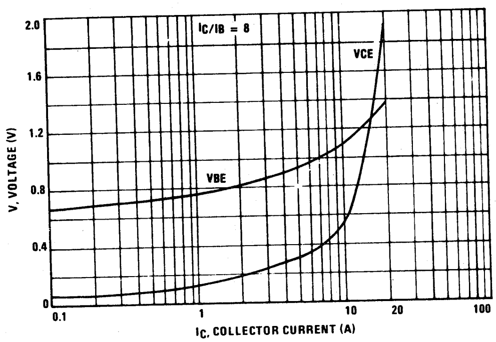


FIGURE 4 – DC CURRENT GAIN

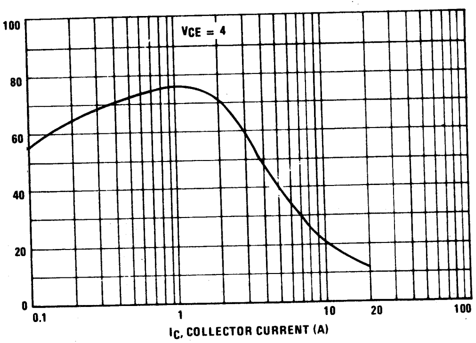


FIGURE 5 -- SWITCHING TIMES VERSUS COLLECTOR CURRENT

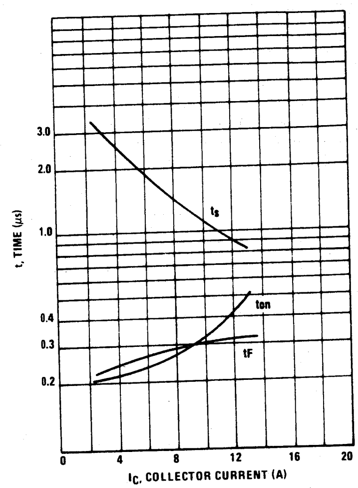
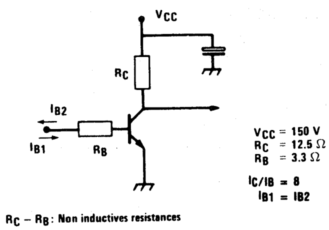


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

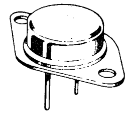
BUV11N

NPN SILICON POWER METAL TRANSISTOR

. . . designed for high speed, high current, high power applications.

- High DC Current gain — H_{FE} min 20 @ I_C = 8 A
- Very fast switching times
  t_F max. = 0.25 μs @ I_C = 15 A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$ max. = 0.6 V, @ I_C = 8A
- High V_{CEO}: 160 V.

NPN SILICON
POWER
METAL TRANSISTOR
20 AMPERES



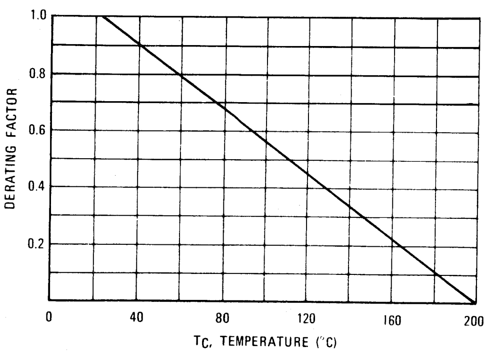
MAXIMUM RATINGS

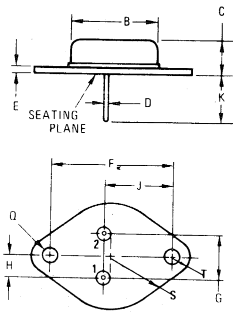
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	160	Vdc
Collector-Base Voltage	V_{CBO}	220	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = −1.5 V)	V_{CEX}	220	Vdc
Collector-Emitter Voltage (R_{BE} = 100Ω)	V_{CER}	200	Vdc
Collector-Current — continuous — peak (pw ≤ 10 ms)	I_C I_{CM}	20 25	Adc Apk
Base-Current continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25 °C	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR
STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE-EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	160		Vdc
Collector Cutoff Current at Reverse Bias: (V_{CE} = 220 V, V_{BE} = −1.5 V) (V_{CE} = 220 V, V_{BE} = −1.5 V, T_C = 125 °C)	I_{CEX}		1.5 6.0	mAdc
Collector-Emitter Cutoff Current (V_{CE} = 130 V)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter-Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 30 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	5 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 8 A, V_{CE} = 2 V) (I_C = 15 A, V_{CE} = 4 V)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage (I_C = 8 A, I_B = 0.8 A) (I_C = 15 A, I_B = 1.88 A)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 15 A, I_B = 1.88 A)	$V_{BE(sat)}$		1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 1 A, f = 4 MHz)	f_T	8		MHz

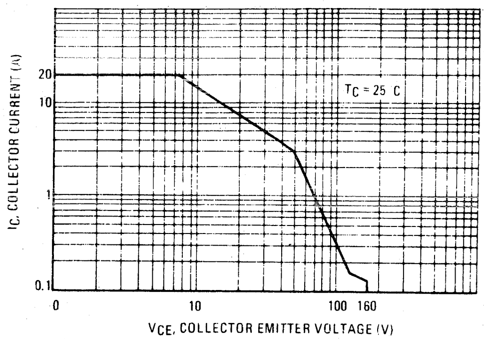
SWITCHING CHARACTERISTICS (Resistive Load)

Characteristic	Conditions	Symbol	Min.	Max.	Unit
Turn on Time	(I_C = 15 A, I_{B1} = I_{B2} = 1.88 A, V_{CC} = 30 V, RL ≃ 2Ω)	t_{on}		1.2	μs
Storage Time		t_s		1.2	
Fall Time		t_f		0.25	

[1] Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽2%.

3

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data of figure 2 is based on $T_C = 25\,°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.
At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 — "ON" VOLTAGES

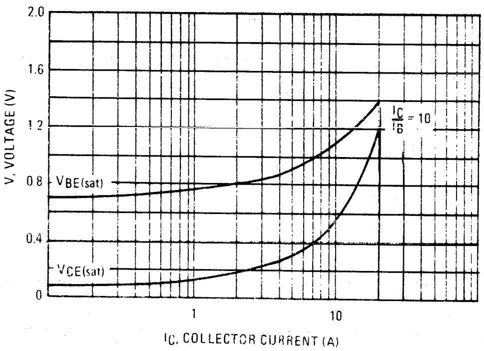


FIGURE 4 — DC CURRENT GAIN

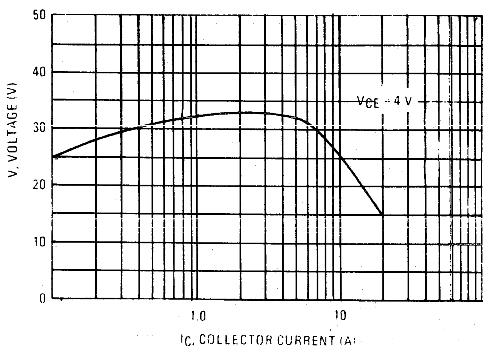


FIGURE 5 — RESISTIVE SWITCHING PERFORMANCE

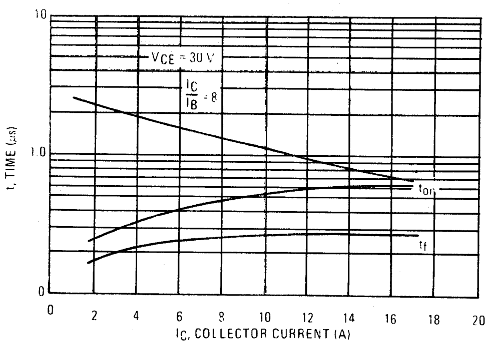
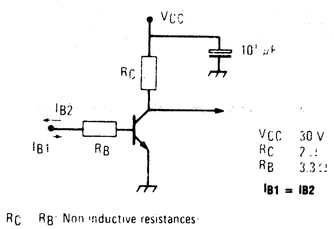


FIGURE 6 — SWITCHING TIMES TEST CIRCUIT



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUV12

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

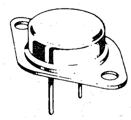
. . . designed for high speed, high voltage, high power applications.

- High DC current gain:
  HFE min. = 20 at Ic = 5 A
- Very fast switching times:
  T_S max. = 1.5 μs at Ic = 10 A
  T_F max. = 0.5 μs at Ic = 10 A

20 AMPERES

NPN SILICON POWER METAL TRANSISTOR

250 VOLTS
150 WATTS



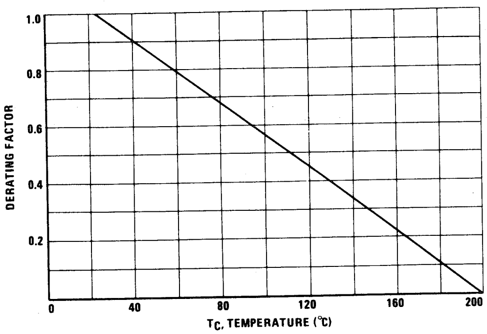
MAXIMUM RATINGS

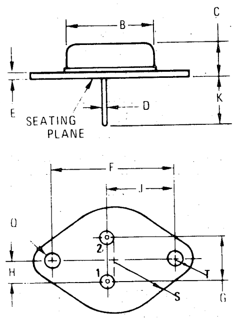
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector-Base Voltage	V_{CBO}	300	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	300	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	290	Vdc
Collector-Current – continuous – peak (pw ⩽ 10 ms)	I_C I_{CM}	20 25	Adc Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ $T_C = 25°C$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE-EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

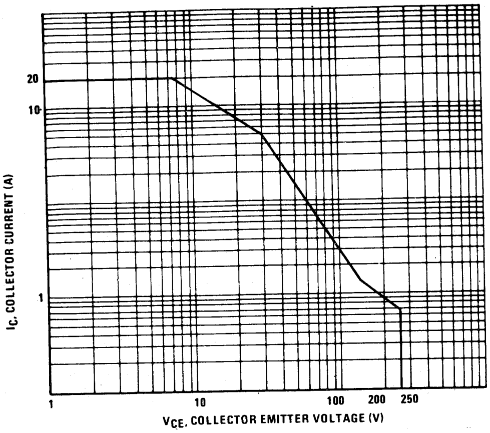
Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, $L = 25$ mH)	$V_{CEO(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Biais: ($V_{CE} = 300$ V, $V_{BE} = -1.5$ V)	I_{CEX}		1.5	mAdc
($V_{CE} = 300$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)			6	
Collector-Emitter Cutoff Current ($V_{CE} = 200$ V)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 30$ V, $t = 1$ s)	$I_{S/b}$	5.0		Adc
($V_{CE} = 140$ V, $t = 1$ s)		0.15		
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 5$ A, $V_{CE} = 4$ V)	h_{FE}	20	60	
($I_C = 10$ A, $V_{CE} = 4$ V)		10		
Collector-Emitter Saturation Voltage ($I_C = 5$ A, $I_B = 0.5$ A)	$V_{CE(sat)}$		1.0	Vdc
($I_C = 10$ A, $I_B = 1.25$ A)			1.5	
Base-Emitter Saturation Voltage ($I_C = 10$ A, $I_B = 1.25$ A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product ($V_{CE} = 15$ V, $I_C = 1$ A, $f = 4$ MHz)	f_T	8.0		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 10$ A, $I_{B1} = I_{B2} = 1.25$ A, ($V_{CC} = 150$ V, $R_C = 15\ \Omega$)	t_{on}		0.7	μs
Storage Time		t_s		1.5	
Fall Time		t_f		0.5	

[1] Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data of figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.
At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

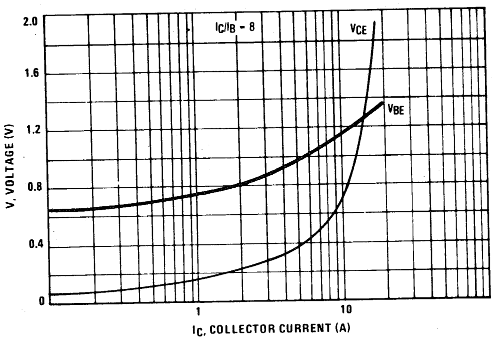


FIGURE 4 – DC CURRENT GAIN

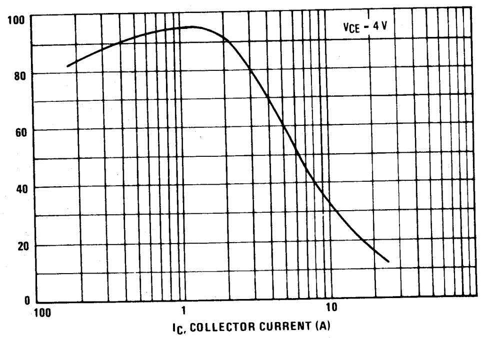


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

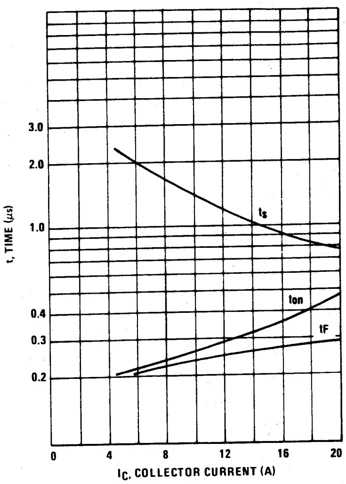
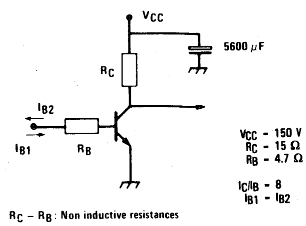


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUV20

SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTOR

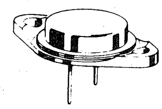
. . . designed for high speed, high current, high power applications.

- High DC current gain:
  HFE min. = 20 at Ic = 25 A
  = 10 at Ic = 50 A
- Low $V_{CE(sat)}$:
  $V_{CE(sat)}$ max. = 0.6 V at Ic = 25 A
  = 1.2 V at Ic = 50 A
- Very fast switching times:
  $T_F = 0.25\ \mu s$ at Ic = 50 A

50 AMPERES

NPN SILICON POWER METAL TRANSISTOR

125 VOLTS
250 WATTS

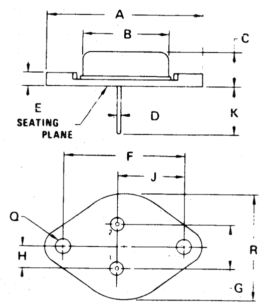


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	125	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	160	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	150	Vdc
Collector-Current — continuous — peak (pw ≤ 10 ms)	I_C I_{CM}	50 60	Adc Apk
Base-Current continuous	I_B	10	Adc
Total Power Dissipation @ $T_C = 25°C$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

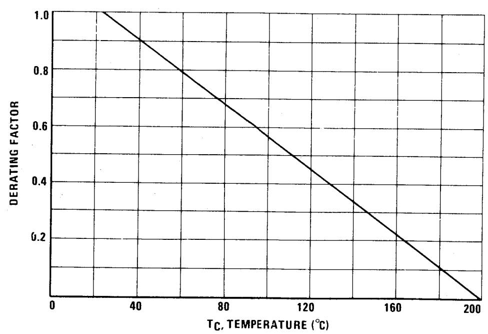


STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3

FIGURE 1 — POWER DERATING



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ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, $L = 25$ mH)	$V_{CEO(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Biais: ($V_{CE} = 140$ V, $V_{BE} = -1.5$ V) ($V_{CE} = 140$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)	I_{CEX}		3.0 12	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 100$ V)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 20$ V, $t = 1$ s) ($V_{CE} = 40$ V, $t = 1$ s)	$I_{S/b}$	12 1.5		Adc
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 25$ A, $V_{CE} = 2$ V) ($I_C = 50$ A, $V_{CE} = 4$ V)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 25$ A, $I_B = 2.5$ A) ($I_C = 50$ A, $I_B = 5$ A)	$V_{CE(sat)}$		0.6 1.2	Vdc
Base-Emitter Saturation Voltage ($I_C = 50$ A, $I_B = 5$ A)	$V_{BE(sat)}$		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product ($V_{CE} = 15$ V, $I_C = 2$ A, $f = 4$ MHz)	f_T	8.0		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 50$ A, $I_{B1} = I_{B2} = 5$ A, ($V_{CC} = 30$ V, $R_C = 0.6\ \Omega$)	t_{on}		1.5	μs
Storage Time		t_s		1.2	
Fall Time		t_f		0.25	

[1] Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

3

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

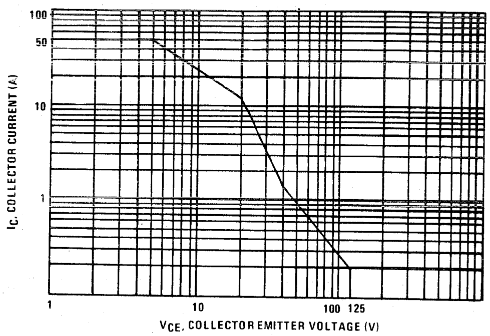


FIGURE 3 – "ON" VOLTAGES

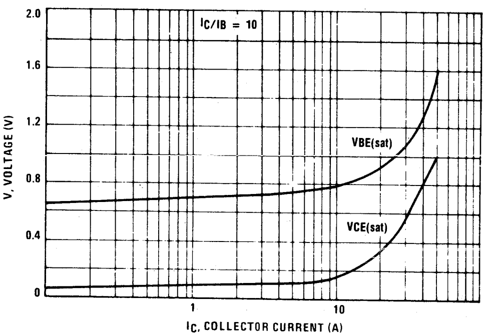
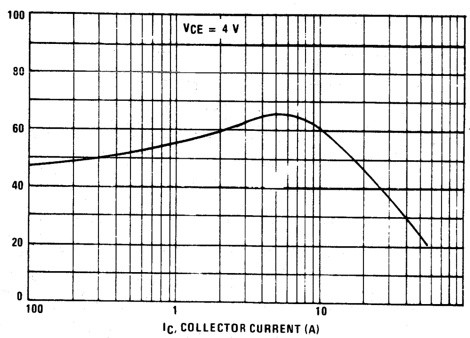


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

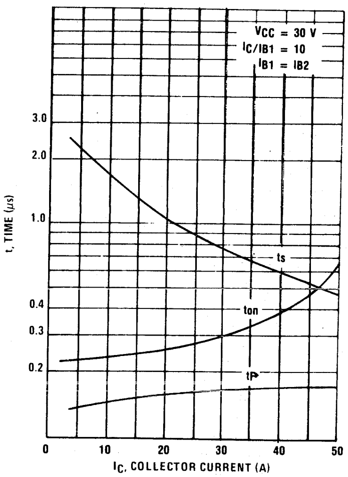
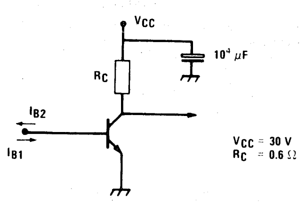


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



RC – Non inductive resistance

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUV21

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

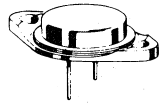
. . . designed for high speed, high current, high power applications.

- High DC current gain:
  HFE min. = 20 at Ic = 12 A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 0.6 V at Ic = 8 A
- Very fast switching times:
  T_F max. = 0.4 μs at Ic = 25 A

40 AMPERES

NPN SILICON POWER METAL TRANSISTOR

200 VOLTS
250 WATTS



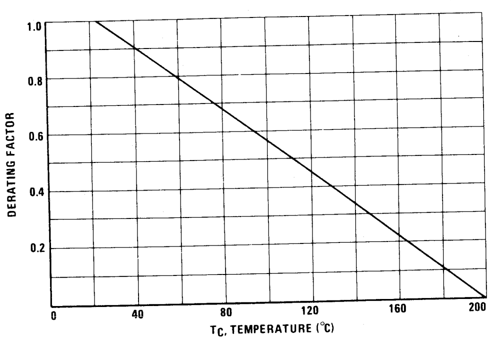
MAXIMUM RATINGS

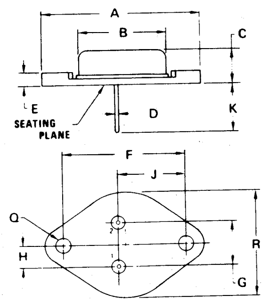
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector-Base Voltage	V_{CBO}	250	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	250	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	240	Vdc
Collector-Current — continuous — peak (pw ≤ 10 ms)	I_C I_{CM}	40 50	Adc Apk
Base-Current continuous	I_B	8	Adc
Total Power Dissipation @ $T_C = 25°C$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Biais: (V_{CE} = 250 V, V_{BE} = −1.5 V) (V_{CE} = 250 V, V_{BE} = −1.5 V, T_C = 125°C)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current (V_{CE} = 160 V)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter-Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	12 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 12 A, V_{CE} = 2 V) (I_C = 25 A, V_{CE} = 4 V)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage (I_C = 12 A, I_B = 1,2 A) (I_C = 25 A, I_B = 3 A)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 25 A, I_B = 3 A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)	f_T	8.0		MHz

3

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	I_C = 25 A, I_{B1} = I_{B2} = 3 A, (V_{CC} = 100 V, RC = 4 Ω)	t_{on}		1.0	μs
Storage Time		t_s		1.8	
Fall Time		t_f		0.4	

[1] Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩽2%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

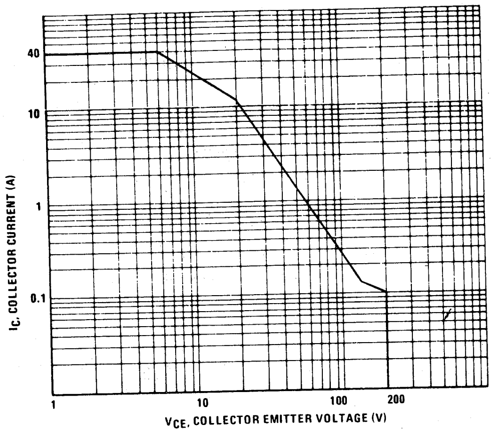


FIGURE 3 – "ON" VOLTAGES

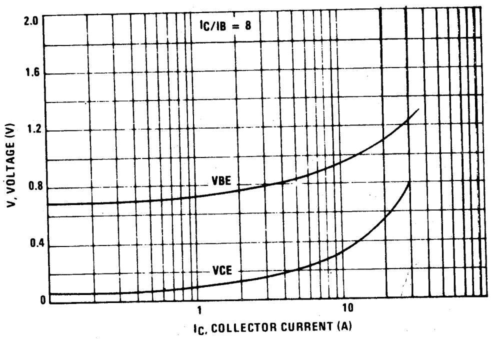
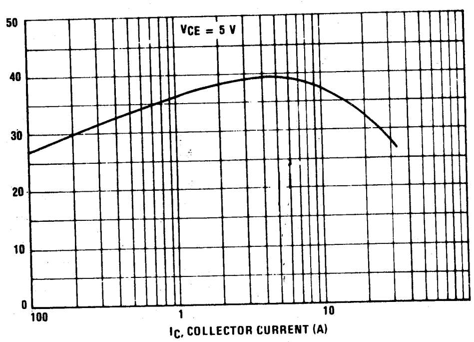


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data of figure 2 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.
At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

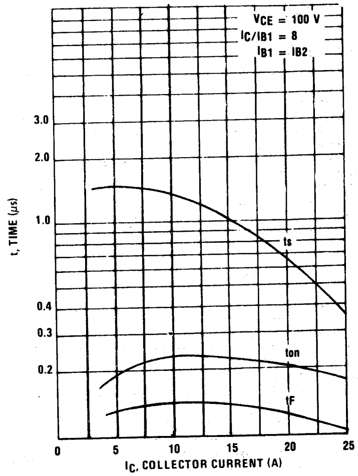
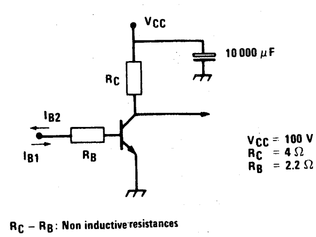


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUV21N

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

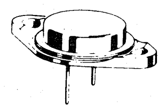
. . . designed for high speed, high current, high power and low cost applications.

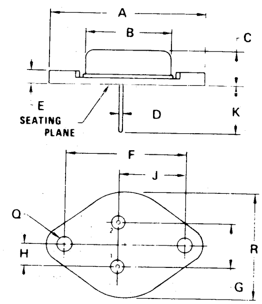
- High DC current gain: HFE min. = 15 at Ic = 20 A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$ max. = 1.0 V at Ic = 20 A
  = 1.8 V at Ic = 40 A
- Very fast switching times:
  T_F max. = 0.2 μs at Ic = 40 A

40 AMPERES

NPN SILICON
POWER
METAL TRANSISTOR

160 VOLTS
250 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
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J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3

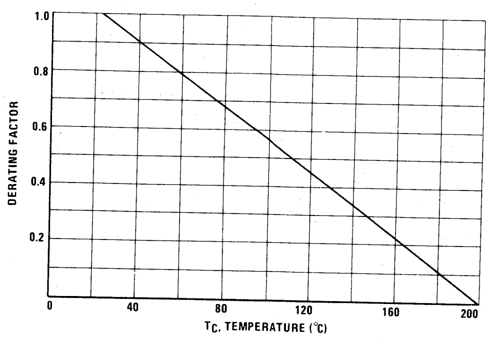
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	160	Vdc
Collector-Base Voltage	V_{CBO}	220	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	220	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	200	Vdc
Collector-Current — continuous — peak (pw ≤ 10 ms)	I_C I_{CM}	40 50	Adc Apk
Base-Current continuous	I_B	10	Adc
Total Power Dissipation @ $T_C = 25°C$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

FIGURE 1 – POWER DERATING



3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, L = 25 mH)	$V_{CEO(sus)}$	160		Vdc
Collector Cutoff Current at Reverse.Biais: ($V_{CE} = 220$ V, $V_{BE} = -1.5$ V) ($V_{CE} = 220$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 130$ V)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 25$ V, t = 0.5 s) ($V_{CE} = 140$ V, t = 0.5 s)	$I_{S/b}$	10 0.3		Adc
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 20$ A, $V_{CE} = 4$ V) ($I_C = 40$ A, $V_{CE} = 4$ V)	h_{FE}	15 10	60	
Collector-Emitter Saturation Voltage ($I_C = 20$ A, $I_B = 2$ A) ($I_C = 40$ A, $I_B = 5$ A)	$V_{CE(sat)}$		1.0 1.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 40$ A, $I_B = 5$ A)	$V_{BE(sat)}$		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product ($V_{CE} = 15$ V, $I_C = 2$ A, f = 4 MHz)	f_T	8.0		MHz

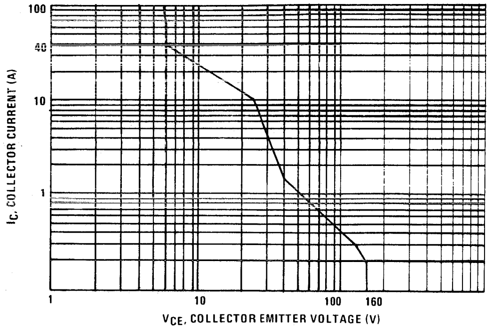
SWITCHING CHARACTERISTICS (Resistive Load)

Characteristic	Conditions	Symbol	Min.	Max.	Unit
Turn on Time	$I_C = 40$ A, $I_{B1} = I_{B2} = 5$ A, ($V_{CC} = 30$ V, $R_C = 0.75\ \Omega$)	t_{on}		1.2	μs
Storage Time		t_s		1.0	
Fall Time		t_f		0.2	

[1] Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩽2%.

3

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25°C$, $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

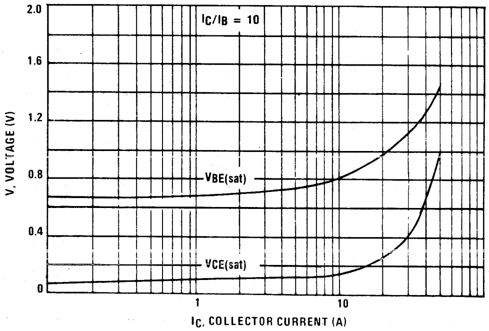


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

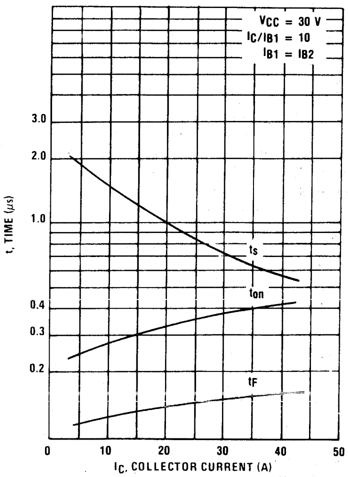


FIGURE 4 – DC CURRENT GAIN

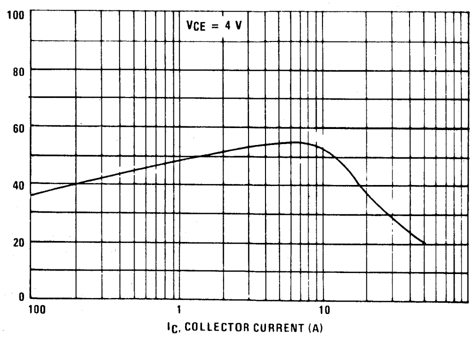
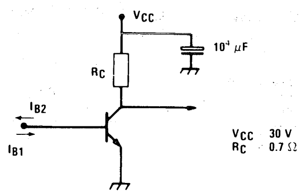


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



R_C: Non inductive resistance

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUV22

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

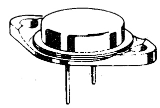
. . . designed for high current, high speed, high power applications.

- High DC current gain: HFE min. = 20 at Ic = 10 A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$ max. = 1.0 V at Ic = 10 A
- Very fast switching times:
  T_F max. = 0.35 μs at Ic = 20 A

40 AMPERES

NPN SILICON POWER METAL TRANSISTOR

250 VOLTS
250 WATTS

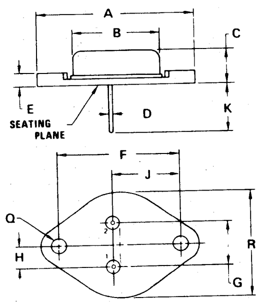


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	125	Vdc
Collector-Base Voltage	V_{CBO}	300	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = −1.5 V)	V_{CEX}	300	Vdc
Collector-Emitter Voltage (R_{BE} = 100Ω)	V_{CER}	290	Vdc
Collector-Current – continuous – peak (pw ⩽ 10 ms)	I_C I_{CM}	40 50	Adc Apk
Base-Current continuous	I_B	8	Adc
Total Power Dissipation @ T_C = 25°C	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
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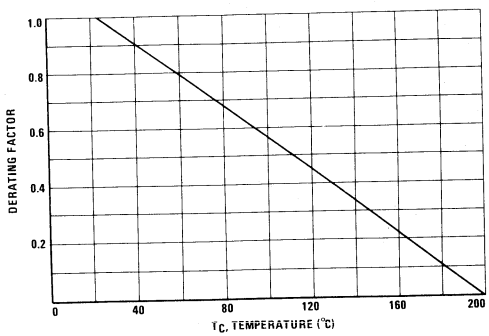
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3

FIGURE 1 – POWER DERATING



3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, L = 25 mH)	$V_{CEO(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Biais: ($V_{CE} = 300$ V, $V_{BE} = -1.5$ V) ($V_{CE} = 300$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 200$ V)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 20$ V, t = 1 s) ($V_{CE} = 140$ V, t = 1 s)	$I_{S/b}$	12 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 10$ A, $V_{CE} = 4$ V) ($I_C = 20$ A, $V_{CE} = 4$ V)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 10$ A, $I_B = 1$ A) ($I_C = 20$ A, $I_B = 2.5$ A)	$V_{CE(sat)}$		1.0 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 40$ A, $I_B = 4$ A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product ($V_{CE} = 15$ V, $I_C = 2$ A, f = 4 MHz)	f_T	8.0		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 20$ A, $I_{B1} = I_{B2} = 2.5$ A, ($V_{CC} = 100$ V, $R_C = 5\ \Omega$)	t_{on}		0.8	μs
Storage Time		t_s		1.1	
Fall Time		t_f		0.35	

[1] Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩽2%.

3

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

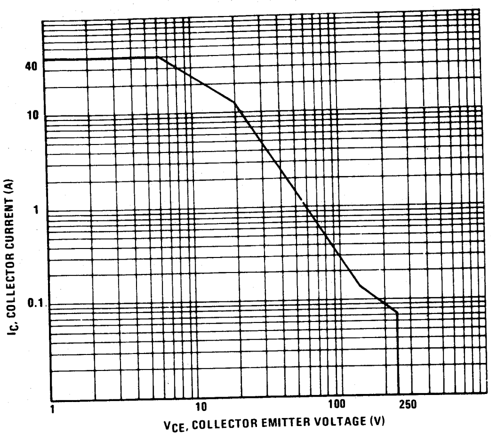


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FIGURE 3 – "ON" VOLTAGES

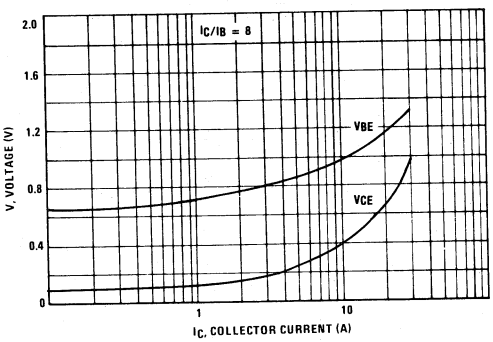


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

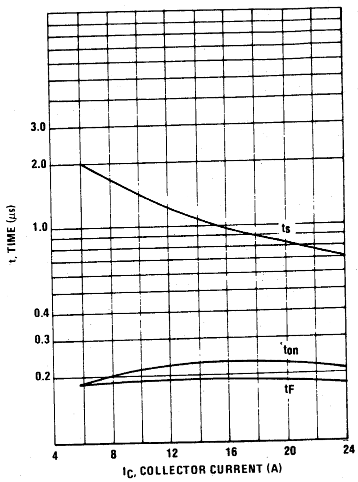


FIGURE 4 – DC CURRENT GAIN

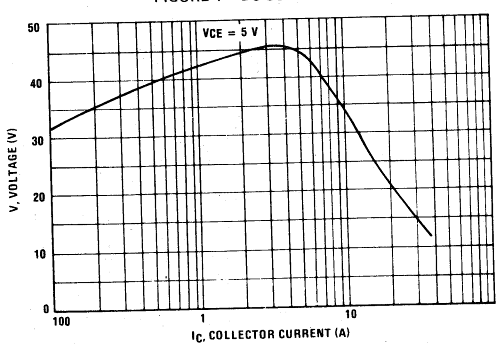
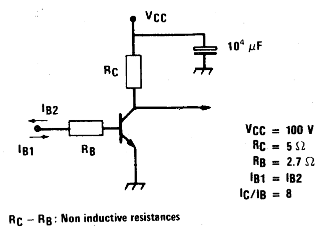


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUV23

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

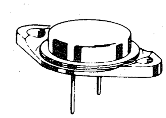
. . . designed for high current, high speed, high power applications.

- High DC current gain: HFE min. = 15 at Ic = 8 A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 0.8 V at Ic = 8 A
- Very fast switching times:
  T_F = 0.4 μs at Ic = 16 A

30 AMPERES

NPN SILICON POWER METAL TRANSISTOR

325 VOLTS
250 WATTS

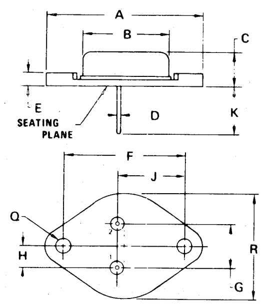


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	325	Vdc
Collector-Base Voltage	V_{CBO}	400	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = −1.5 V)	V_{CEX}	400	Vdc
Collector-Emitter Voltage (R_{BE} = 100Ω)	V_{CER}	390	Vdc
Collector-Current — continuous — peak (pw ≤ 10 ms)	I_C I_{CM}	30 40	Adc Apk
Base-Current continuous	I_B	6	Adc
Total Power Dissipation @ T_C = 25°C	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

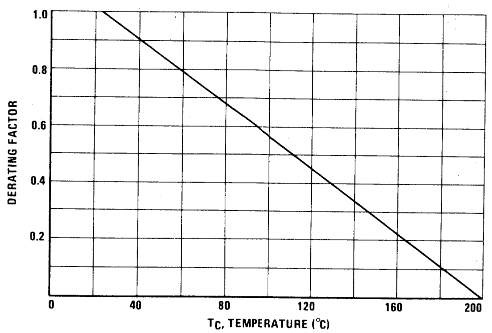


STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3

FIGURE 1 — POWER DERATING



3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	325		Vdc
Collector Cutoff Current at Reverse Biais: (V_{CE} = 400 V, V_{BE} = −1.5 V) (V_{CE} = 400 V, V_{BE} = −1.5 V, T_C = 125°C)	I_{CEX}		3.0 12	mAdc
Collector-Emitter Cutoff Current (V_{CE} = 260 V)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter-Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	12 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 8 A, V_{CE} = 4 V) (I_C = 16 A, V_{CE} = 4 V)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage (I_C = 8 A, I_B = 1.6 A) (I_C = 16 A, I_B = 3.2 A)	$V_{CE(sat)}$		0.8 1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 16 A, I_B = 3.2 A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)	f_T	8.0		MHz

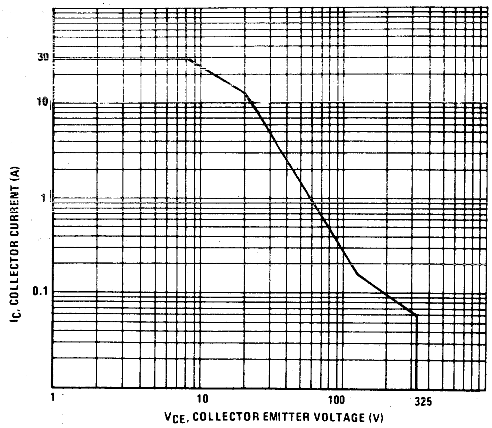
SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	I_C = 16 A, I_{B1} = I_{B2} = 3.2 A, (V_{CC} = 100 V, RC = 6.25 Ω)	t_{on}		0.8	μs
Storage Time		t_s		1.8	
Fall Time		t_f		0.4	

[1] Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩽2%.

3

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data of figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.
At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

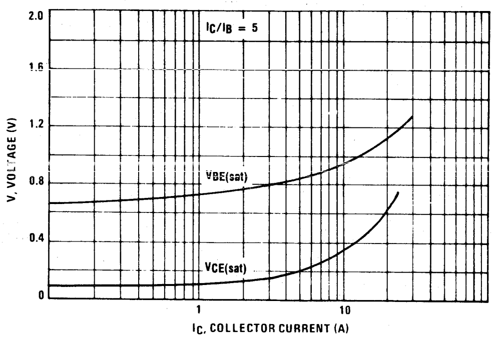


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

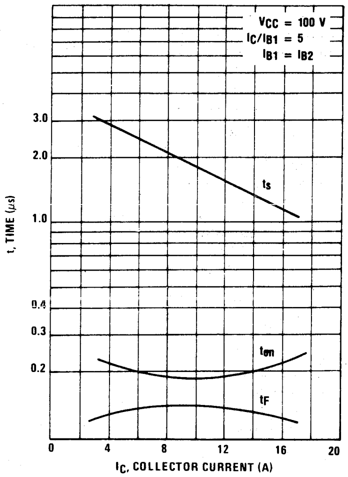


FIGURE 4 – DC CURRENT GAIN

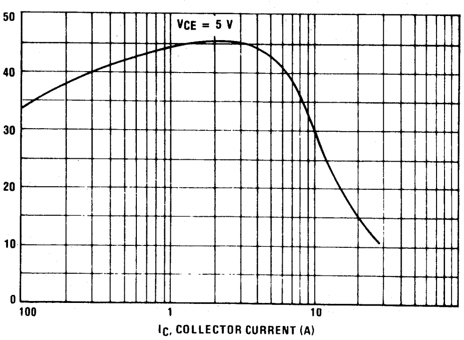
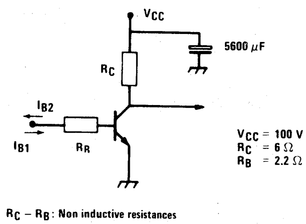


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUV24

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

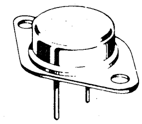
. . . designed for high current, high speed, high power applications.

- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 1.0 V at Ic = 12 A
- Very fast switching times:
  T_F max. = 0.9 μs at Ic = 12 A

20 AMPERES

NPN SILICON
POWER
METAL TRANSISTOR

400 VOLTS
250 WATTS



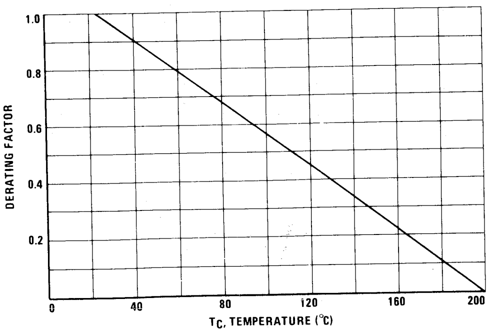
MAXIMUM RATINGS

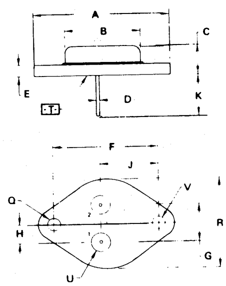
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Base Voltage	V_{CBO}	450	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	450	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	440	Vdc
Collector-Current — continuous — peak (pw ≤ 10 ms)	I_C I_{CM}	20 30	Adc Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ $T_C = 25°C$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

FIGURE 1 – POWER DERATING





NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. [T] IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
   ⌖ ⌀0.13 (0.005) Ⓜ T V Ⓜ
   FOR LEADS
   ⌖ ⌀0.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37		1.550
B		21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E		3.43		0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67		1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, L = 25 mH)	$V_{CEO(sus)}$	400		Vdc
Collector Cutoff Current at Reverse Biais: ($V_{CE} = 450$ V, $V_{BE} = -1.5$ V) ($V_{CE} = 450$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 320$ V)	I_{CEO}		30	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 20$ V, t = 1 s) ($V_{CE} = 140$ V, t = 1 s)	$I_{S/b}$	12 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 6$ A, $V_{CE} = 4$ V) ($I_C = 12$ A, $V_{CE} = 4$ V)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage ($I_C = 6$ A, $I_B = 1.2$ A) ($I_C = 12$ A, $I_B = 2.4$ A)	$V_{CE(sat)}$		0.6 1.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 12$ A, $I_B = 2.4$ A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product ($V_{CE} = 15$ V, $I_C = 2$ A, f = 4 MHz)	f_T	8.0		MHz

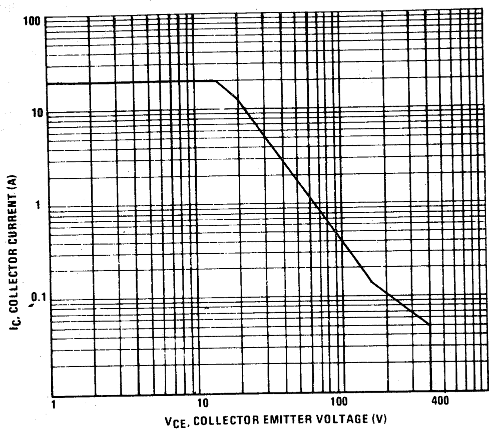
SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 12$ A, $I_{B1} = I_{B2} = 2.4$ A, ($V_{CC} = 120$ V, RC = 8.3 Ω)	t_{on}		1.6	μs
Storage Time		t_s		3.0	
Fall Time		t_f		0.9	

[1] Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

3

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25°C$, $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

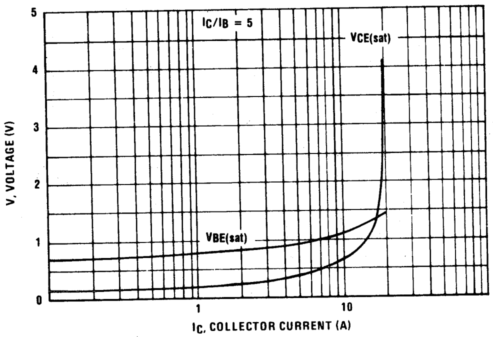


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

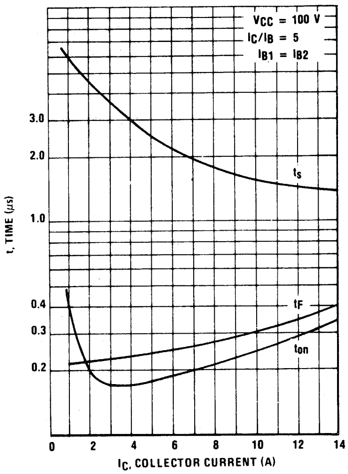


FIGURE 4 – DC CURRENT GAIN

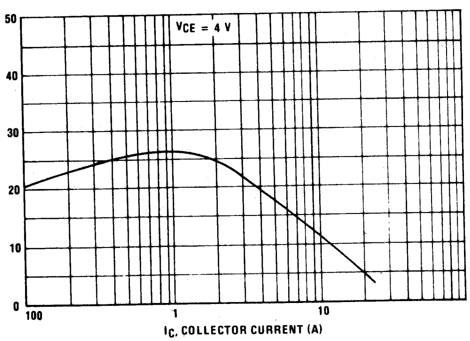
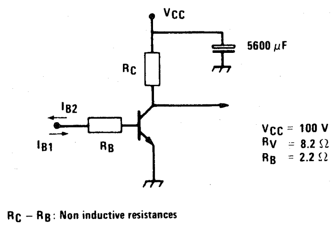


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

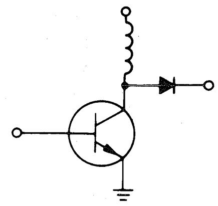
BUW11,A
BUW12,A

Designer's Data Sheet

NPN Silicon Power Transistors

Switchmode Series

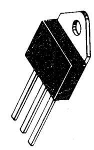
POWER TRANSISTORS
5 and 8 AMPERES
400 and 450 VOLTS
125 WATTS



These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:
- Collector-Emitter Voltage — V_{CEV} = 850 and 1000
- Fast Turn-Off Times
  - 140 ns Inductive Fall Time – 100°C (Typ)
  - 170 & 250 ns Inductive Crossover Time – 100°C (Typ)
  - 1200 & 1800 ns Inductive Storage Time – 100°C (Typ)
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Load
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents
- Extremely High RBSOA Capability



CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-Emitter Voltage	BUW11/12 BUW11A/12A	$V_{CEO(sus)}$	400 450	Vdc
Collector-Emitter Voltage	BUW11/12 BUW11A/12A	V_{CEV}	850 1000	Vdc
Emitter-Base Voltage		V_{EB}	10	Vdc
Collector Current — Continuous	BUW11/11A BUW12/12A	I_C	5 8	Adc
— Peak (1)	BUW11/11A BUW12/12A	I_{CM}	10 20	
Base Current — Continuous	BUW11/11A BUW12/12A	I_B	2 4	Adc
— Peak (1)	BUW11/11A BUW12/12A	I_{BM}	4 8	
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C		P_D	125 50 1	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	BUW11/12 BUW11A/12A	$V_{CEO(sus)}$	400 450	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated V_{CEV}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated V_{CEV}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	— —	— —	0.1 1	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	1	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	—	—	0.1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figures 8 and 9			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figures 10 and 11			
BUW11 **ON CHARACTERISTICS(1)**						
Collector-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc) (I_C = 3 Adc, I_B = 0.6 Adc) (I_C = 3 Adc, I_B = 0.6 Adc, T_C = 100°C)		$V_{CE(sat)}$	— — —	— — —	1 1.5 2	Vdc
Base-Emitter Saturation Voltage (I_C = 3 Adc, I_B = 0.6 Adc) (I_C = 3 Adc, I_B = 0.6 Adc, T_C = 100°C)		$V_{BE(sat)}$	— —	— —	1.4 1.4	Vdc
DC Current Gain (I_C = 3 Adc, V_{CE} = 5 Vdc)		h_{FE}	6	—	—	—
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)		C_{ob}	—	125	—	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Inductive Load (Table 1)							
Storage Time	(I_C = 3 Adc, I_{B1} = 0.6 Adc, $V_{BE(off)}$ = 5 Vdc, $V_{CE(pk)}$ = 300 Vdc)	(T_J = 100°C)	t_{sv}	—	1.2	1.5	μs
Fall Time			t_{fi}	—	0.14	0.3	
Crossover Time			t_c	—	0.25	0.5	
Resistive Load (Table 2)							
Delay Time	(I_C = 3 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.6 Adc, PW = 20 μs, Duty Cycle ≤ 2%)	(I_{B2} = 0.6 Adc, R_{B2} = 4 Ω)	t_d	—	—	0.1	μs
Rise Time			t_r	—	—	0.8	
Storage Time			t_s	—	—	4	
Fall Time			t_f	—	—	0.8	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
BUW11A							
ON CHARACTERISTICS(1)							
Collector-Emitter Saturation Voltage			$V_{CE(sat)}$				Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)				—	—	1	
(I_C = 2.5 Adc, I_B = 0.5 Adc)				—	—	1.5	
(I_C = 2.5 Adc, I_B = 0.5 Adc, T_C = 100°C)				—	—	2	
Base-Emitter Saturation Voltage			$V_{BE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 0.5 Adc)				—	—	1.4	
(I_C = 2.5 Adc, I_B = 0.5 Adc, T_C = 100°C)				—	—	1.4	
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 5 Vdc)			h_{FE}	6	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)			C_{ob}	—	125	—	pF
SWITCHING CHARACTERISTICS							
Inductive Load (Table 1)							
Storage Time	(I_C = 2.5 Adc, I_{B1} = 0.5 Adc, $V_{BE(off)}$ = 5 Vdc, $V_{CE(pk)}$ = 300 Vdc)	(T_J = 100°C)	t_{sv}	—	1.2	1.5	μs
Fall Time			t_{fi}	—	0.14	0.3	
Crossover Time			t_c	—	0.25	0.5	
Resistive Load (Table 2)							
Delay Time	(I_C = 2.5 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.5 Adc, PW = 20 μs, Duty Cycle ≤ 2%)	(I_{B2} = 0.5 Adc, R_{B2} = 4 Ω)	t_d	—	—	0.1	μs
Rise Time			t_r	—	—	0.8	
Storage Time			t_s	—	—	4	
Fall Time			t_f	—	—	0.8	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
BUW12							
ON CHARACTERISTICS(1)							
Collector-Emitter Saturation Voltage (I_C = 3 Adc, I_B = 0.6 Adc)			$V_{CE(sat)}$	—	—	1	Vdc
(I_C = 6 Adc, I_B = 1.2 Adc)				—	—	1.5	
(I_C = 6 Adc, I_B = 1.2 Adc, T_C = 100°C)				—	—	2	
Base-Emitter Saturation Voltage (I_C = 6 Adc, I_B = 1.2 Adc)			$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 6 Adc, I_B = 1.2 Adc, T_C = 100°C)				—	—	1.5	
DC Current Gain (I_C = 6 Adc, V_{CE} = 5 Vdc)			h_{FE}	6	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)			C_{ob}	—	125	—	pF
SWITCHING CHARACTERISTICS							
Inductive Load (Table 1)							
Storage Time	(I_C = 6 Adc, I_{B1} = 1.2 Adc, $V_{BE(off)}$ = 5 Vdc, $V_{CE(pk)}$ = 300 Vdc)	(T_J = 100°C)	t_{sv}	—	1.8	2.3	μs
Fall Time			t_{fi}	—	0.14	0.3	
Crossover Time			t_c	—	0.17	0.5	
Resistive Load (Table 2)							
Delay Time	(I_C = 6 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.2 Adc, PW = 20 μs, Duty Cycle ≤ 2%)	(I_{B2} = 1.2 Adc, R_{B2} = 4 Ω)	t_d	—	—	0.1	μs
Rise Time			t_r	—	—	0.8	
Storage Time			t_s	—	—	4	
Fall Time			t_f	—	—	0.8	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

Characteristic			Symbol	Min	Typ	Max	Unit
BUW12A							
ON CHARACTERISTICS(1)							
Collector-Emitter Saturation Voltage (I_C = 3 Adc, I_B = 0.6 Adc)			$V_{CE(sat)}$	—	—	1	Vdc
(I_C = 5 Adc, I_B = 1 Adc)				—	—	1.5	
(I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)				—	—	2	
Base-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc)			$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)				—	—	1.5	
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)			h_{FE}	6	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)			C_{ob}	—	125	—	pF
SWITCHING CHARACTERISTICS							
Inductive Load (Table 1)							
Storage Time	(I_C = 5 Adc, I_{B1} = 1 Adc, $V_{BE(off)}$ = 5 Vdc, $V_{CE(pk)}$ = 300 Vdc)	(T_J = 100°C)	t_{sv}	—	1.8	2.3	μs
Fall Time			t_{fi}	—	0.14	0.3	
Crossover Time			t_c	—	0.17	0.5	
Resistive Load (Table 2)							
Delay Time	(I_C = 5 Adc, V_{CC} = 250 Vdc, I_{B1} = 1 Adc, PW = 20 μs, Duty Cycle ≤ 2%)	(I_{B2} = 1 Adc, R_{B2} = 4 Ω)	t_d	—	—	0.1	μs
Rise Time			t_r	—	—	0.8	
Storage Time			t_s	—	—	4	
Fall Time			t_f	—	—	0.8	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

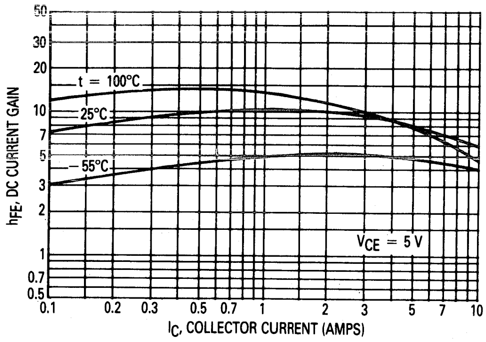


Figure 1. Typical DC Current Gain

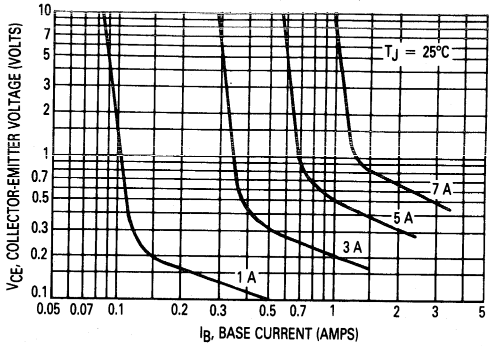


Figure 2. Typical Collector Saturation Region

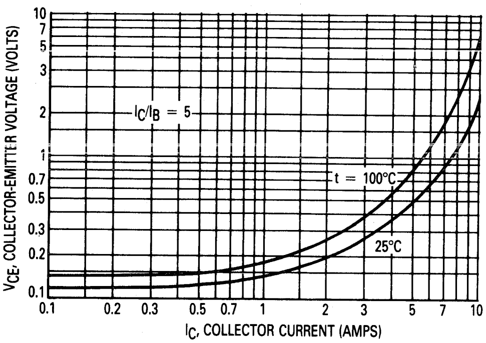


Figure 3. Typical Collector Saturation Region

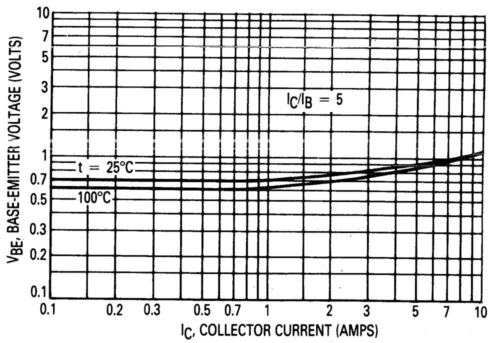


Figure 4. Typical Base-Emitter Voltage

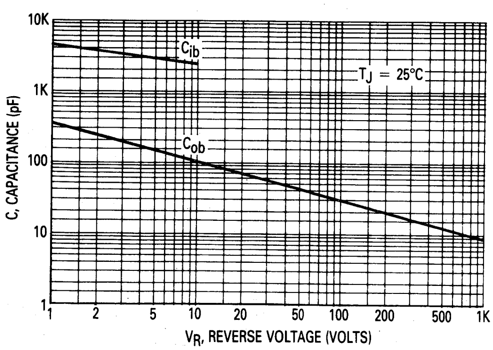


Figure 5. Typical Capacitance

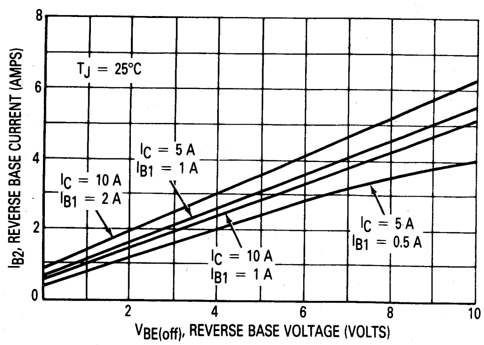


Figure 6. Peak Reverse Base Current

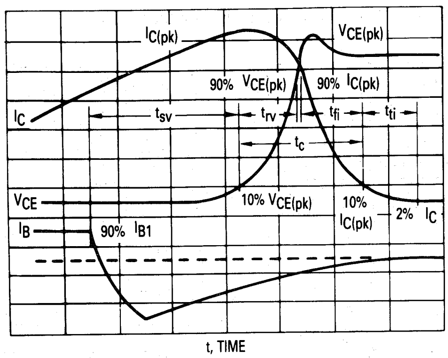


Figure 7. Inductive Switching Measurements

Table 1. Inductive Load Switching

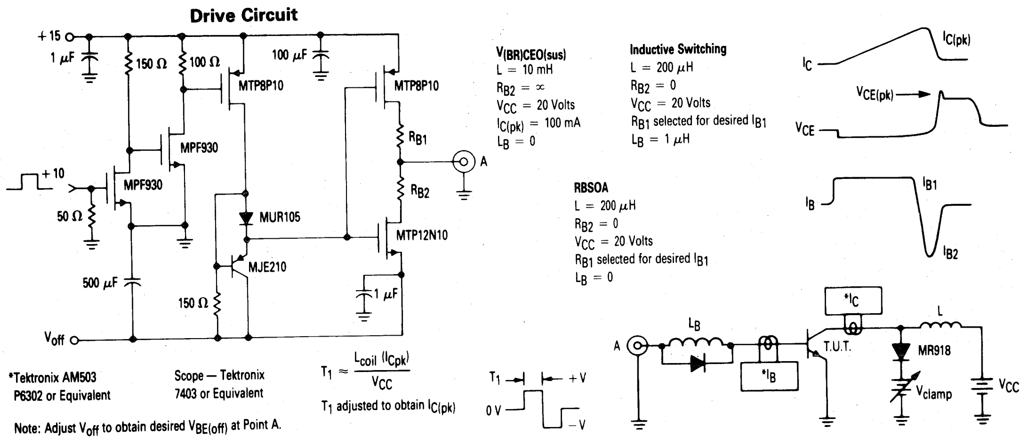
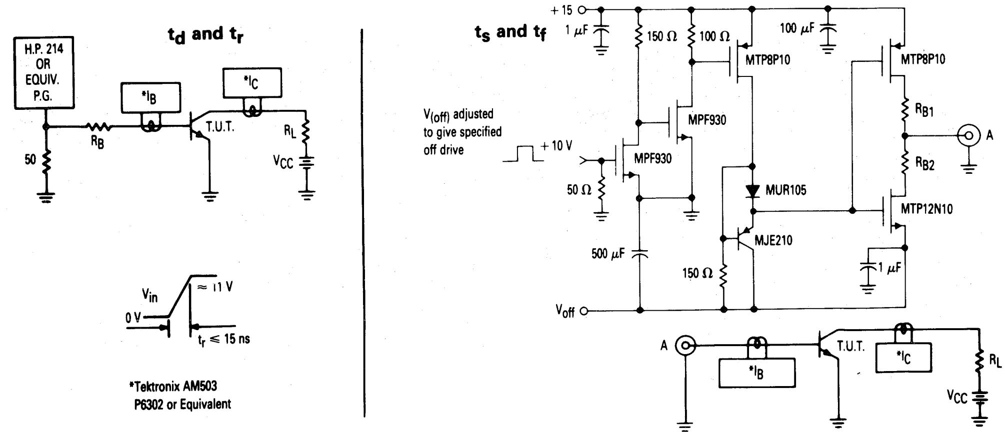


Table 2. Resistive Load Switching



MAXIMUM FORWARD BIAS SAFE OPERATING AREA

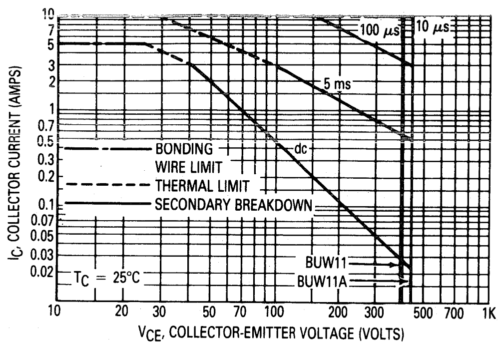


Figure 8. BUW11,A

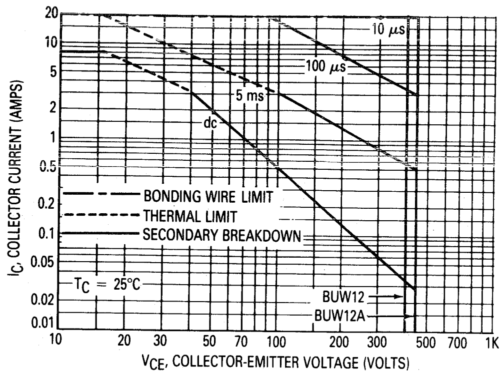


Figure 9. BUW12,A

MAXIMUM REVERSE BIAS SAFE OPERATING AREA

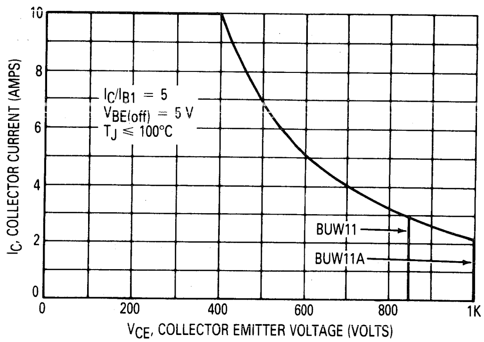


Figure 10. BUW11,A

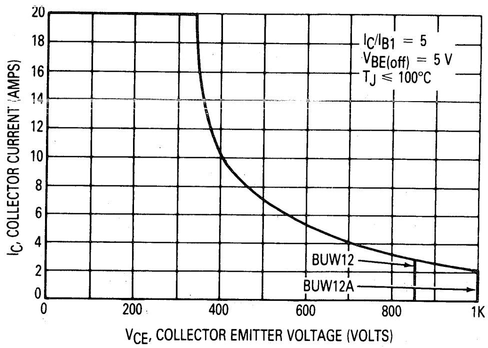


Figure 11. BUW12,A

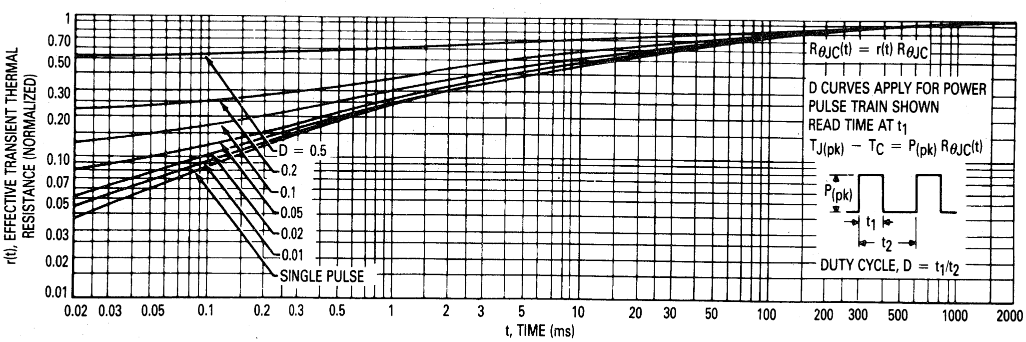


Figure 12. Thermal Response

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 8 and 9 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 8 and 9 may be found at any case temperature by using the appropriate curve on Figure 13.

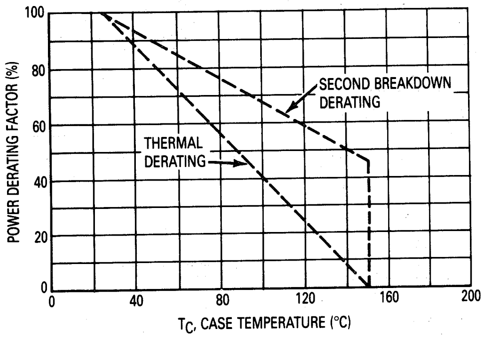


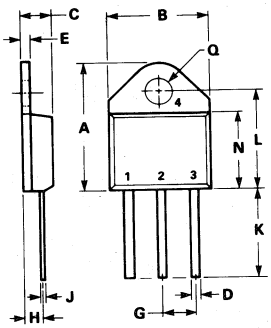
Figure 13. Power Derating

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figures 10 and 11 gives the RBSOA characteristics.

OUTLINE DIMENSIONS



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340-01
TO-218AC

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUX13

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

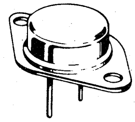
. . . designed for high speed, high voltage, high power applications.

- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 1.5 V at Ic = 8 A
- Very fast switching times:
  T_F max. = 0.8 μs at Ic = 8 A

15 AMPERES

NPN SILICON
POWER
METAL TRANSISTOR

325 VOLTS
150 WATTS



MAXIMUM RATINGS

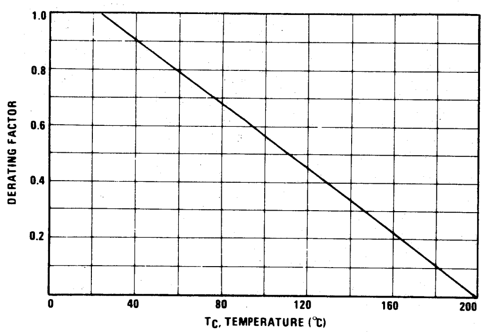
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	325	Vdc
Collector-Base Voltage	V_{CBO}	400	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = −2.5 V)	V_{CEX}	400	Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	390	Vdc
Collector-Current — continuous — peak (pw ⩽ 10 ms)	I_C I_{CM}	15 20	Adc Apk
Base-Current continuous	I_B	3	Adc
Total Power Dissipation @ T_C = 25 °C	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

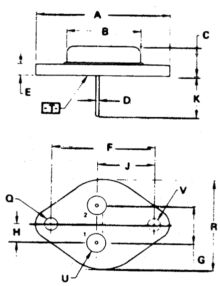
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

3

FIGURE 1 — POWER DERATING





NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. T IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ⌀ 0.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS
   ⌖ | ⌀ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	325		Vdc
Collector Cutoff Current at Reverse Biais: (V_{CE} = 400 V, V_{BE} = −1.5 V) (V_{CE} = 400 V, V_{BE} = −1.5 V, T_C = 125°C)	I_{CEX}		1.5 6.0	mAdc
Collector-Emitter Cutoff Current (V_{CE} = 260 V)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter-Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 30 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	5 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 4 A, V_{CE} = 4 V) (I_C = 8 A, V_{CE} = 4 V)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage (I_C = 4 A, I_B = 0.8 A) (I_C = 8 A, I_B = 1.6 A)	$V_{CE(sat)}$		0.8 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 8 A, I_B = 1.6 A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (V_{CE} = 15 V, I_C = 1 A, f = 4 MHz)	f_T	8.0		MHz

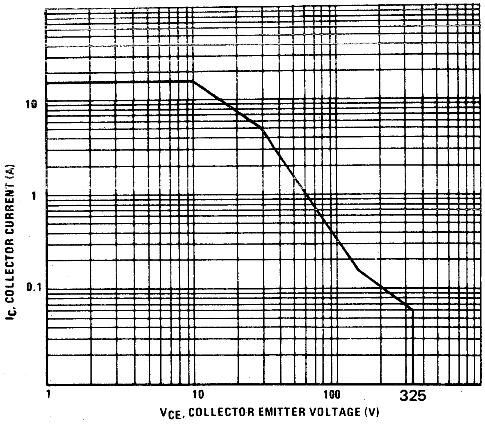
SWITCHING CHARACTERISTICS (Resistive Load)

Characteristic	Conditions	Symbol	Min.	Max.	Unit
Turn on Time	I_C = 8 A, I_{B1} = I_{B2} = 1.6 A, (V_{CC} = 150 V, RC = 18.7 Ω)	t_{on}		1.2	μs
Storage Time		t_s		2.5	
Fall Time		t_f		0.8	

[1] Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩽2%.

3

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data of figure 2 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.
At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

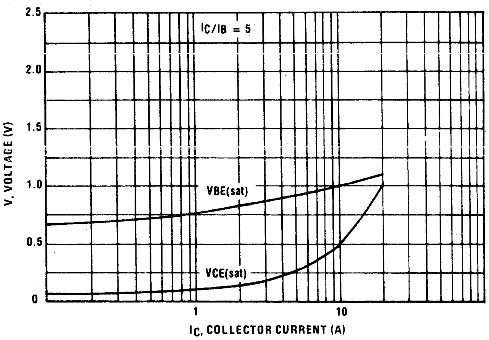


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

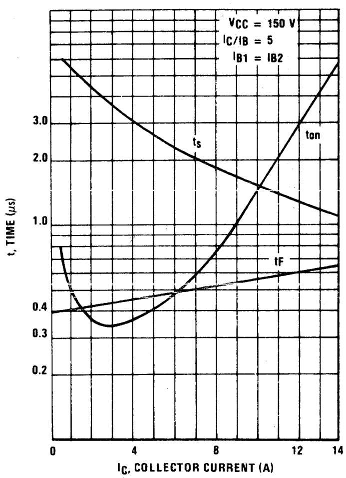


FIGURE 4 – DC CURRENT GAIN

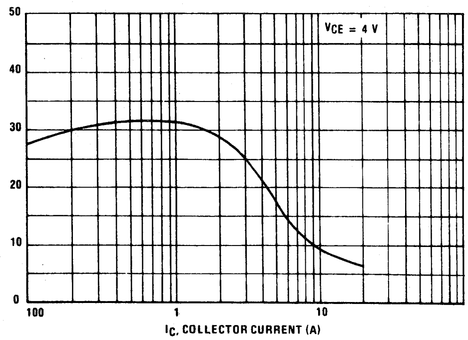
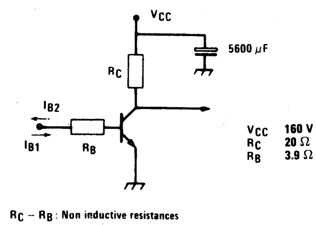


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUX39

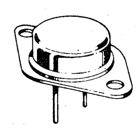
NPN SILICON POWER METAL TRANSISTOR

. . . designed for high speed, high current, high power application.

- High current gain — bandwidth product Ft min. = 8.0 MHz
- High DC current gain H_{FE} min. 15 @ I_C = 12 A.
- Very fast switching times
  t_F max. = 0.25 μs @ I_C = 20 A

NPN SILICON POWER METAL TRANSISTOR

30 AMPERES



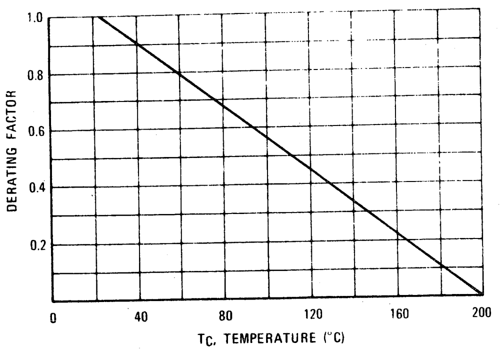
MAXIMUM RATINGS

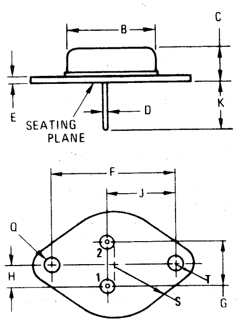
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	90	Vdc
Collector-Base Voltage	V_{CBO}	120	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = −1.5 V)	V_{CEX}	120	Vdc
Collector-Emitter Voltage (R_{BE} = 100Ω)	V_{CER}	110	Vdc
Collector-Current — continuous — peak (pw ≤ 10 ms)	I_C I_{CM}	30 40	Adc Apk
Base-Current continuous	I_B	6	Adc
Total Power Dissipation @ T_C = 25 °C	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE-EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

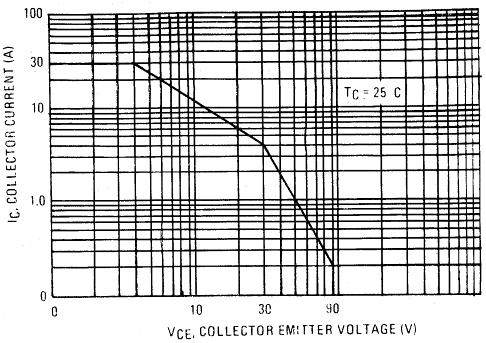
Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	90		Vdc
Collector-Emitter Cutoff Current at Reverse Bias Voltage (V_{CE} = 120 V, V_{BE} = −1.5 V) (V_{CE} = 120 V, V_{BE} = −1.5 V, T_C = 125 °C)			 1 5	mAdc
Collector-Emitter Cutoff Current (V_{CE} = 70 V)	I_{CEO}		1	mAdc
Emitter-Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter-Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 45 V, t = 1 s) (V_{CE} = 30 V, t = 1 s)	$I_{S/b}$	 1 4		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 12 A, V_{CE} = 4 V) (I_C = 20 A, V_{CE} = 4 V)	h_{FE}	 15 8	 45	
Collector-Emitter Saturation Voltage (I_C = 12 A, I_B = 1.2 A) (I_C = 20 A, I_B = 2.5 A)	$V_{CE(sat)}$		 1.2 1.6	Vdc
Base-Emitter Saturation Voltage (I_C = 20 A, I_B = 2.5 A)	$V_{BE(sat)}$		2.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 1 A, f = 4 MHz)	f_T	8		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Characteristic	Conditions	Symbol	Min.	Max.	Unit
Turn on Time	I_C = 20 A, I_{B1} = I_{B2} = 2.5 A, V_{CE} = 30 V, RC = 1.5 Ω	t_{on}		1.2	μs
Storage Time		t_s		1.0	
Fall Time		t_f		0.25	

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25\,°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

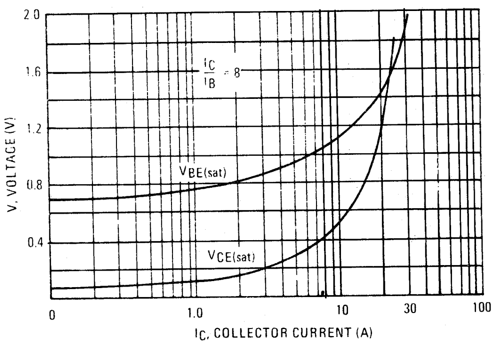


FIGURE 4 – DC CURRENT GAIN

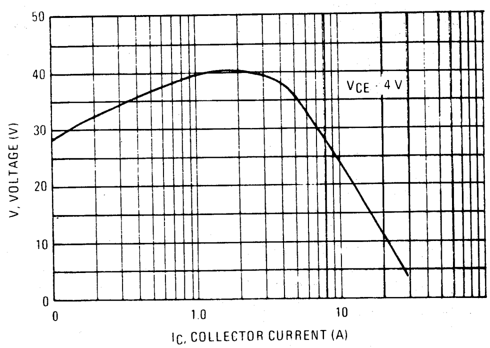


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

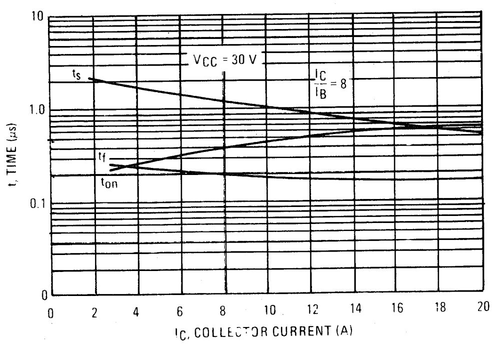
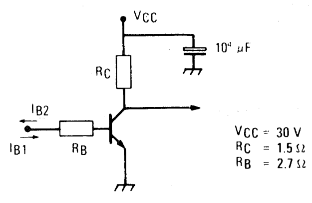


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



RC – RB: Non inductive resistances

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUX40

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

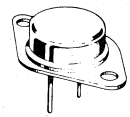
. . . designed for high speed, high current, high power applications.

- High D.C. current gain:
  HFE min.: 15 at Ic = 10 A
- Very fast switching times:
  T_F max. = 0.25 μs at Ic = 15 A

20 AMPERES

NPN SILICON POWER METAL TRANSISTOR

125 VOLTS
120 WATTS



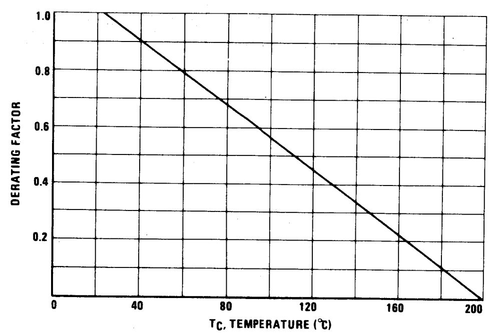
MAXIMUM RATINGS

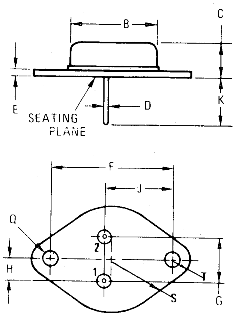
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	125	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5$ V)	V_{CEX}	160	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\ \Omega$)	V_{CER}	150	Vdc
Collector-Current — continuous — peak (pw ⩽ 10 ms)	I_C I_{CM}	20 28	Adc Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ $T_C = 25°C$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Biais: (V_{CE} = 160 V, V_{BE} = −1.5 V) (V_{CE} = 160 V, V_{BE} = −1.5 V, T_C = 125°C)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current (V_{CE} = 100 V)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter-Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 30 V, t = 1 s) (V_{CE} = 50 V, t = 1 s)	$I_{S/b}$	4.0 1.0		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 10 A, V_{CE} = 4 V) (I_C = 15 A, V_{CE} = 4 V)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage (I_C = 10 A, I_B = 1 A) (I_C = 15 A, I_B = 1.88 A)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage (I_C = 15 A, I_B = 1.88 A)	$V_{BE(sat)}$		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 1 A, f = 4 MHz)	f_T	8.0		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	I_C = 15 A, I_{B1} = I_{B2} = 1.88 A, (V_{CC} = 30 V, RC = 2 Ω)	t_{on}		1.2	μs
Storage Time		t_s		1.0	
Fall Time		t_f		0.25	

[1] Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩽2%.

3

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

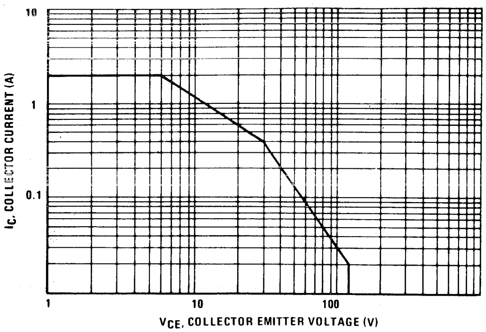


FIGURE 3 – "ON" VOLTAGES

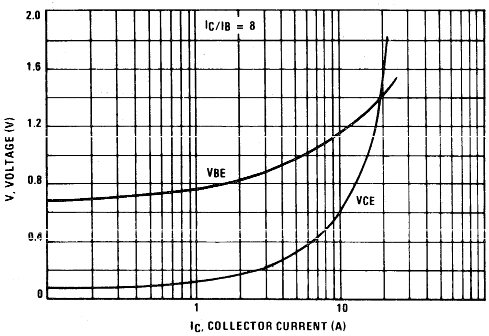
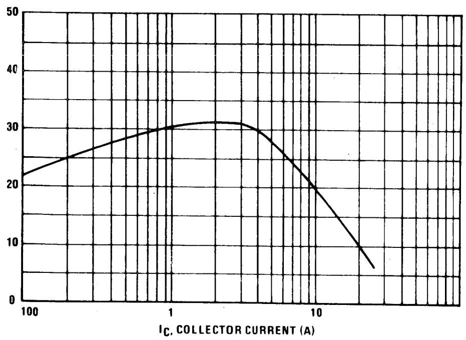


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data of figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.
At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

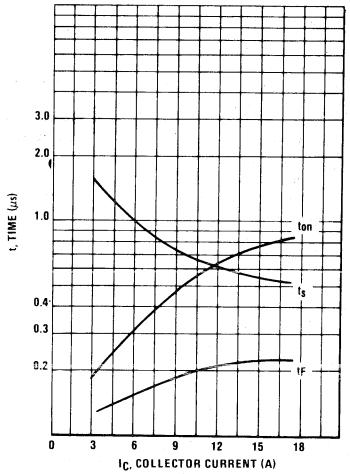
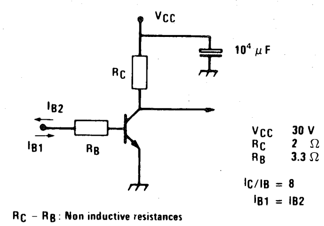


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUX41

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

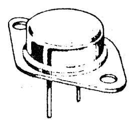
. . . designed for high speed, high current, high power applications.

- Very fast switching times:
  T_F max. = 0.4 μs at I_C = 8 A

15 AMPERES

NPN SILICON POWER METAL TRANSISTOR

200 VOLTS
120 WATTS



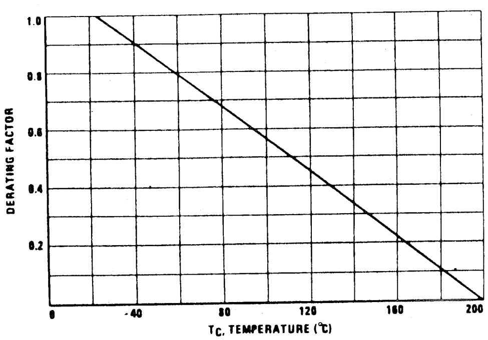
MAXIMUM RATINGS

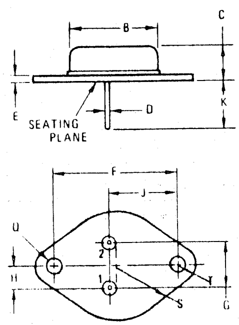
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector-Base Voltage	V_{CBO}	250	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = −2.5 V)	V_{CEX}	250	Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	240	Vdc
Collector-Current — continuous — peak (pw ≤ 10 ms)	I_C I_{CM}	15 20	Adc Apk
Base-Current continuous	I_B	3	Adc
Total Power Dissipation @ T_C = 25°C	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR
STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE-EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, $L = 25$ mH)	$V_{CEO(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Biais: ($V_{CE} = 250$ V, $V_{BE} = -1.5$ V) ($V_{CE} = 250$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 160$ V)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 30$ V, t = 1 s) ($V_{CE} = 135$ V, t = 1 s)	$I_{S/b}$	4.0 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 5$ A, $V_{CE} = 4$ V) ($I_C = 8$ A, $V_{CE} = 4$ V)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage ($I_C = 5$ A, $I_B = 0.5$ A) ($I_C = 8$ A, $I_B = 1$ A)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 8$ A, $I_B = 1$ A)	$V_{BE(sat)}$		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product ($V_{CE} = 15$ V, $I_C = 1$ A, f = 4 MHz)	f_T	8.0		MHz

3

SWITCHING CHARACTERISTICS (Resistive Load)

Characteristic	Conditions	Symbol	Min.	Max.	Unit
Turn on Time	$I_C = 8$ A, $I_{B1} = I_{B2} = 1$ A, ($V_{CC} = 150$ V, $R_C = 18.75\ \Omega$)	t_{on}		0.6	μs
Storage Time		t_s		1.5	
Fall Time		t_f		0.4	

[1] Pulse Test: Pulse Width ⩽300 μs, Duty Cycle ⩽2%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

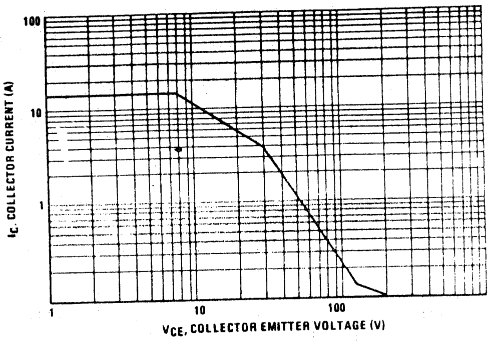


FIGURE 3 – "ON" VOLTAGES

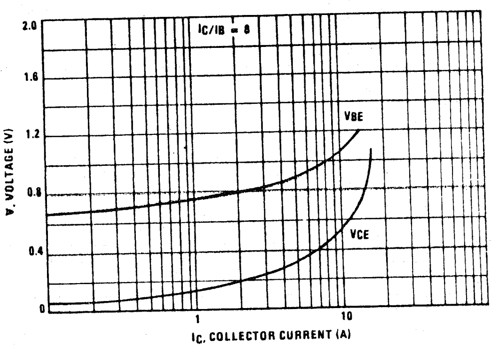
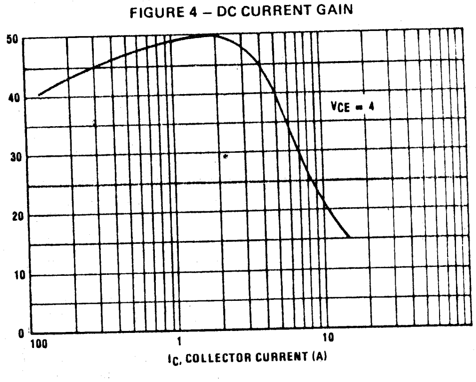


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data of figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

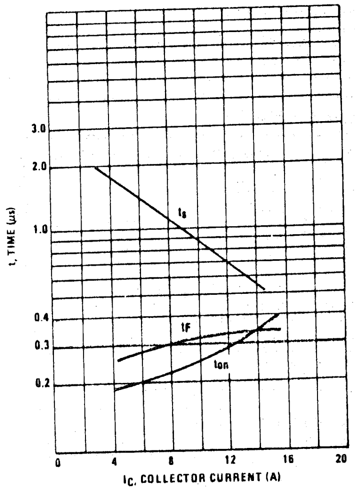
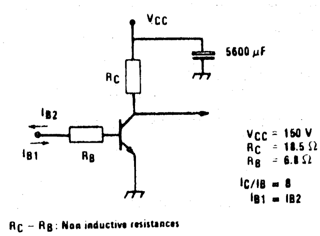


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUX41N

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

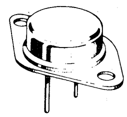
. . . designed for high speed, high current, high power applications.

- High DC current gain:
  HFE min. = 15 at Ic = 8 A
- Very fast switching times:
  T_F max. = 0.25 μs at Ic = 12 A

18 AMPERES

NPN SILICON
POWER
METAL TRANSISTOR

160 VOLTS
120 WATTS



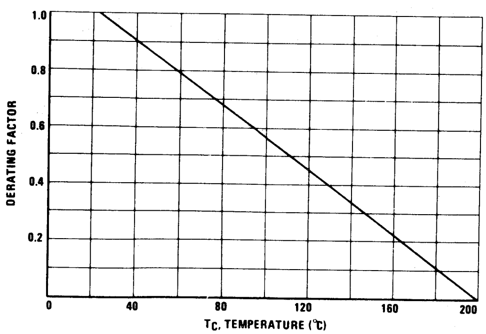
MAXIMUM RATINGS

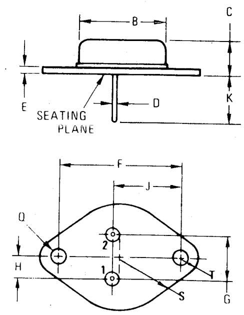
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	160	Vdc
Collector-Base Voltage	V_{CBO}	220	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = −2.5 V)	V_{CEX}	220	Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	200	Vdc
Collector-Current — continuous — peak (pw ≤ 10 ms)	I_C I_{CM}	18 25	Adc Apk
Base-Current continuous	I_B	3.6	Adc
Total Power Dissipation @ T_C = 25°C	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR
STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE-EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	-	3.43	-	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	--
Q	3.84	4.09	0.151	0.161
S	-	13.34	-	0.525
T	-	4.78	-	0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, L = 25 mH)	$V_{CEO(sus)}$	160		Vdc
Collector Cutoff Current at Reverse Biais: ($V_{CE} = 220$ V, $V_{BE} = -1.5$ V) ($V_{CE} = 220$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 130$ V)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 30$ V, t = 1 s) ($V_{CE} = 100$ V, t = 1 s)	$I_{S/b}$	4 0.27		Adc
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 8$ A, $V_{CE} = 4$ V) ($I_C = 12$ A, $V_{CE} = 4$ V)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage ($I_C = 8$ A, $I_B = 0.8$ A) ($I_C = 12$ A, $I_B = 1.5$ A)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 12$ A, $I_B = 1.5$ A)	$V_{BE(sat)}$		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product ($V_{CE} = 15$ V, $I_C = 1$ A, f = 4 MHz)	f_T	8.0		MHz

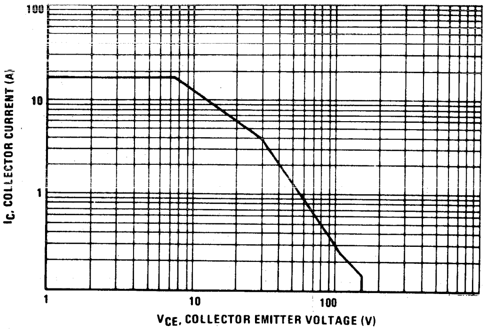
SWITCHING CHARACTERISTICS (Resistive Load)

	Conditions	Symbol	Min.	Max.	Unit
Turn on Time	$I_C = 12$ A, $I_{B1} = I_{B2} = 1.5$ A, ($V_{CC} = 30$ V, RC = 2.5 Ω)	t_{on}		1.2	μs
Storage Time		t_s		1.2	
Fall Time		t_f		0.25	

[1] Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

3

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to'values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

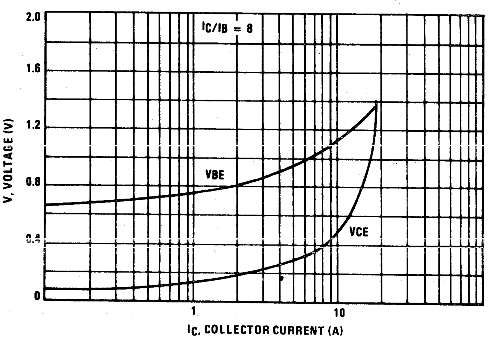


FIGURE 4 – DC CURRENT GAIN

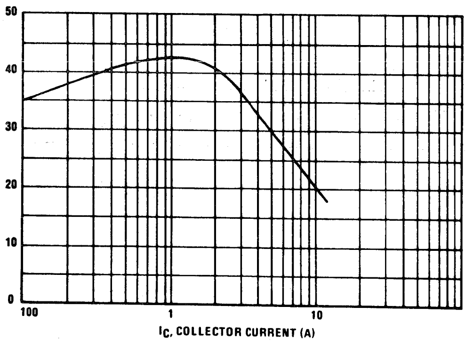


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

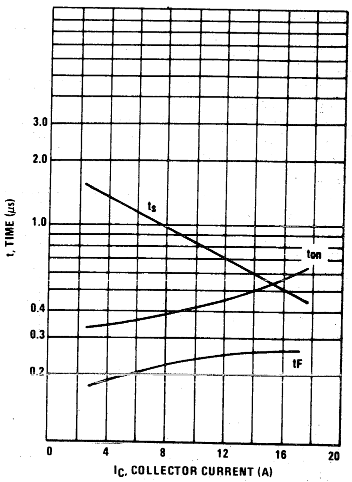
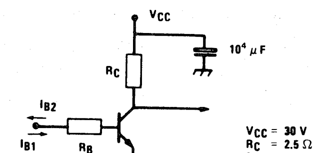


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



R_C – R_B: Non inductive resistances

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUX42

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTOR

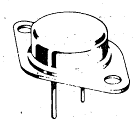
. . . designed for high speed, high voltage, high power applications.

- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 1.2 V at Ic = 4 A
- Very fast switching times:
  T_F max. = 0.4 μs at Ic = 6 A

12 AMPERES

NPN SILICON POWER METAL TRANSISTOR

250 VOLTS
120 WATTS



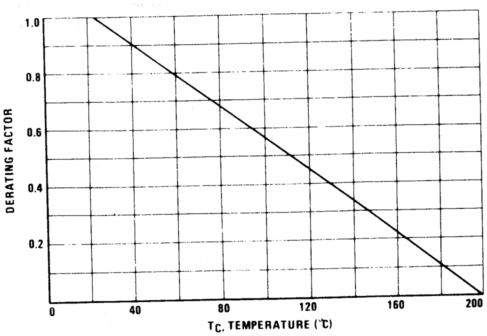
MAXIMUM RATINGS

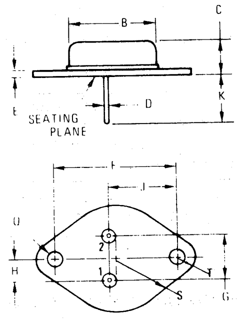
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector-Base Voltage	V_{CBO}	300	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage (V_{BE} = −2.5 V)	V_{CEX}	300	Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	290	Vdc
Collector-Current — continuous — peak (pw ⩽ 10 ms)	I_C I_{CM}	12 15	Adc Apk
Base-Current continuous	I_B	2.4	Adc
Total Power Dissipation @ T_C = 25 °C	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B		22.23	-	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E		3.43		0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92		0.312	
Q	3.84	4.09	0.151	0.161
S		13.34		0.525
T		4.78		0.188

All JEDEC dimensions and notes apply

CASE 1-03
(TO-3)

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Biais: (V_{CE} = 300 V, V_{BE} = −1.5 V) (V_{CE} = 300 V, V_{BE} = −1.5 V, T_C = 125°C)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current (V_{CE} = 200 V)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter-Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 30 V, t = 1 s) (V_{CE} = 135 V, t = 1 s)	$I_{S/b}$	4.0 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 4 A, V_{CE} = 4 V) (I_C = 6 A, V_{CE} = 4 V)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage (I_C = 4 A, I_B = 0.4 A) (I_C = 6 A, I_B = 0.75 A)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage (I_C = 6 A, I_B = 0.75 A)	$V_{BE(sat)}$		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 1 A, f = 4 MHz)	f_T	8.0		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	I_C = 6 A, I_{B1} = I_{B2} = 0.75 A, (V_{CC} = 150 V, RC = 25 Ω)	t_{on}		0.6	μs
Storage Time		t_s		2.0	
Fall Time		t_f		0.4	

[1] Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

3

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

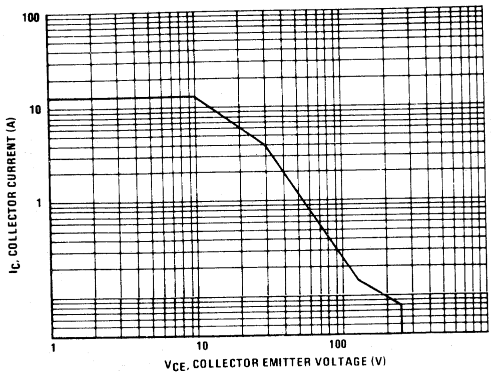


FIGURE 3 – "ON" VOLTAGES

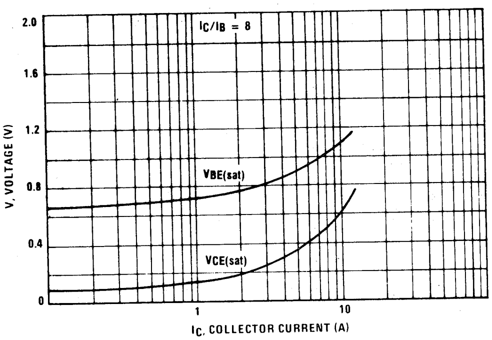
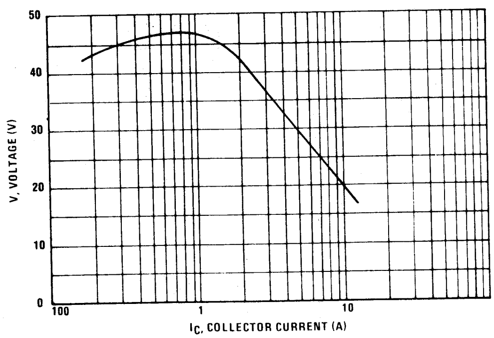


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C \cdot V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25\ C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

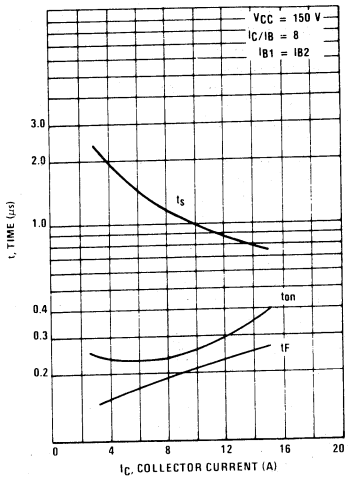
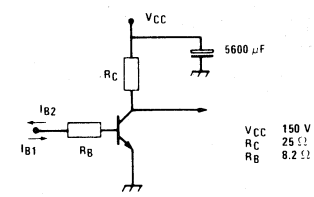


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



R_C – R_B: Non inductive resistances

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUX43

SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTOR

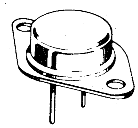
. . . designed for high speed, high voltage, high power applications.

- $V_{CE(sat)}$ max. = 1.6 V at I_C = 6 A
- Very fast switching times:
  T_F max. = 0.90 μs at I_C = 5 A

10 AMPERES

**NPN SILICON
POWER
METAL TRANSISTOR**

**325 VOLTS
120 WATTS**



MAXIMUM RATINGS

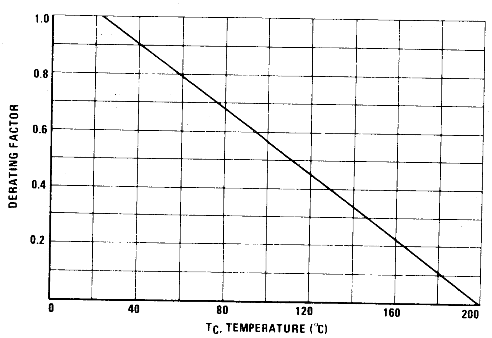
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	325	Vdc
Collector-Base Voltage	V_{CBO}	400	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5$ V)	V_{CEX}	400	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\ \Omega$)	V_{CER}	360	Vdc
Collector-Current — continuous — peak (pw ⩽ 10 ms)	I_C I_{CM}	10 12	Adc Apk
Base-Current continuous	I_B	2	Adc
Total Power Dissipation @ $T_C = 25°C$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

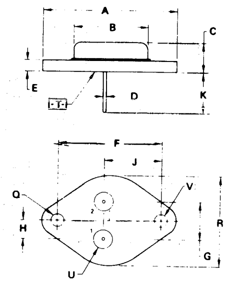
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	°C/W

3

FIGURE 1 — POWER DERATING





NOTES
1. DIMENSIONS Q AND V ARE DATUMS
2. [T] IS SEATING PLANE AND DATUM
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
   | ⌖ | ∅ 0.13 (0.005) Ⓜ | T | V Ⓜ |
   FOR LEADS
   | ⌖ | ∅ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, L = 25 mH)	$V_{CEO(sus)}$	325		Vdc
Collector Cutoff Current at Reverse Biais: ($V_{CE} = 400$ V, $V_{BE} = -1.5$ V) ($V_{CE} = 400$ V, $V_{BE} = -1.5$ V, $T_C = 125°C$)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 260$ V)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50$ mA)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased ($V_{CE} = 30$ V, t = 1 s) ($V_{CE} = 135$ V, t = 1 s)	$I_{S/b}$	4.0 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain ($I_C = 3$ A, $V_{CE} = 4$ V) ($I_C = 5$ A, $V_{CE} = 4$ V)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage ($I_C = 3$ A, $I_B = 0.375$ A) ($I_C = 5$ A, $I_B = 1$ A)	$V_{CE(sat)}$		1.0 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 5$ A, $I_B = 1$ A)	$V_{BE(sat)}$		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product ($V_{CE} = 15$ V, $I_C = 1$ A, f = 4 MHz)	f_T	8.0		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Characteristic	Conditions	Symbol	Min.	Max.	Unit
Turn on Time	$I_C = 5$ A, $I_{B1} = I_{B2} = 1$ A, ($V_{CC} = 150$ V, RC = 30 Ω)	t_{on}		1.0	μs
Storage Time		t_s		2.2	
Fall Time		t_f		0.9	

[1] Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

3

FIGL RE 2 – ACTIVE REGION SAFE OPERATING AREA

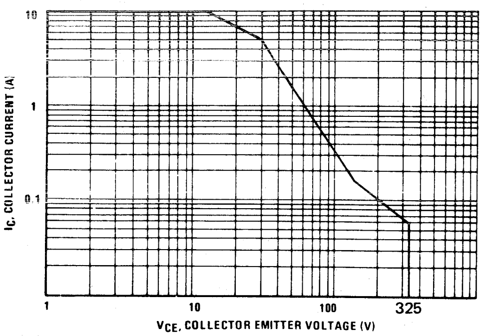


FIGURE 3 – "ON" VOLTAGES

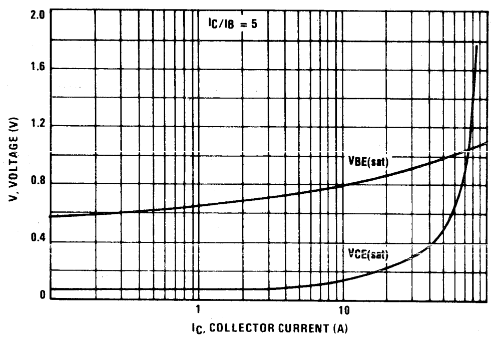
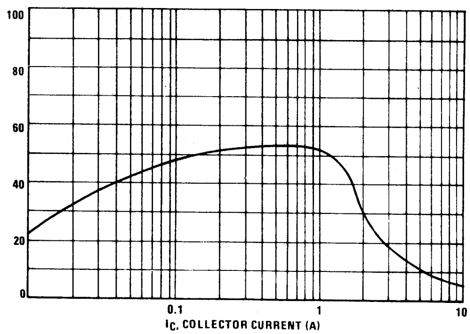


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25°C$, $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

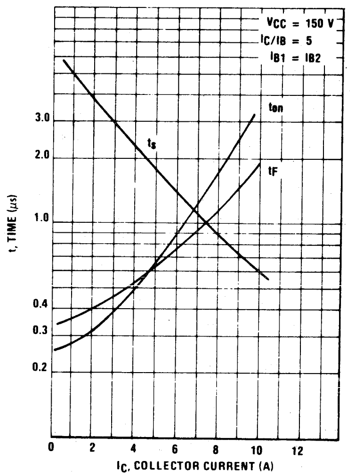
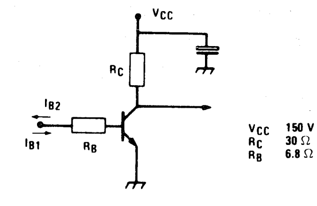


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



R_C – R_B : Non inductive resistances

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUX84
BUX85

SWITCHMODE
NPN SILICON POWER TRANSISTORS

The BUX 84/85 are designed for high voltage, high speed power switching applications like converters, inverters, switching regulators, motor control systems.

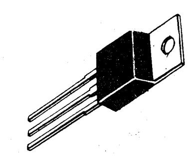
SPECIFICATIONS FEATURES:

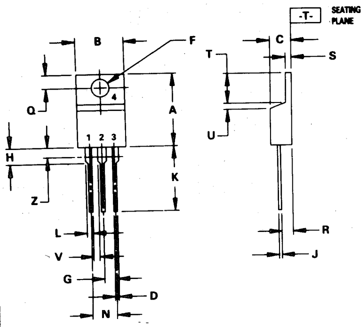
- $V_{CEO(sus)}$ { 400 V BUX 84; 450 V BUX 85
- $V_{CES(sus)}$ { 800 V BUX 84; 1000 V BUX 85
- Fall time = 0.3 us (typ) at I_C = 1 A
- $V_{CE(sat)}$ = 1 V (max) at I_C = 1 A, I_B = 0.2 A

2 AMPERES

TRIPLE DIFFUSED POWER TRANSISTORS NPN SILICON

400 - 450 VOLTS
50 WATTS





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	BUX 84	BUX 85	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CES}	800	1000	Vdc
Emitter Base Voltage	V_{EBO}	5		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	2 3.0		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	0.75 1.0		Adc
Reverse Base Current: – Peak	I_{BM}	1		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 400		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambien:	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, (L = 25 mH) See fig. 1) BUX 84	$V_{CEO(sus)}$	400	–	–	Vdc
BUX 85		450	–	–	
Collector Cutoff Current (V_{CES} = Rated Value)	I_{CES}	–	–	0.2	mAdc
(V_{CES} = Rated Value, T_C = 125 °C)		–	–	1.5	
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc

ON CHARACTERISTICS (1)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 5 V)	h_{FE}	30	50	–	–
Collector-Emitter Saturation Voltage (I_C = 0.3 Adc, I_B = 30 mAdc)	$V_{CE(sat)}$	–	–	0.8	Vdc
(I_C = 1 Adc, I_B = 200 mAdc)		–	–	1	
Base-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	$V_{BE(sat)}$	–	–	1.1	Vdc

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	–	–	MHz

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Turn-on Time	V_{CC} = 250 Vdc, I_C = 1 A	t_{on}	–	0.3	0.5	μs
Storage Time	I_{B1} = 0.2 A, I_{B2} = 0.4 A	t_s	–	2	3.5	μs
Fall Time	See fig. 2	t_f	–	0.3	–	μs
Fall Time	Same above cond. at T_C = 95°C	t_f	–	–	1.4	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 1 – TEST CIRCUIT FOR $V_{CEO\,sust}$

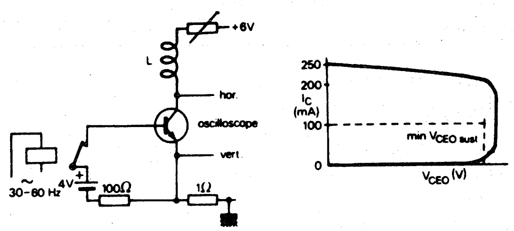
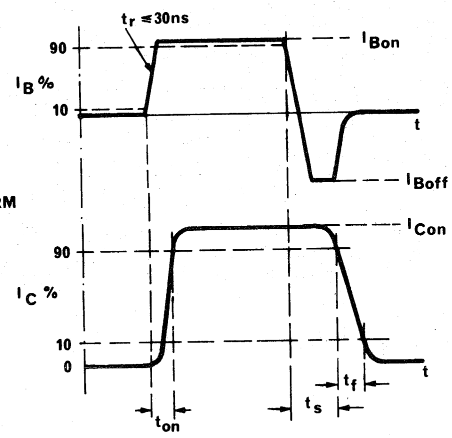
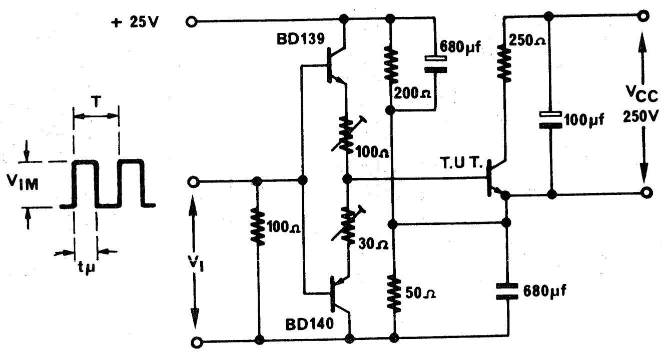


FIGURE 2 – SWITCHING TIMES / TEST CIRCUIT

WAVEFORM





3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
D44E Series
PNP
D45E Series

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

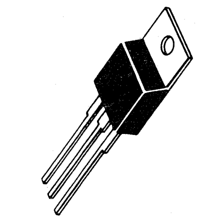
. . . for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)} = 2.0$ V (Max) @ 10 A
- High DC Current Gain — 1000 (Min) @ 5.0 Adc
- Complementary Pairs Simplifies Designs

DARLINGTON
10 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40-80 VOLTS
50 WATTS



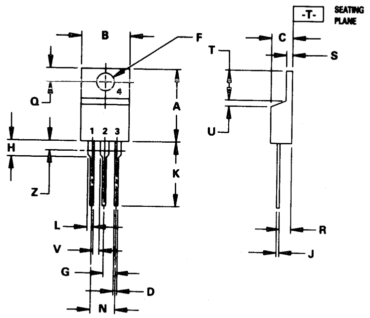
MAXIMUM RATINGS

Rating	Symbol	D44E or D45E 1	2	3	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter Base Voltage	V_{EB}		7.0		Vdc
Collector Current — Continuous Peak (1)	I_C		10 20		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_A = 25°C$	P_D		50 1.67		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.



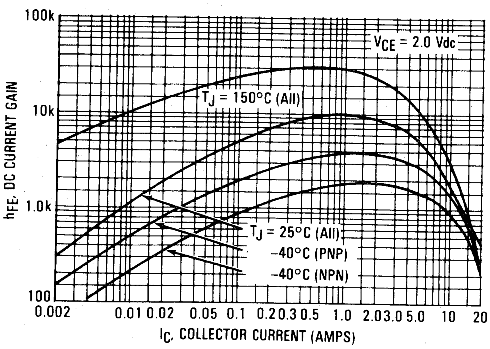
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

FIGURE 1 — TYPICAL DC CURRENT GAIN



3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)	I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 7.0 Vdc)	I_{EBO}	—	—	1.0	μA
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	1000	—	—	—
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 10 mAdc) (I_C = 10 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	— —	— —	1.5 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 10 mAdc)	$V_{BE(sat)}$	—	—	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1.0 MHz) D44E Series D45E Series	C_{CBO}	— —	— —	130 220	pF
SWITCHING CHARACTERISTICS					
Delay and Rise Times (I_C = 10 Adc, I_{B1} = 20 mAdc)	$t_d + t_r$	—	0.6	—	μs
Storage Time (I_C = 10 Adc, I_{B1} = I_{B2} = 20 mAdc)	t_s	—	2.0	—	μs
Fall Time (I_C = 10 Adc, I_{B1} = I_{B2} = 20 mAdc)	t_f	—	0.5	—	μs

SAFE OPERATING AREA INFORMATION

FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (NPN)

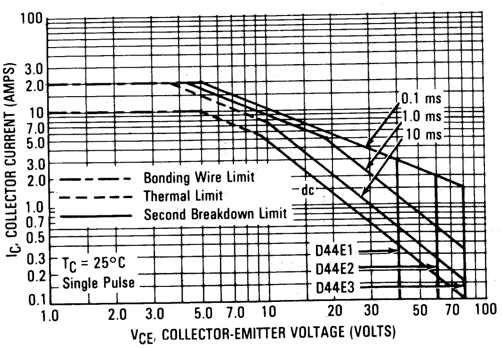
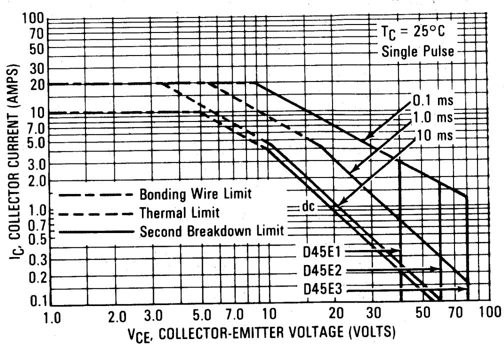


FIGURE 3 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (PNP)



3

NPN D44H Series PNP D45H Series

COMPLEMENTARY SILICON POWER TRANSISTORS

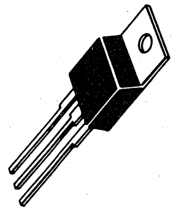
. . . for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

10 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

30-80 VOLTS



MAXIMUM RATINGS

Rating	Symbol	D44H or D45H 1,2	4,5	7,8	10,11	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	60	80	Vdc
Emitter Base Voltage	V_{EB}	5.0				Vdc
Collector Current — Continuous Peak (1)	I_C	10 20				Adc
Total Power Dissipation @ T_C = 25°C @ T_A = 25°C	P_D	50 1.67				Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				°C

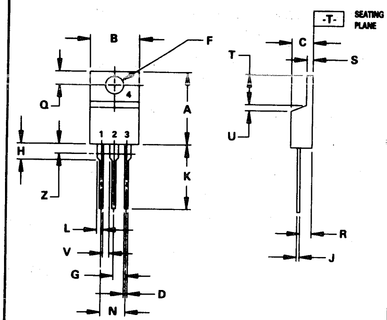
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
DC Current Gain (V_{CE} = 1.0 Vdc, I_C = 2.0 Adc)	D44H1,4,7,10 D45H1,4,7,10	h_{FE}	35	—	—
	D44H2,5,8,11 D45H2,5,8,11		60	—	
(V_{CE} = 1.0 Vdc, I_C = 4.0 Adc)	D44H1,4,7,10 D45H1,4,7,10		20	—	
	D44H2,5,8,11 D45H2,5,8,11		40	—	



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
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L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)	I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)	I_{EBO}	—	—	100	μA
ON CHARACTERISTICS					
Collector-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.4 Adc) D44H/D45H2,5,8,11 (I_C = 8.0 Adc, I_B = 0.8 Adc) D44H/D45H1,4,7,10	$V_{CE(sat)}$	— —	— —	1.0 1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.8 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1.0 MHz) D44H Series D45H Series	C_{cb}	— —	130 230	— —	pF
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz) D44H Series D45H Series	f_T	— —	50 40	— —	MHz
SWITCHING TIMES					
Delay and Rise Times (I_C = 5.0 Adc, I_{B1} = 0.5 Adc) D44H Series D45H Series	$t_d + t_r$	— —	300 135	— —	ns
Storage Time (I_C = 5.0 Adc, I_{B1} = I_{B2} = 0.5 Adc) D44H Series D45H Series	t_s	— —	500 500	— —	ns
Fall Time (I_C = 5.0 Adc, I_{B1} = I_{B2} = 0.5 Adc) D44H Series D45H Series	t_f	— —	140 100	— —	ns

3

FIGURE 1 — NORMALIZED DC CURRENT GAIN

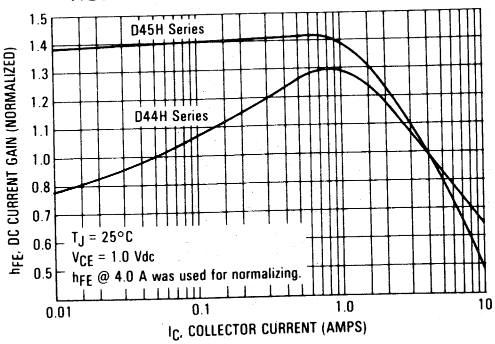
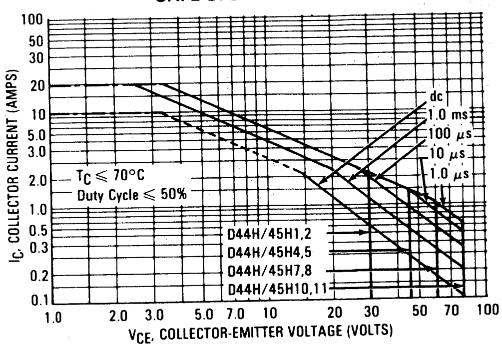


FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
D44VH Series
PNP
D45VH Series

COMPLEMENTARY SILICON POWER TRANSISTORS

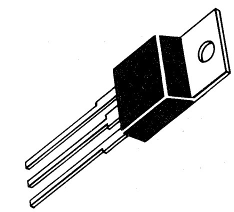
These complementary silicon power transistors are designed for high-speed switching applications, such as switching regulators and high frequency inverters. The devices are also well-suited for drivers for high power switching circuits.

- Fast Switching — t_f = 90 ns (Max)
- Key Parameters Specified @ 100°C
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Complementary Pairs Simplify Circuit Designs

15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

30, 45, 60 and 80 VOLTS
83 WATTS



MAXIMUM RATINGS

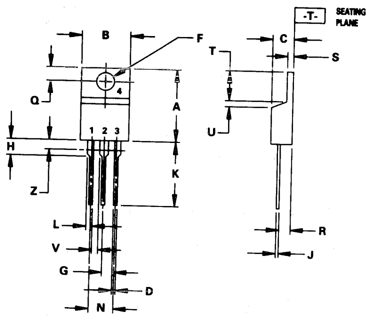
Rating	Symbol	D44VH or D45VH 1	4	7	10	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	60	80	Vdc
Collector-Emitter Voltage	V_{CEV}	50	70	80	100	Vdc
Emitter Base Voltage	V_{EB}	7.0				Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	15 20				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	83 1.67				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

Note 1: All polarities are shown for NPN transistors. For PNP transistors, reverse polarities.
Note 2: See MJE5220/5230 Series data sheet for characteristic curves.



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B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
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N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 25 mAdc, I_B = 0) D44VH1, D45VH1	$V_{CEO(sus)}$	30	—	—	Vdc
D44VH4, D45VH4		45	—	—	
D44VH7, D45VH7		60	—	—	
D44VH10, D45VH10		80	—	—	
Collector-Emitter Cutoff Current (V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc)	I_{CEV}	—	—	10	μAdc
(V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc, T_C = 100°C)		—	—	100	
Emitter Base Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	35	—	—	—
(I_C = 4.0 Adc, V_{CE} = 1.0 Vdc)		20	—	—	
Collector-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.4 Adc) D44VH Series	$V_{CE(sat)}$	—	—	0.4	Vdc
(I_C = 8.0 Adc, I_B = 0.8 Adc) D45VH Series		—	—	1.0	
(I_C = 15 Adc, I_B = 3.0 Adc, T_C = 100°C) D44VH Series		—	—	0.8	
D45VH Series		—	—	1.5	
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.4 Adc) D44VH Series	$V_{BE(sat)}$	—	—	1.2	Vdc
(I_C = 8.0 Adc, I_B = 0.8 Adc) D45VH Series		—	—	1.0	
(I_C = 8.0 Adc, I_B = 0.4 Adc, T_C = 100°C) D44VH Series		—	—	1.1	
(I_C = 8.0 Adc, I_B = 0.8 Adc, T_C = 100°C) D45VH Series		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	—	50	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_C = 0, f_{test} = 1.0 MHz) D44VH Series	C_{cb}	—	120	—	pF
D45VH Series		—	275	—	
SWITCHING CHARACTERISTICS					
Delay Time (V_{CC} = 20 Vdc, I_C = 8.0 Adc, I_{B1} = I_{B2} = 0.8 Adc)	t_d	—	—	50	ns
Rise Time	t_r	—	—	250	
Storage Time	t_s	—	—	700	
Fall Time	t_f	—	—	90	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

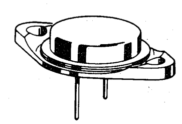
MJ410
MJ411

HIGH VOLTAGE NPN SILICON TRANSISTORS

. . . designed for medium to high voltage inverters, converters, regulators and switching circuits.

- High Collector-Emitter Voltage –
  V_{CEO} = 200 Volts – MJ410
  300 Volts – MJ411
- DC Current Gain Specified @ 1.0 and 2.5 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.8 Vdc @ I_C = 1.0 Adc

5 AMPERE
POWER TRANSISTORS
NPN SILICON
200–300 VOLTS
100 WATTS



MAXIMUM RATINGS

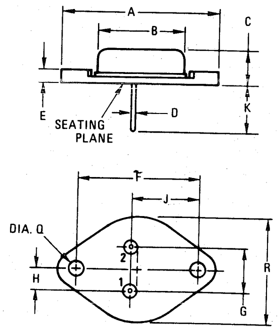
Rating	Symbol	MJ410	MJ411	Unit
Collector-Emitter Voltage	V_{CEO}	200	300	Vdc
Collector-Base Voltage	V_{CB}	200	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	5.0 10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	100 1.33		Watts W/°C
Operating Junction Temperature Range	T_J	-65 to +150		°C
Storage Temperature Range	T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	MJ410 MJ411	$V_{CEO(sus)}$	200 300	– –	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	MJ410 MJ411	I_{CEO}	– –	0.25 0.25	mAdc
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 300 Vdc, $V_{EB(off)}$ - 1.5 Vdc, T_C = 125°C)	MJ410 MJ411	I_{CEX}	– –	0.5 0.5	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	30 10	90 –	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.5	–	MHz



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

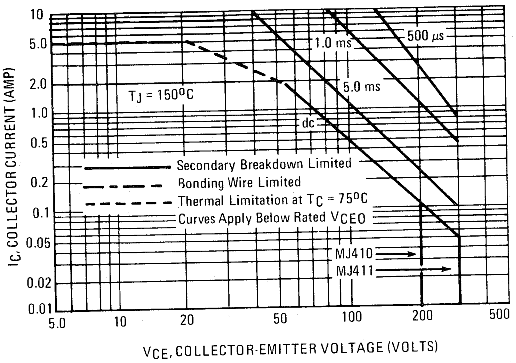
NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-3

3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 2 – DC CURRENT GAIN

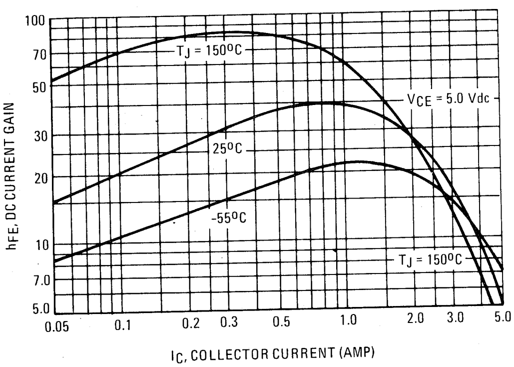


FIGURE 3 – "ON" VOLTAGES

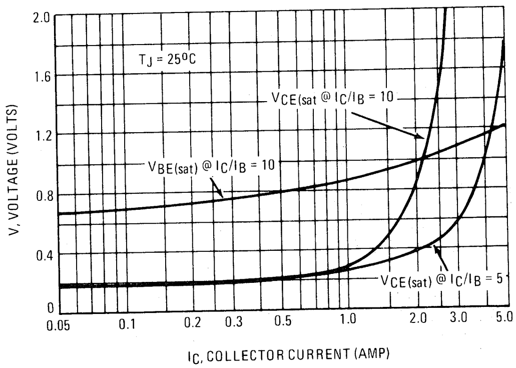


FIGURE 4 – SUSTAINING VOLTAGE TEST LOAD LINE

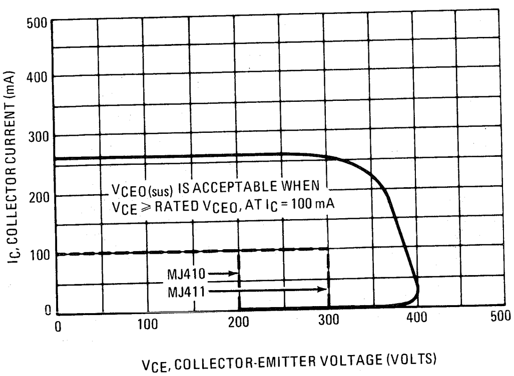
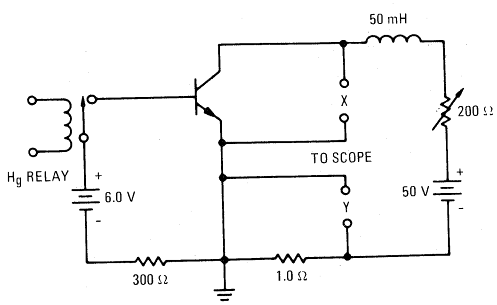


FIGURE 5 – SUSTAINING VOLTAGE TEST CIRCUIT



3

MJ413
MJ423
MJ431

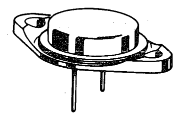
HIGH-VOLTAGE NPN SILICON TRANSISTORS

. . . designed for medium-to-high voltage inverters, converters, regulators and switching circuits.

- High Voltage — V_{CEX} = 400 Vdc
- Gain Specified to 3.5 Amp
- High Frequency Response to 2.5 MHz

10 AMPERE
POWER TRANSISTORS
NPN SILICON

400 VOLTS
125 WATTS



MAXIMUM RATINGS

Rating	Symbol	MJ413	MJ423	MJ431	Unit
Collector-Emitter Voltage	V_{CEX}	400	400	400	Vdc
Collector-Base Voltage	V_{CB}	400	400	400	Vdc
Emitter-Base Voltage	V_{EB}	5.0	5.0	5.0	Vdc
Collector Current — Continuous	I_C	10	10	10	Adc
Base Current	I_B	2.0	2.0	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		125 1.0		Watts W/°C
Operation Junction Temperature Range	T_J		-65 to +150		°C
Storage Temperature Range	T_{stg}		-65 to +200		°C

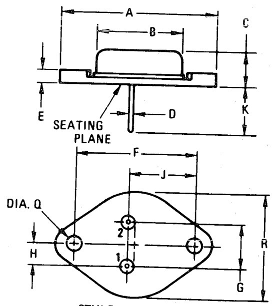
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage*(1) (I_C = 100 mAdc, I_B = 0)		$V_{(BR)CEO(sus)}$	325	—	Vdc
Collector Cutoff Current (V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	MJ413, MJ423 MJ431	I_{CEX}	— —	0.25 2.5	mAdc
(V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	MJ413, MJ423 MJ431		— —	0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	MJ413, MJ423 MJ431	I_{EBO}	— —	5.0 2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	MJ413	h_{FE}	20 15	80 —	—
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	MJ423		30 10	90 —	
(I_C = 2.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 3.5 Adc, V_{CE} = 5.0 Vdc)	MJ431		15 10	35 —	
Collector-Emitter Saturation Voltage (1) (I_C = 0.5 Adc, I_B = 0.05 Adc) (I_C = 1.0 Adc, I_B = 0.10 Adc) (I_C = 2.5 Adc, I_B = 0.5 Adc)	 MJ413 MJ423 MJ431	$V_{CE(sat)}$	 — — —	 0.8 0.8 0.7	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 0.5 Adc, I_B = 0.05 Adc) (I_C = 1.0 Adc, I_B = 0.1 Adc) (I_C = 2.5 Adc, I_B = 0.5 Adc)	 MJ413 MJ423 MJ431	$V_{BE(sat)}$	 — — —	 1.25 1.25 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10Vdc, f = 1.0 MHz)		f_T	2.5	—	MHz

(1) PW ≤ 300 μs, Duty Cycle ≤ 2.0%



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-3

FIGURE 1 — ACTIVE-REGION SAFE-OPERATING AREA

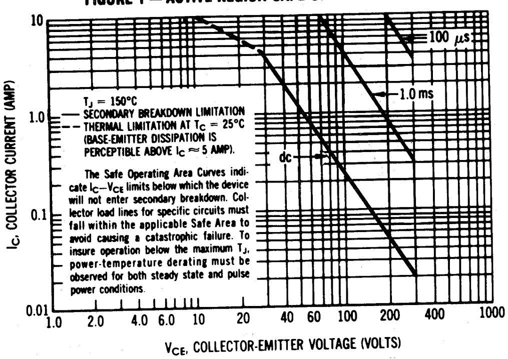


FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

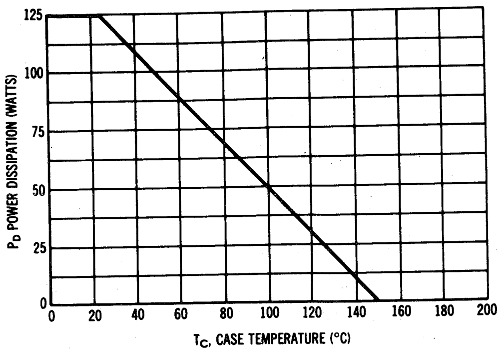


FIGURE 3 — SUSTAINING VOLTAGE TEST LOAD LINE

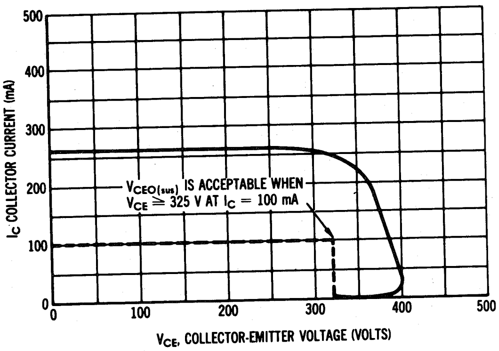


FIGURE 4 — SUSTAINING VOLTAGE TEST CIRCUIT

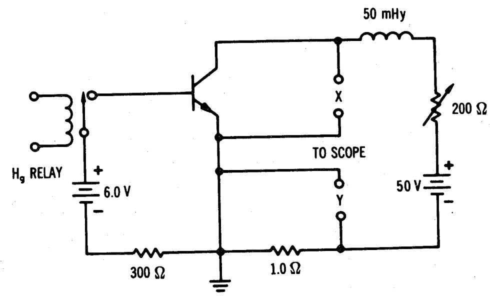


FIGURE 5 — CURRENT GAIN

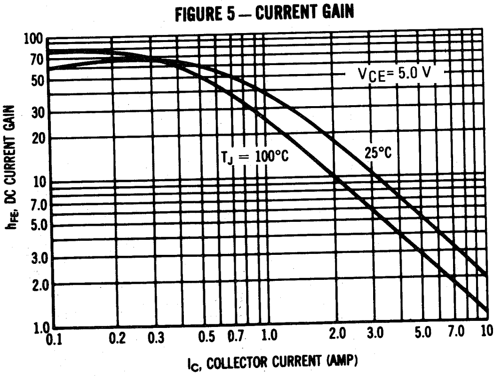
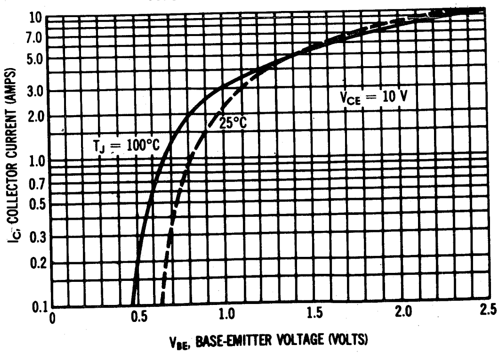


FIGURE 6 — TRANSCONDUCTANCE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ802

HIGH-POWER NPN SILICON TRANSISTOR

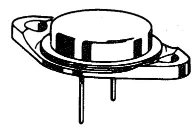
. . . for use as an output device in complementary audio amplifiers to 100-Watts music power per channel.

- High DC Current Gain – h_{FE} = 25–100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the PNP MJ4502

30 AMPERE POWER TRANSISTOR

NPN SILICON

100 VOLTS
200 WATTS



MAXIMUM RATINGS

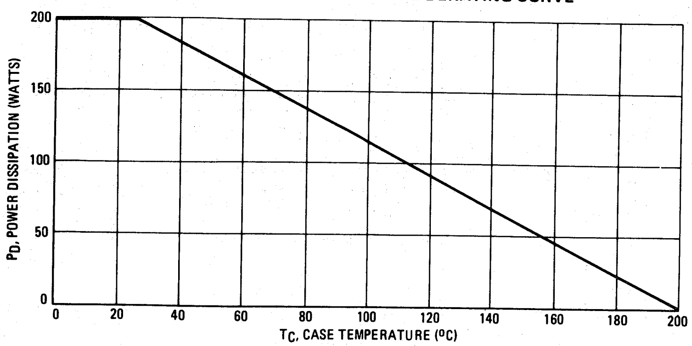
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CER}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Collector-Emitter Voltage	V_{CEO}	90	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

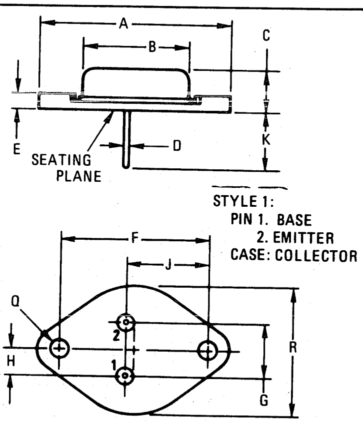
3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	BV_{CER}	100	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	– –	1.0 5.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (1) (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter "On" Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.3	Vdc
Collector-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

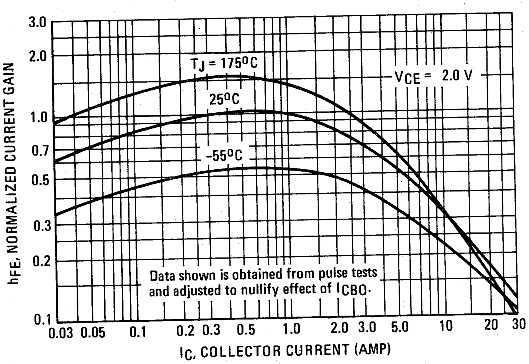


FIGURE 3 – "ON" VOLTAGES

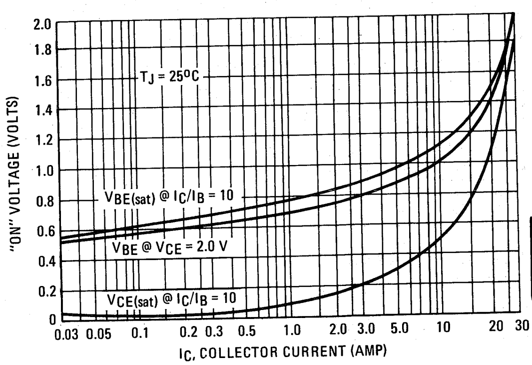
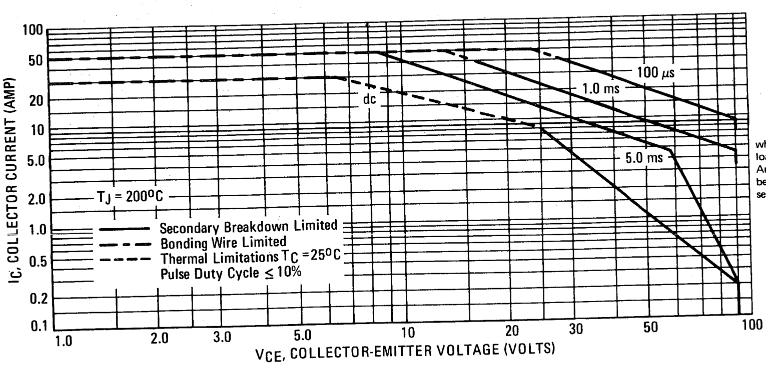


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
MJ900, MJ901
NPN
MJ1000, MJ1001

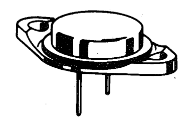
MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 6000 (Typ) @ I_C = 3.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

8.0 AMPERE DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

60–80 VOLTS
90 WATTS

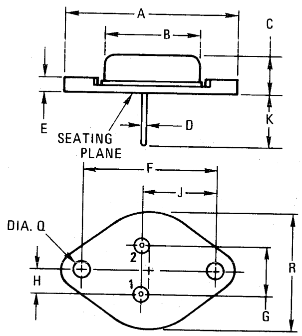


MAXIMUM RATINGS

Rating	Symbol	MJ900 MJ1000	MJ901 MJ1001	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	8.0		Adc
Base Current	I_B	0.1		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	90 0.515		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.94	°C/W



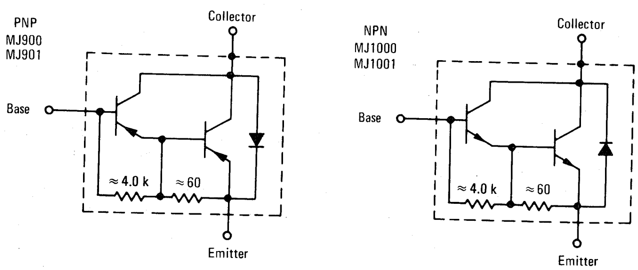
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

FIGURE 1 — DARLINGTON CIRCUIT SCHEMATIC



3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 100 mAdc, I_B = 0)	MJ900, MJ1000	$V_{(BR)CEO}$	60	–	Vdc
	MJ901, MJ1001		80	–	
Collector Emitter Leakage Current (V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ900, MJ1000	I_{CER}	–	1.0	mAdc
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ901, MJ1001		–	1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ900, MJ1000		–	5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ901, MJ1001		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
Collector-Emitter Leakage Current (V_{CE} = 30 Vdc, I_B = 0)	MJ900, MJ1000	I_{CEO}	–	500	μAdc
(V_{CE} = 40 Vdc, I_B = 0)	MJ901, MJ1001		–	500	
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	–	–
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			750	–	
Collector-Emitter Saturation Voltage(1) (I_C = 3.0 Adc, I_B = 12 mAdc)		$V_{CE(sat)}$	–	2.0	Vdc
(I_C = 8.0 Adc, I_B = 40 mAdc)			–	4.0	
Base-Emitter Voltage(1) (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		V_{BE}	–	2.5	Vdc

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — DC CURRENT GAIN

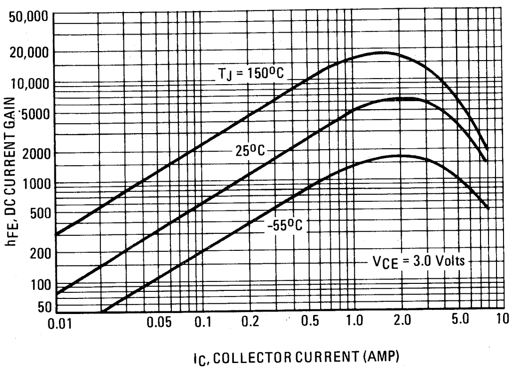


FIGURE 3 — SMALL-SIGNAL CURRENT GAIN

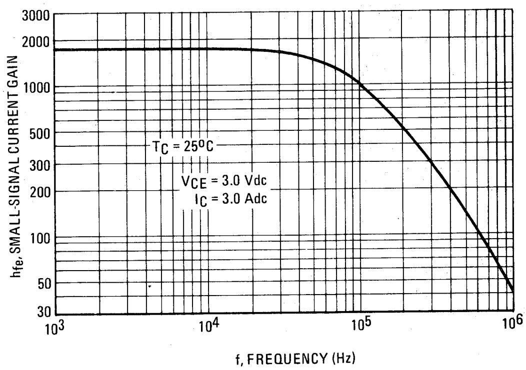


FIGURE 4 — "ON" VOLTAGES

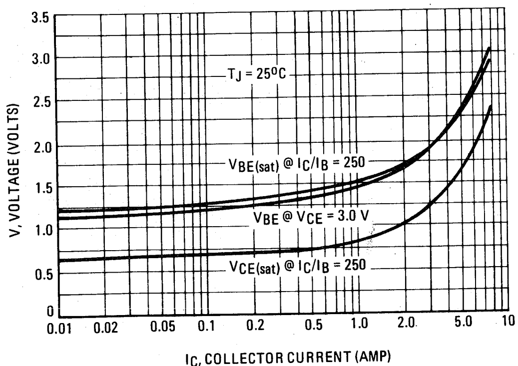
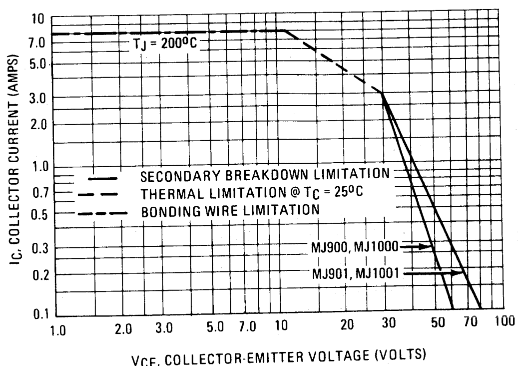


FIGURE 5 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
MJ2500, MJ2501
NPN
MJ3000, MJ3001

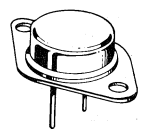
MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 4000 (Typ) @ I_C = 5.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

10 AMPERE DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

60–80 VOLTS
150 WATTS



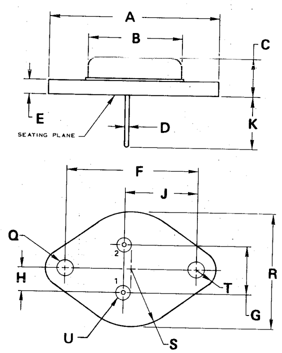
MAXIMUM RATINGS

Rating	Symbol	MJ2500 MJ3000	MJ2501 MJ3001	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	10		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

3



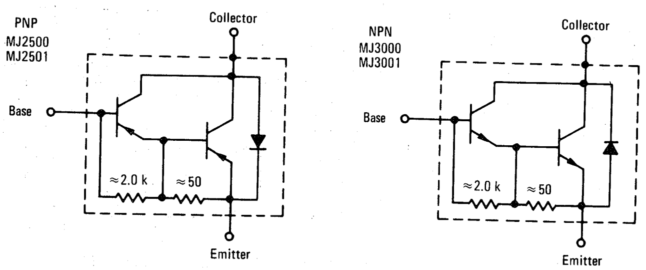
STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1–04

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

FIGURE 1 — DARLINGTON CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ2500, MJ3000 MJ2501, MJ3001	$V_{(BR)CEO}$	60 80	– –	Vdc
Collector-Emitter Leakage Current (V_{EB} = 60 Vdc, R_{BE} = 1.0 k ohm) (V_{EB} = 80 Vdc, R_{BE} = 1.0 k ohm) (V_{EB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C) (V_{EB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ2500, MJ3000 MJ2501, MJ3001 MJ2500, MJ3000 MJ2501, MJ3001	I_{CER}	– – – –	1.0 1.0 5.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
Collector-Emitter Leakage Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	MJ2500, MJ3000 MJ2501, MJ3001	I_{CEO}	– –	1.0 1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	–	–
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 20 mAdc) (I_C = 10 Adc, I_B = 50 mAdc)		$V_{CE(sat)}$	– –	2.0 4.0	Vdc
Base-Emitter Voltage (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		V_{BE}	–	3.0	Vdc

(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 2 – DC CURRENT GAIN

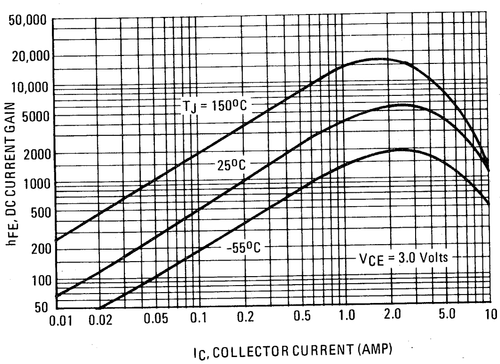


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

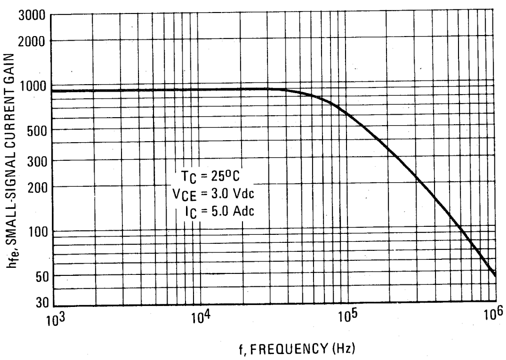


FIGURE 4 – "ON" VOLTAGES

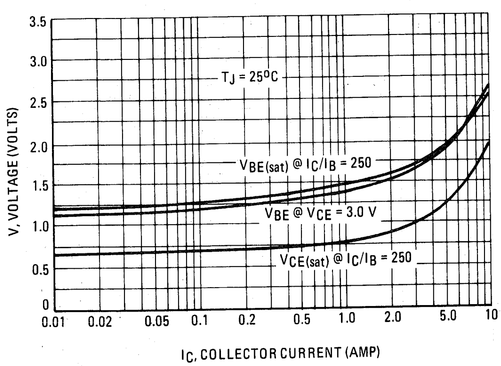
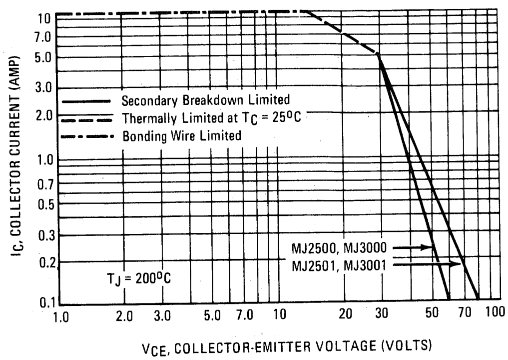


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ2955 — See Pg. 3-6
MJ2955A — See Pg. 3-9

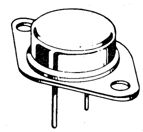
MJ3029

NPN SILICON HIGH-VOLTAGE TRANSISTOR

. . . designed for TV horizontal and vertical deflection amplifier circuits.

- High Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 250 Vdc (Min) MJ3029
- Fast Fall Time in Horizontal Deflection
- Excellent Gain Linearity for Vertical Deflection — h_{fe} @ 0.4 Adc, h_{fe} @ 0.3 Adc = 0.95 (Min)

5 AMPERE
POWER TRANSISTOR
NPN SILICON
250-325 VOLTS
125 WATTS



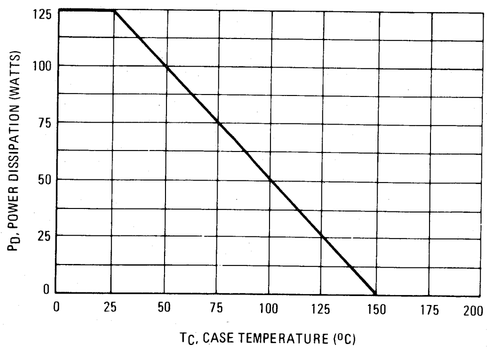
MAXIMUM RATINGS

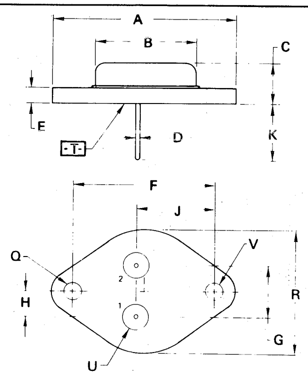
Rating	Symbol	MJ3029	Unit
Collector-Emitter Voltage	V_{CEO}	250	Vdc
Collector-Emitter Voltage	V_{CER}	500	Vdc
Collector-Emitter Voltage	V_{CEX}	–	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	5.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ϕ.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ϕ.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage(1) (I_C = 0.1 Adc, I_B = 0)	MJ3029	$V_{CEO(sus)}$	250	–	Vdc
Collector Cutoff Current (V_{CE} = 500 Vdc, R_{BE} = 1.5 k Ohms)	MJ3029	I_{CER}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 5.0 Vdc)(1)		h_{FE1}	25	–	–
(I_C = 0.4 Adc, V_{CE} = 5.0 Vdc)(1)		h_{FE2}	30	–	
Gain Linearity		$\frac{h_{FE2}}{h_{FE1}}$	0.95	–	–

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — DC CURRENT GAIN

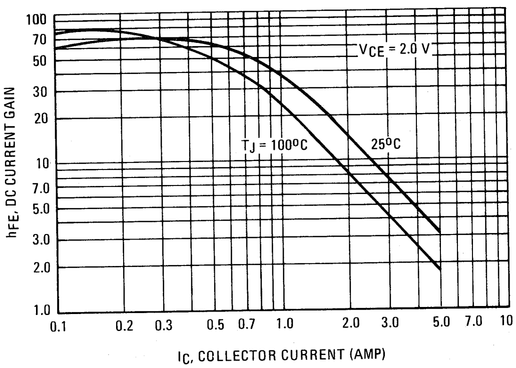
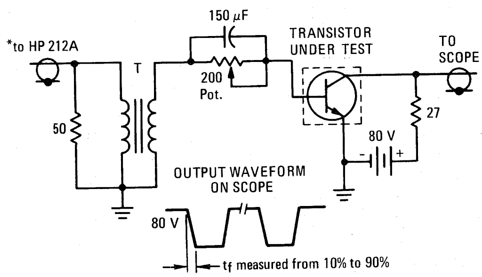
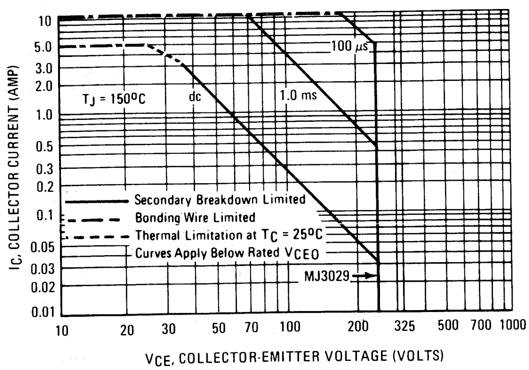


FIGURE 3 — TEST FOR FALL TIME



*HP 212A: Set for 10 μs wide pulses at 2000 pulses per sec. (500 μs intervals). Adjust for I_{B1} = 0.8 A.
Bias: Adjust to 1.5 V on a VTVM across the 200 Ω Pot.
T: Pulse Transformer: Motorola Part No. 25D68782A01.

FIGURE 4 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ3040
MJ3041
MJ3042

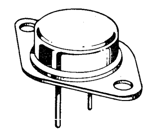
HIGH VOLTAGE SILICON POWER DARLINGTONS

. . . developed for line operated amplifier, series pass and switching regulator applications.

- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 300 Vdc (Min) – MJ3040, MJ3041
  = 350 Vdc (Min) – MJ3042
- High DC Current Gain –
  h_{FE} = 100 (Min) @ I_C = 2.5 Adc – MJ3040
  = 250 (Min) @ I_C = 2.5 Adc – MJ3041, MJ3042
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.2 Vdc (Max) @ I_C = 2.5 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON
10 AMPERE
POWER TRANSISTORS
NPN SILICON

300, 350 VOLTS
175 WATTS



MAXIMUM RATINGS

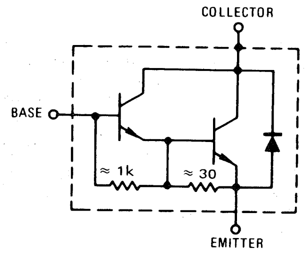
Rating	Symbol	MJ3040	MJ3041	MJ3042	Unit
Collector-Base Voltage	V_{CB}	400	400	500	Vdc
Collector-Emitter Voltage	V_{CEO}	300	300	350	Vdc
Emitter-Base Voltage	V_{EB}	← 8.0 →			Vdc
Collector Current – Continuous – Peak (1)	I_C	← 10 → ← 15 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 175 → ← 1.0 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← –65 to +200 →			°C

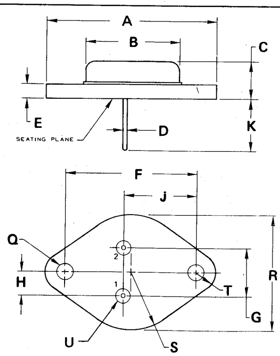
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

(1) Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

DARLINGTON SCHEMATIC





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120

CASE 1–04

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	MJ3040, MJ3041 MJ3042	$V_{CEO(sus)}$	300 350	– –	Vdc
Collector Cutoff Current (V_{CB} = 400 Vdc, I_E = 0) (V_{CB} = 500 Vdc, I_E = 0) (V_{CB} = 400 Vdc, I_E = 0, T_C = 100°C) (V_{CB} = 500 Vdc, I_E = 0, T_C = 100°C)	 MJ3040, MJ3041 MJ3042 MJ3040, MJ3041 MJ3042	I_{CBO}	 – – – –	 1.0 1.0 5.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	40	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	 MJ3040 MJ3041, MJ3042 MJ3040 MJ3041, MJ3042	h_{FE}	 100 250 25 50	 – – –	–
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 50 mAdc) (I_C = 5.0 Adc, I_B = 400 mAdc)		$V_{CE(sat)}$	 – –	 2.2 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 400 mAdc)		$V_{BE(sat)}$	–	3.0	Vdc
Base-Emitter On Voltage (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	2.5	Vdc

FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA

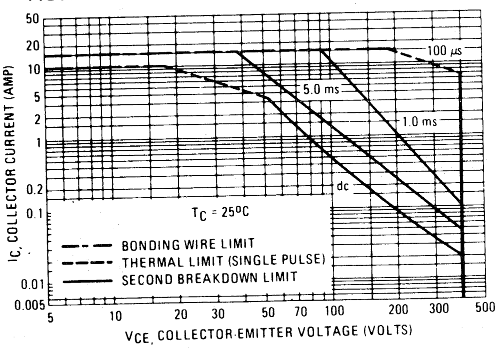
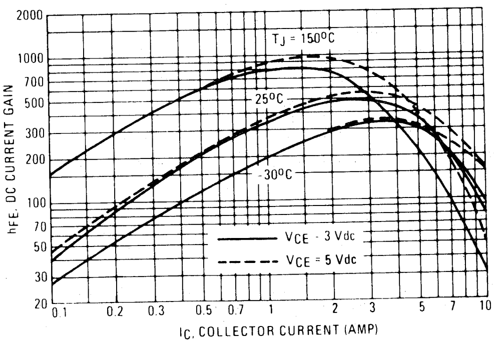


FIGURE 2 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor – average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

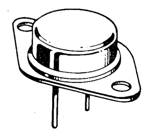
PNP	NPN
MJ4030	**MJ4033**
MJ4031	**MJ4034**
MJ4032	**MJ4035**

MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 3500 (Typ) @ I_C = 10 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor

16 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON
60–100 VOLTS
150 WATTS



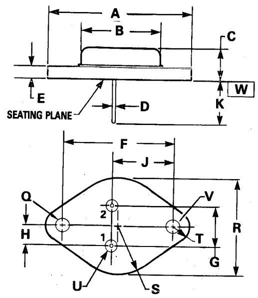
MAXIMUM RATINGS

Rating	Symbol	MJ4030 MJ4033	MJ4031 MJ4034	MJ4032 MJ4035	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current	I_C	16			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	150 0.857			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

3



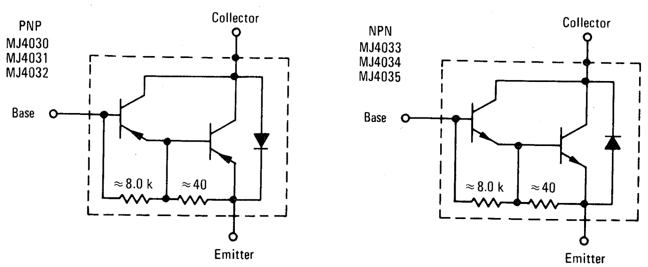
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⌖ φ 0.25 (0.010) Ⓜ W V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⌖ φ 0.30 (0.012) Ⓜ W V Ⓜ Q Ⓜ

CASE 1-04
TO-204AA

FIGURE 1 — DARLINGTON CIRCUIT SCHEMATIC



PNP MJ4030, MJ4031, MJ4032
NPN MJ4033, MJ4034, MJ4035

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ4030, MJ4033 MJ4031, MJ4034 MJ4032, MJ4035	$V_{(BR)CEO}$	60 80 100	– – –	Vdc
Collector Emitter Leakage Current (V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm) (V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm) (V_{CB} = 100 Vdc, R_{BE} = 1.0 k ohm) (V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C) (V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C) (V_{CB} = 100 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4030, MJ4033 MJ4031, MJ4034 MJ4032, MJ4035 MJ4030, MJ4033 MJ4031, MJ4034 MJ4032, MJ4035	I_{CER}	– – – – – –	1.0 1.0 1.0 5.0 5.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
Collector-Emitter Leakage Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	MJ4030, MJ4033 MJ4031, MJ4034 MJ4032, MJ4035	I_{CEO}	– – –	3.0 3.0 3.0	mAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	–	–
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 40 mAdc) (I_C = 16 Adc, I_B = 80 mAdc)		$V_{CE(sat)}$	– –	2.5 4.0	Vdc
Base-Emitter Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		V_{BE}	–	3.0	Vdc

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — DC CURRENT GAIN

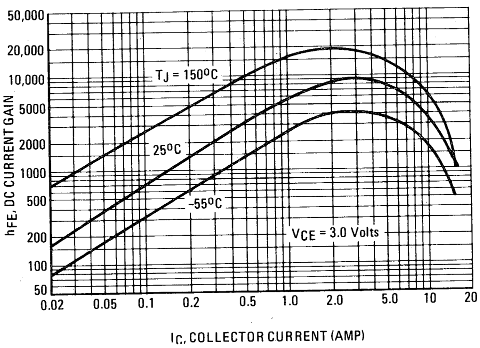


FIGURE 3 — SMALL-SIGNAL CURRENT GAIN

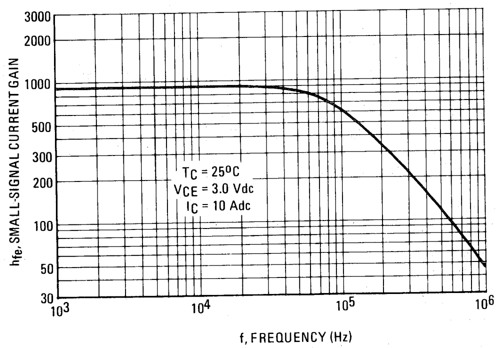


FIGURE 4 — "ON" VOLTAGES

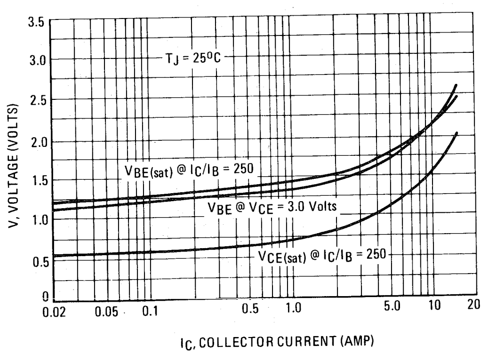
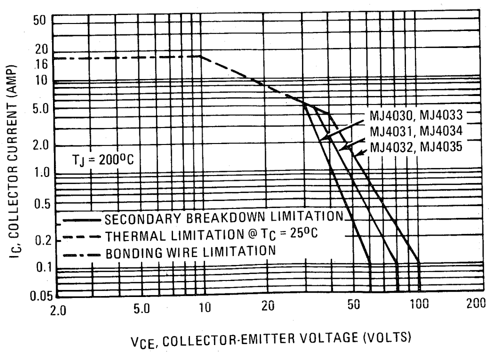


FIGURE 5 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ4502

HIGH-POWER PNP SILICON TRANSISTOR

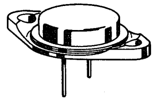
. . . for use as an output device in complementary audio amplifiers to 100-Watts music power per channel.

- High DC Current Gain — h_{FE} = 25–100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the NPN MJ802

30 AMPERE POWER TRANSISTOR

PNP SILICON

100 VOLTS
200 WATTS



MAXIMUM RATINGS

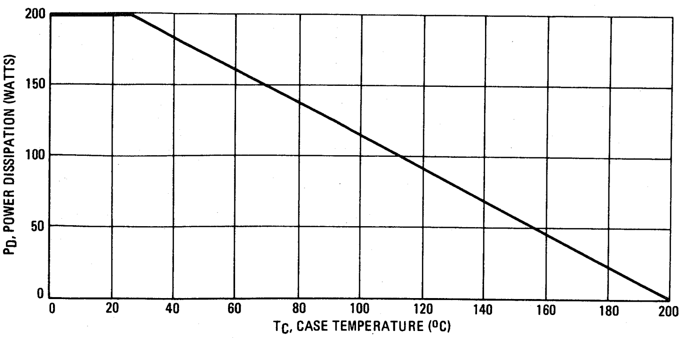
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CER}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Collector-Emitter Voltage	V_{CEO}	90	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

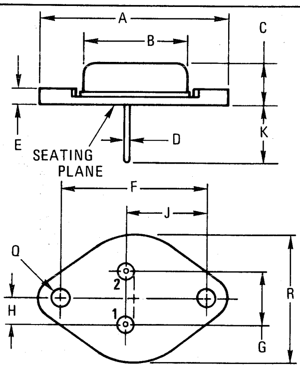
3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-204AA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	$V_{(BR)CER}$	100	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	– –	1.0 5.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter "On" Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.3	Vdc
Collector-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

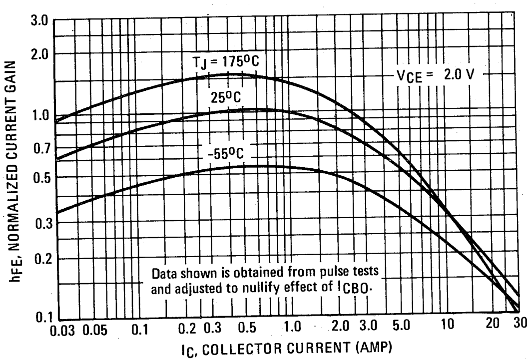
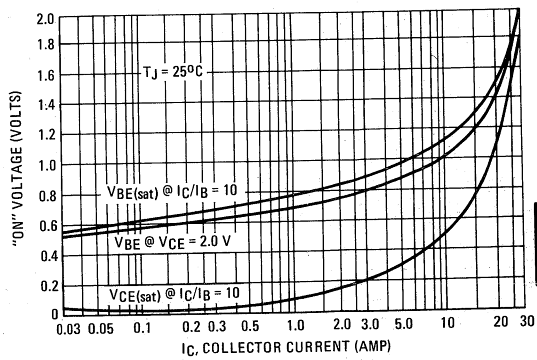
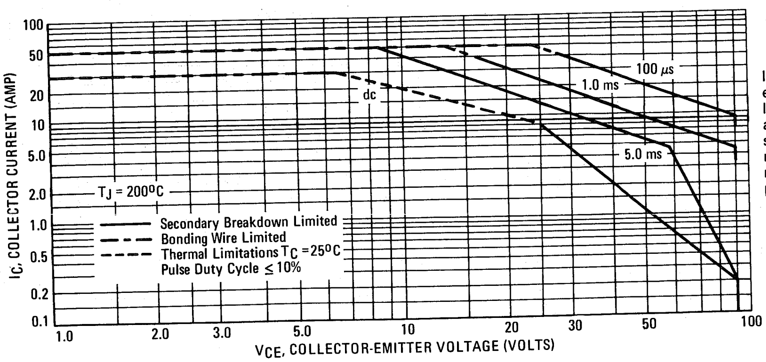


FIGURE 3 – "ON" VOLTAGES



3

FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

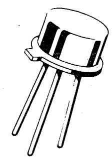
MJ4646
MJ4647

PNP SILICON POWER TRANSISTORS

. . . designed for high-voltage amplifier and saturated switching applications at collector currents to one Ampere. Ideally suited for applications of dc-to-dc converters, relay and hammer drivers, motor controls, and servo and pulse amplifiers. High-voltage ratings permit direct-line operation.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = < 1.5 Vdc (Max) @ I_C = 500 mAdc
- High Collector-Emitter Breakdown Voltage — $V_{(BR)CEO}$ = 300 and 400 Vdc (Min)
- DC Current Gain Specified — 10 mAdc to 500 mAdc

1.0 AMPERE
POWER TRANSISTORS
PNP SILICON
200-300-400 VOLTS
5 WATTS

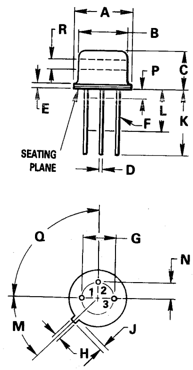


MAXIMUM RATINGS

Rating	Symbol	MJ4646	MJ4647	Unit
Collector-Emitter Voltage	V_{CEO}	300	400	Vdc
Collector-Base Voltage	V_{CB}	300	400	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	0.5 1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.6		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	θ_{JC}	35	°C/W



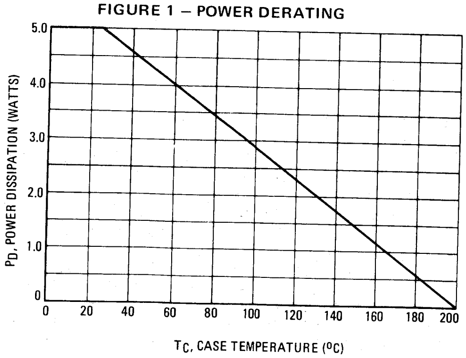
STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
Q	90° NOM		90° NOM	
R	2.54	—	0.100	—

All JEDEC Dimensions and Notes Apply.

CASE 79-02
TO-205AD

FIGURE 1 — POWER DERATING



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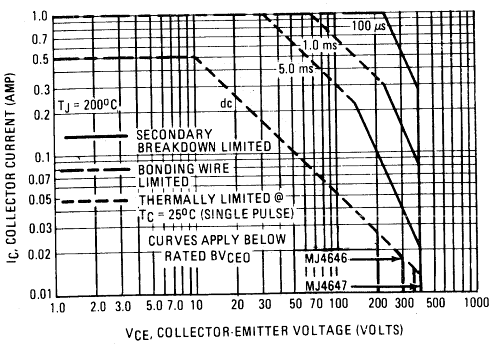
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0) MJ4646	$V_{(BR)CEO}$	300	–	–	Vdc
MJ4647		400	–	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0) MJ4646	$V_{(BR)CBO}$	300	–	–	Vdc
MJ4647		400	–	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 0.5 Vdc)	I_{CEX}	–	–	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	–	–	–
(I_C = 100 mAdc, V_{CE} = 10 Vdc) (1)		25	–	–	
(I_C = 500 mAdc, V_{CE} = 10 Vdc) (1)		20	–	–	
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 100 mAdc) MJ4646	$V_{CE(sat)}$	–	0.6	1.2	Vdc
MJ4647		–	0.75	1.5	
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 70 mAdc, V_{CE} = 20 Vdc, f = 20 MHz) MJ4646	f_T	40	–	–	MHz
MJ4647		30	–	–	
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 100 kHz) MJ4647	C_{ob}	–	–	60	pF
SWITCHING CHARACTERISTICS					
Delay Time (V_{CC} = 100 Vdc, I_C = 500 mAdc,	t_d	–	–	100	ns
Rise Time I_{B1} = 50 mAdc, $V_{BE(off)}$ = 5.0 Vdc)	t_r	–	–	100	ns
Turn-Off Time (V_{CC} = 100 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc, Pulse Width = 1.0 μs)	t_{off}	–	–	720	ns

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJ6503

Designers Data Sheet

SWITCHMODE SERIES
PNP SILICON POWER TRANSISTOR

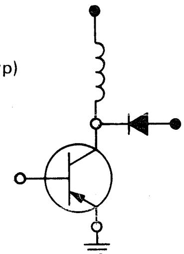
The MJ6503 transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
100 ns Inductive Fall Time @ 25°C (Typ)
125 ns Inductive Crossover Time @ 25°C (Typ)

Operating Temperature Range −65 to +200°C

100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



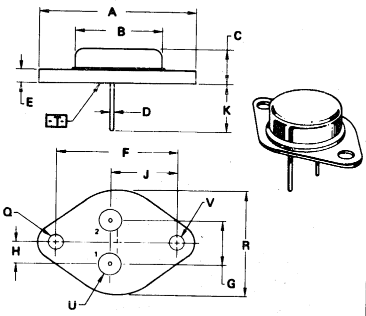
8 AMPERE

PNP SILICON POWER TRANSISTOR

400 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	ϕ.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	ϕ.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MJ6503	Unit
Collector-Emitter Voltage	V_{CEO}	400	Vdc
Collector-Emitter Voltage	V_{CEV}	450	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	8.0 16	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	4.0 8.0	Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	125 71.5 0.714	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 10 mA, I_B = 0) MJ6503	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	— —	— —	0.5 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5 Vdc)	h_{FE}	15	—	—	—
Collector-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 1.0 Adc) (I_C = 8 Adc, I_B = 3.0 Adc) (I_C = 4 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	— — —	1.5 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 1.0 Adc) (I_C = 4 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	100	—	400	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — (V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, t_p = 50 μs, Duty Cycle ≤ 2%)	t_d	—	0.025	0.1	μs
Rise Time — (V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, t_p = 50 μs, Duty Cycle ≤ 2%)	t_r	—	0.100	0.5	μs
Storage Time — (V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%)	t_s	—	0.60	2.0	μs
Fall Time — (V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%)	t_f	—	0.11	0.5	μs
Inductive Load, Clamped (Table 1)					
Storage Time — (I_C = 4 A(pk), $V_{CE(pk)}$ = 250 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	0.8	3.0	μs
Crossover Time — (I_C = 4 A(pk), $V_{CE(pk)}$ = 250 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	—	0.4	1.5	μs
Fall Time — (I_C = 4 A(pk), $V_{CE(pk)}$ = 250 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{fi}	—	0.1	—	μs
Storage Time — (I_C = 4 A(pk), $V_{CE(pk)}$ = 250 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	—	0.5	—	μs
Crossover Time — (I_C = 4 A(pk), $V_{CE(pk)}$ = 250 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_c	—	0.125	—	μs
Fall Time — (I_C = 4 A(pk), $V_{CE(pk)}$ = 250 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{fi}		0.1	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

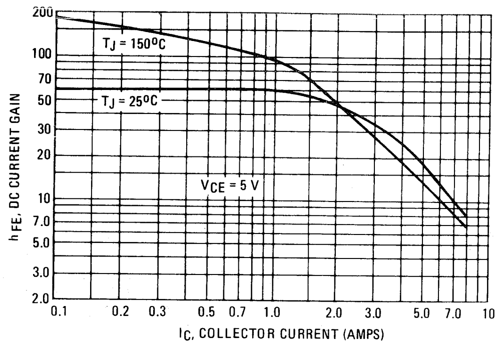


FIGURE 2 – COLLECTOR SATURATION REGION

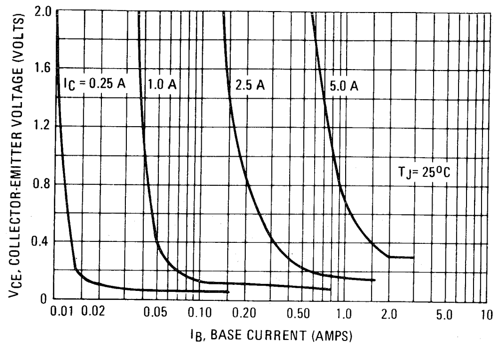


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

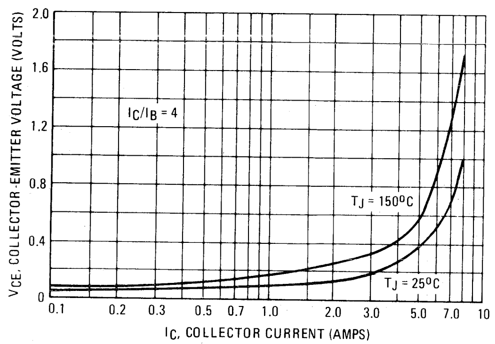


FIGURE 4 – BASE-EMITTER VOLTAGE

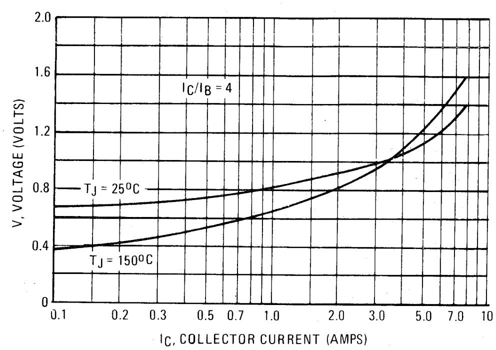


FIGURE 5 – COLLECTOR CUTOFF REGION

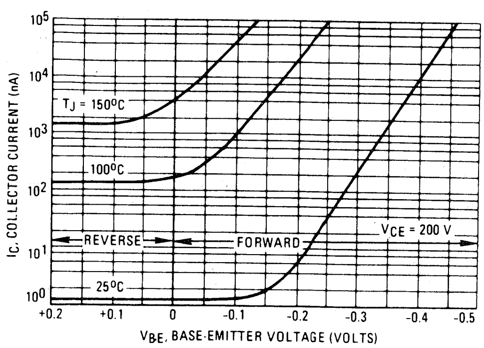


FIGURE 6 – CAPACITANCE

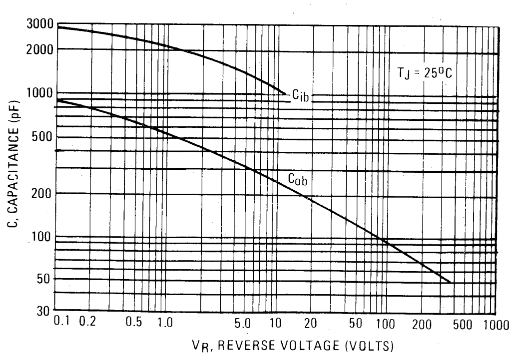


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TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

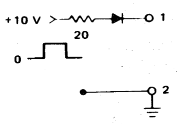
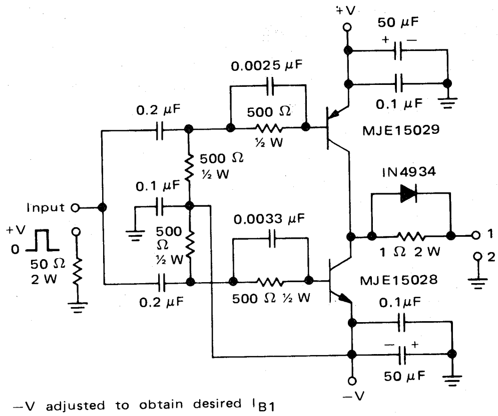
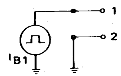
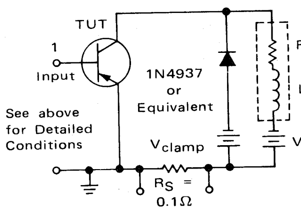
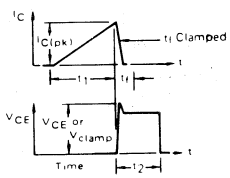
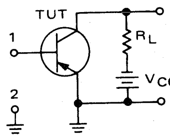
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 −V adjusted to obtain desired I_{B1} +V adjusted to obtain desired $V_{BE(off)}$	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain I_{B1}	V_{CC} = 250 V R_L = 62 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

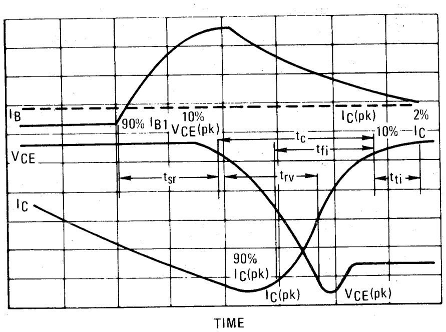
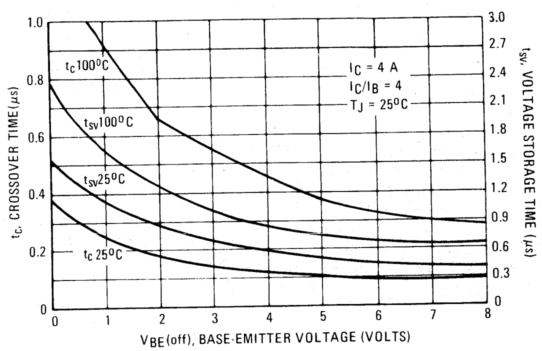


FIGURE 8 — INDUCTIVE SWITCHING TIMES



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SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE}(pk)$
t_{rv} = Voltage Rise Time, 10–90% $V_{CE}(pk)$
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% $V_{CE}(pk)$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 9 — TURN-ON SWITCHING TIMES

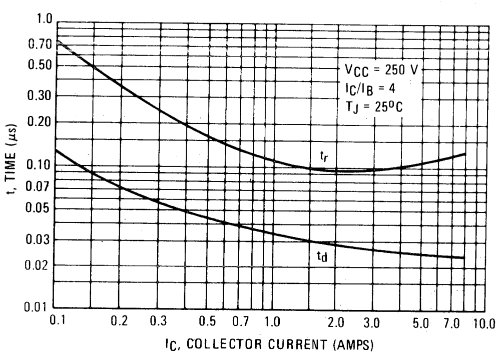


FIGURE 10 — TURN-OFF SWITCHING TIMES

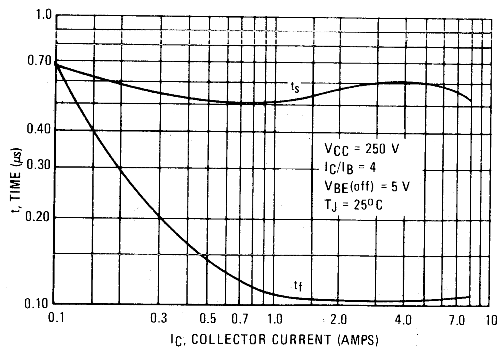
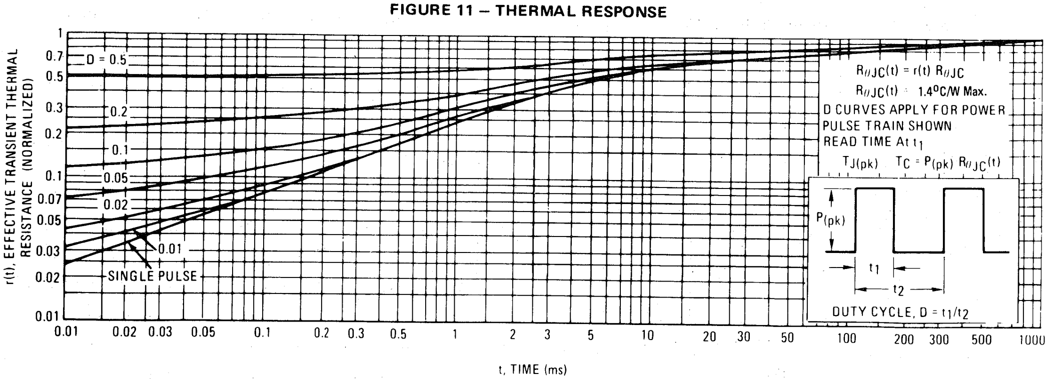


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

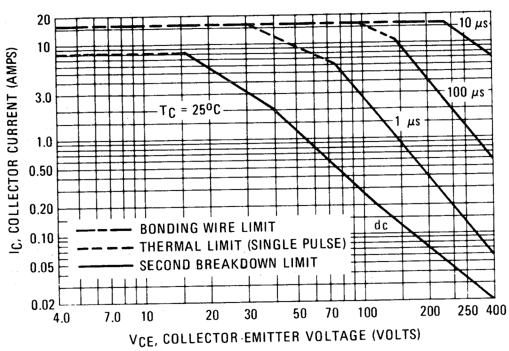
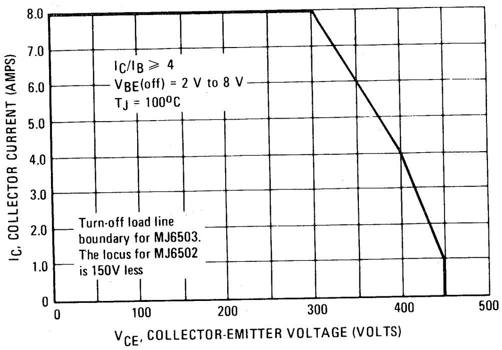


FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

FIGURE 14 PEAK REVERSE BASE CURRENT

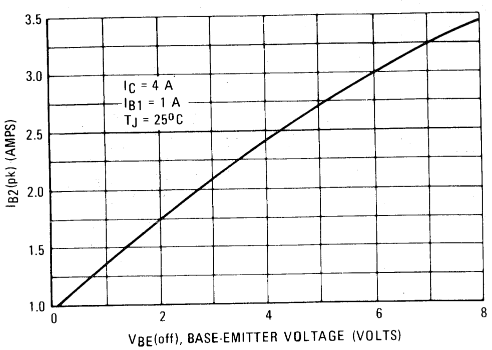
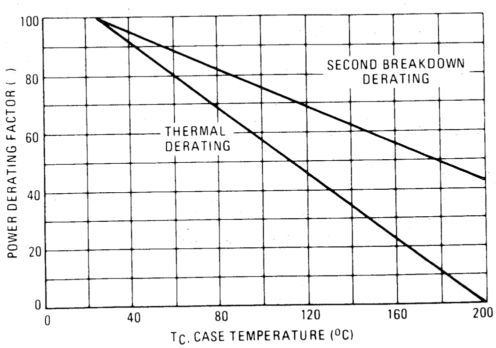


FIGURE 15 POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ8501

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTOR

The MJ8501 transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 300 ns Inductive Fall Time – 25°C (Typ)
- 500 ns Inductive Crossover Time – 25°C (Typ)
- 900 ns Inductive Storage Time – 25°C (Typ)

Operating Temperature Range −65 to +200°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

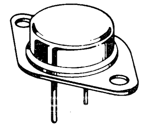
2.5 AMPERE

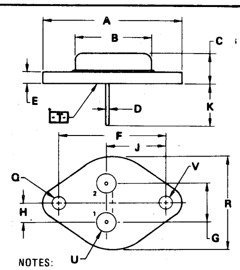
NPN SILICON POWER TRANSISTOR

800 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅0.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MJ8501	Unit
Collector-Emitter Voltage	V_{CEO}	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	2.5 5.0	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	2.0 4.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	125 71 0.71	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ8501	$V_{CEO(sus)}$	800	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.25	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		—	—	5 0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	7.5	—	—	—
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.33 Adc)	$V_{CE(sat)}$	—	—	2.0	Vdc
(I_C = 2.5 Adc, I_B = 1.0 Adc)		—	—	5.0	
(I_C = 1.0 Adc, I_B = 0.33 Adc, T_C = 100°C)		—	—	3.0	
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.33 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 1.0 Adc, I_B = 0.33 Adc, TC = 100°C)		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	50	—	250	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 500 Vdc, I_C = 1.0 A, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	—	0.045	0.20	μs
Rise Time	t_r	—	0.2	2.0	μs
Storage Time	t_s	—	1.0	4.0	μs
Fall Time	t_f	—	0.5	2.0	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_C = 1.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	1.3	4.0	μs
Crossover Time	t_c	—	0.6	2.0	μs
Storage Time (I_C = 1.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	—	0.9	—	μs
Crossover Time	t_c	—	0.5	—	μs
Fall Time	t_{fi}	—	0.3	—	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 1 — DC CURRENT GAIN

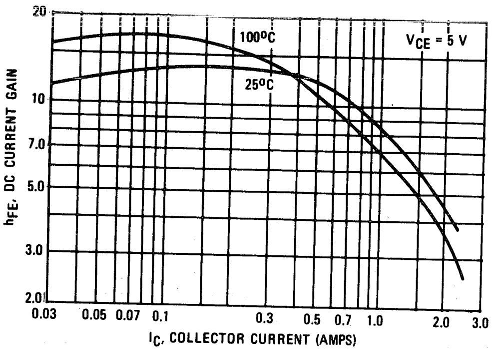


FIGURE 2 — COLLECTOR SATURATION REGION

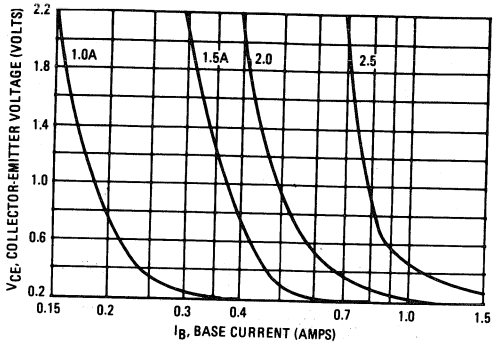


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

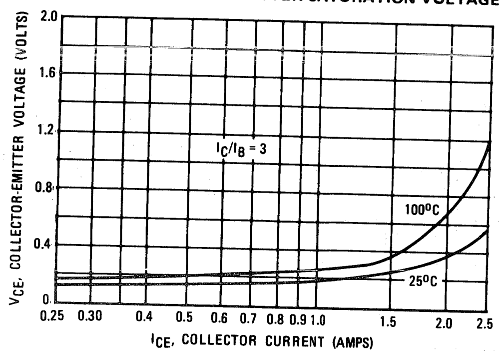


FIGURE 4 — BASE-EMITTER VOLTAGE

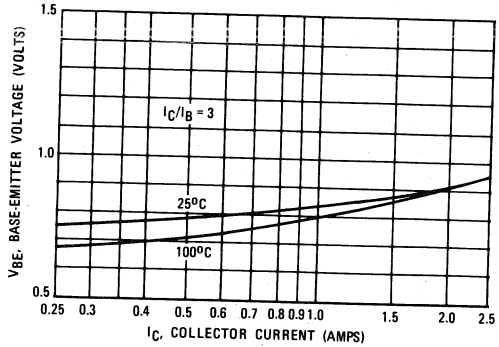


FIGURE 5 — COLLECTOR CUTOFF REGION

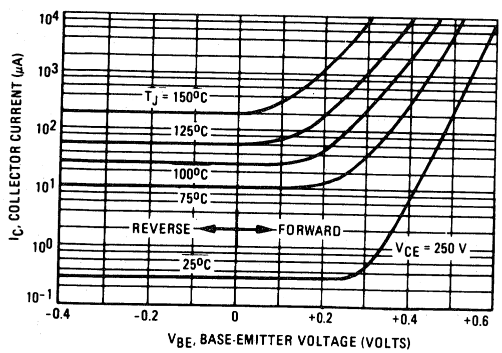


FIGURE 6 — CAPACITANCE

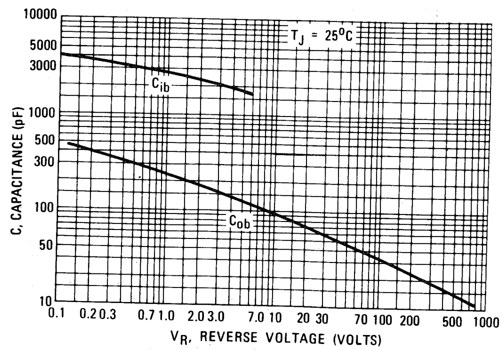


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FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

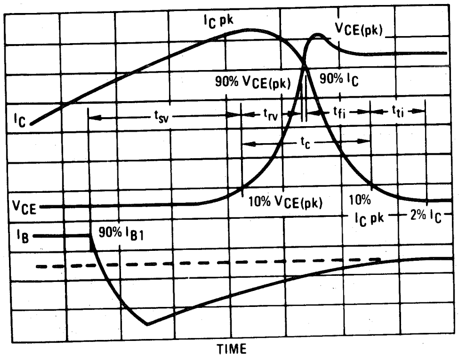
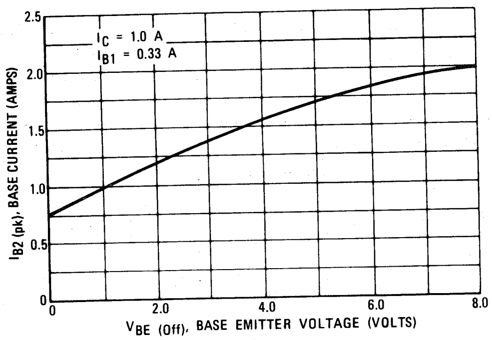


FIGURE 8 — PEAK REVERSE BASE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CE} (pk)
t_{rv} = Voltage Rise Time, 10–90% V_{CE} (pk)
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{CE} (pk) to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

3

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 — TURN - ON SWITCHING TIMES

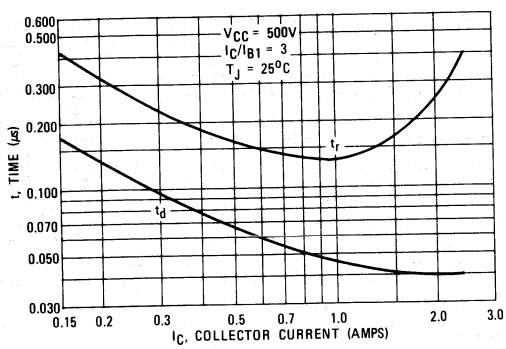


FIGURE 10 — TURN - OFF SWITCHING TIMES

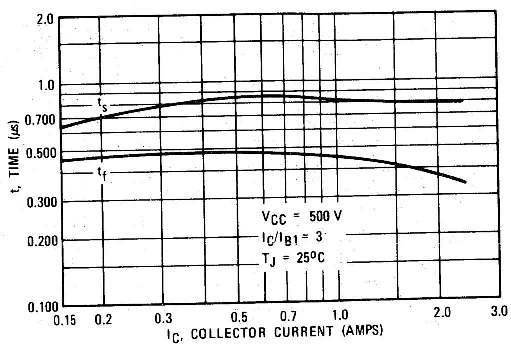


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

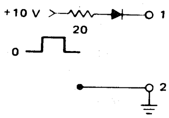
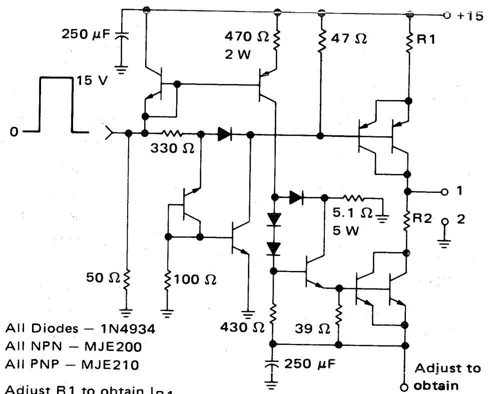
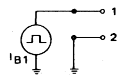
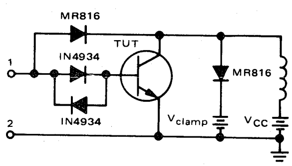
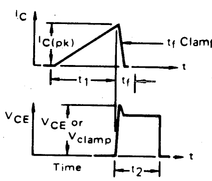
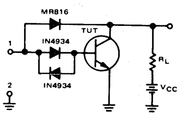
<table>
<tr><th></th><th>$V_{CEO(sus)}$</th><th>RBSOA AND INDUCTIVE SWITCHING</th><th>RESISTIVE SWITCHING</th></tr>
<tr><td>INPUT CONDITIONS</td><td>
PW Varied to Attain
I_C = 100 mA</td><td>
All Diodes – 1N4934
All NPN – MJE200
All PNP – MJE210
Adjust R1 to obtain I_{B1}
For switching and RB_{SOA}, R2 = 0
For $V_{CEO(sus)}$, R2 = ∞</td><td>TURN-ON TIME

I_{B1} adjusted to obtain the forced h_{FE} desired
TURN-OFF TIME
Use inductive switching driver as the input to the resistive test circuit.</td></tr>
<tr><td>CIRCUIT VALUES</td><td>L_{coil} = 80 mH V_{CC} = 10 V
R_{coil} = 0.7 Ω</td><td>L_{coil} = 180 μH
R_{coil} = 0.05 Ω
V_{CC} = 20 V
V_{clamp} = 500 V</td><td>V_{CC} = 500 V
R_L = 500 Ω
Pulse Width = 50 μs</td></tr>
<tr><td>TEST CIRCUITS</td><td colspan="2">INDUCTIVE TEST CIRCUIT

OUTPUT WAVEFORMS

t_1 Adjusted to Obtain I_C
$t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$
$t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$
Test Equipment
Scope – Tektronix
475 or Equivalent</td><td>RESISTIVE TEST CIRCUIT
</td></tr>
</table>

FIGURE 11 – THERMAL RESPONSE

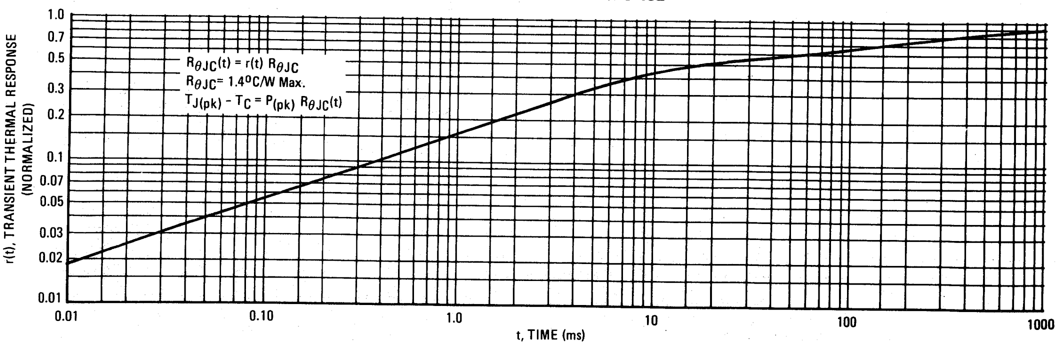


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FIGURE 12 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

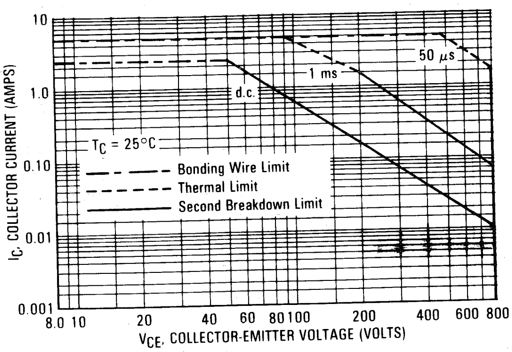
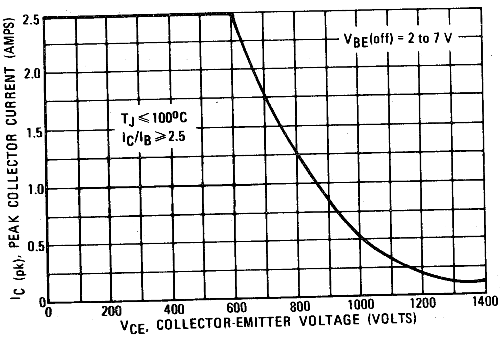


FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

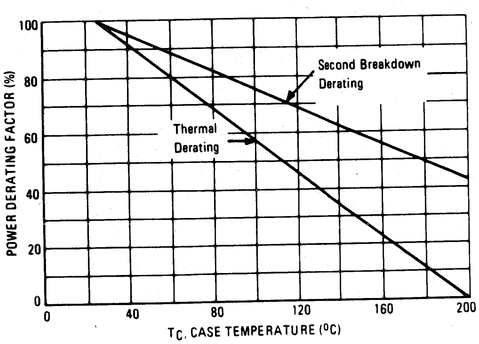
$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

3

FIGURE 14 — POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ8502
MJ8503

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ8502 and MJ8503 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
 150 ns Inductive Fall Time—25°C (Typ)
 400 ns Inductive Crossover Time—25°C (Typ)
 1200 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range −65 to + 200°C

100°C Performance Specified for:
 Reverse-Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents

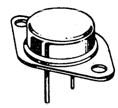
5.0 AMPERE

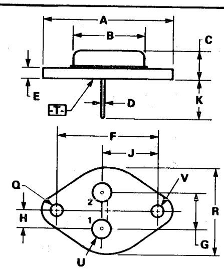
NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
 ⌖ 0.13 (0.005) Ⓜ | T | V Ⓜ
 FOR LEADS:
 ⌖ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA

3

MAXIMUM RATINGS

Rating	Symbol	MJ8502	MJ8503	Unit
Collector-Emitter Voltage	V_{CEO}	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	5.0 10	5.0 10	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	4.0 8.0	4.0 8.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 86 0.85	150 86 0.85	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.16	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ8502 / MJ8503	$V_{CEO(sus)}$	700 / 800	— / —	— / —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	— / —	— / —	0.25 / 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	7.5	—	—	—
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 2.0 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	— / — / —	— / — / —	2.0 / 5.0 / 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	— / —	— / —	1.5 / 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	60	—	300	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — (V_{CC} = 500 Vdc, IC = 2.5A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	—	0.040	0.20	μs
Rise Time	t_r	—	0.125	2.0	μs
Storage Time	t_s	—	1.2	4.0	μs
Fall Time	t_f	—	0.65	2.0	μs
Inductive Load, Clamped (Table 1)					
Storage Time — (I_C = 2.5 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, TC = 100°C)	t_{sv}	—	1.6	5.0	μs
Crossover Time	t_c	—	0.60	2.0	μs
Storage Time — (I_C = 2.5 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	—	1.2	—	μs
Crossover Time	t_c	—	0.4	—	μs
Fall Time	t_{fi}	—	0.15	—	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 1 — DC CURRENT GAIN

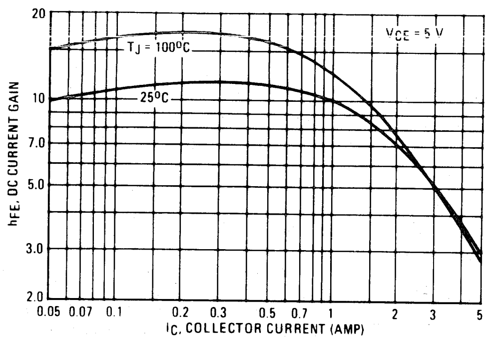


FIGURE 2 — COLLECTOR SATURATION REGION

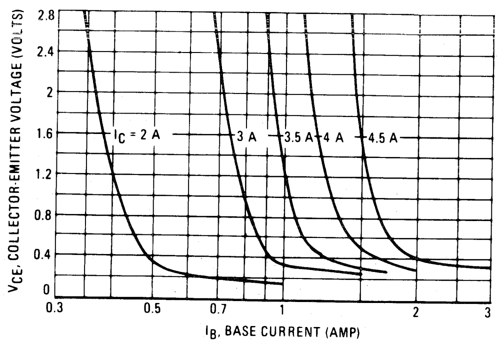


FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION

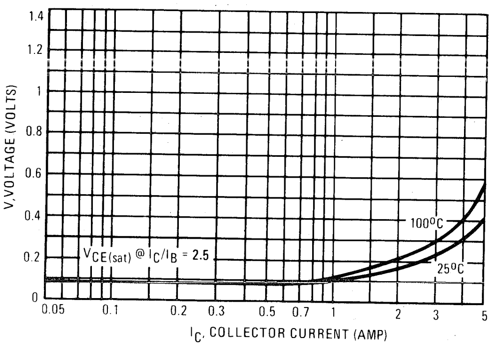


FIGURE 4 — BASE-EMITTER VOLTAGE

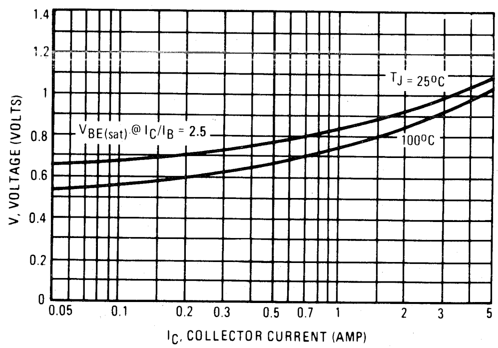


FIGURE 5 — COLLECTOR CUTOFF REGION

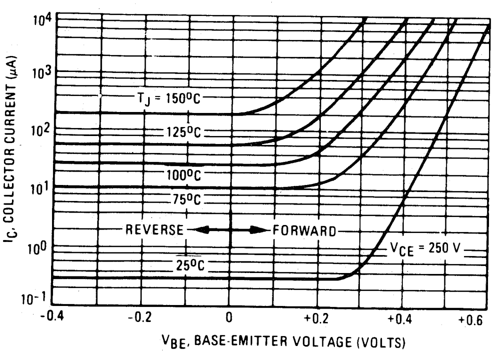


FIGURE 6 — CAPACITANCE

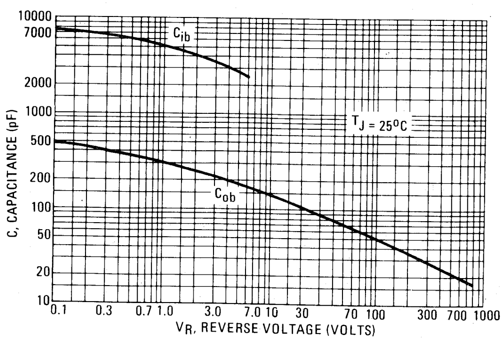


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FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

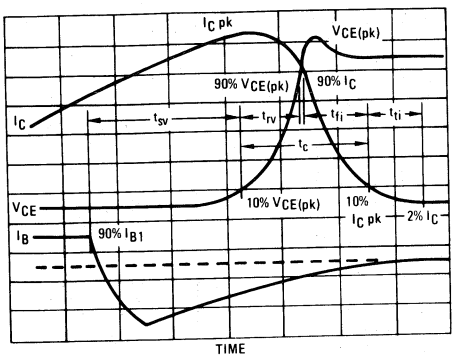
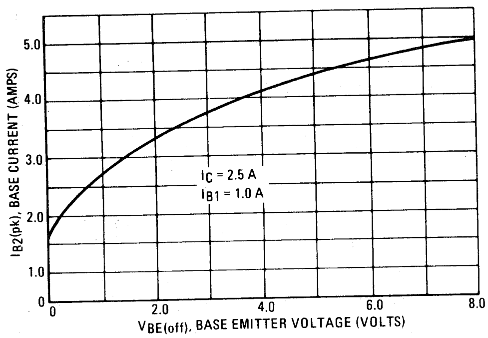


FIGURE 8 – PEAK REVERSE BASE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$

t_{rv} = Voltage Rise Time, 10–90% $V_{CE(pk)}$

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

3

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON SWITCHING TIMES

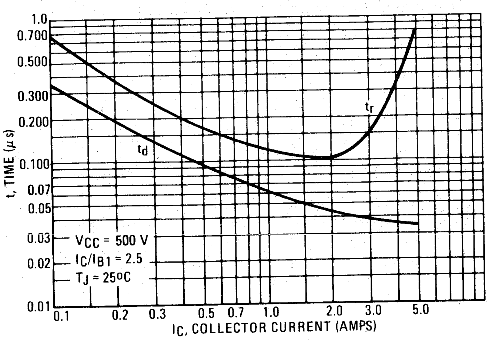


FIGURE 10 – TURN-OFF SWITCHING TIMES

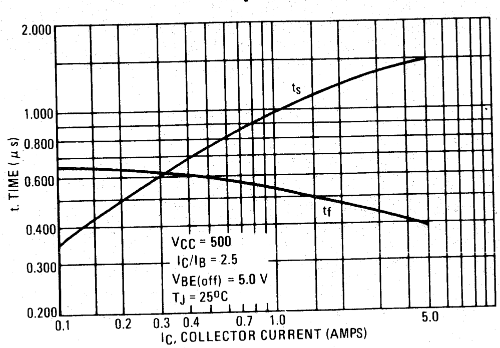


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

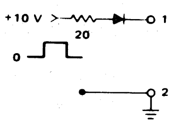
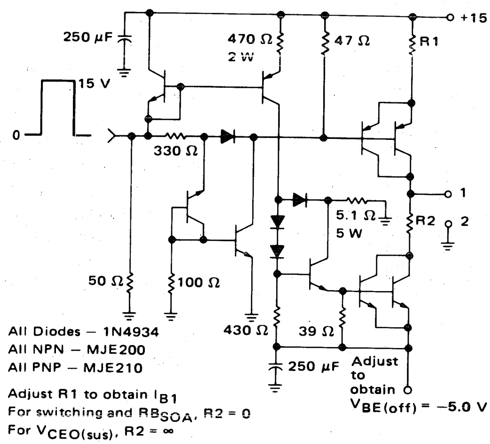
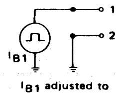
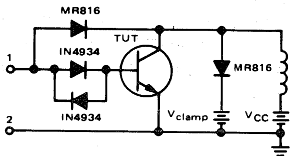
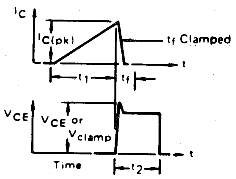
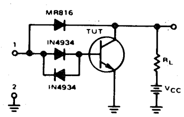
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $V_{CEO(sus)}$, R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 500 V	V_{CC} = 500 V R_L = 200 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

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FIGURE 11 – THERMAL RESPONSE

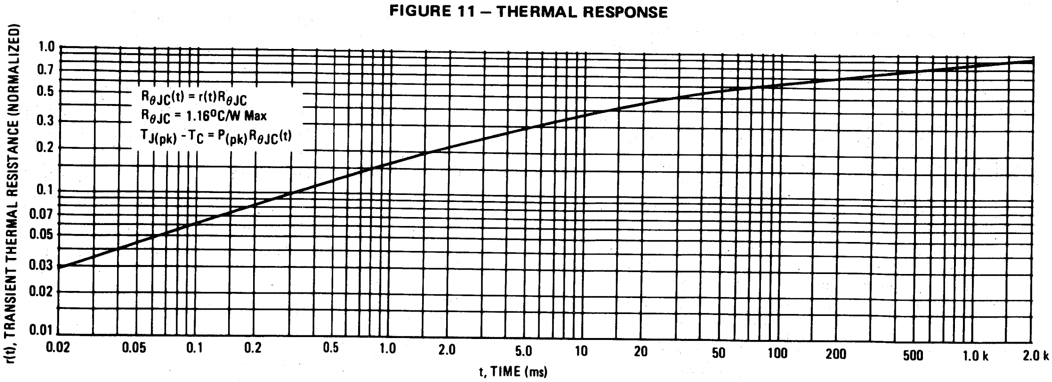
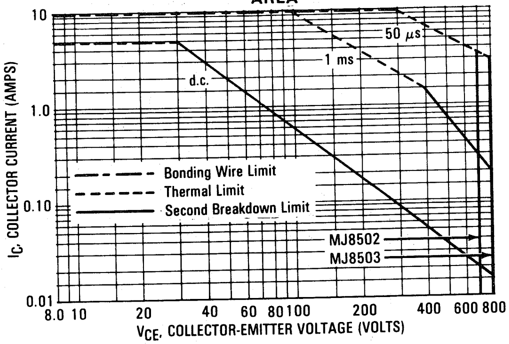


FIGURE 12 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



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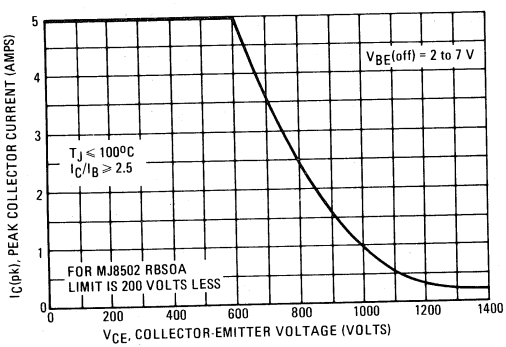

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

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3

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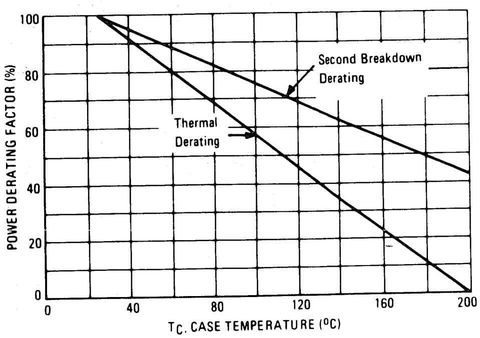

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- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 75 ns Inductive Fall Time −25°C (typ)
- 150 ns Inductive Crossover Time −25°C (typ)
- 1.25 μs Inductive Storage Time −25°C (typ)

Operating Temperature Range −65 to + 200°C

100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

10 AMPERE

NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
175 WATTS

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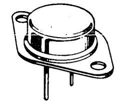

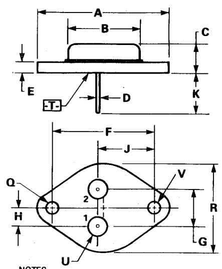

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   FOR LEADS:
   ⌖ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
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C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
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F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MJ8504	MJ8505	Unit
Collector-Emitter Voltage	V_{CEO}	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	10 15	10 15	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	8 12	8 12	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	175 100 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) MJ8504 (I_C = 100 mA, I_B = 0) MJ8505	$V_{CEO(sus)}$	700 800	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 – –	 – –	 0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	7.5	–	–	–
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 2.0 Adc) (I_C = 10 Adc, I_B = 4.0 Adc) (I_C = 5.0 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	 – – –	 – – –	 2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 2.0 Adc) (I_C = 5.0 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	 – –	 – –	 1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	90	–	450	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 500 Vdc, I_C = 5.0 A, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.050	0.20	μs
Rise Time	t_r	–	0.175	2.0	μs
Storage Time	t_s	–	1.25	4.0	μs
Fall Time	t_f	–	0.60	2.0	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_C = 5.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	1.75	5.5	μs
Crossover Time	t_c	–	0.400	2.0	μs
Storage Time (I_C = 5.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	1.25	–	μs
Crossover Time	t_c	–	0.150	–	μs
Fall Time	t_{fi}	–	0.075	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 1 – DC CURRENT GAIN

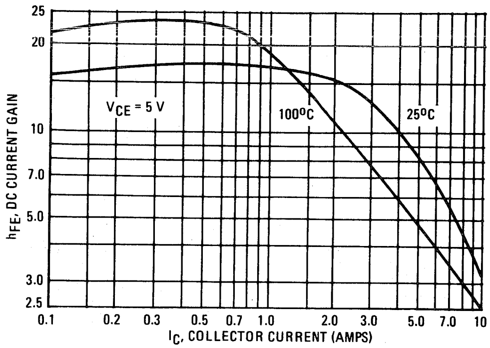


FIGURE 2 – COLLECTOR SATURATION REGION

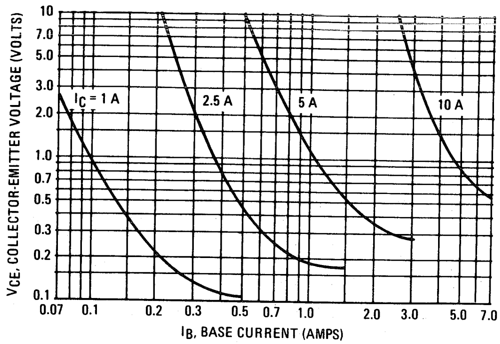


FIGURE 3 – COLLECTOR-EMITTER SATURATION REGION

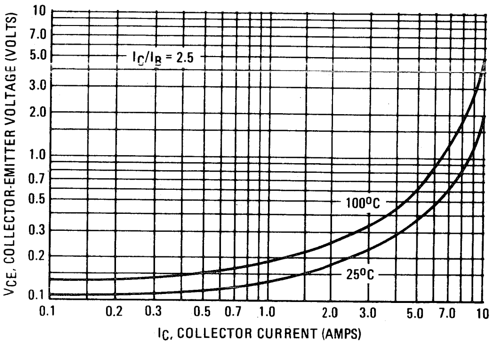


FIGURE 4 – BASE EMITTER VOLTAGE

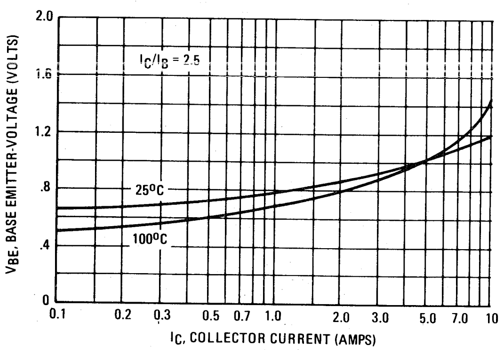


FIGURE 5 – COLLECTOR CUTOFF REGION

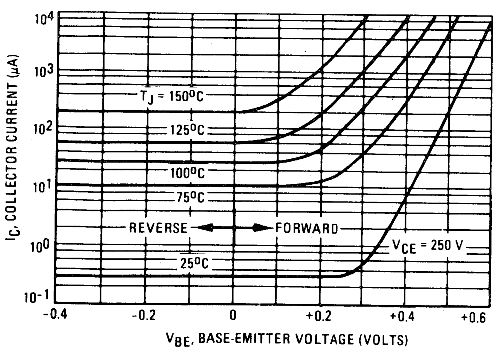


FIGURE 6 – CAPACITANCE

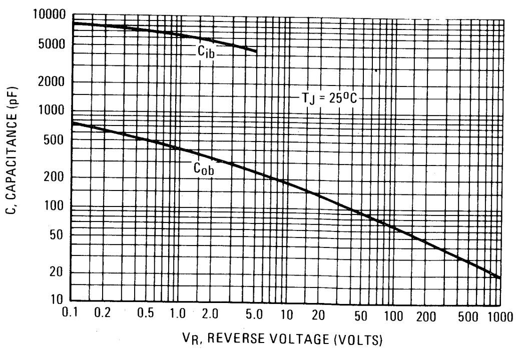


FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

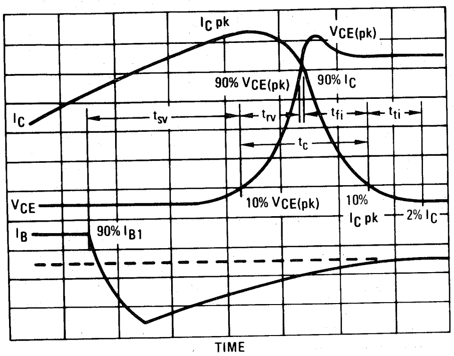
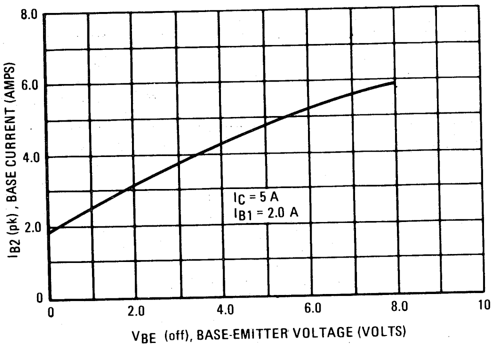


FIGURE 8 — PEAK REVERSE BASE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$

t_{rv} = Voltage Rise Time, 10–90% $V_{CE(pk)}$

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

3

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 — TURN-ON SWITCHING TIMES

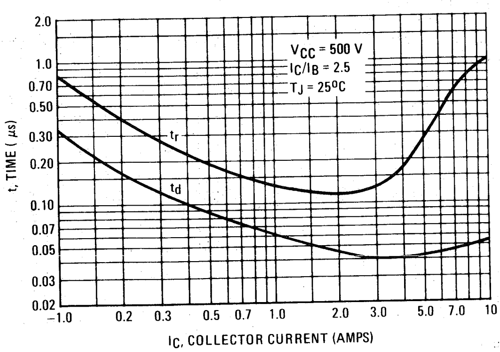


FIGURE 10 — TURN-OFF SWITCHING TIMES

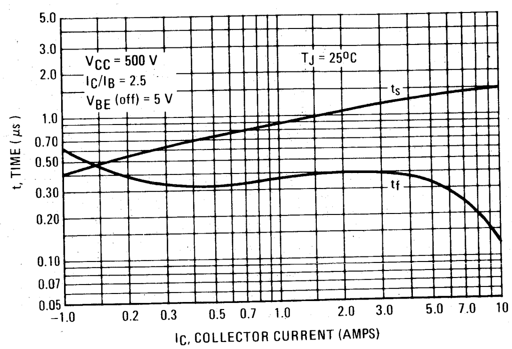
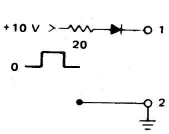


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

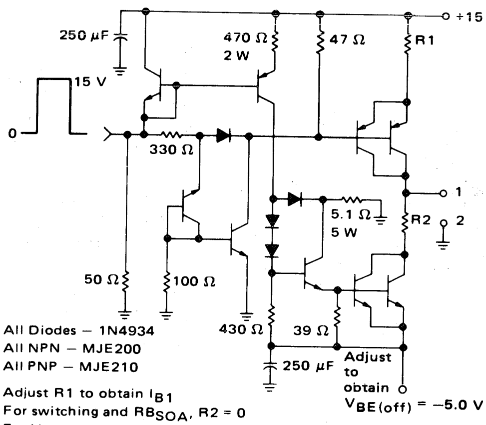
INPUT CONDITIONS

$V_{CEO(sus)}$



PW Varied to Attain I_C = 100 mA

RBSOA AND INDUCTIVE SWITCHING

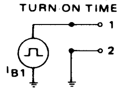


All Diodes – 1N4934
All NPN – MJE200
All PNP – MJE210

Adjust R1 to obtain I_{B1}
For switching and RB_{SOA}, R2 = 0
For $V_{CEO(sus)}$, R2 = ∞

RESISTIVE SWITCHING

TURN ON TIME



I_{B1} adjusted to obtain the forced h_{FE} desired

TURN OFF TIME

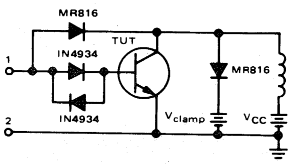
Use inductive switching driver as the input to the resistive test circuit.

CIRCUIT VALUES

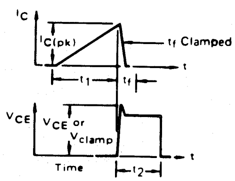
$V_{CEO(sus)}$	RBSOA and Inductive Switching		Resistive Switching
L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V	V_{clamp} = 500 V	V_{CC} = 500 V R_L = 100 Ω Pulse Width = 50 μs

TEST CIRCUITS

INDUCTIVE TEST CIRCUIT



OUTPUT WAVEFORMS



t_1 Adjusted to Obtain I_C

$$t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$$

$$t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$$

Test Equipment
Scope – Tektronix
475 or Equivalent

RESISTIVE TEST CIRCUIT

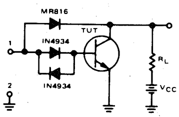
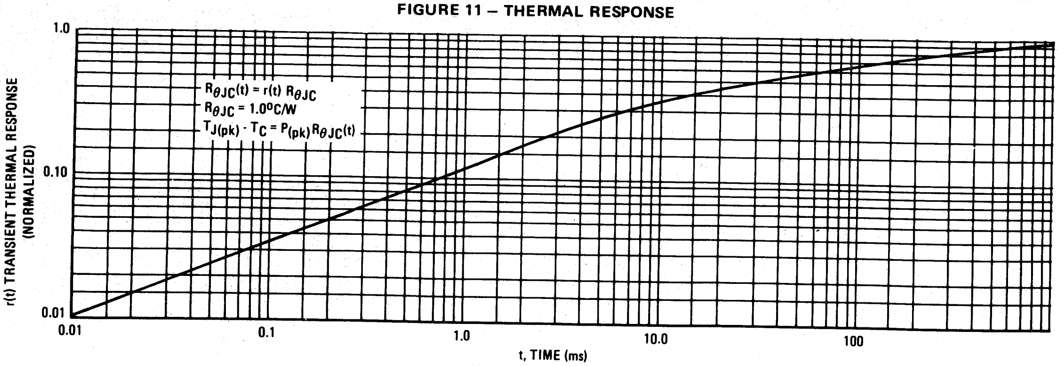


FIGURE 11 – THERMAL RESPONSE



3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

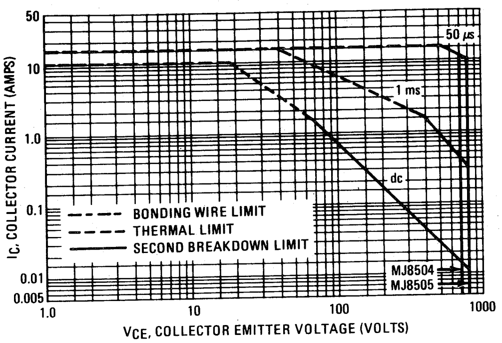


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA

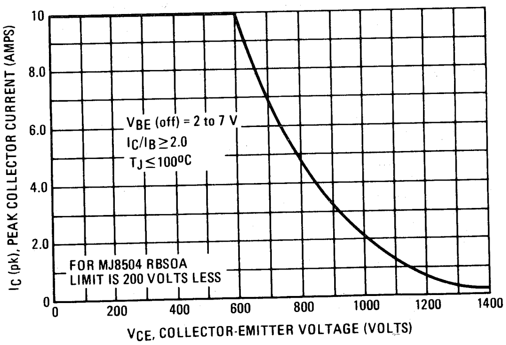
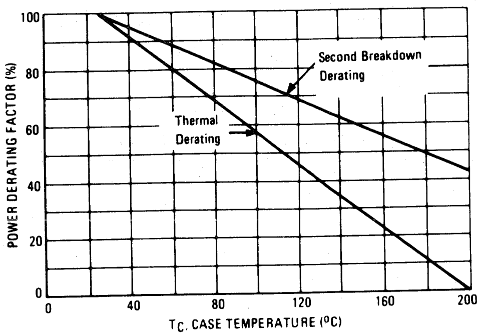


FIGURE 14 – POWER DERATING



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

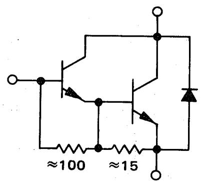
MJ10000
MJ10001

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10000 and MJ10001 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

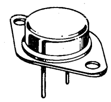


100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times With Inductive Loads — 210 ns Inductive Fall Time (Typ)
- Saturation Voltages
- Leakage Currents

20 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
350 and 400 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



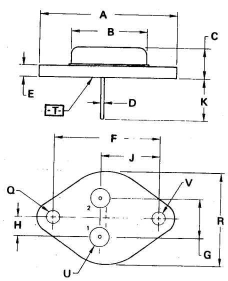
MAXIMUM RATINGS

Rating	Symbol	MJ10000	MJ10001	Unit
Collector-Emitter Voltage	V_{CEO}	350	400	Vdc
Collector-Emitter Voltage	V_{CEX}	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10000 / MJ10001	$V_{CEO(sus)}$	350 400	— —	— —	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) I_C = 2 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C MJ10000 / MJ10001; I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C MJ10000 / MJ10001	$V_{CEX(sus)}$	400 450 275 325	— — — —	— — — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	— —	— —	0.25 5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	5	mAdc
Emitter Cutoff Current (V_{EB} = 8 Vdc, I_C = 0)	I_{EBO}	—	—	150	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			Adc
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc) (I_C = 10 Adc, V_{CE} = 5 Vdc)	h_{FE}	50 40	— —	600 400	—
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 400 mAdc) (I_C = 20 Adc, I_B = 1 Adc) (I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)	$V_{CE(sat)}$	— — —	— — —	1.9 3 2	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)	$V_{BE(sat)}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage (1) (I_F = 10 Adc)	V_f	—	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	$\|h_{fe}\|$	10		—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	100		325	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%).	t_d	—	0.12	0.2	μs
Rise Time	t_r	—	0.20	0.6	μs
Storage Time	t_s	—	1.5	3.5	μs
Fall Time	t_f	—	1.1	2.4	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	3.5	5.5	μs
Crossover Time	t_c	—	1.5	3.7	μs
Storage Time (I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	—	1.0	—	μs
Crossover Time	t_c	—	0.7	—	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

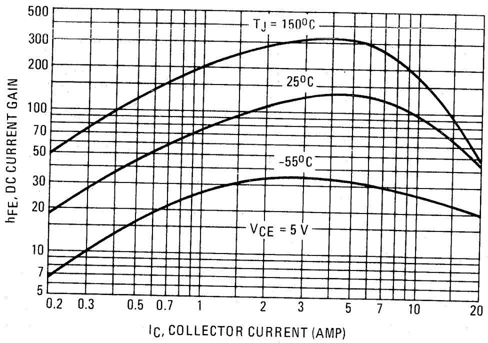


FIGURE 2 – COLLECTOR SATURATION REGION

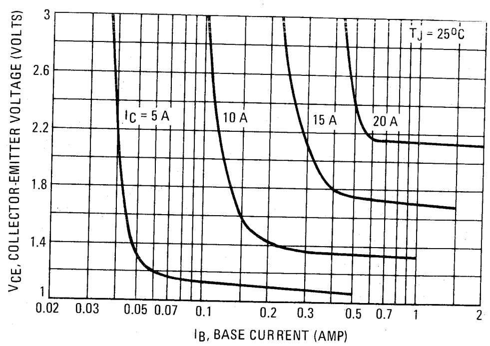


FIGURE 3 – COLLECTOR EMMITTER SATURATION VOLTAGES

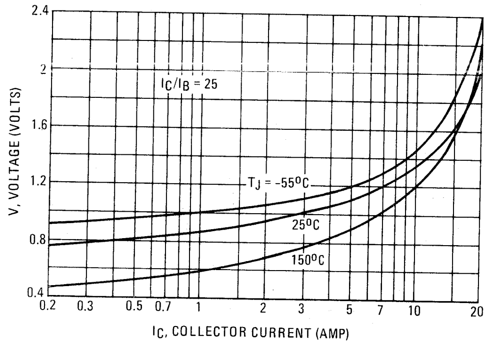


FIGURE 4 – BASE-EMITTER VOLTAGE

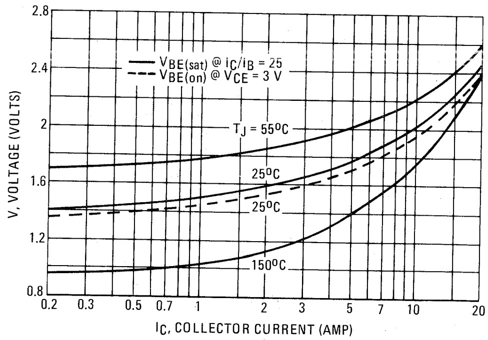


FIGURE 5 – COLLECTOR CUTOFF REGION

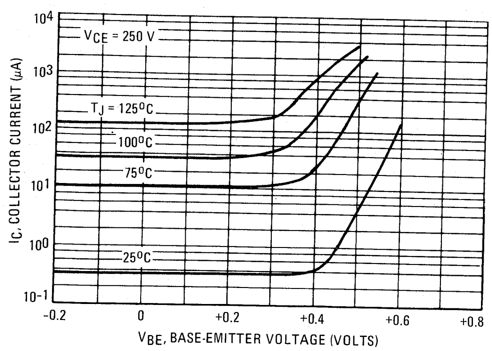


FIGURE 6 – OUTPUT CAPACITANCE

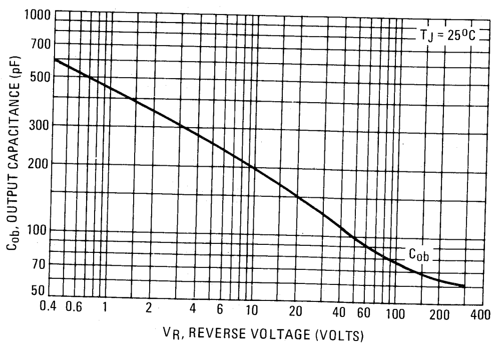


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

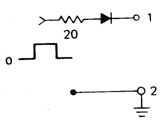
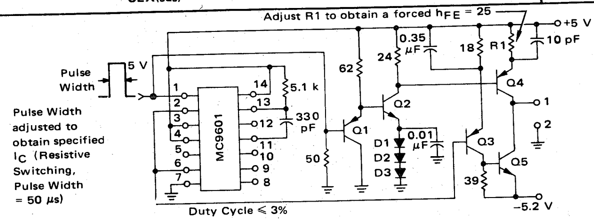
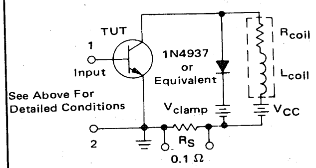
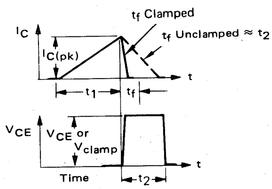
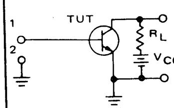
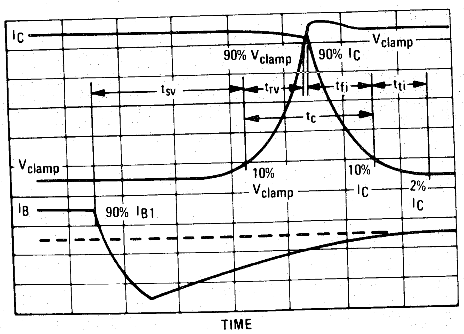
	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA	 Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 µs)	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above For Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope-Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

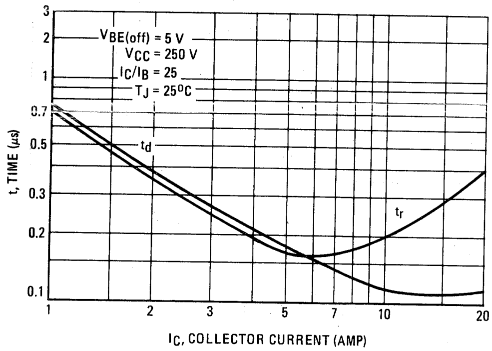


FIGURE 9 – TURN-OFF TIME

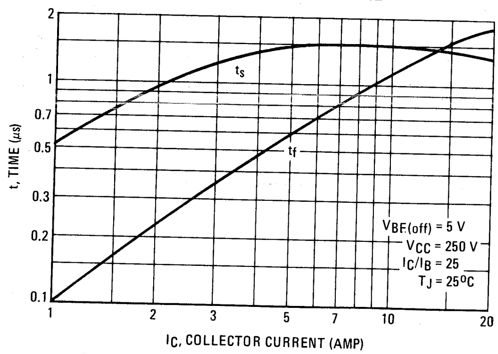
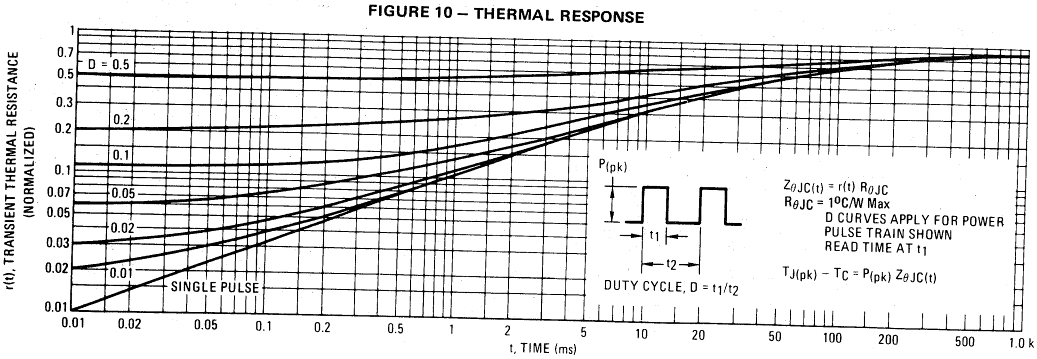


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

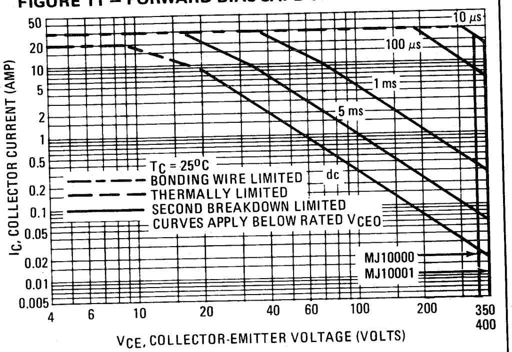
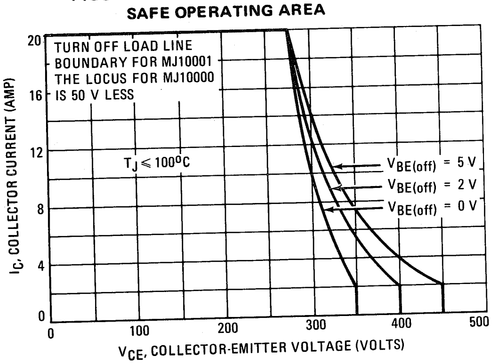


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

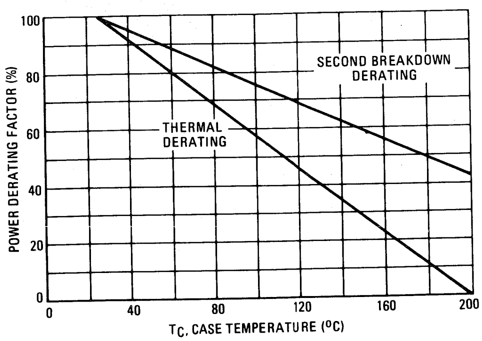
$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

3

FIGURE 13 – POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

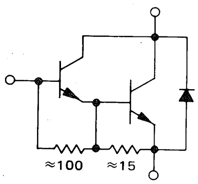
MJ10002

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10002 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads

Switching Times with Inductive Loads — 140 ns Inductive Fall Time (Typ)

Saturation Voltages

Leakage Currents

10 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS

350 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

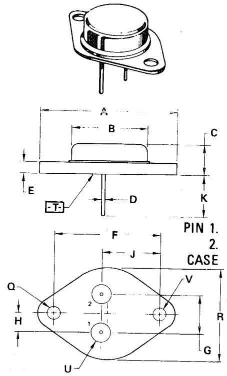
MAXIMUM RATINGS

Rating	Symbol	MJ10002	Unit
Collector-Emitter Voltage	V_{CEO}	350	Vdc
Collector-Emitter Voltage	V_{CEX}	400	Vdc
Collector-Emitter Voltage	V_{CEV}	450	Vdc
Emitter Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 20	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 100 0.86	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
⌖ ∅0.13 (0.005) Ⓜ T V Ⓜ
FOR LEADS:
⌖ ∅0.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10002	$V_{CEO(sus)}$	350	–	–	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) (I_C = 1.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10002 (I_C = 5.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10002	$V_{CEX(sus)}$	400 275	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	– –	– –	0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			Adc
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40 30	– –	500 300	–
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 250 mAdc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 250 mAdc, T_C = 100°C)	$V_{CE(sat)}$	– – –	– – –	1.9 2.9 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 250 mAdc) (I_C = 5.0 Adc, I_B = 250 mAdc, T_C = 100°C)	$V_{BE(sat)}$	– –	– –	2.5 2.5	Vdc
Diode Forward Voltage (1) (I_F = 5.0 Adc)	V_f	–	3.0	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	$\lvert h_{fe} \rvert$	10	–	–	–
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	60	–	275	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — (V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%).	t_d	–	0.05	0.2	μs
Rise Time	t_r	–	0.25	0.6	μs
Storage Time	t_s	–	1.2	3.0	μs
Fall Time	t_f	–	0.6	1.5	μs
Inductive Load, Clamped (Table 1)					
Storage Time — (I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_{sv}	–	2.1	5.0	μs
Crossover Time	t_c	–	1.3	3.3	μs
Storage Time — (I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_{sv}	–	0.92	–	μs
Crossover Time	t_c	–	0.5	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

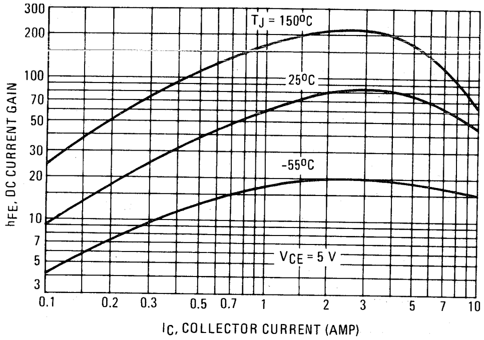


FIGURE 2 — COLLECTOR SATURATION REGION

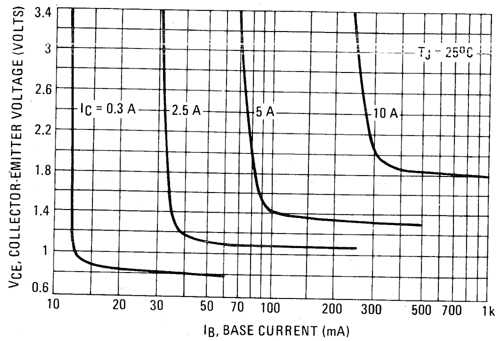


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

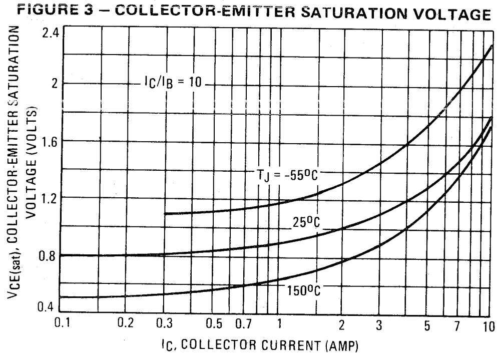


FIGURE 4 — BASE-EMITTER VOLTAGE

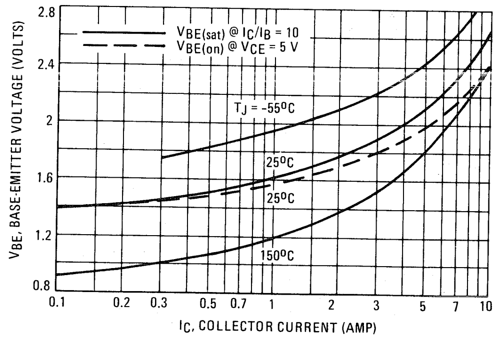


FIGURE 5 — COLLECTOR CUT-OFF REGION

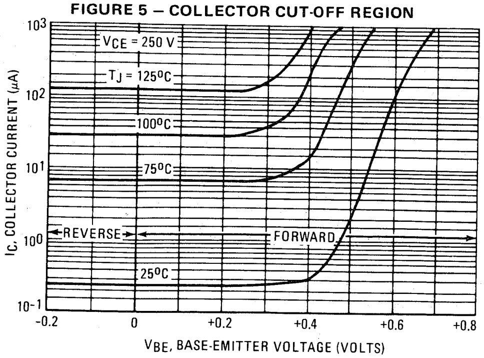


FIGURE 6 — OUTPUT CAPACITANCE

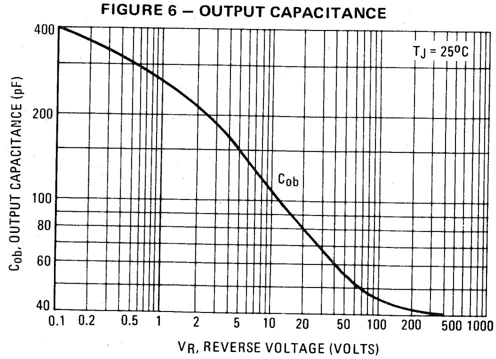


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

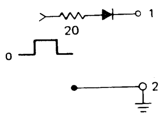
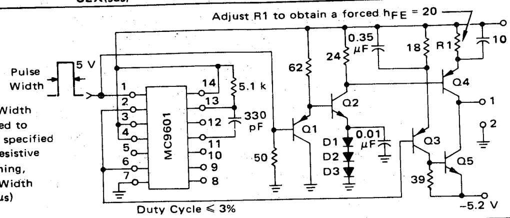
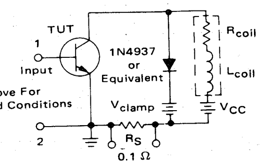
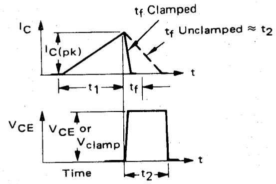
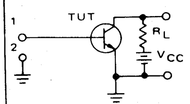
	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA	Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 µs)  Adjust R1 to obtain a forced h_{FE} = 20; Duty Cycle ≤ 3%	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 50 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above For Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope-Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

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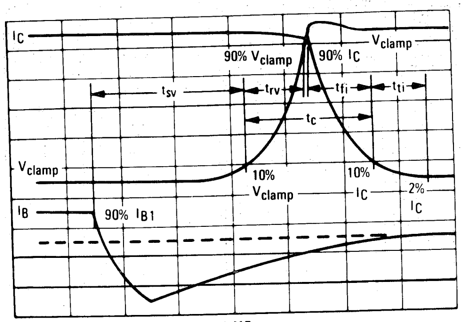
FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

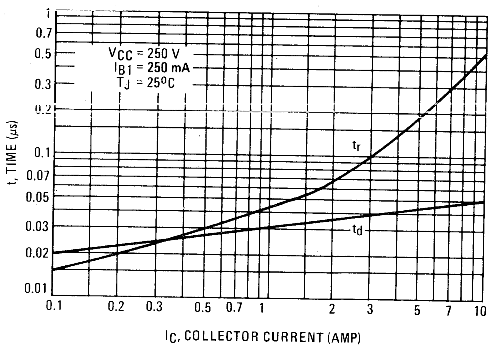


FIGURE 9 – TURN-OFF TIME

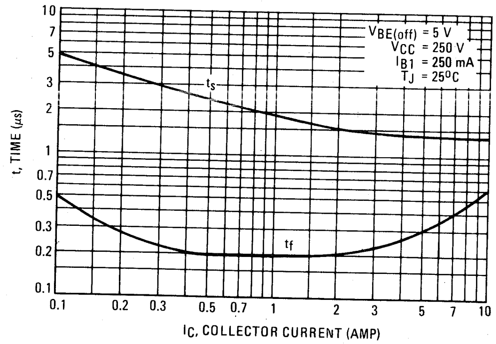
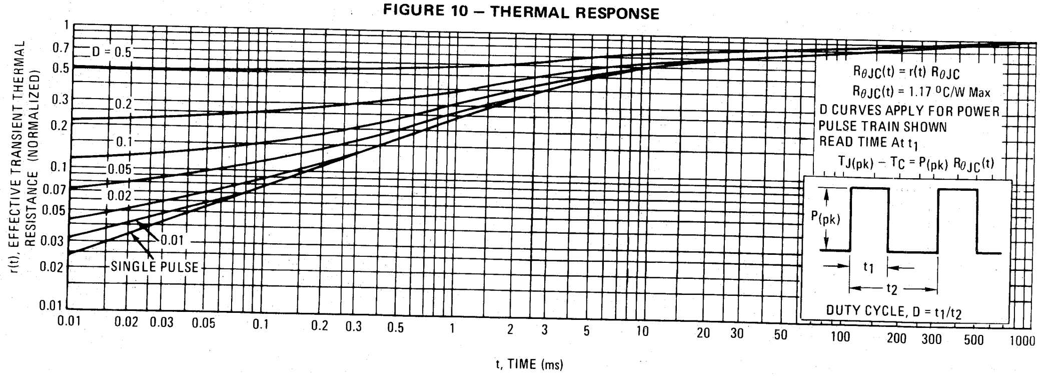


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – ACTIVE-REGION SAFE OPERATING AREA

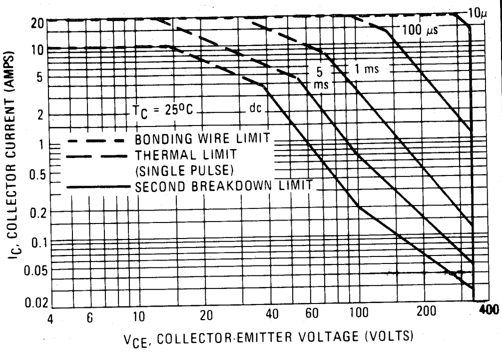
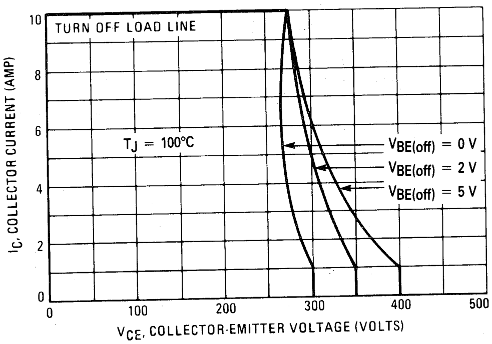


FIGURE 12 – REVERSE BIASED SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

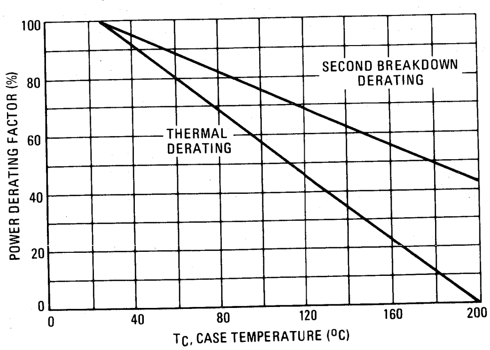
$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

3

FIGURE 13 – POWER DERATING



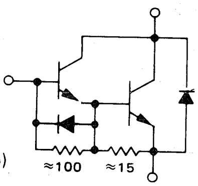
MJ10004
MJ10005

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10004 and MJ10005 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
40 ns Inductive Fall Time – 25°C (Typ)
650 ns Inductive Storage Time – 25°C (Typ)

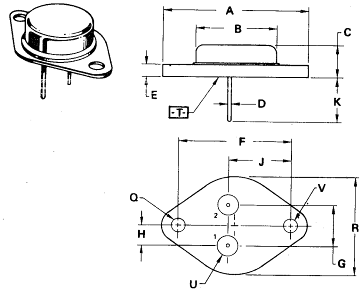
Operating Temperature Range -65 to +200°C

100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

20 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
350 and 400 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

| ⌖ | ∅0.13 (0.005) Ⓜ | T | V Ⓜ |

FOR LEADS:

| ⌖ | ∅0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MJ10004	MJ10005	Unit
Collector-Emitter Voltage	V_{CEO}	350	400	Vdc
Collector-Emitter Voltage	V_{CEX}	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	20 30		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2.5 5.0		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	175 100 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10004	$V_{CEO(sus)}$	350	–	–	Vdc
MJ10005		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) (I_C = 2.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10004	$V_{CEX(sus)}$	400	–	–	Vdc
MJ10005		450	–	–	
(I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10004		275	–	–	
MJ10005		325	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	0.25	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	–	5.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	50	–	600	–
(I_C = 10 Adc, V_{CE} = 5.0 Vdc)		40	–	400	
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 400 mAdc)	$V_{CE(sat)}$	–	–	1.9	Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)		–	–	3.0	
(I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)		–	–	2.0	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 400 mAdc)	$V_{BE(sat)}$	–	–	2.5	Vdc
(I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)		–	–	2.5	
Diode Forward Voltage (1) (I_F = 10 Adc)	V_f	–	3.0	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	$\lvert h_{fe} \rvert$	10	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	100	–	325	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — (V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 400 mA, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ⩽ 2%).	t_d	–	0.12	0.2	μs
Rise Time	t_r	–	0.2	0.6	μs
Storage Time	t_s	–	0.6	1.5	μs
Fall Time	t_f	–	0.15	0.5	μs
Inductive Load, Clamped (Table 1)					
Storage Time — (I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_{sv}	–	1.0	2.5	μs
Crossover Time	t_c	–	0.4	1.5	μs
Storage Time — (I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_{sv}	–	0.65	–	μs
Crossover Time	t_c	–	0.2	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ⩽ 2%.

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TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

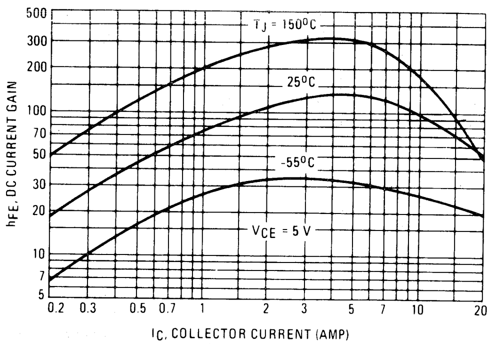

FIGURE 2 – COLLECTOR SATURATION REGION

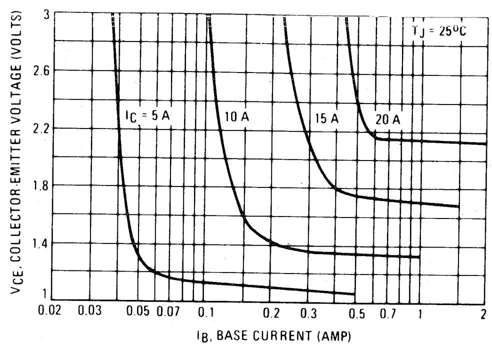

FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

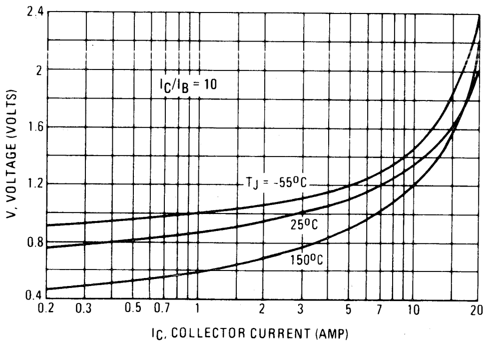

FIGURE 4 – BASE-EMITTER VOLTAGE

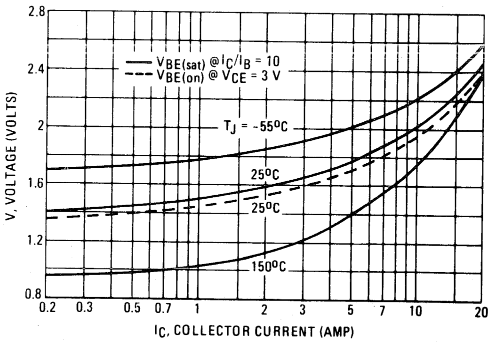

FIGURE 5 – COLLECTOR CUTOFF REGION

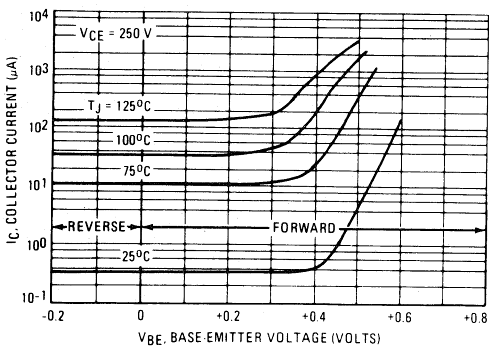

FIGURE 6 – OUTPUT CAPACITANCE

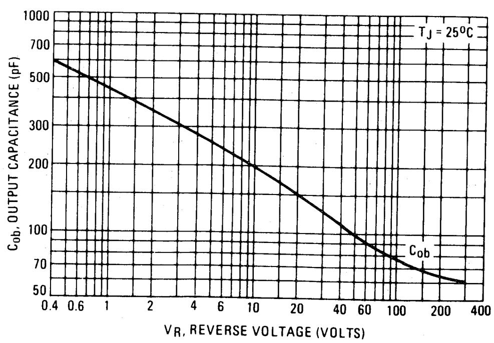

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TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

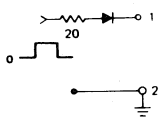
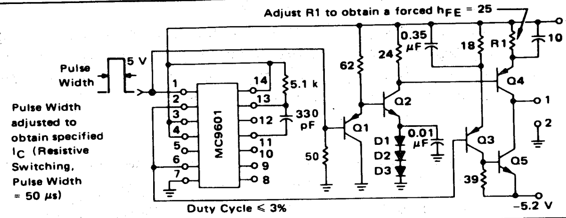
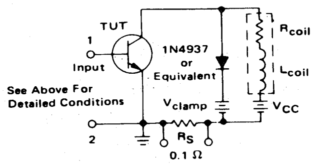
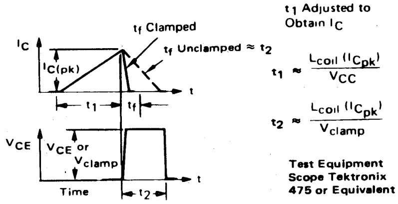
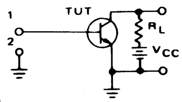
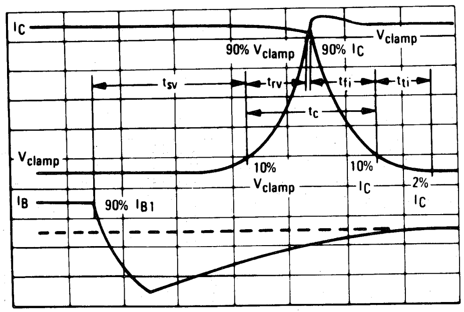
	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA		Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS 	RESISTIVE TEST CIRCUIT 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

TYPICAL CHARACTERISTICS

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

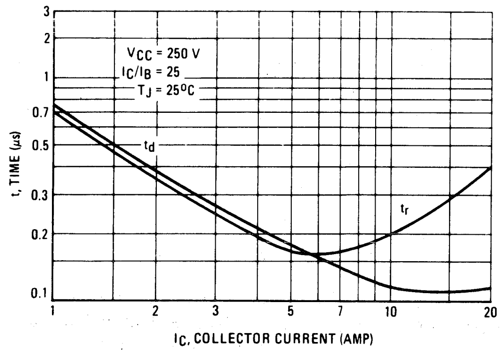


FIGURE 9 – TURN-OFF TIME

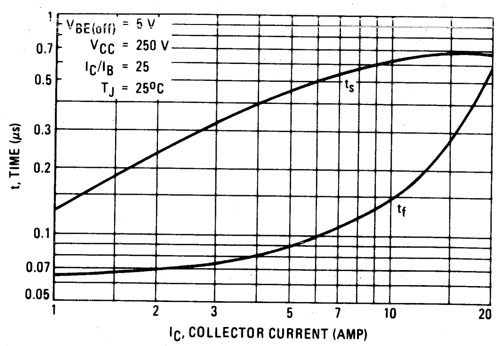
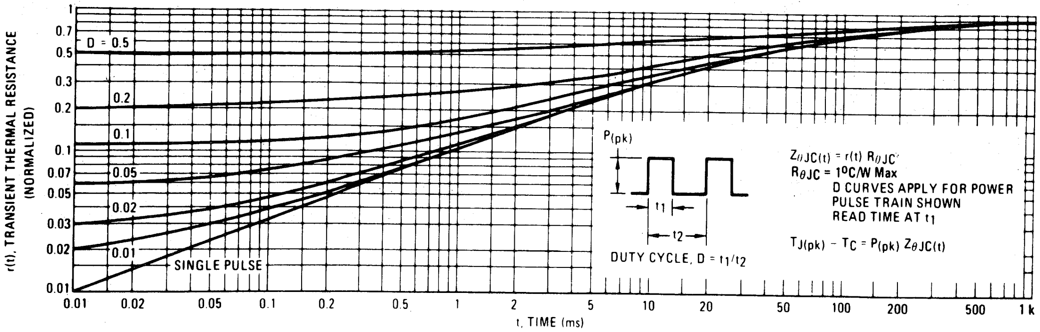


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

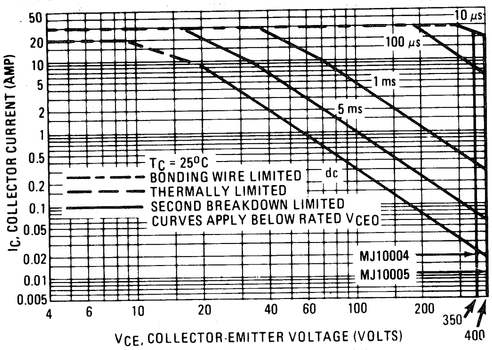


FIGURE 11 — FORWARD BIAS SAFE OPERATING AREA

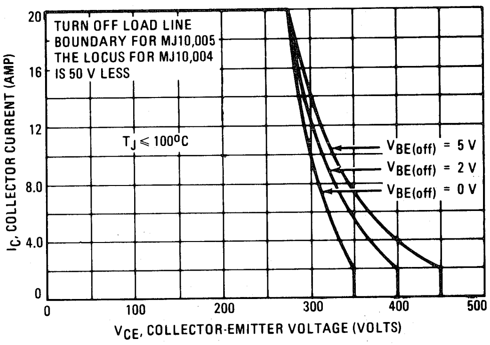


FIGURE 12 — REVERSE BIAS SWITCHING SAFE OPERATING AREA

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

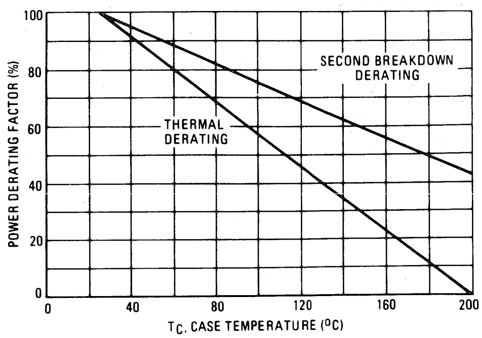
The data of Figure 11 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 — POWER DERATING



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

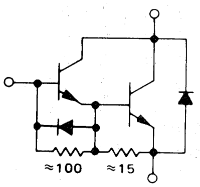
MJ10006
MJ10007

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10006 and MJ10007 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
30 ns Inductive Fall Time – 25°C (Typ)
500 ns Inductive Storage Time – 25°C (Typ))

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

10 AMPERE

NPN SILICON

POWER DARLINGTON TRANSISTORS

350 AND 400 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

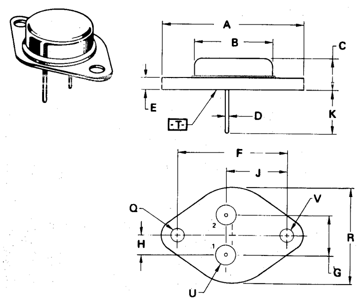
MAXIMUM RATINGS

Rating	Symbol	MJ10006	MJ10007	Unit
Collector-Emitter Voltage	V_{CEO}	350	400	Vdc
Collector-Emitter Voltage	V_{CEX}	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	10 20		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2.5 5.0		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 100 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ
FOR LEADS:
⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10006 MJ10007	$V_{CEO(sus)}$	350 400	– –	– –	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) (I_C = 1 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10006 MJ10007 (I_C = 5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10006 MJ10007	$V_{CEX(sus)}$	400 450 275 325	– – – –	– – – –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	– –	– –	0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40 30	– –	500 300	–
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 250 mAdc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 250 mAdc, T_C = 100°C)	$V_{CE(sat)}$	– – –	– – –	1.9 2.9 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 250 mAdc) (I_C = 5.0 Adc, I_B = 250 mAdc, T_C = 100°C)	$V_{BE(sat)}$	– –	– –	2.5 2.5	Vdc
Diode Forward Voltage (1) (I_F = 5.0 Adc)	V_f	–	3.0	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	$\|h_{fe}\|$	10	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	60	–	275	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — (V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%).	t_d	–	0.05	0.2	μs
Rise Time	t_r	–	0.25	0.6	μs
Storage Time	t_s	–	0.5	1.5	μs
Fall Time	t_f	–	0.06	0.5	μs
Inductive Load, Clamped (Table 1)					
Storage Time — (I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_{sv}	–	0.8	2.0	μs
Crossover Time	t_c	–	0.6	1.5	μs
Storage Time — (I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_{sv}	–	0.5	–	μs
Crossover Time	t_c	–	0.3	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

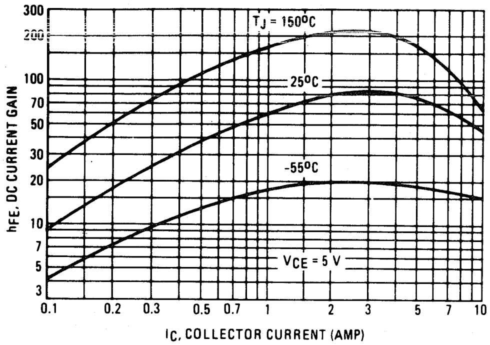


FIGURE 2 — COLLECTOR SATURATION REGION

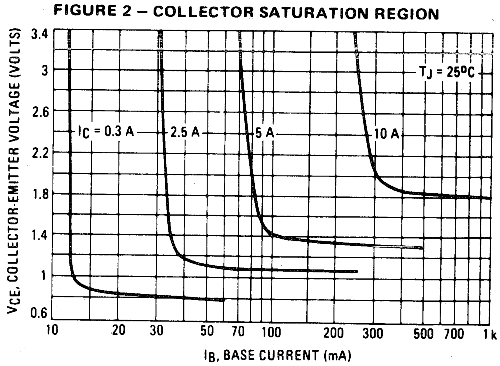


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

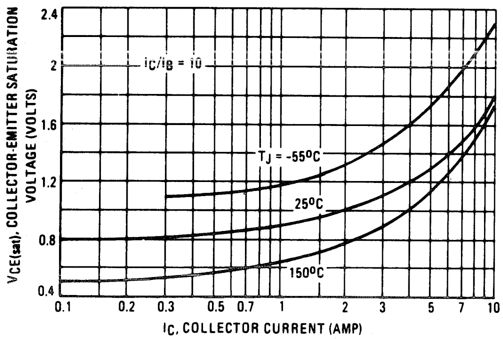


FIGURE 4 — BASE-EMITTER VOLTAGE

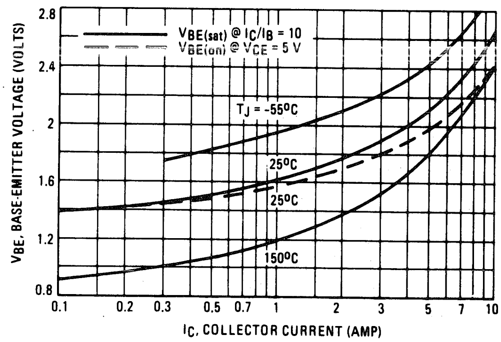


FIGURE 5 — COLLECTOR CUTOFF REGION

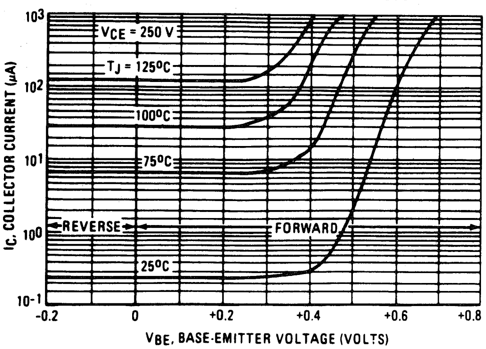


FIGURE 6 — OUTPUT CAPACITANCE

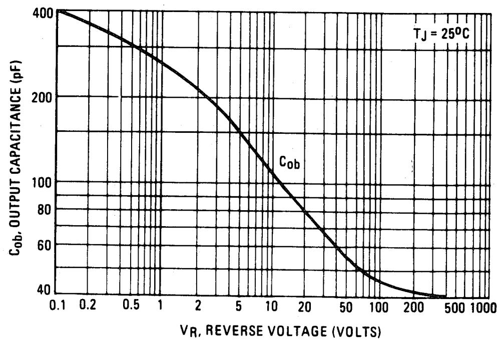


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

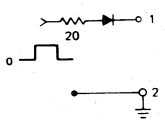
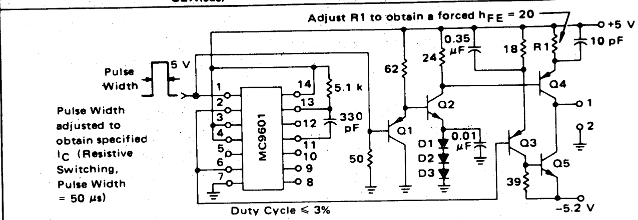
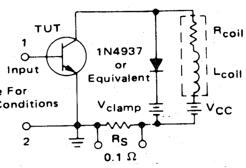
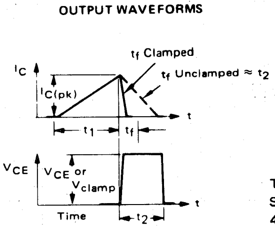
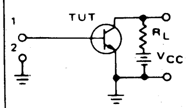
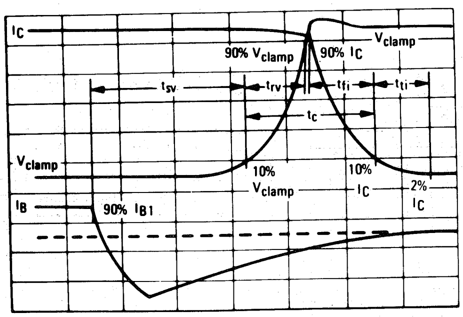
	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA	 Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 µs)	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V f_o = 500 kHz V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 50 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above For Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope-Tektronix 475 or Equipment	RESISTIVE TEST CIRCUIT 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

3

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

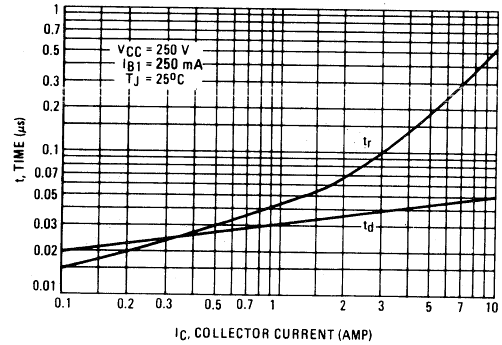


FIGURE 9 — TURN-OFF TIME

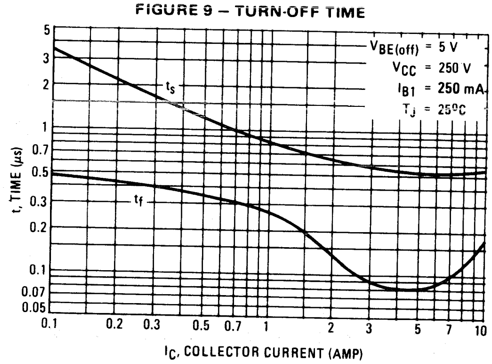
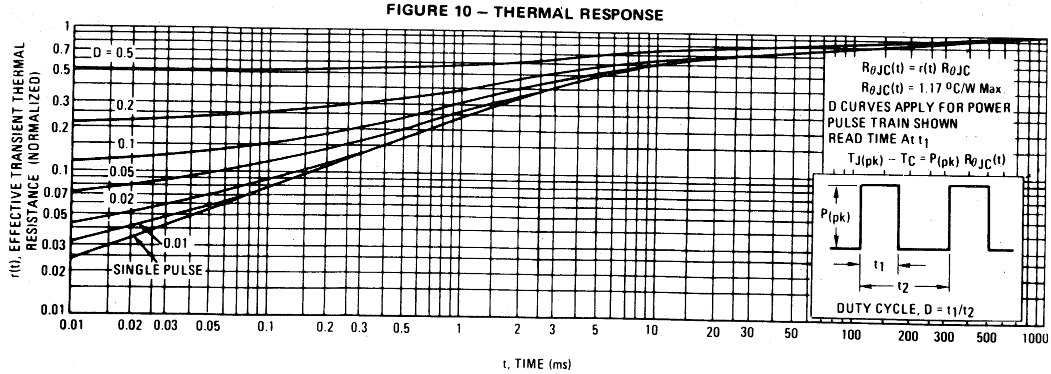


FIGURE 10 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

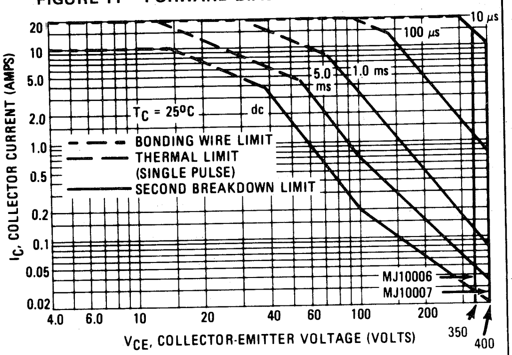
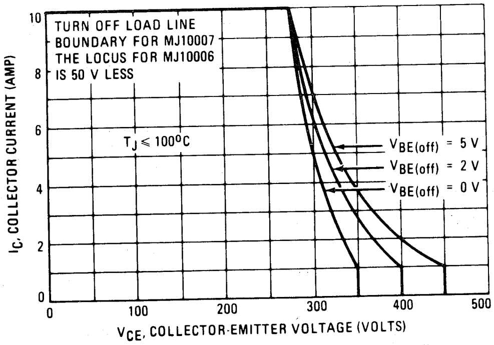


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

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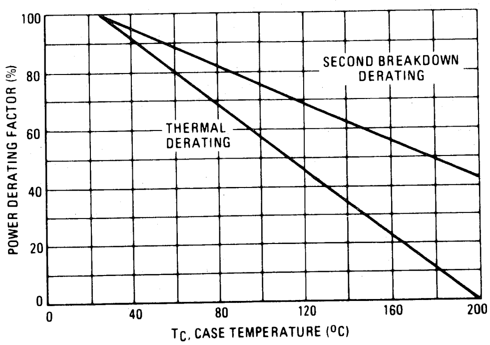
FIGURE 13 – POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

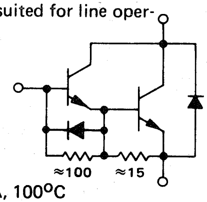
MJ10008
MJ10009

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10008 and MJ10009 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
  1.6 μs (max) Inductive Crossover Time — 10 A, 100°C
  3.5 μs (max) Inductive Storage Time — 10 A, 100°C

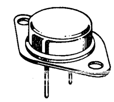
Operating Temperature Range -65 to +200°C

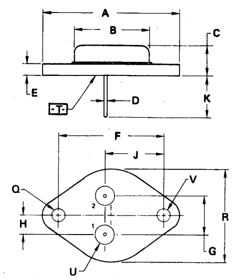
100°C Performance Specified for:
  Reversed Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents

20 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
450 and 500 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MJ10008	MJ10009	Unit
Collector-Emitter Voltage	V_{CEO}	450	500	Vdc
Collector-Emitter Voltage	V_{CEX}	450	500	Vdc
Collector-Emitter Voltage	V_{CEV}	650	700	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10008 MJ10009	$V_{CEO(sus)}$	450 500	– –	– –	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) (I_C = 2 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C, $V_{BE(off)}$ = 5 V) MJ10008 MJ10009 (I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C, $V_{BE(off)}$ = 5 V) MJ10008 MJ10009	$V_{CEX(sus)}$	450 500 325 375	– – – –	– – – –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	– –	– –	0.25 5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc) (I_C = 10 Adc, V_{CE} = 5 Vdc)	h_{FE}	40 30	– –	400 300	–
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 500 mAdc) (I_C = 20 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 500 mAdc, T_C = 100°C)	$V_{CE(sat)}$	– – –	– – –	2 3.5 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 500 mAdc) (I_C = 10 Adc, I_B = 500 mAdc, T_C = 100°C)	$V_{BE(sat)}$	– –	– –	2.5 2.5	Vdc
Diode Forward Voltage (1) (I_F = 10 Adc)	V_f	–	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	$\|h_{fe}\|$	8	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	100	–	325	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 25 μs Duty Cycle ≤ 2%)	t_d	–	0.12	0.25	μs
Rise Time	t_r	–	0.5	1.5	μs
Storage Time	t_s	–	0.8	2.0	μs
Fall Time	t_f	–	0.2	0.6	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_C = 10 A(pk), V_{clamp} = 250 V, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	1.5	3.5	μs
Crossover Time	t_c	–	0.36	1.6	μs
Storage Time (I_C = 10 A(pk), V_{clamp} = 250 V, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc)	t_{sv}	–	0.8	–	μs
Crossover Time	t_c	–	0.18	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

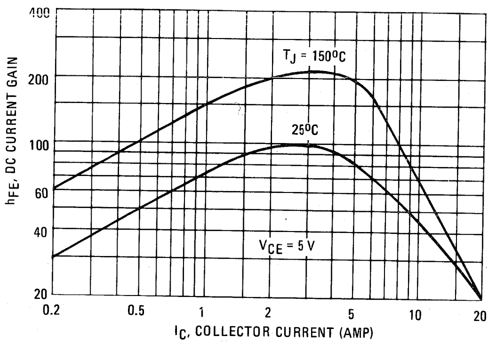


FIGURE 2 — COLLECTOR SATURATION REGION

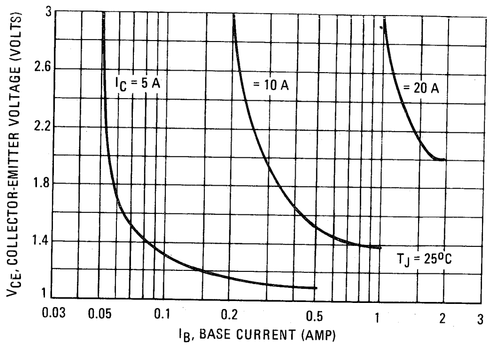


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

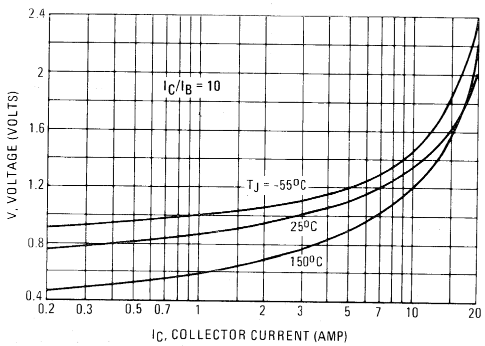


FIGURE 4 — BASE-EMITTER VOLTAGE

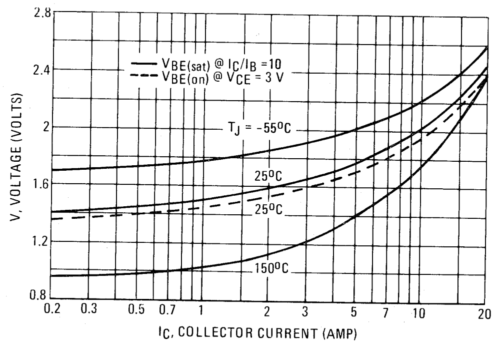


FIGURE 5 — COLLECTOR CUTOFF REGION

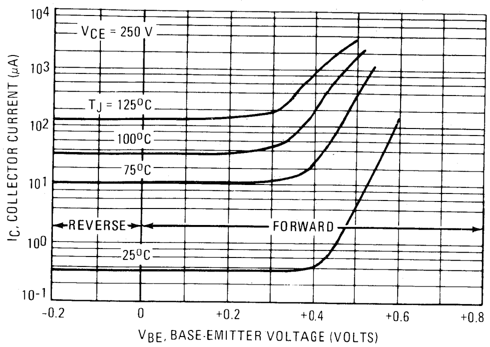


FIGURE 6 — OUTPUT CAPACITANCE

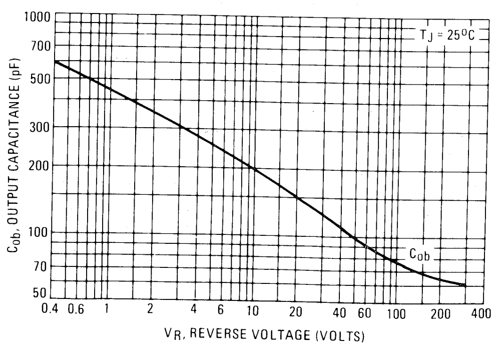
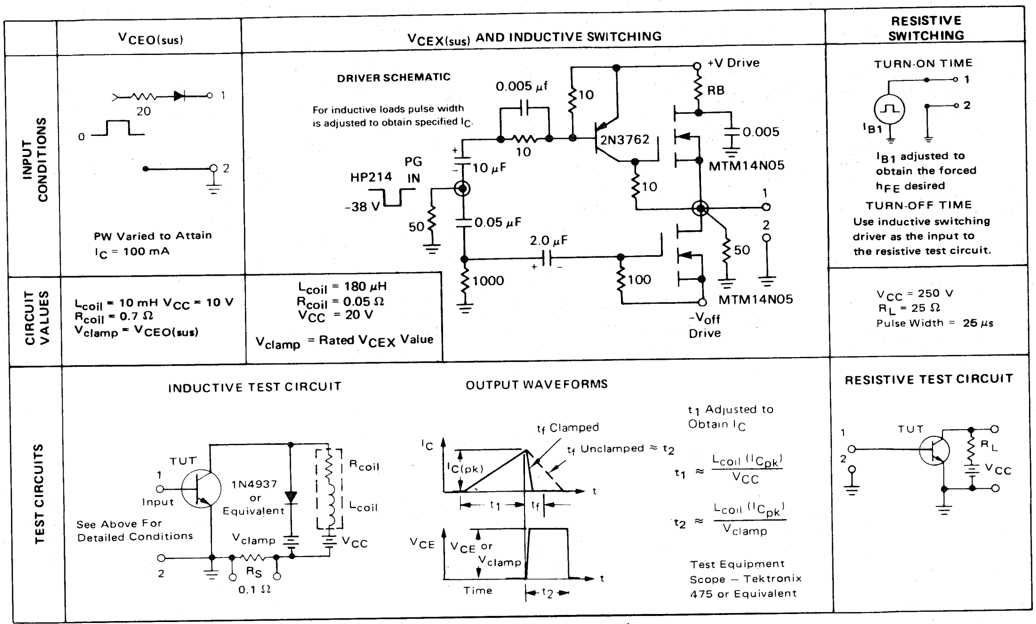
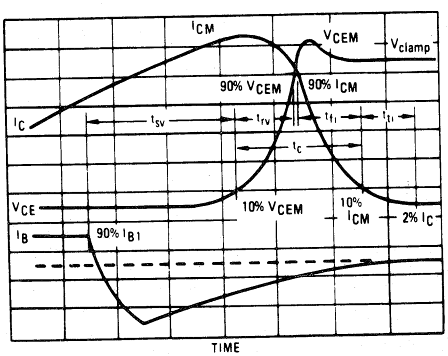


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust −V such that $V_{BE(off)}$ = 5 V except as required for RB SOA (Figure 12).

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

— continued —

3

TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 7. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at T_C = 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at T_C = 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

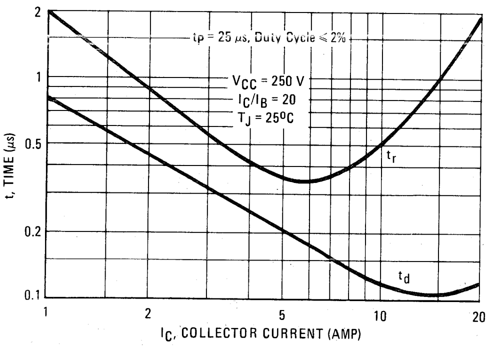


FIGURE 9 — TURN-OFF TIME

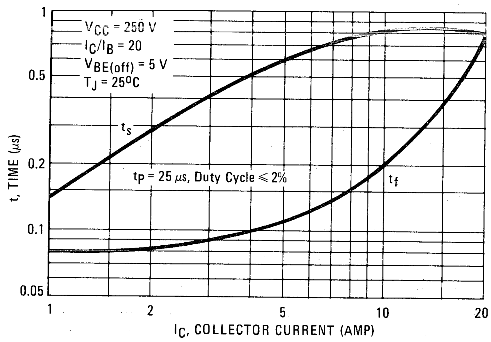
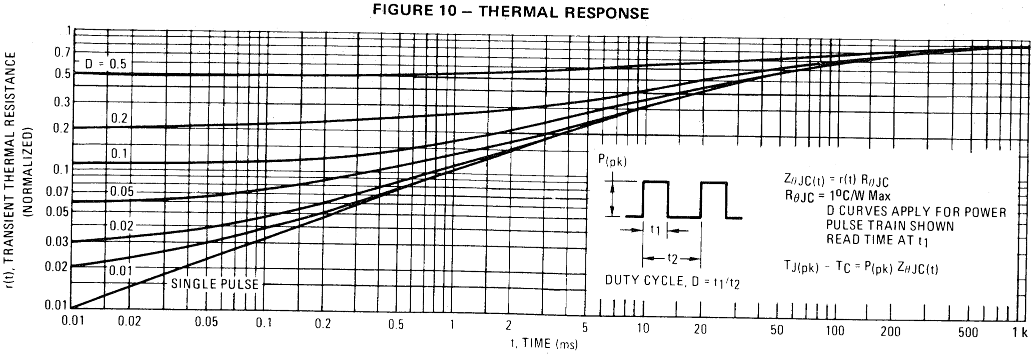


FIGURE 10 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

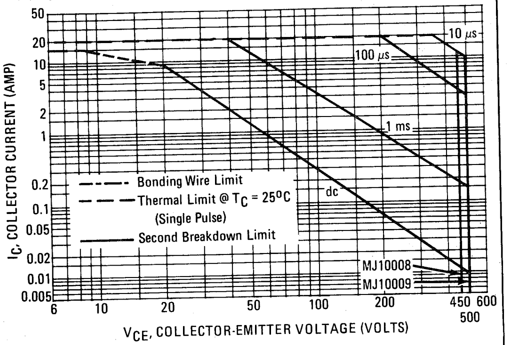


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA (MJ10009)

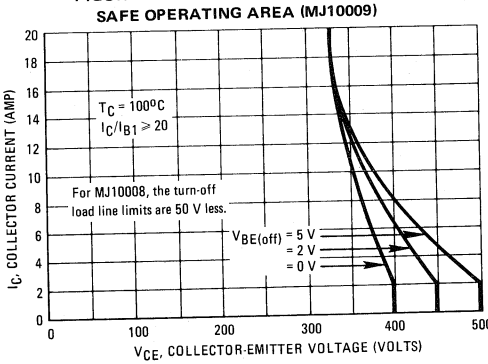
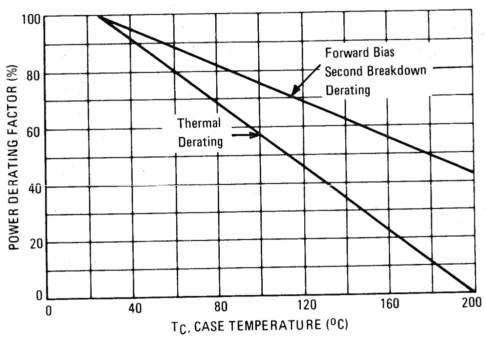


FIGURE 13 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

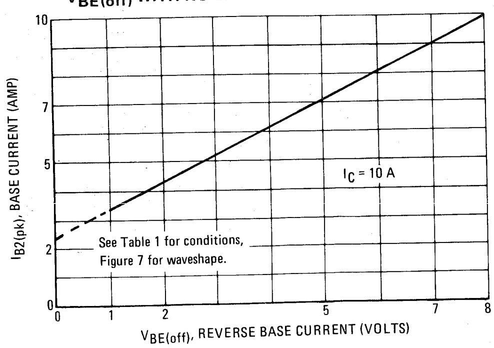
The data of Figure 11 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics. See Table 1 for circuit conditions.

FIGURE 14 – REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



3

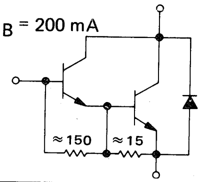
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ10011

DARLINGTON HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in deflection circuits.

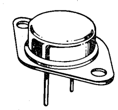
- $V_{CE(sat)}$ = 3.0 Volts (Max) @ I_C = 4.0 Amps, I_B = 200 mA
- Built-In Damper Diode
- V_{CEX} = 1400 Volts
- Glassivated Base-Collector Junction
- Safe Operating Area @ 50 μs = 25 A, 200 V



8.0 AMPERE

NPN SILICON DARLINGTON POWER TRANSISTOR

1400 VOLTS
80 WATTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEX}	1400	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	8.0 16	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	2.0 4.0	Adc
Emitter Current — Continuous Peak (1)	I_E I_{EM}	10 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.6	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

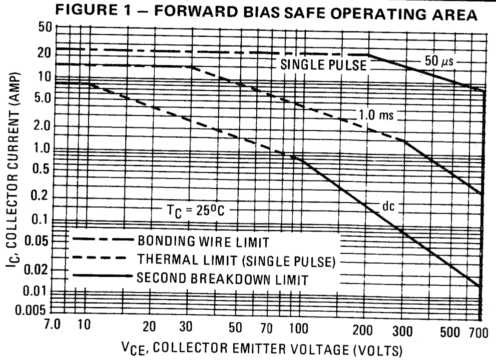
THERMAL CHARACTERISTICS

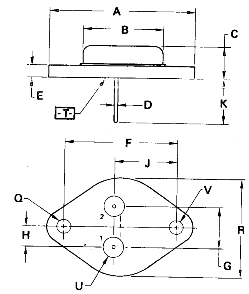
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1.8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 1.0 ms, Duty Cycle ≤ 10%.

3

FIGURE 1 — FORWARD BIAS SAFE OPERATING AREA





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
⌖ | ⌀.13 (0.005) Ⓜ | T | V Ⓜ
FOR LEADS:
⌖ | ⌀.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

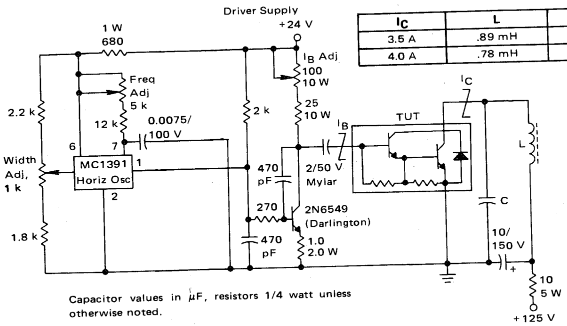
ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	700	—	—	Vdc
Collector Cutoff Current (V_{CE} = 1400 Vdc, V_{BE} = 0)	I_{CES}	—	—	0.25	mAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	—	50	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 3.5 Adc, I_B = 0.15 Adc) (I_C = 4.0 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$	— —	— —	3.0 3.0	Vdc
Base Emitter Saturation Voltage (I_C = 3.5 Adc, I_B = 0.15 Adc) (I_C = 4.0 Adc, I_B = 0.2 Adc)	$V_{BE(sat)}$	— —	— —	2.0 2.0	Vdc
Forward Diode Voltage (I_F = 4.0 Adc)	V_f	—	1.2	2.0	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 1			
SWITCHING CHARACTERISTICS					
Fall Time (See Figure 2) (I_C = 4.0 Adc, I_{B1} = 0.2 Adc)	t_f	—	0.65	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

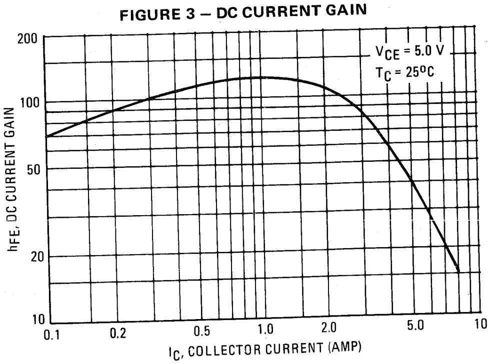
FIGURE 2 — FALL TIME TEST CIRCUIT

I_C	L	C
3.5 A	.89 mH	0.014 μF
4.0 A	.78 mH	0.016 μF



Capacitor values in μF, resistors 1/4 watt unless otherwise noted.

FIGURE 3 — DC CURRENT GAIN



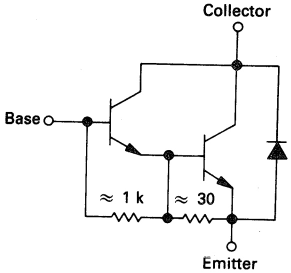
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ10012
MJH10012

NPN SILICON POWER DARLINGTON TRANSISTOR

The MJ10012 and MJH10012 are high-voltage, high-current Darlington transistors designed for automotive ignition, switching regulator and motor control applications.

- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 400 Vdc (Min)
- 175 Watts Capability at 50 Volts
- Automotive Functional Tests

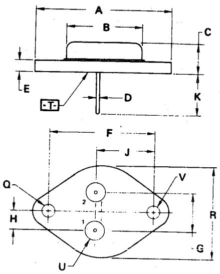


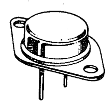
10 AMPERE

POWER TRANSISTORS
DARLINGTON NPN SILICON

400 VOLTS
175 AND 118 WATTS

MJ10012





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [-T-] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	ϕ0.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

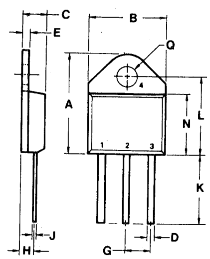
⌖	ϕ0.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

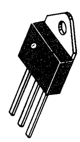
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA

MJH10012





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MJ10012	MJH10012	Unit
Collector-Emitter Voltage	V_{CEO}	400		Vdc
Collector-Emitter Voltage (R_{BE} = 27 Ω)	V_{CER}	550		Vdc
Collector-Base Voltage	V_{CBO}	600		Vdc
Emitter-Base Voltage	V_{EBO}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C	10 15		Adc
Base Current	I_B	2.0		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	118 47.5 1.05	Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	0.95	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Figure 1) (I_C = 200 mAdc, I_B = 0, V_{clamp} = Rated V_{CEO})	$V_{CEO(sus)}$	400	–	–	Vdc
Collector-Emitter Sustaining Voltage (Figure 1) (I_C = 200 mAdc, R_{BE} = 27 Ohms, V_{clamp} = Rated V_{CER})	$V_{CER(sus)}$	425	–	–	Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 27 Ohms)	I_{CER}	–	–	1.0	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	–	40	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 6.0 Vdc) (I_C = 6.0 Adc, V_{CE} = 6.0 Vdc) (I_C = 10 Adc, V_{CE} = 6.0 Vdc)	h_{FE}	 300 100 20	 550 350 150	 – 2000 –	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 6.0 Adc, I_B = 0.6 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	 – – –	 – – –	 1.5 2.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 0.6 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	 – –	 – –	 2.5 3.0	Vdc
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 6.0 Vdc)	$V_{BE(on)}$	–	–	2.8	Vdc
Diode Forward Voltage (I_F = 10 Adc)	V_f	–	2.0	3.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	–	165	350	pF
SWITCHING CHARACTERISTICS					
Storage Time (V_{CC} = 12 Vdc, I_C = 6.0 Adc, I_{B1} = I_{B2} = 0.3 Adc) Figure 2	t_s	–	7.5	15	μs
Fall Time (V_{CC} = 12 Vdc, I_C = 6.0 Adc, I_{B1} = I_{B2} = 0.3 Adc) Figure 2	t_f	–	5.2	15	μs
FUNCTIONAL TESTS					
Second Breakdown Collector Current with Base-Forward Biased	$I_{S/B}$	See Figure 10			–
Pulsed Energy Test (See Figure 12)	$\frac{I_C{}^2L}{2}$	–	–	180	mJ

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – SUSTAINING VOLTAGE TEST CIRCUIT

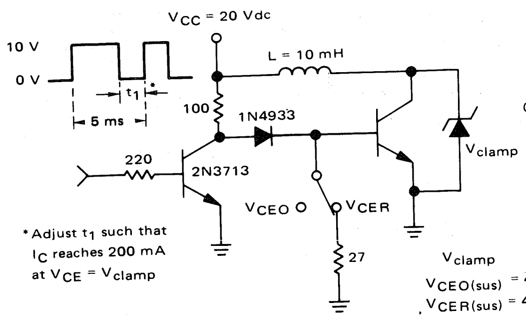


FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

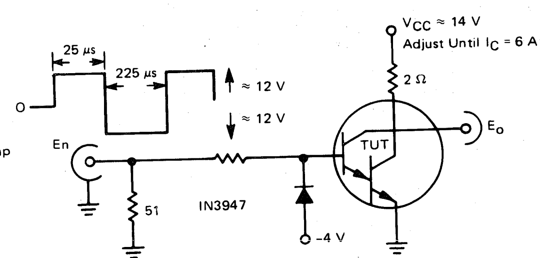


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FIGURE 3 — DC CURRENT GAIN

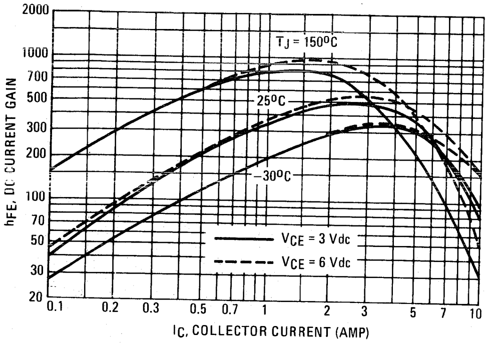


FIGURE 4 — COLLECTOR-SATURATION REGION

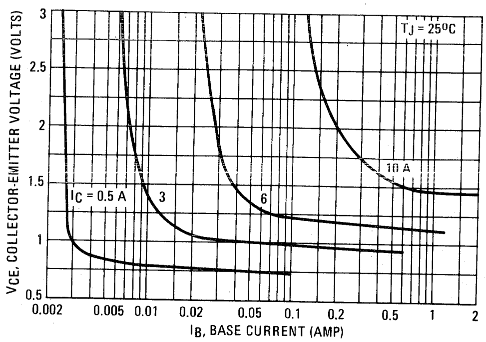


FIGURE 5 — COLLECTOR-EMITTER SATURATION VOLTAGE

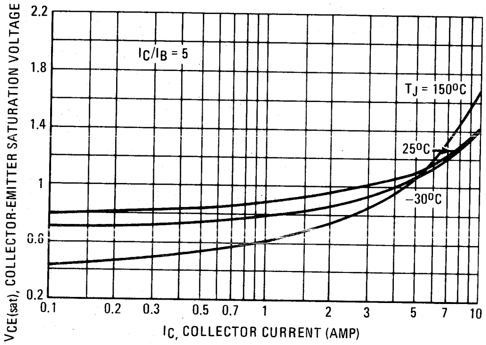


FIGURE 6 — BASE-EMITTER VOLTAGE

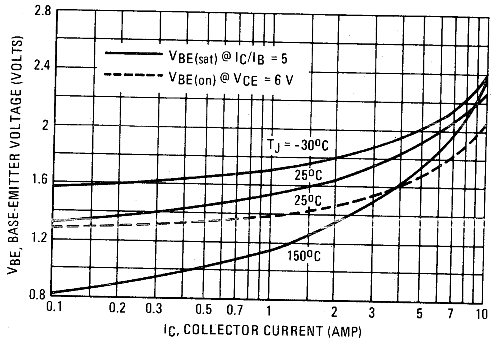


FIGURE 7 — TURN-OFF SWITCHING TIME

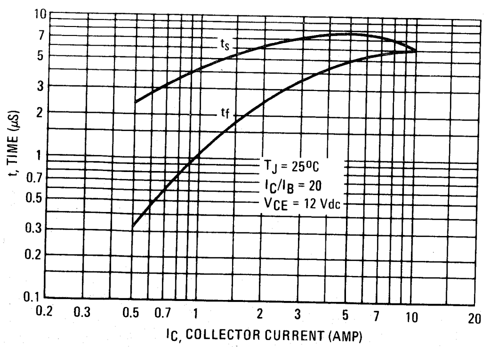


FIGURE 8 — COLLECTOR CUTOFF REGION

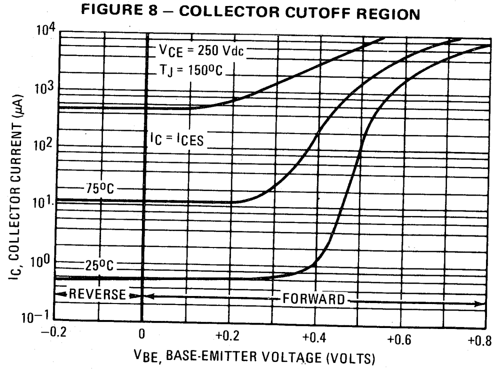


FIGURE 9 — THERMAL RESPONSE

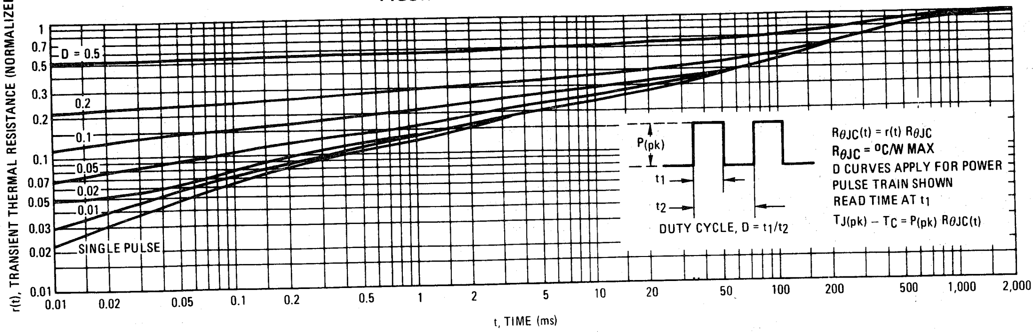
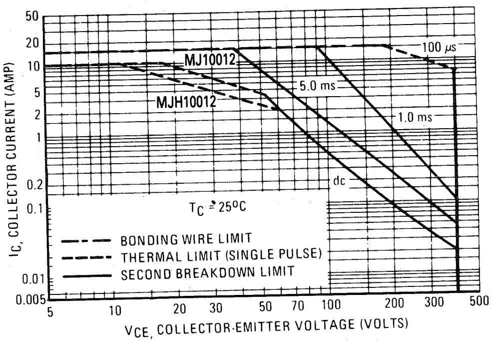


FIGURE 10 — FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^\circ C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^\circ C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 — POWER DERATING

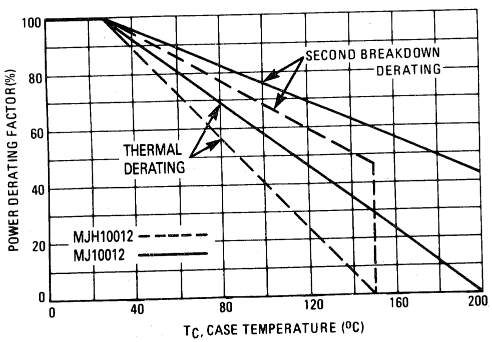
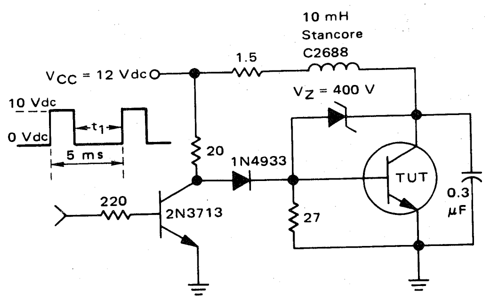


FIGURE 12 — USAGE TEST CIRCUIT



t_1 to be selected such that I_C reaches 6 Adc before switch-off.

NOTE:

"Usage Test," Figure 12 specifies energy handling capabilities in an automotive ignition circuit.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

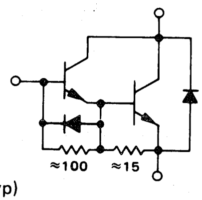
MJ10014

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTOR

The MJ10014 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



- Fast Turn-Off Times
  - 250 ns Inductive FAll Time—25°C (Typ)
  - 500 ns Inductive Crossover Time—25°C (Typ)
  - 1.4 μs Inductive Storage Time—25°C (Typ)
- Operating Temperature Range: -65 to +200°C
- 100°C Performance Specified for:
  - Reversed Biased SOA With Inductive Loads
  - Switching Times With Inductive Loads
  - Saturation Voltages
  - Leakage Currents

10 AMPERE
NPN SILICON POWER DARLINGTON TRANSISTOR
600 VOLTS
175 WATTS

Designers Data for "Worst-Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristic boundaries—are given to facilitate "worst-case" design.

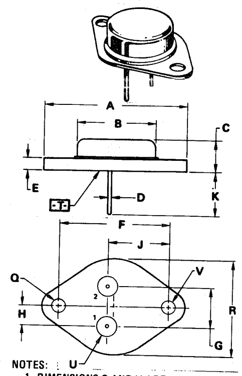
MAXIMUM RATINGS

Rating	Symbol	MJ10014	Unit
Collector-Emitter Voltage	V_{CEO}	600	Vdc
Collector-Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EB}	8	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 15	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	7 10	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ10014	$V_{CEO(sus)}$	600	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.3	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		—	—	5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	5	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)	I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	—	500	—
(I_C = 10 Adc, V_{CE} = 5 Vdc)		10	—	250	
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc)	$V_{CE(sat)}$	—	—	2.5	Vdc
(I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)		—	—	2.6	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc)	$V_{BE(sat)}$	—	—	3	Vdc
(I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)		—	—	3	
Diode Forward Voltage (1) (I_F = 10 Adc)	V_f	—	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	$\|h_{fe}\|$	10	—	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	100	—	350	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — (V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%).	t_d	—	0.02	0.2	μs
Rise Time	t_r	—	0.9	2	μs
Storage Time	t_s	—	0.95	4	μs
Fall Time	t_f	—	0.22	1	μs
Inductive Load, Clamped (Table 1)					
Storage Time — (I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_s	—	2.3	6	μs
Crossover Time	t_c	—	1	3	μs
Storage Time — (I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_s	—	1.4	—	μs
Crossover Time	t_c	—	0.5	—	μs
Fall Time	t_{fi}	—	0.25	—	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

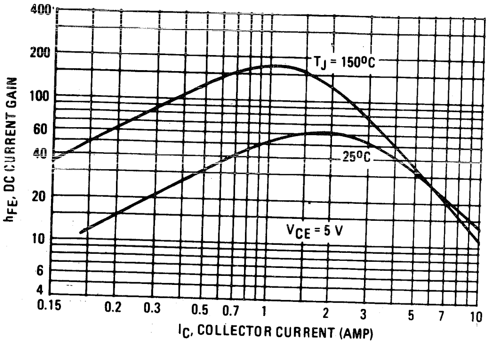


FIGURE 2 — COLLECTOR SATURATION REGION

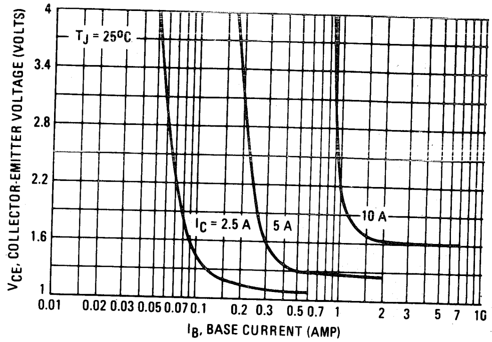


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

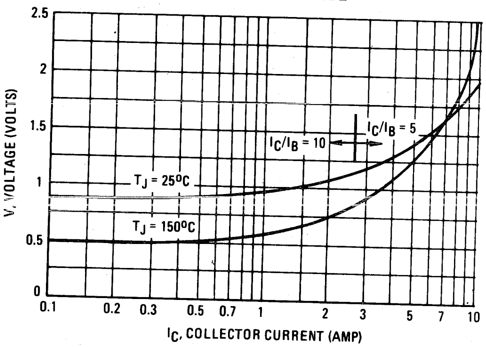


FIGURE 4 — BASE-EMITTER VOLTAGE

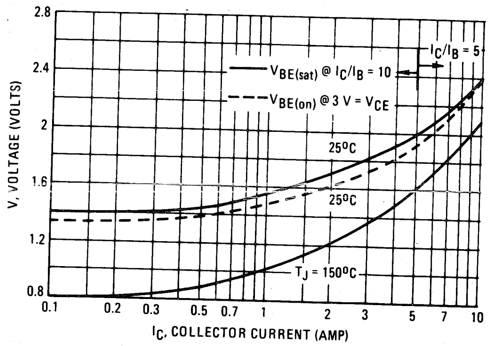


FIGURE 5 — COLLECTOR CUTOFF REGION

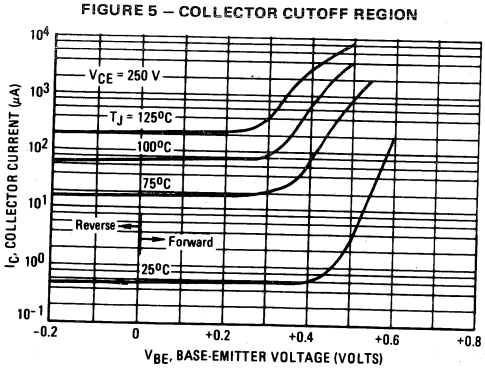


FIGURE 6 — OUTPUT CAPACITANCE

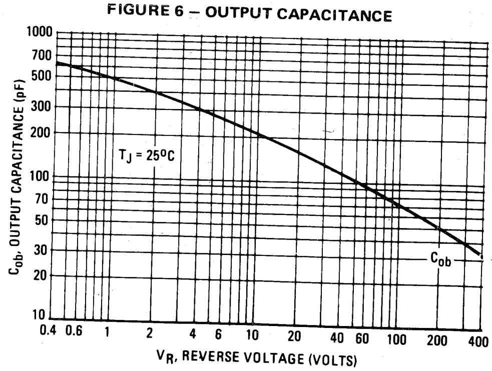
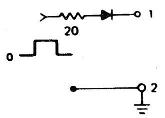
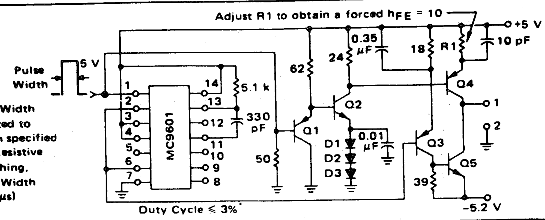
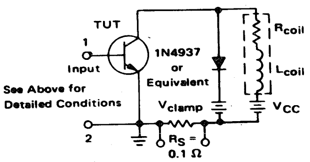
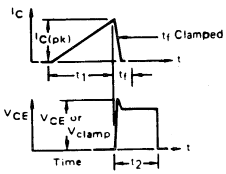
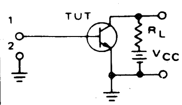


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA	 Pulse Width adjusted to obtain specified I_C (Resistive Switching. Pulse Width = 50 μs)	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

SWITCHING TIME NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

— continued —

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

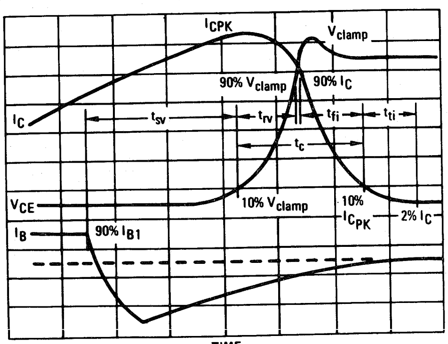
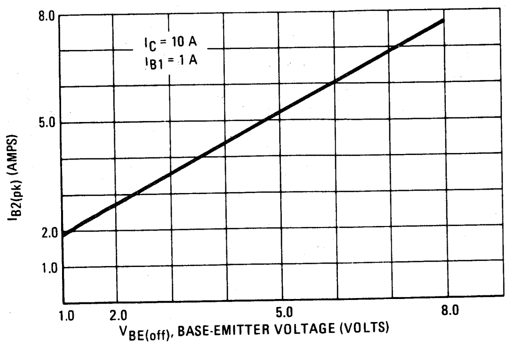


FIGURE 8 — PEAK REVERSE CURRENT



3

TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON TIME

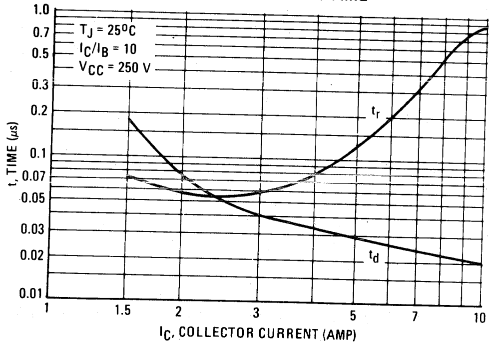


FIGURE 10 – TURN-OFF TIME

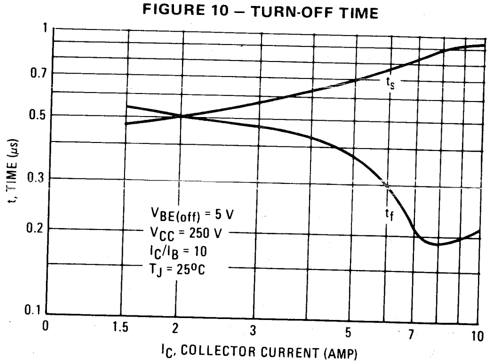
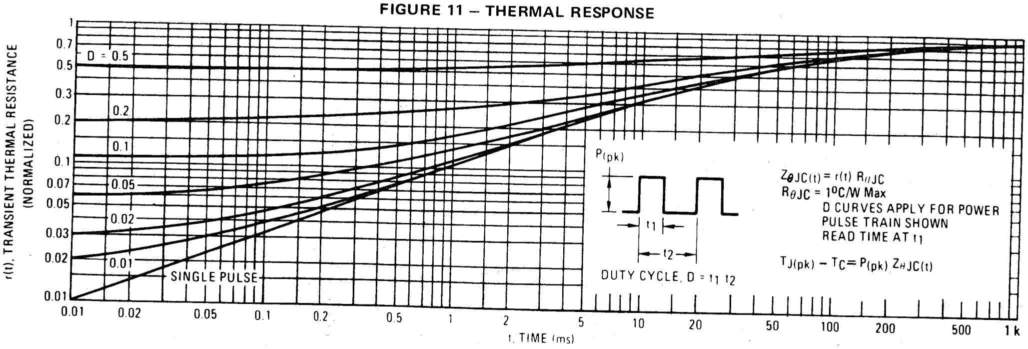


FIGURE 11 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for theses devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

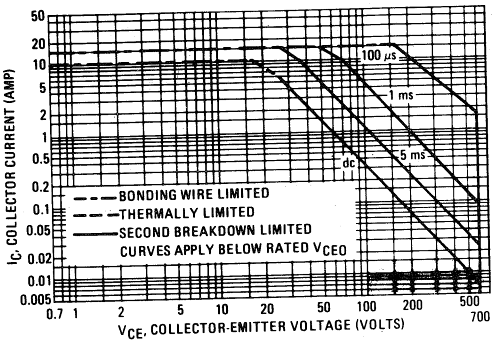
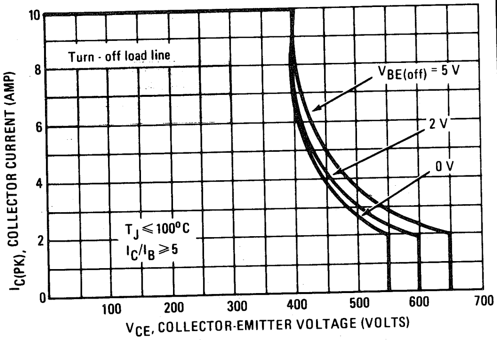


FIGURE 13 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

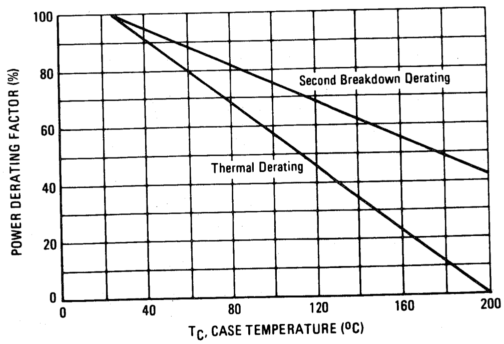
$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

3

FIGURE 14 – POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ10015
MJ10016

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

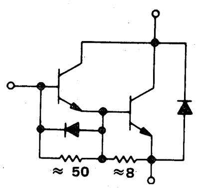
The MJ10015 and MJ10016 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

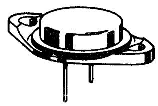
- Switching Regulators
- Motor Controls
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  - 1.0 μs (max) Inductive Crossover Time — 20 Amps
  - 2.5 μs (max) Inductive Storage Time — 20 Amps
- Operating Temperature Range −65 to +200°C
- Performance Specified for
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

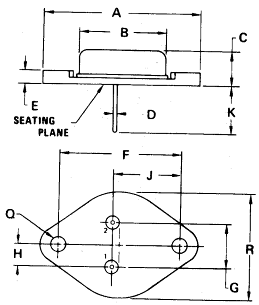
50 AMPERE

NPN SILICON POWER DARLINGTON TRANSISTORS

400 and 500 VOLTS
250 WATTS







STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

MAXIMUM RATINGS

Rating	Symbol	MJ10015	MJ10016	Unit
Collector-Emitter Voltage	V_{CEO}	400	500	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	50 75		Adc
Base Current — Continous — Peak (1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10015	$V_{CEO(sus)}$	400	—	—	Vdc
MJ10016		500	—	—	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.25	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)	I_{EBO}	—	—	350	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 7			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 8			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 20 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	25	—	—	—
(I_C = 40 Adc, V_{CE} = 5.0 Vdc)		10	—	—	
Collector-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	—	—	2.2	Vdc
(I_C = 50 Adc, I_B = 10 Adc)		—	—	5.0	
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	—	—	2.75	Vdc
Diode Forward Voltage (2) (I_F = 20 Adc)	V_f	—	2.5	5.0	Vdc
DYNAMIC CHARACTERISTIC					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	—	—	750	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — (V_{CC} = 250 Vdc, I_C = 20 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5 Vdc, t_p = 25 μs Duty Cycle ⩽ 2%).	t_d	—	0.14	0.3	μs
Rise Time	t_r	—	0.3	1.0	μs
Storage Time	t_s	—	0.8	2.5	μs
Fall Time	t_f	—	0.3	1.0	μs
Inductive Load, Clamped (Table 1)					
Storage Time — (I_C = 20 A(pk), V_{clamp} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc)	t_{sv}	—	1.0	2.5	μs
Crossover Time	t_c	—	0.36	1.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ⩽ 2%.
(2) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

3

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

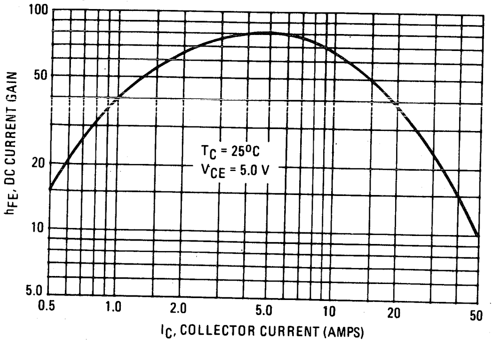


FIGURE 2 — COLLECTOR-EMITTER SATURATION VOLTAGE

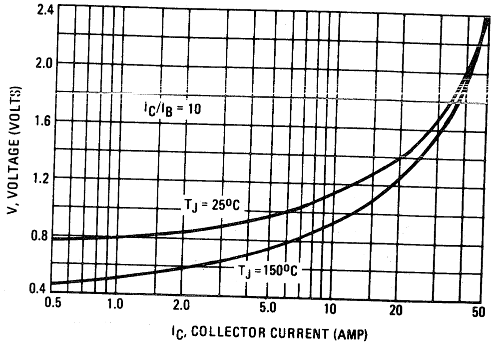


FIGURE 3 — BASE-EMITTER SATURATION VOLTAGE

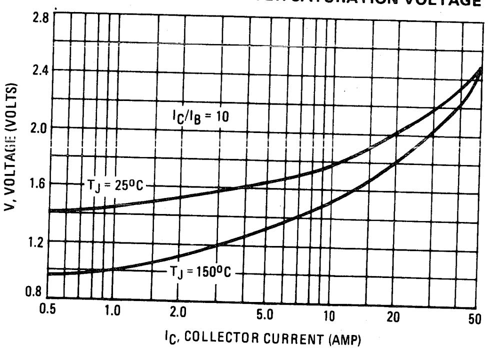


FIGURE 4 — COLLECTOR CUTOFF REGION

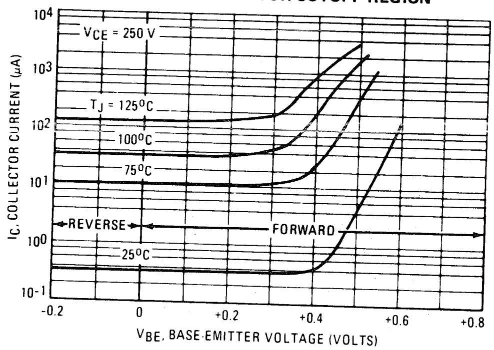


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FIGURE 5 — OUTPUT CAPACITANCE

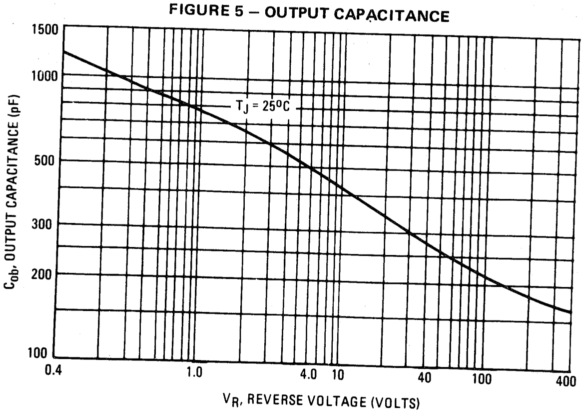
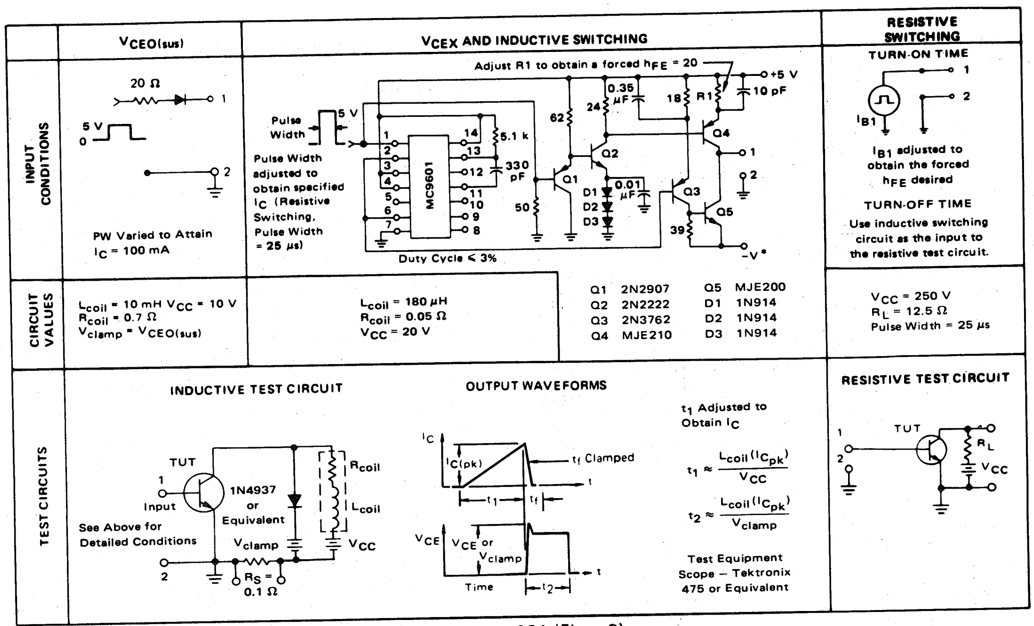
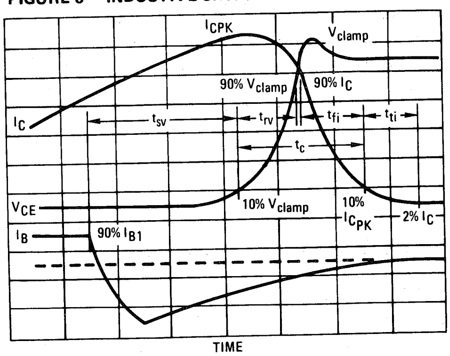


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust –V such that $V_{BE(off)}$ = 5 V except as required for RB SOA (Figure 8).

FIGURE 6 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed.

3

The Safe Operating Area figures shown in Figures 7 and 8 are specified ratings for these devices under the test conditions shown.

FIGURE 7 — FORWARD BIAS SAFE OPERATING AREA

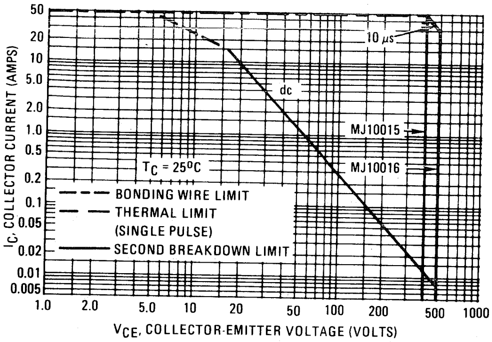
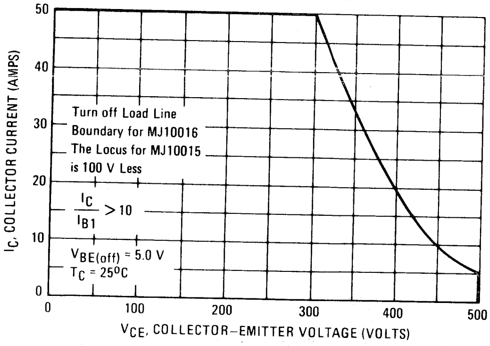


FIGURE 8 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the complete RBSOA characteristics.

FIGURE 9 — POWER DERATING

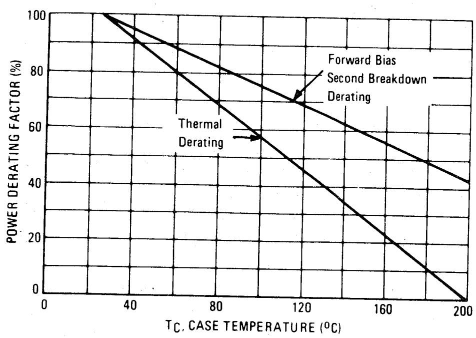
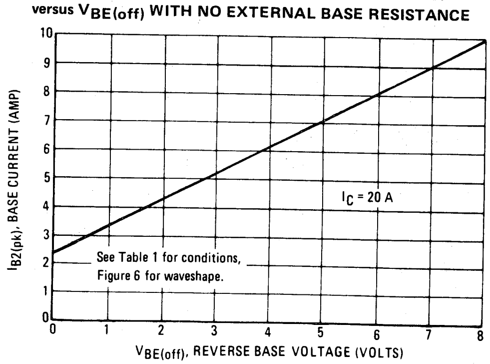


FIGURE 10 — TYPICAL REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



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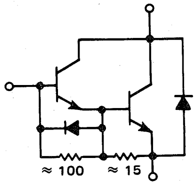
MJ10020
MJ10021

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10020 and MJ10021 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  - 150 ns Inductive Fall Time at 25°C (Typ)
  - 750 ns Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range −65 to +200°C
- 100°C Performance Specified for:
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



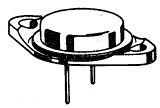
60 AMPERE

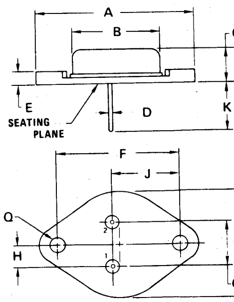
NPN SILICON POWER DARLINGTON TRANSISTORS

200 and 250 VOLTS
250 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

MAXIMUM RATINGS

Rating	Symbol	MJ10020	MJ10021	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Emitter Voltage	V_{CEV}	300	350	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	60 100		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	20 30		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJ10020 MJ10021	$V_{CEO(sus)}$	200 250	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	– –	– –	0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)		I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$		See Figure 13		
Clamped Inductive SOA with Base Reverse Biased		RBSOA		See Figure 14		
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 15 Adc, V_{CE} = 5.0 V)		h_{FE}	75	–	1000	–
Collector-Emitter Saturation Voltage (I_C = 30 Adc, I_B = 1.2 Adc) (I_C = 60 Adc, I_B = 4.0 Adc) (I_C = 30 Adc, I_B = 1.2 Adc, T_C = 100°C)		$V_{CE(sat)}$	– – –	– – –	2.2 4.0 2.4	Vdc
Base-Emitter Saturation Voltage (I_C = 30 Adc, I_B = 1.2 Adc) (I_C = 30 Adc, I_B = 1.2 Adc, T_C = 100°C)		$V_{BE(sat)}$	– –	– –	3.0 3.5	Vdc
Diode Forward Voltage (I_F = 30 Adc)		V_f	–	2.5	5.0	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	175	–	700	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 175 Vdc, I_C = 30 A, I_{B1} = 1.2 Adc, $V_{BE(off)}$ = 5.0 V, t_p = 25 μs Duty Cycle ≤ 2.0%).	t_d	–	0.02	0.2	μs
Rise Time		t_r	–	0.30	1.0	μs
Storage Time		t_s	–	1.0	3.5	μs
Fall Time		t_f	–	0.07	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	I_{CM} = 30 A(pk), V_{CEM} = 200 V, I_{B1} = 1.2 A, $V_{BE(off)}$ = 5 V, T_C = 100°C)	t_{sv}	–	1.2	3.5	μs
Crossover Time		t_c	–	0.45	2.0	μs
Storage Time	(I_{CM} = 30 A(pk), V_{CEM} = 200 V, I_{B1} = 1.2 A, $V_{BE(off)}$ = 5 V, T_C = 25°C)	t_{sv}	–	0.75	–	μs
Crossover Time		t_c	–	0.25	–	μs
Fall Time		t_{fi}	–	0.15	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%

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TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

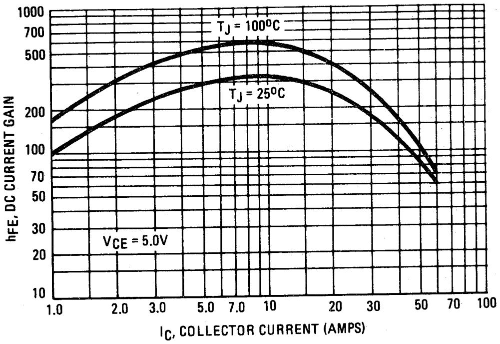

FIGURE 2 — COLLECTOR SATURATION REGION

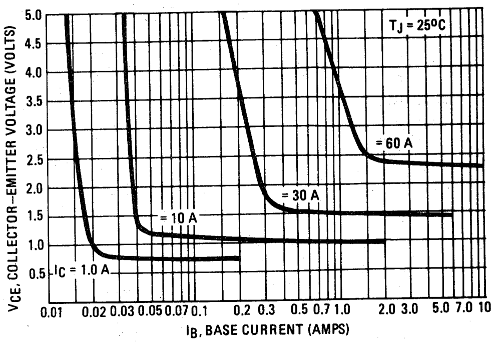

FIGURE 3 — COLLECTOR–EMITTER SATURATION VOLTAGE

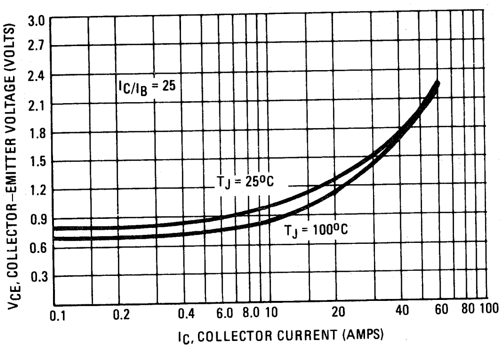

FIGURE 4 — BASE–EMITTER VOLTAGE

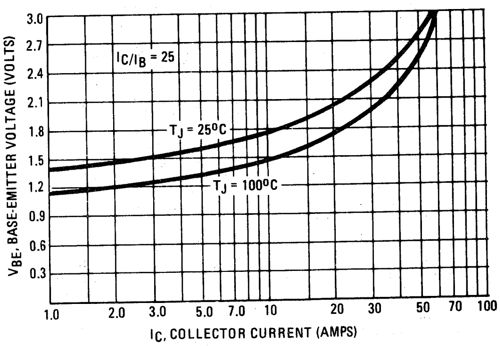

FIGURE 5 — COLLECTOR CUTOFF REGION

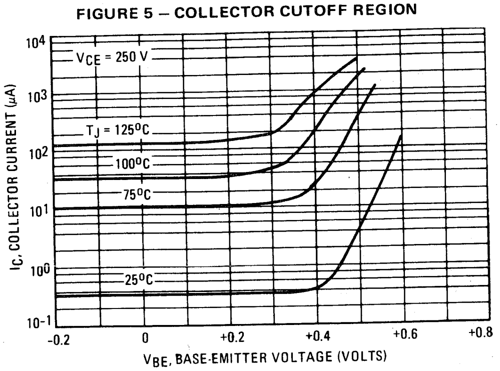

FIGURE 6 — OUTPUT CAPACITANCE

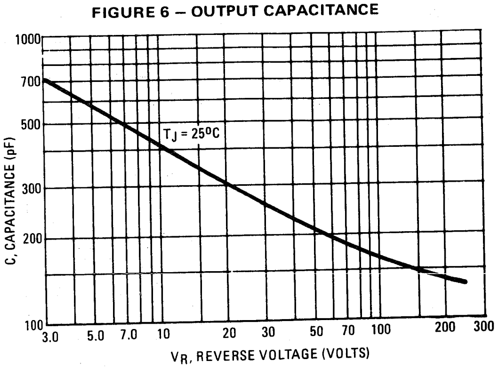

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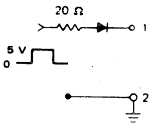
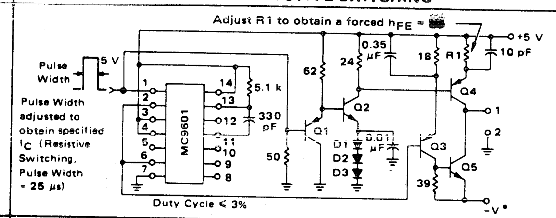
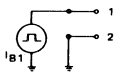
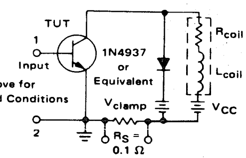
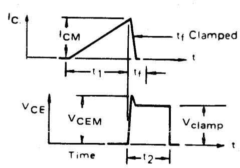
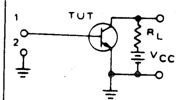
TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 25 μs)	TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching circuit as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V Q1 2N2907 Q5 MJE15028 Q2 2N2222 D1 1N914 Q3 2N3762 D2 1N914 Q4 MJE15029 D3 1N914	V_{CC} = 175 V R_L = 5.6 Ω Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

*Adjust – V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

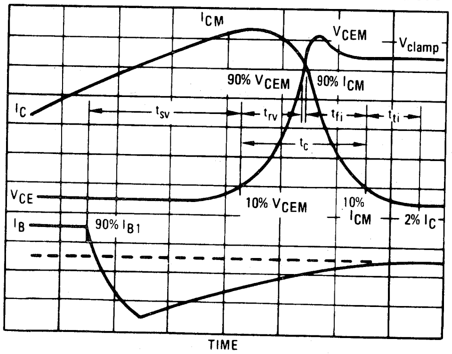


FIGURE 8 – TYPICAL PEAK REVERSE BASE CURRENT

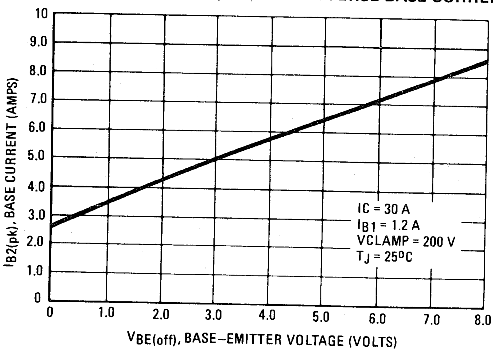
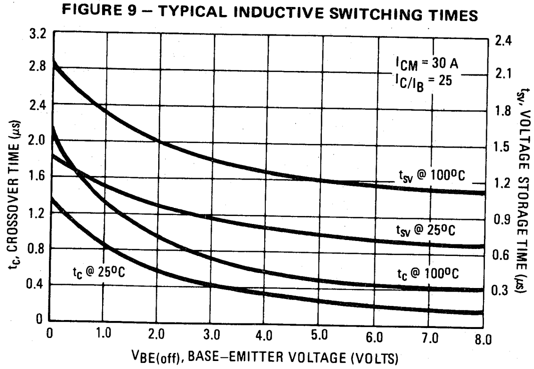


FIGURE 9 – TYPICAL INDUCTIVE SWITCHING TIMES



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SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{rv} = Voltage Rise Time, 10 – 90% V_{CEM}

t_{fi} = Current Fall Time, 90 – 10% I_{CM}

t_{ti} = Current Tail, 10 – 2% I_{CM}

t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

FIGURE 10 – TYPICAL TURN-ON SWITCHING TIMES

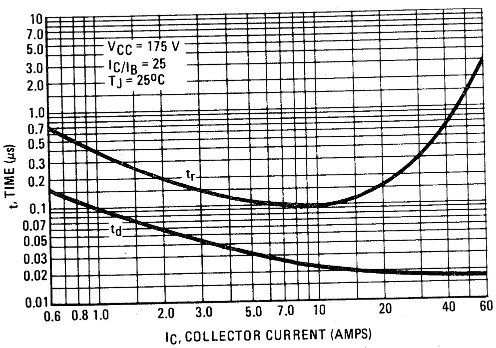


FIGURE 11 – TYPICAL TURN-OFF SWITCHING TIMES

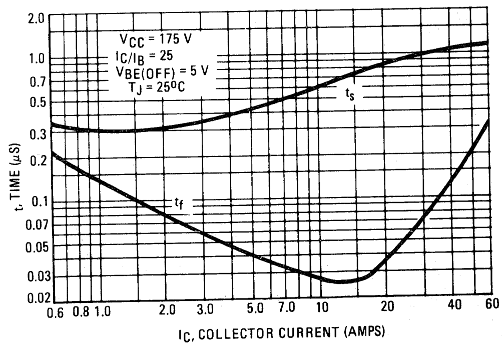
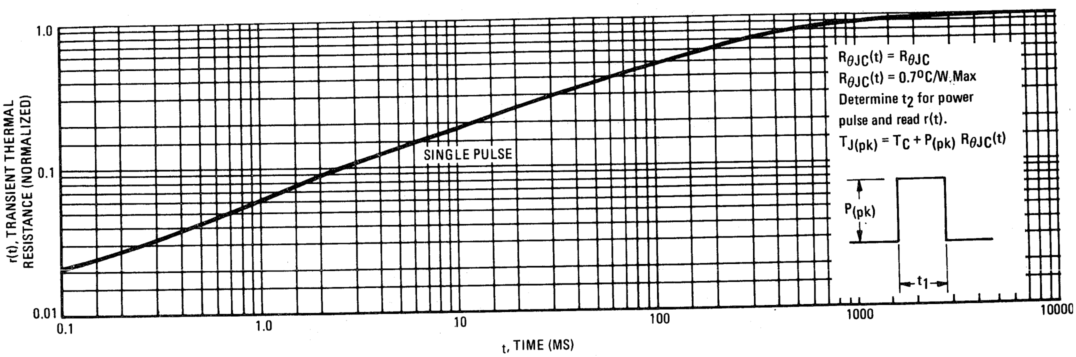


FIGURE 12 – THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA

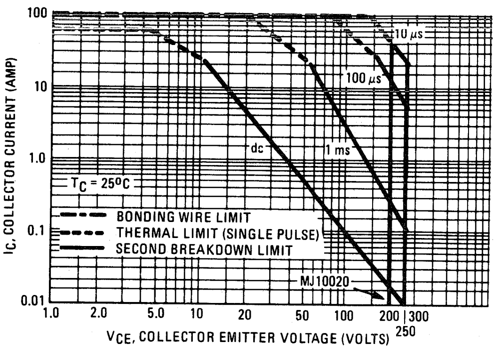
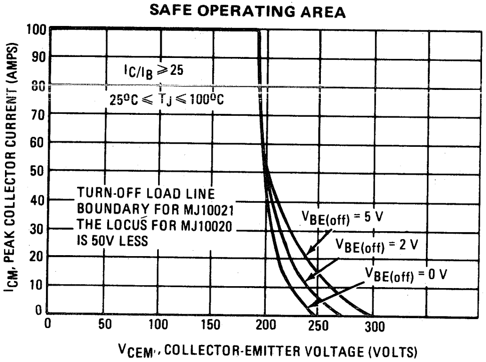


FIGURE 14 – MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

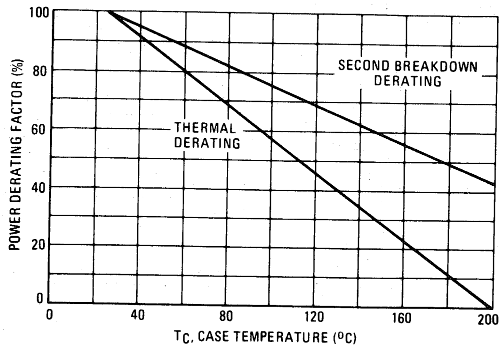
The data of Figure 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25° C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

FIGURE 15 – POWER DERATING



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

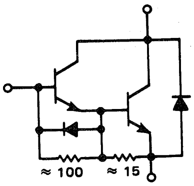
MJ10022
MJ10023

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10022 and MJ10023 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  150 ns Inductive Fall Time @ 25°C (Typ)
  300 ns Inductive Storage Time @ 25°C (Typ)
- Operating Temperature Range −65 to +200°C
- 100°C Performance Specified for:
  Reversed Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents



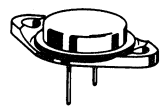
40 AMPERE

NPN SILICON POWER DARLINGTON TRANSISTORS

350 and 400 VOLTS
250 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



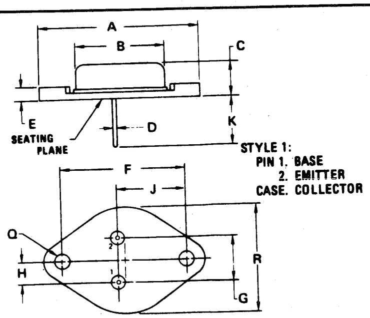
MAXIMUM RATINGS

Rating	Symbol	MJ10022	MJ10023	Unit
Collector-Emitter Voltage	V_{CEO}	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	450	600	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	40 80		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	20 40		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ⩽ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJ10022 MJ10023	$V_{CEO(sus)}$	350 400	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)		I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$		See Figure 13		
Clamped Inductive SOA with Base Reverse Biased		RBSOA		See Figure 14		
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 V)		h_{FE}	50	—	600	—
Collector-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc) I_C = 40 Adc, I_B = 5.0 Adc) (I_C = 20 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	— — —	— — —	2.2 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.2 Adc) (I_C = 20 Adc, I_B = 1.2 Adc, T_C = 100°C)		$V_{BE(sat)}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage (I_F = 20 Adc)		V_f	—	2.5	5.0	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	150	—	600	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 20 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5.0 V, t_p = 50 μs, Duty Cycle ⩽ 2.0%)	t_d	—	0.03	0.2	μs
Rise Time		t_r	—	0.4	1.2	μs
Storage Time		t_s	—	0.9	2.5	μs
Fall Time		t_f	—	0.3	0.9	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_{CM} = 20 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 V, T_C = 100°C)	t_{sv}	—	1.9	4.4	μs
Crossover Time		t_c	—	0.6	2.0	μs
Fall Time		t_{fi}	—	0.3	—	μs
Storage Time	(I_{CM} = 20 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 V, T_C = 25°C)	t_{sv}	—	1.0	—	μs
Crossover Time		t_c	—	0.3	—	μs
Fall Time		t_{fi}	—	0.15	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ⩽ 2%

3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

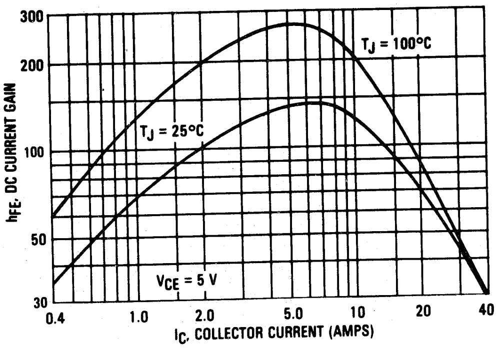


FIGURE 2 — COLLECTOR SATURATION REGION

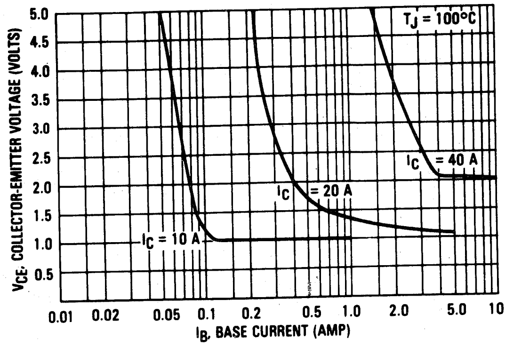


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

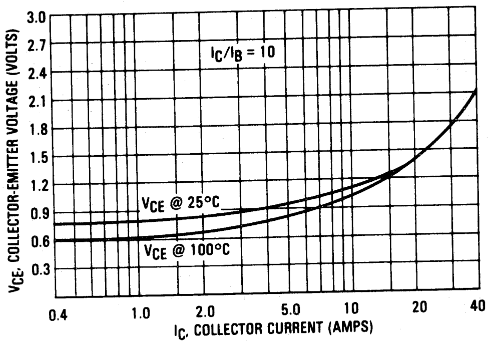


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

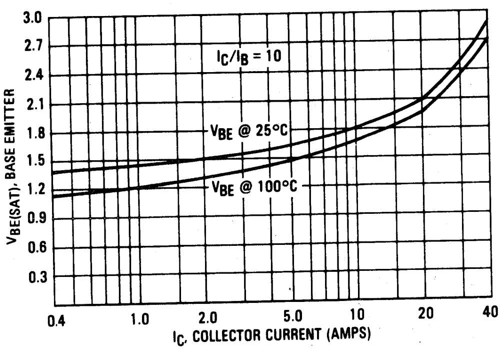


FIGURE 5 — COLLECTOR CUTOFF REGION

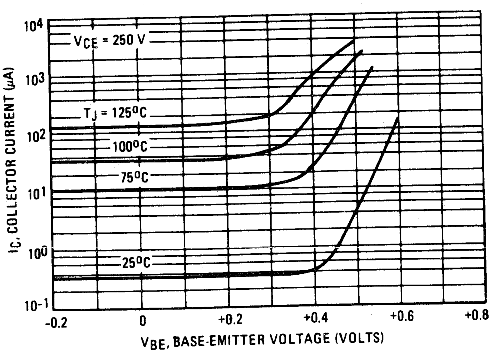
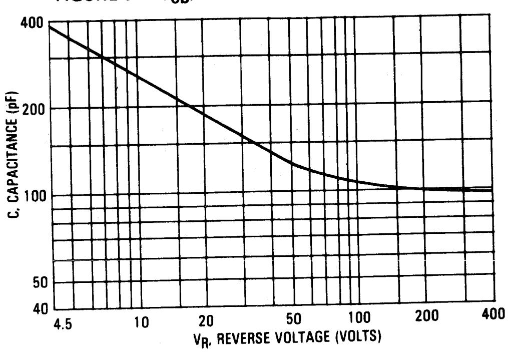
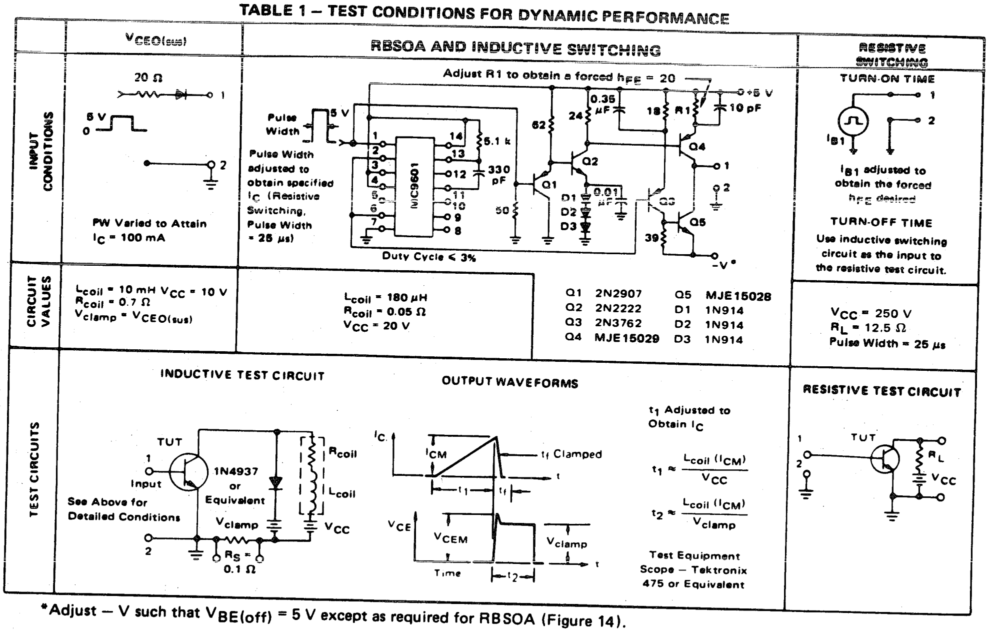


FIGURE 6 — C_{ob}, OUTPUT CAPACITANCE



3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust — V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

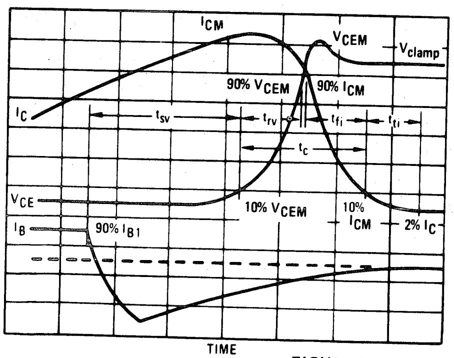


FIGURE 8 — TYPICAL PEAK REVERSE BASE CURRENT

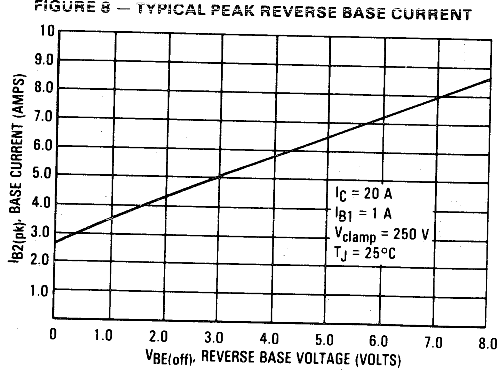
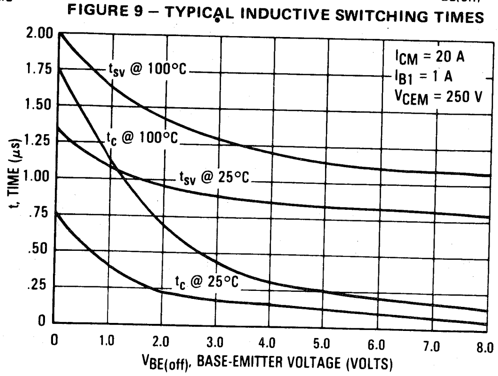


FIGURE 9 — TYPICAL INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user orinented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 10 — TYPICAL TURN-ON SWITCHING TIMES

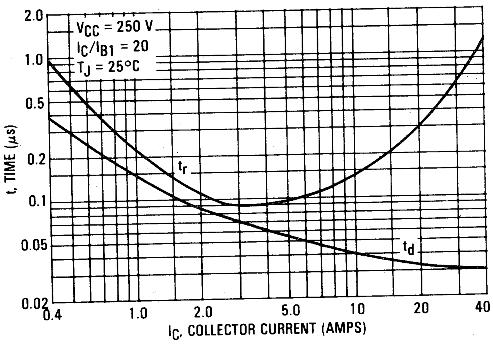


FIGURE 11 — TYPICAL TURN-OFF SWITCHING TIMES

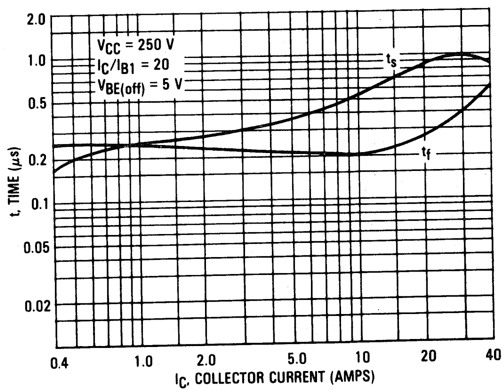
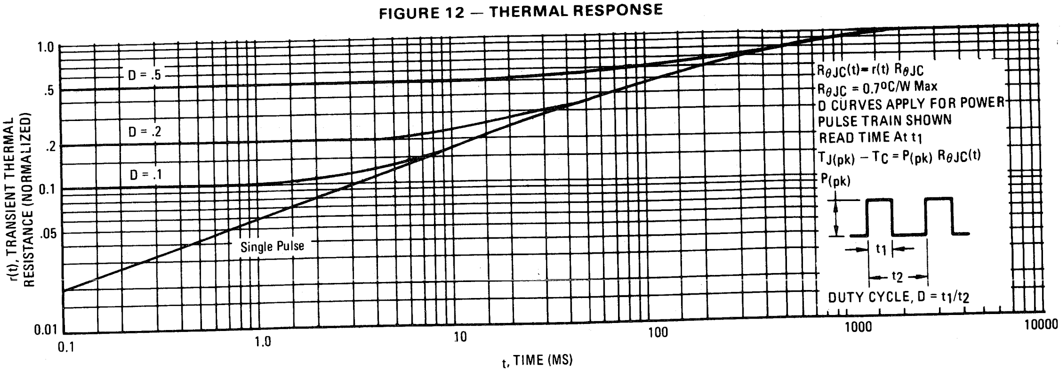


FIGURE 12 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA

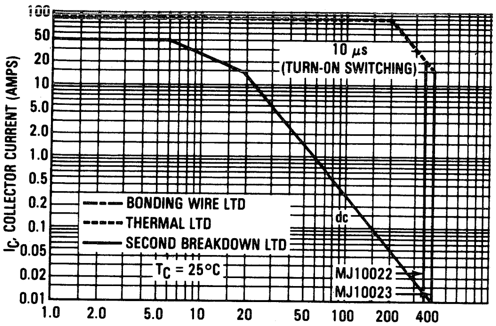
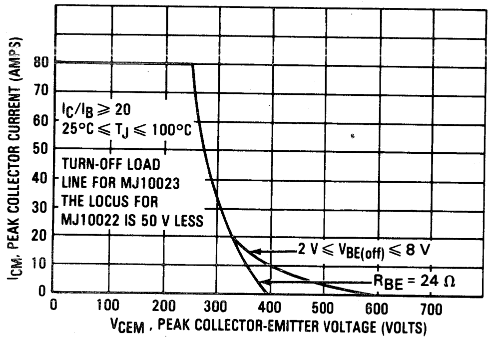


FIGURE 14 – MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

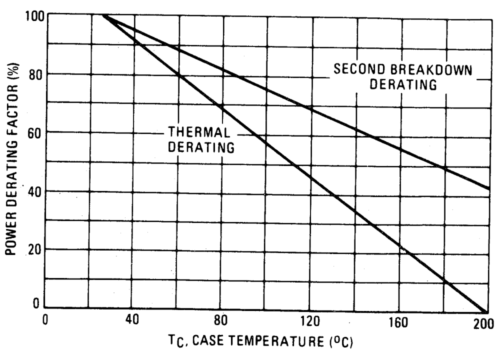
The data of Figure 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

FIGURE 15 – POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ10024
MJ10025

Designer's Data Sheet

20 AMPERE

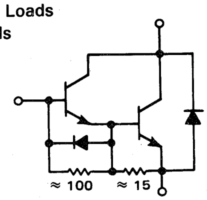
NPN SILICON POWER DARLINGTON TRANSISTORS

750 and 850 VOLTS
250 WATTS

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

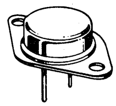
The MJ10024 and MJ10025 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

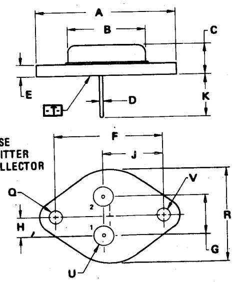
- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Operating Temperature Range −65 to +200°C
- 100°C Performance Specified for:
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.





STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
⌖ | ⌀0.13 (0.005) Ⓜ | T | V Ⓜ
FOR LEADS:
⌖ | ⌀0.13 (0.005) Ⓜ | T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05

MAXIMUM RATINGS

Rating	Symbol	MJ10024	MJ10025	Unit
Collector-Emitter Voltage	V_{CEO}	750	850	Vdc
Collector-Emitter Voltage	V_{CEV}	1000	1200	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 40		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 20		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ10024		$V_{CEO(sus)}$	750	—	—	Vdc
MJ10025			850	—	—	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	—	—	0.25	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			—	—	5.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)		I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$		See Figure 14		
Clamped Inductive SOA with base reverse biased		RBSOA		See Figure 15		
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 V)		h_{FE}	50	—	600	—
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	—	—	2.2	Vdc
(I_C = 20 Adc, I_B = 5.0 Adc)			—	—	5.0	
(I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)			—	—	2.5	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	—	—	2.5	Vdc
(I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)			—	—	2.5	
Diode Forward Voltage (I_F = 10 Adc)		V_f	—	1.25	4.0	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	110	—	500	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5.0 V, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	—	0.03	0.3	μs
Rise Time		t_r	—	0.6	1.8	
Storage Time		t_s	—	2.0	5.0	
Fall Time		t_f	—	0.6	1.8	
Inductive Load, Clamped (Table 1)						
Storage Time	(I_{CM} = 10 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 V, T_C = 100°C)	t_{sv}	—	2.9	7.0	μs
Crossover Time		t_c	—	1.0	3.3	
Storage Time	(I_{CM} = 10 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, R_{BE} = 24 Ω, T_C = 100°C	t_{sv}	—	21	50	μs
Crossover Time		t_c	—	9.0	25	
Storage Time	(I_{CM} = 10 A, V_{CEM} = 250 V, $V_{BE(off)}$ = 5.0 V, I_{B1} Baker Clamped [1 Ampere Source], T_C = 100°C)	t_{sv}	—	2.2	—	μs
Crossover Time		t_c	—	0.5	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%

3

FIGURE 1 — DC CURRENT GAIN

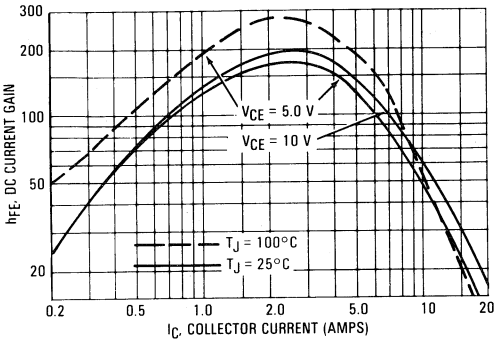


FIGURE 2 — COLLECTOR SATURATION REGION

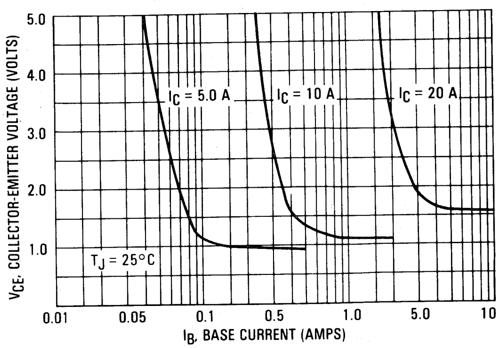


FIGURE 3 — COLLECTOR SATURATION VOLTAGE

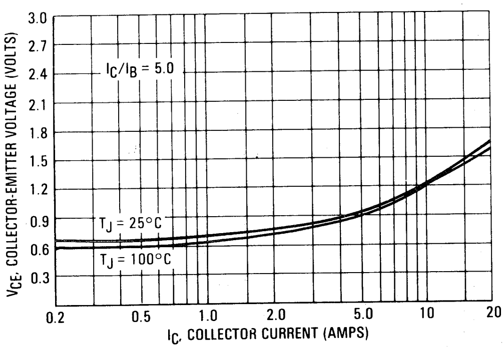


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

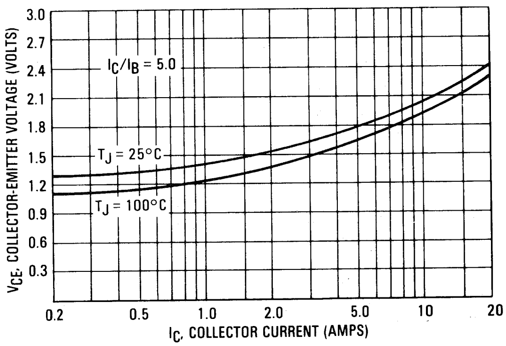


FIGURE 5 — COLLECTOR CUTOFF REGION

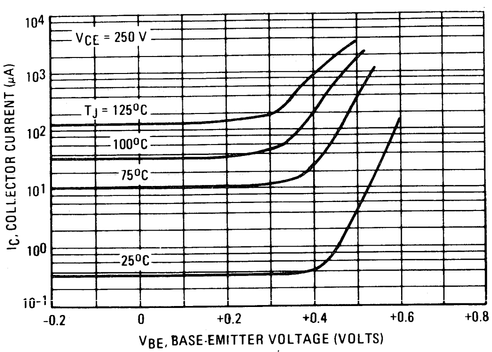


FIGURE 6 — C_{ob}, OUTPUT CAPACITANCE

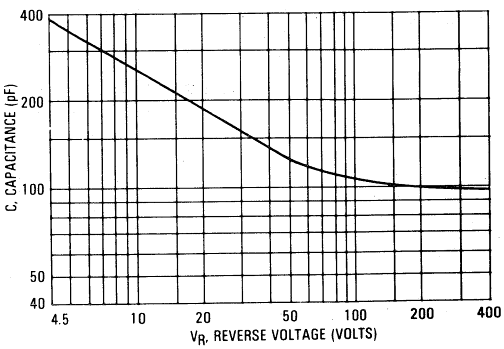
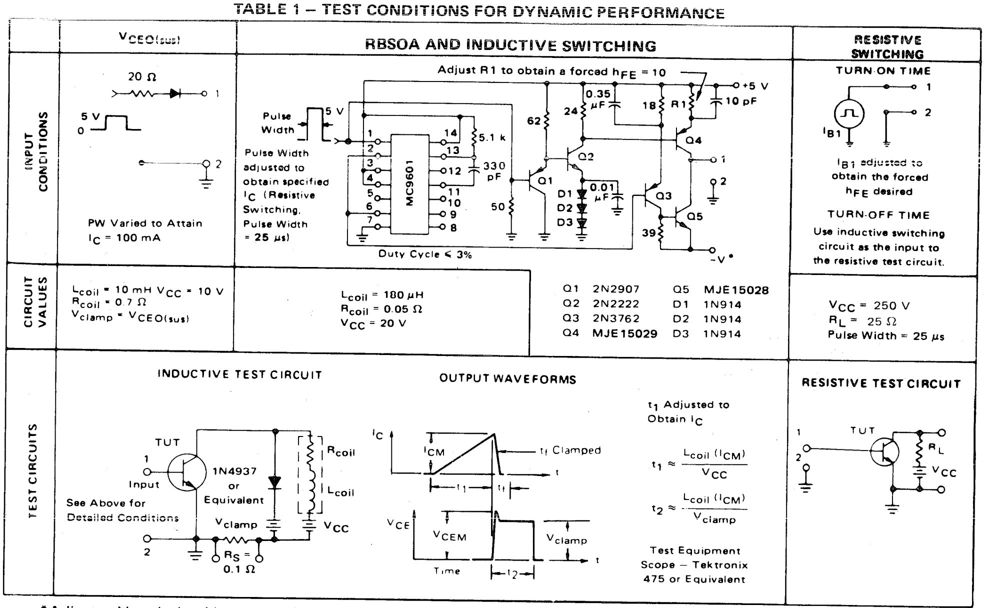


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust — V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

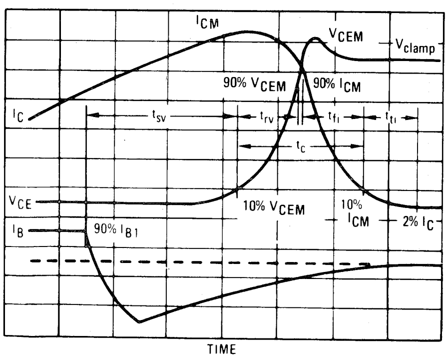


FIGURE 8 — TYPICAL PEAK REVERSE BASE CURRENT

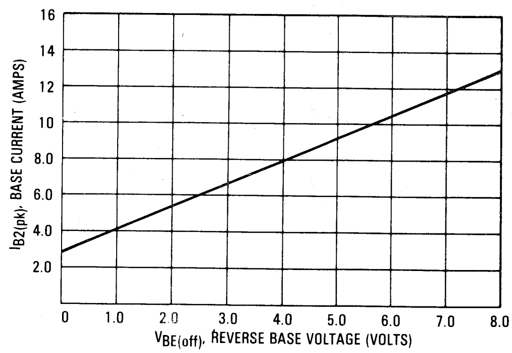


FIGURE 9 — TYPICAL INDUCTIVE SWITCHING TIMES

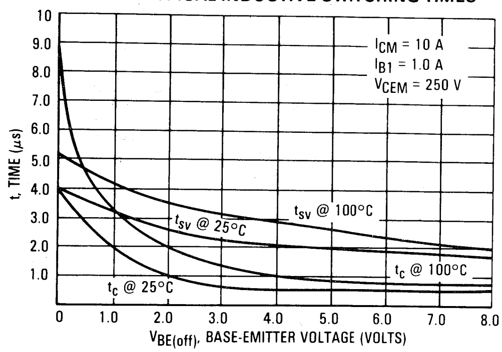
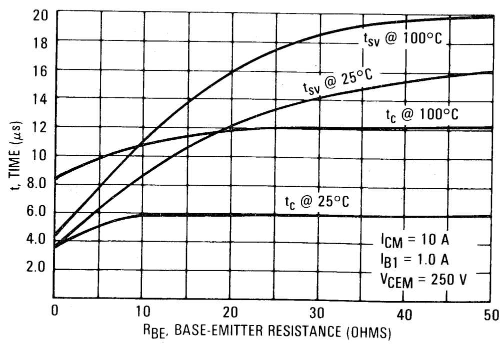


FIGURE 10 — TYPICAL INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user orinented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 11 — TYPICAL TURN-ON SWITCHING TIMES

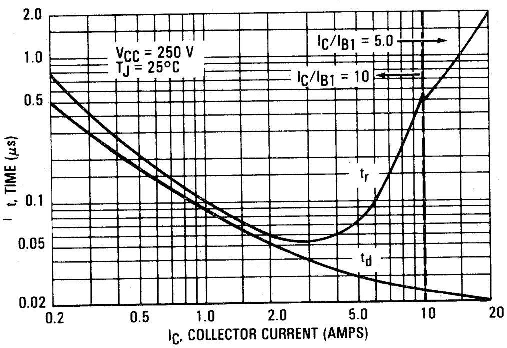


FIGURE 12 — TYPICAL TURN-OFF SWITCHING TIMES

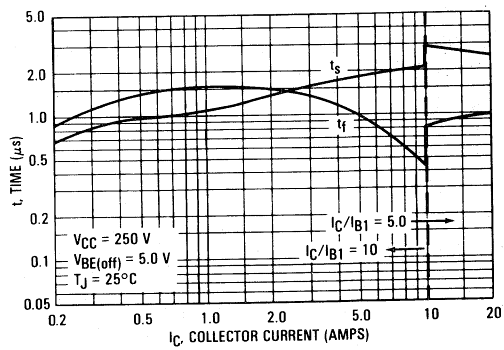
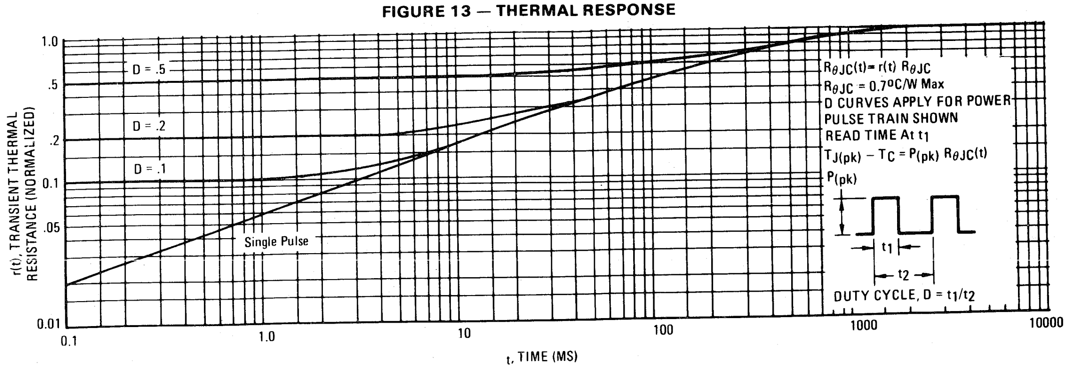


FIGURE 13 — THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 14 and 15 are specified for these devices under the test conditions shown.

FIGURE 14 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

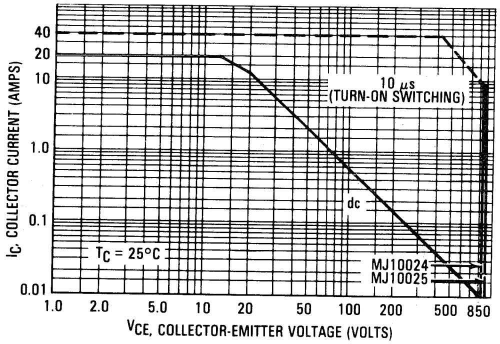
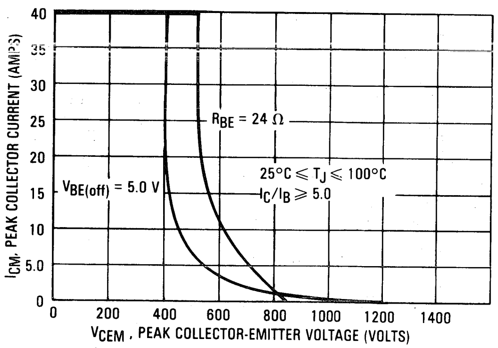


FIGURE 15 — MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

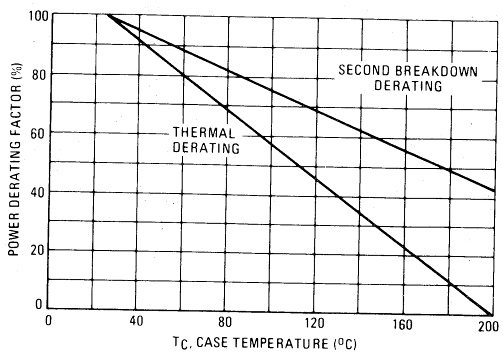
The data of Figure 14 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 14 may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

FIGURE 16 — POWER DERATING



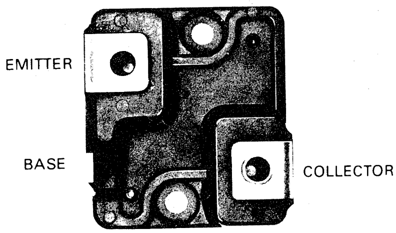
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

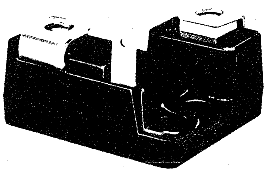
MJ10041
MJ10044
MJ10047

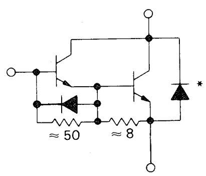
Designer's Data Sheet

25 kVA ENERGY MANAGEMENT SERIES SWITCHMODE DARLINGTON TRANSISTORS
25, 50 and 100 Ampere Operating Current

These Darlington transistors are designed for industrial service under practical operating environments requiring fast switching speed for highly efficient systems operating at high frequency such as inverters, PWM controllers and other high frequency systems operating from 120, 230 and 460 V lines.





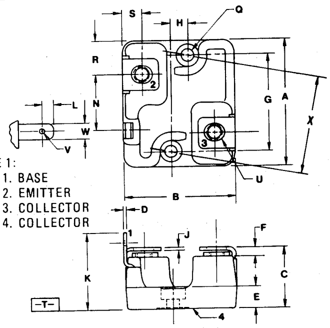


*Emitter-Collector Diode is a fast recovery high power diode.
Note: The 8 ohm resistor is not included in the MJ10044 and MJ10047.

25, 50, and 100 AMPERE
NPN SILICON POWER DARLINGTON TRANSISTOR
250, 450 and 850 VOLTS
250 WATTS

Designer's Data for "Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst-case" design.



STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. COLLECTOR

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
⌖ Ø 0.25 (0.010) Ⓜ T A Ⓜ B Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
4. CONTROLLING DIMENSION: INCH EXCEPT FOR METRICALLY THREADED INSERTS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.11	40.13	1.540	1.580
B	33.93	34.95	1.336	1.376
C	–	20.32	–	0.800
D	0.68	0.83	0.027	0.033
E	8.30	8.81	0.327	0.347
F	–	4.44	–	0.175
G	29.67 BSC		1.168 BSC	
H	5.08 BSC		0.200 BSC	
J	0.93	1.09	0.037	0.043
K	—	25.40	–	1.000
L	2.92	3.30	0.115	0.130
N	17.14	17.39	0.675	0.685
Q	3.73	3.88	0.147	0.153
R	10.41	10.79	0.410	0.425
S	5.84	6.35	0.230	0.250
U	M5 .8 (METRIC THRD)			
V	1.27	1.52	0.050	0.060
W	4.69	4.85	0.185	0.191
X	30.15 BSC		1.187 BSC	

CASE 353-01

MAXIMUM RATINGS

Mechanical Ratings		
Rating	**Value**	**Unit**
Mounting Torque (To heat sink with 6-32 Screw) (Note 1)	8.0	in.-lb
Lead Torque (Lead to bus with 5 mm Screw) (Note 2)	20	in.-lb
Per Unit Weight	41	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.5	°C/W

Mica Insulators available as separate items.
0.003" thick. Motorola Part Number 14CSB12387B003.

Notes:
1. A Belleville washer of 0.281" O.D., 0.138" I.D., 0.013" thick and 43 pounds flat is recommended.
2. The maximum penetration of the screw should be limited to 0.50".
3. To adapt the collector and emitter terminals to quick connect terminals, AMP 250 Series Faston tab P/N 61499-1 is suggested.
4. The mounting holes of this package are compatible with TO-204 (formerly TO-3) mounting holes.

3

MAXIMUM RATINGS (Continued) (T_C = 25°C unless otherwise noted.)

Rating	Symbol	MJ10041	MJ10044	MJ10047	Unit
Collector-Emitter Voltage (I_B = 0)	V_{CEO}	850	450	250	Vdc
Collector-Emitter Voltage (R_{BE} = 10 Ohms)	V_{CER}	900	500	300	Vdc
Collector-Base Voltage	V_{CB}	900	500	300	Vdc
Emitter-Base Voltage	V_{EB}		8.0		Vdc
Collector Current — Operating (T_C = 115°C) (T_C = 85°C) (T_C = 85°C)	$I_{C(op)}$	25 — —	— 50 —	— — 100*	A
Collector Current — Continuous — Peak Repetitive — Peak Nonrepetitive	I_C	37.5 75 125	75 150 250	100 300 500	A
Base Current — Continuous — Peak Nonrepetitive	I_B		25 50		A
Total Device Dissipation Derate above T_C = 25°C For 1-minute overload	P_D		250 2.0 333		Watts W/°C Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}		−55 to +150 −55 to 200		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 125 mAdc)	MJ10041 MJ10044 MJ10047	$V_{CEO(sus)}$	850 450 250	— — —	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	— —	2.0 10	mA
Collector Cutoff Current (V_{CE} = Rated V_{CER}, R_{BE} = 10 Ω, T_C = 100°C)		I_{CER}	—	10	mA
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	MJ10041 MJ10044 MJ10047	I_{EBO}	— —	500 2.5	mA
SAFE OPERATING AREA					
Second Breakdown Collector Current with Base Forward-Biased		FBSOA	See Figures 32, 34 & 36		
Clamped Inductive SOA with Base Reverse-Biased		RBSOA	See Figures 33, 35 & 37		
Overload Safe Operating Area		OLSOA	See Figures 38, 39, 40, 41, 42 & 43		
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	—	2000	pF

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤ 2.0%.
*This rating is with a 50% duty cycle, and is limited by power dissipation. Higher operating currents are allowable at lower duty cycles.

3

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
MJ10041				
DC Current Gain (I_C = 25 Adc, V_{CE} = 5.0 Vdc) (I_C = 25 Adc, V_{CE} = 10 Vdc)	h_{FE}	 25 40	 — —	
Collector-Emitter Saturation Voltage (I_C = 25 Adc, I_B = 2.0 Adc) (I_C = 37.5 Adc, I_B = 7.5 Adc) (I_C = 25 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 2.0 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 25 Adc, I_B = 2.0 Adc) (I_C = 25 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 3.0 3.0	Vdc
MJ10044				
DC Current Gain (I_C = 50 Adc, V_{CE} = 5.0 Vdc) (I_C = 50 Adc, V_{CE} = 10 Vdc)	h_{FE}	 50 60	 — —	
Collector-Emitter Saturation Voltage (I_C = 50 Adc, I_B = 1.67 Adc) (I_C = 75 Adc, I_B = 6.0 Adc) (I_C = 50 Adc, I_B = 1.67 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 2.0 3.3 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 50 Adc, I_B = 1.67 Adc) (I_C = 50 Adc, I_B = 1.67 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 3.0 3.0	Vdc
MJ10047				
DC Current Gain (I_C = 100 Adc, V_{CE} = 5.0 Vdc) (I_C = 100 Adc, V_{CE} = 10 Vdc)	h_{FE}	 75 90	 — —	
Collector-Emitter Saturation Voltage (I_C = 100 Adc, I_B = 2.75 Adc) (I_C = 100 Adc, I_B = 2.75 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — —	 2.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 100 Adc, I_B = 2.75 Adc) (I_C = 100 Adc, I_B = 2.75 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 3.5 3.5	Vdc

(1) Pulse Test: Pulse width of 300 μs, duty cycle ≤ 2.0%.

3

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted.)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
MJ10041							
Resistive Load							
Delay Time	(V_{CC} = 300 Vdc, I_C = 25 A, I_{B1} = 2.5 A, $V_{BE(OFF)}$ = 5.0 V, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.03	0.25	μs
Rise Time			t_r	—	1.2	5.0	
Storage Time			t_s	—	3.3	10	
Fall Time			t_f	—	1.5	5.0	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 25 A, V_{CEM} = 300 V, $V_{BE(OFF)}$ = 5.0 V, I_{B1} = 2.5 A)	T_J = 100°C	t_{sv}	—	5.0	15	μs
Crossover Time			t_c	—	3.0	10	
Storage Time		T_J = 25°C	t_{sv}	—	3.5	10	
Crossover Time			t_c	—	1.5	5.0	

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted.)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
MJ10044							
Resistive Load							
Delay Time	(V_{CC} = 250 Vdc, I_C = 50 A, I_{B1} = 1.67 A, $V_{BE(OFF)}$ = 5.0 V, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.03	0.25	μs
Rise Time			t_r	—	0.9	3.0	
Storage Time			t_s	—	1.5	3.8	
Fall Time			t_f	—	0.4	1.3	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 50 A, V_{CEM} = 250 V, $V_{BE(OFF)}$ = 5.0 V, I_{B1} = 1.67 A)	T_J = 100°C	t_{sv}	—	2.5	7.5	μs
Crossover Time			t_c	—	0.8	3.0	
Storage Time		T_J = 25°C	t_{sv}	—	1.5	3.8	
Crossover Time			t_c	—	0.5	1.5	
MJ10047							
Resistive Load							
Delay Time	(V_{CC} = 150 Vdc, I_C = 100 A, I_{B1} = 2.75 A, $V_{BE(OFF)}$ = 5.0 V, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.035	0.25	μs
Rise Time			t_r	—	1.2	4.0	
Storage Time			t_s	—	1.4	4.0	
Fall Time			t_f	—	0.25	1.0	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 100 A, V_{CEM} = 150 V, $V_{BE(OFF)}$ = 5.0 V, I_{B1} = 2.75 A)	T_J = 100°C	t_{sv}	—	2.8	8.0	μs
Crossover Time			t_c	—	1.4	4.0	
Storage Time		T_J = 25°C	t_{sv}	—	2.2	6.5	
Crossover Time			t_c	—	1.0	3.0	
C-E DIODE CHARACTERISTICS							
Power Dissipation (I_B = 0)			P_D	—	—	125	W
Single Cycle Surge Current (60 Hz)			I_{FSM}	—	—	250	Apk
Forward Voltage (1)			V_F				Vdc
(I_F = 25 Adc)	MJ10041			—	2.7	5.0	
(I_F = 50 Adc)	MJ10044			—	1.7	5.0	
(I_F = 100 Adc)	MJ10047			—	2.5	5.0	
Reverse Recovery Time			t_{rr}				μs
(I_F = 25 Adc, di/dt = 25 A/μs)	MJ10041			—	0.2	1.0	
(I_F = 50 Adc, di/dt = 50 A/μs)	MJ10044			—	0.4	1.0	
(I_F = 100 Adc, di/dt = 100 A/μs)	MJ10047			—	0.4	1.0	
Reverse Recovery Current			$I_{RM(rec)}$				A
(I_F = 25 A, di/dt = 25 A/μs)	MJ10041			—	3.5	12.5	
(I_F = 50 A, di/dt = 50 A/μs)	MJ10044			—	10	25	
(I_F = 100 A, di/dt = 100 A/μs)	MJ10047			—	25	50	
Forward Turn-On Time (Compliance Voltage = 250 V)			t_{on}				μs
(I_F = 25 Adc)	MJ10041			—	0.1	1.0	
(I_F = 50 Adc)	MJ10044			—	0.1	0.5	
(I_F = 100 Adc)	MJ10047			—	0.4	1.0	

(1) Pulse Test: Pulse width of 300 μs, duty cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

MJ10041

FIGURE 1 — DC CURRENT GAIN

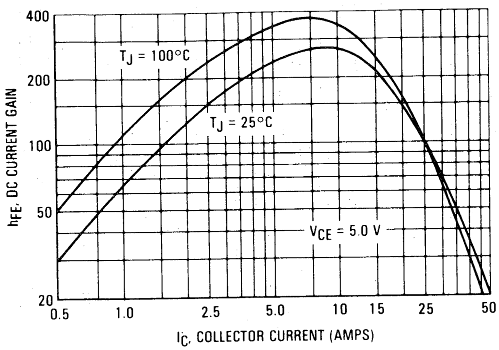
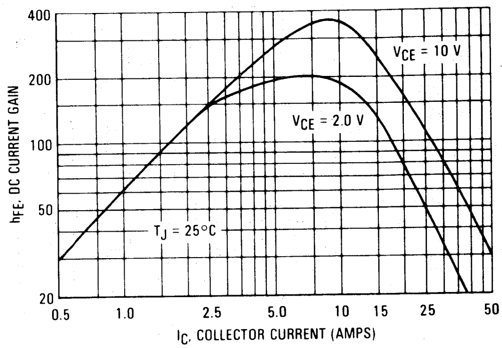


FIGURE 2 — DC CURRENT GAIN



MJ10044

FIGURE 3 — DC CURRENT GAIN

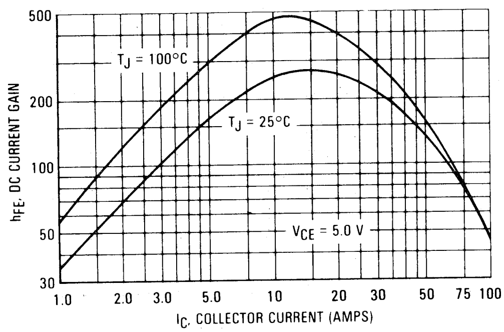
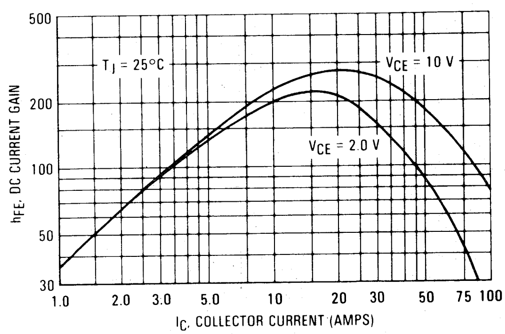


FIGURE 4 — DC CURRENT GAIN



MJ10047

FIGURE 5 — DC CURRENT GAIN

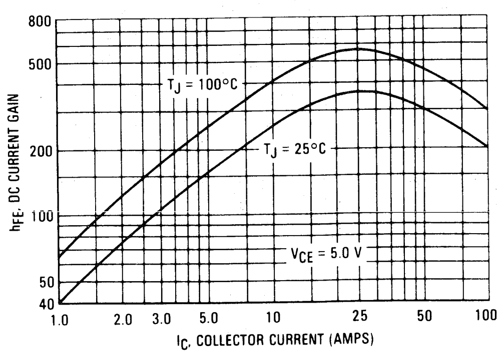
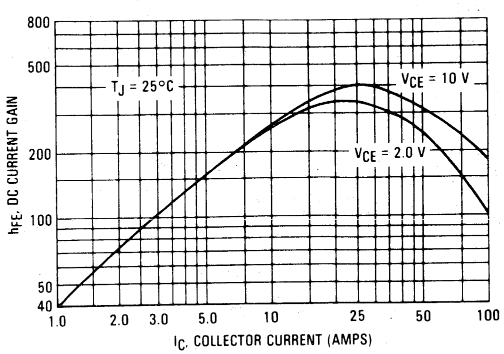


FIGURE 6 — DC CURRENT GAIN



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TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10041

FIGURE 7 — DC CURRENT GAIN

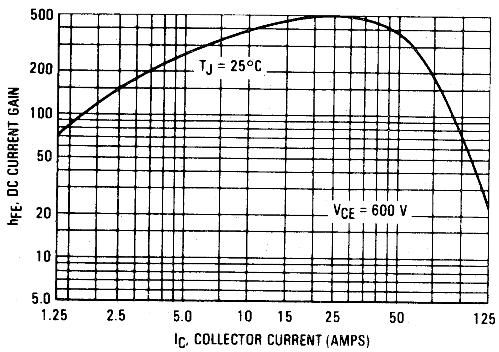
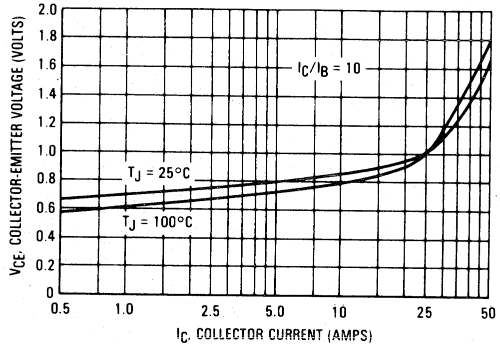


FIGURE 8 — COLLECTOR SATURATION VOLTAGE



MJ10044

FIGURE 9 — DC CURRENT GAIN

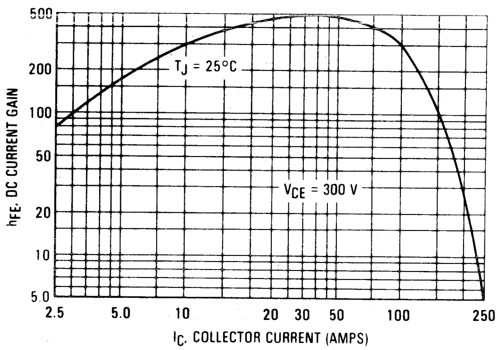
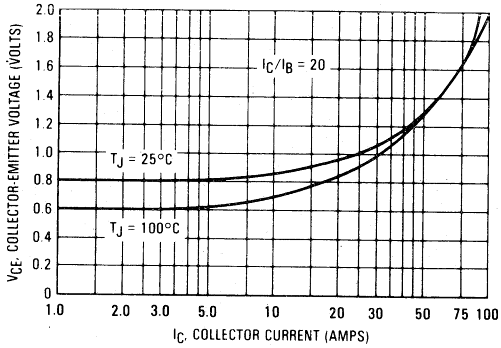


FIGURE 10 — COLLECTOR SATURATION REGION



MJ10047

FIGURE 11 — DC CURRENT GAIN

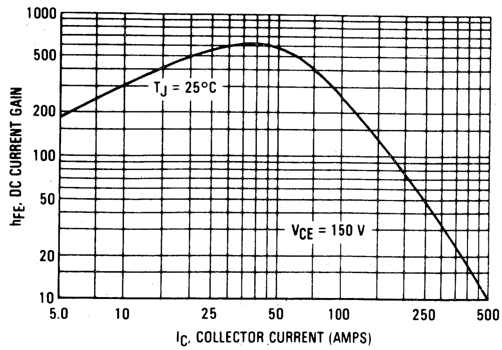
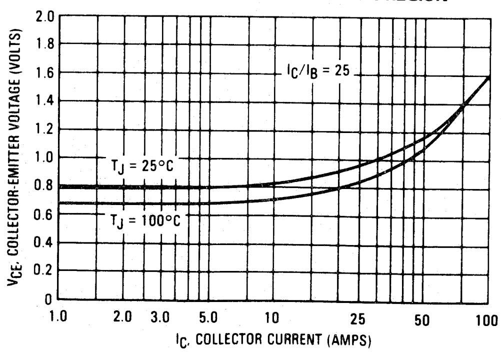


FIGURE 12 — COLLECTOR SATURATION REGION



3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10041

FIGURE 13 — BASE-EMITTER SATURATION VOLTAGE

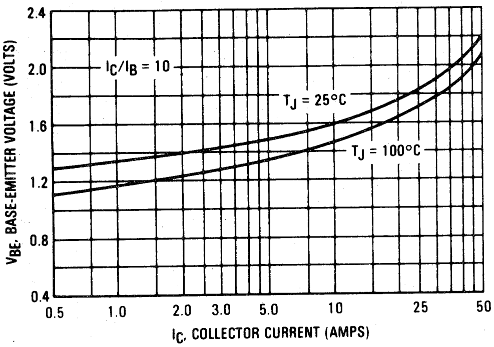
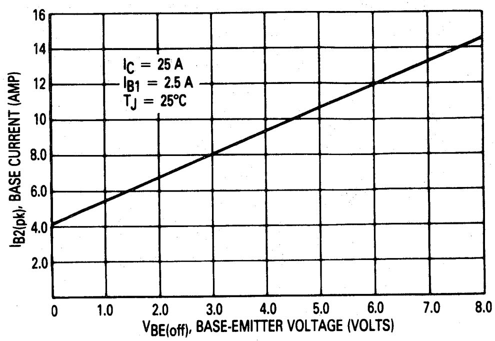


FIGURE 14 — PEAK REVERSE BASE CURRENT



MJ10044

FIGURE 15 — BASE-EMITTER SATURATION VOLTAGE

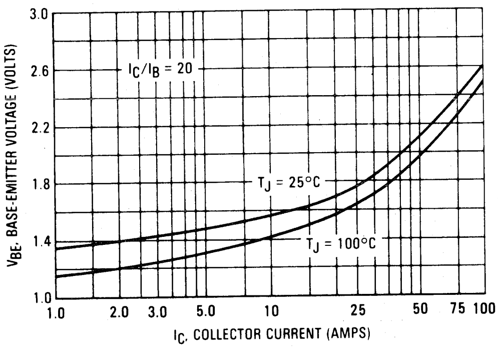
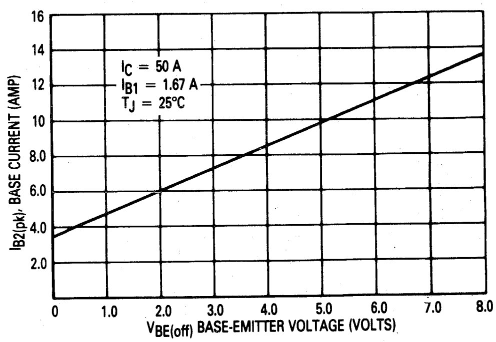


FIGURE 16 — PEAK REVERSE BASE CURRENT



MJ10047

FIGURE 17 — BASE-EMITTER SATURATION VOLTAGE

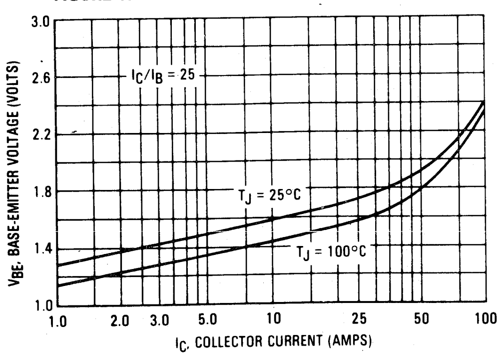
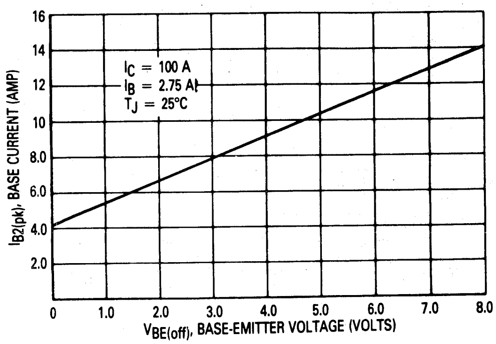


FIGURE 18 — PEAK REVERSE BASE CURRENT



3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10041

FIGURE 19 — TYPICAL INDUCTIVE SWITCHING TIMES

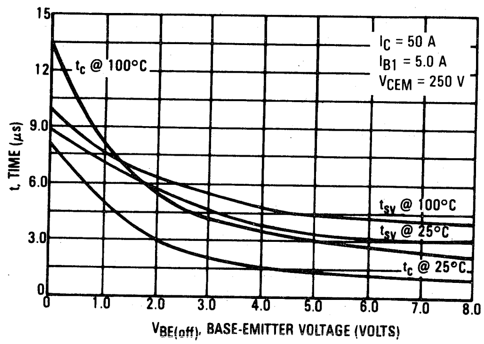
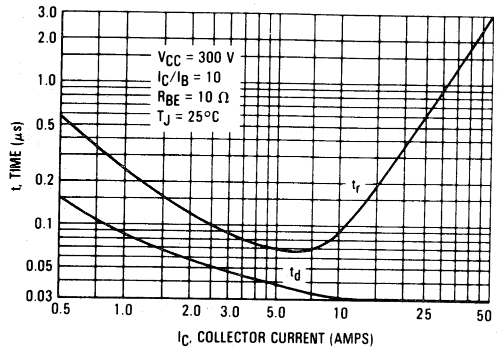


FIGURE 20 — TYPICAL TURN-ON SWITCHING TIMES



MJ10044

FIGURE 21 — TYPICAL INDUCTIVE SWITCHING TIMES

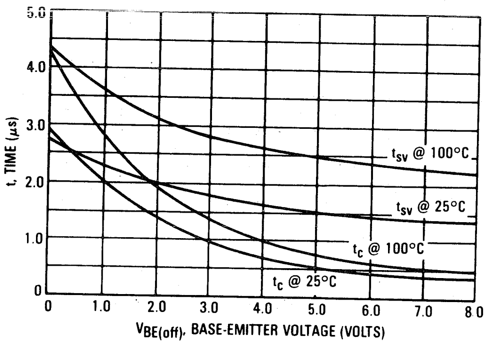
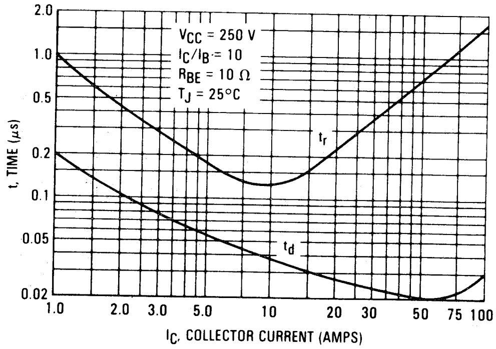


FIGURE 22 — TYPICAL TURN-ON SWITCHING TIMES



MJ10047

FIGURE 23 — TYPICAL INDUCTIVE SWITCHING TIMES

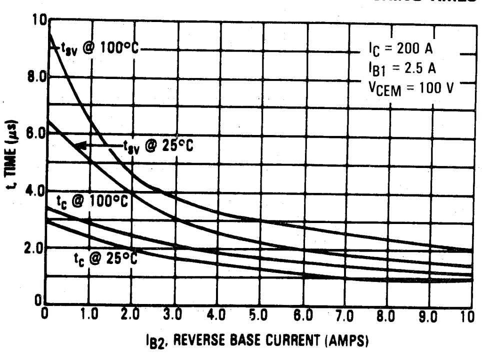
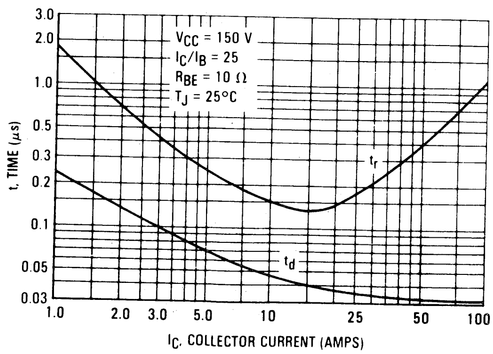


FIGURE 24 — TYPICAL TURN-ON SWITCHING TIMES



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TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 25 — TYPICAL TURN-OFF SWITCHING TIMES MJ10041

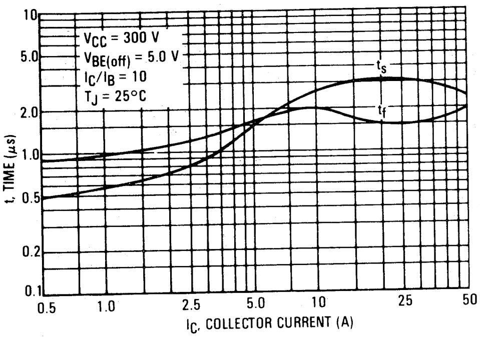

FIGURE 26 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE

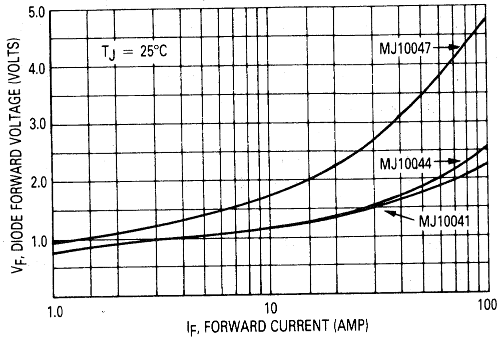

FIGURE 27 — TYPICAL TURN-OFF SWITCHING TIMES MJ10044

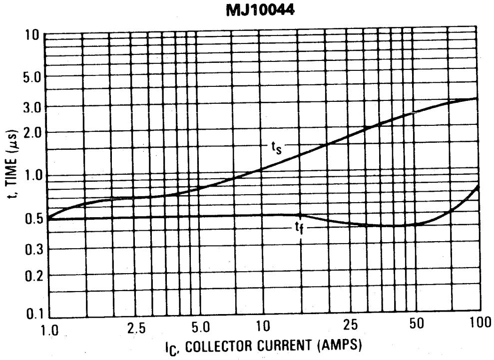

FIGURE 28 — POWER DERATING

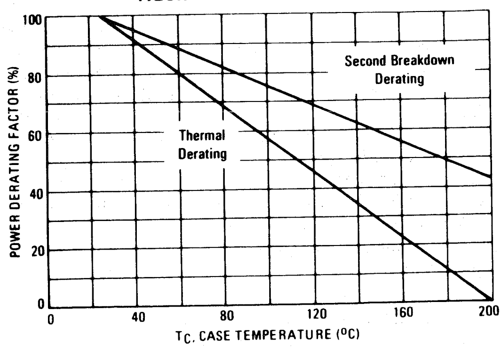

FIGURE 29 — TYPICAL TURN-OFF SWITCHING TIMES MJ10047

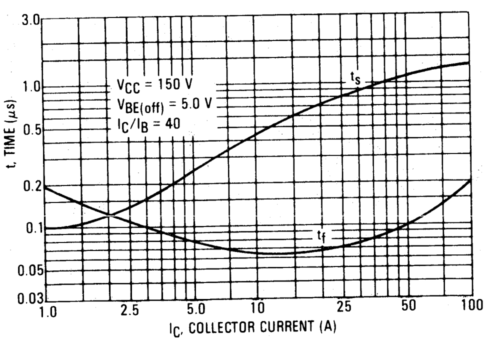

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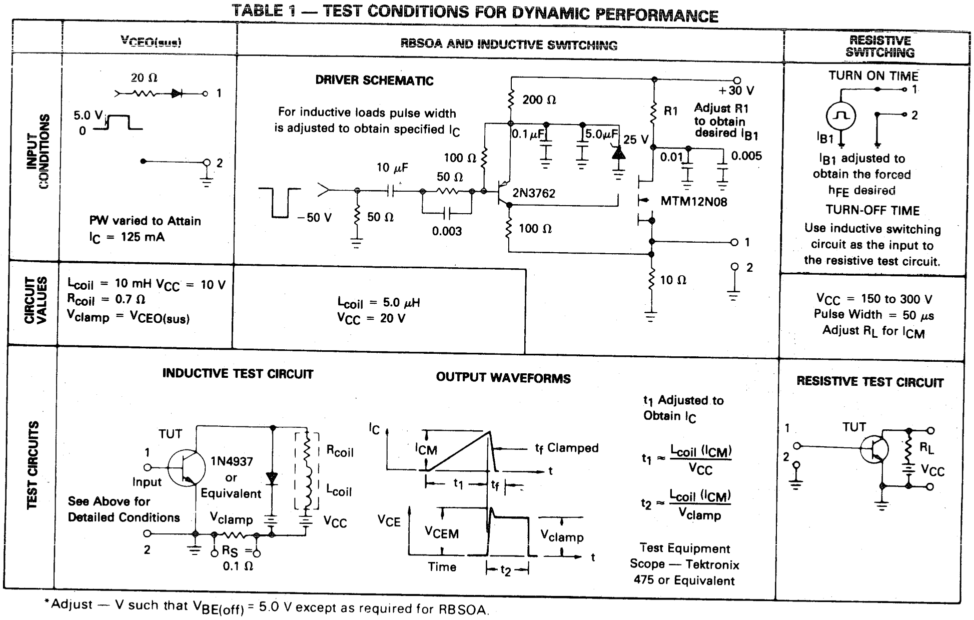
TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust — V such that $V_{BE(off)}$ = 5.0 V except as required for RBSOA.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{rv} = Voltage Rise Time, 10–90% V_{CEM}

t_{fi} = Current Fall Time, 90–10% I_{CM}

t_{ti} = Current Tail, 10–2% I_{CM}

t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 30 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = \tfrac{1}{2} V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 30 — INDUCTIVE SWITCHING MEASUREMENTS

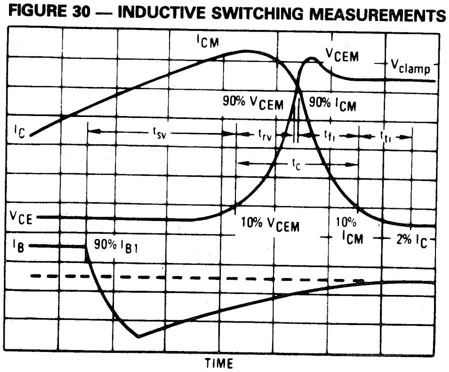
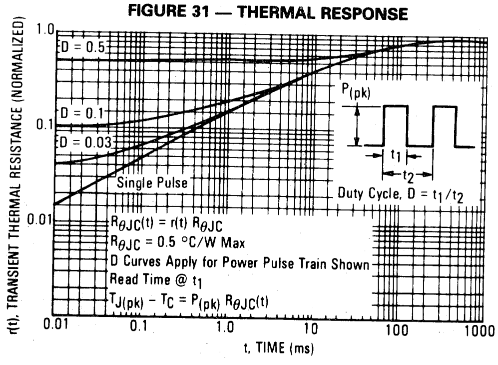


FIGURE 31 — THERMAL RESPONSE



3

SAFE OPERATING AREA INFORMATION

MJ10041

FIGURE 32 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

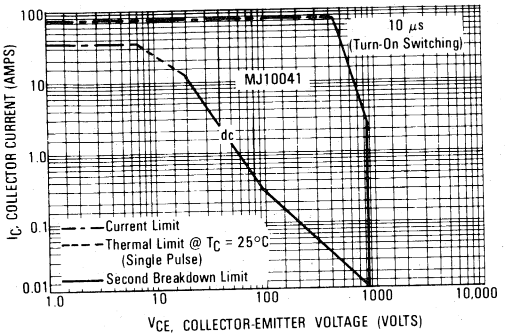
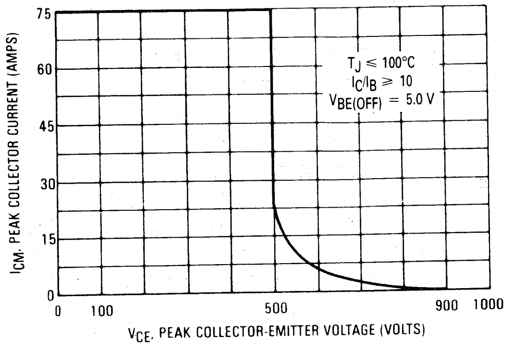


FIGURE 33 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



MJ10044

FIGURE 34 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

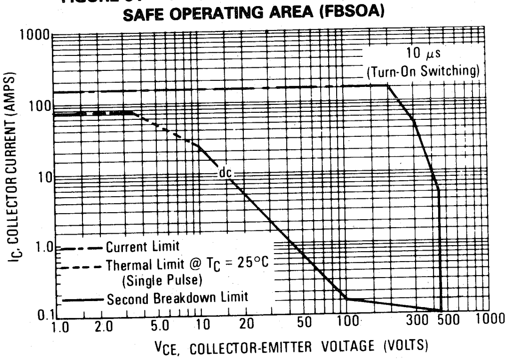
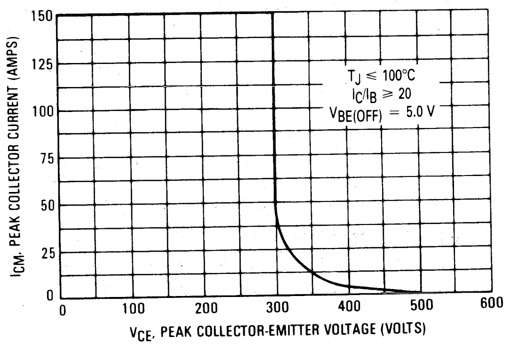


FIGURE 35 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



MJ10047

FIGURE 36 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

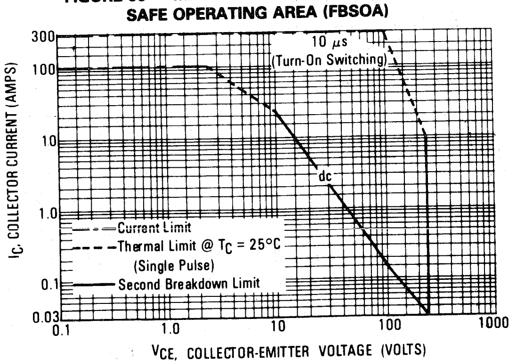
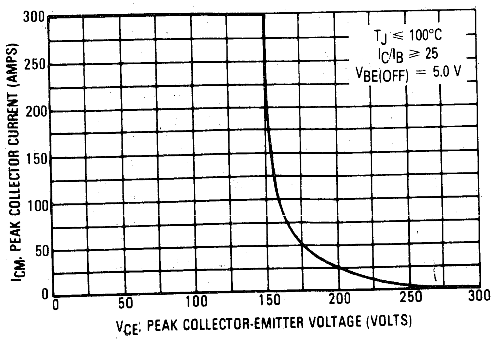


FIGURE 37 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



3

OVERLOAD CHARACTERISTICS

MJ10041

FIGURE 38 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

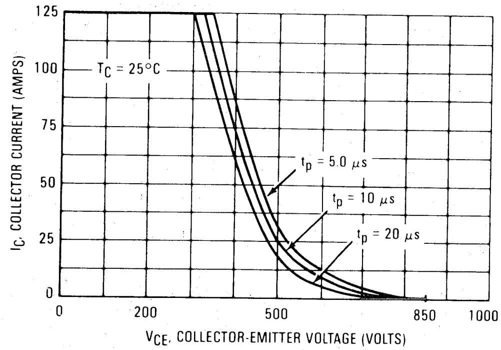
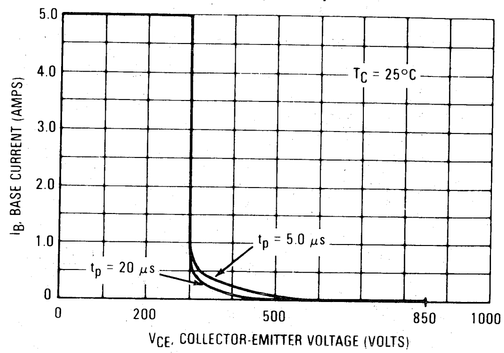


FIGURE 39 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



MJ10044

FIGURE 40 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

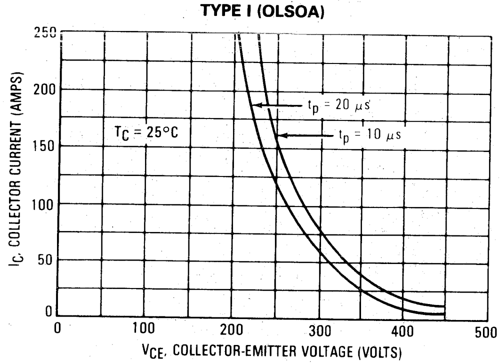
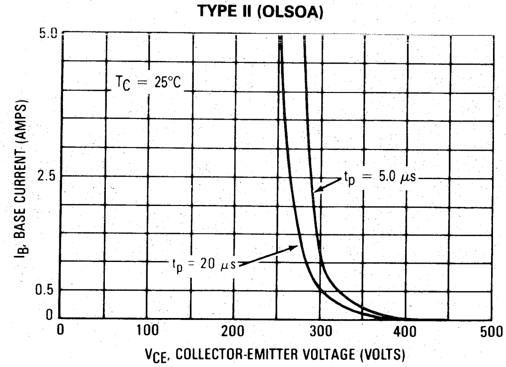


FIGURE 41 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



MJ10047

FIGURE 42 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

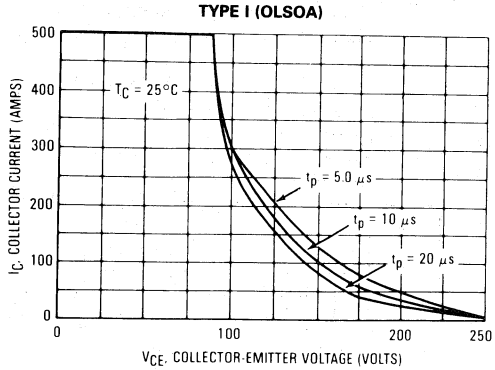
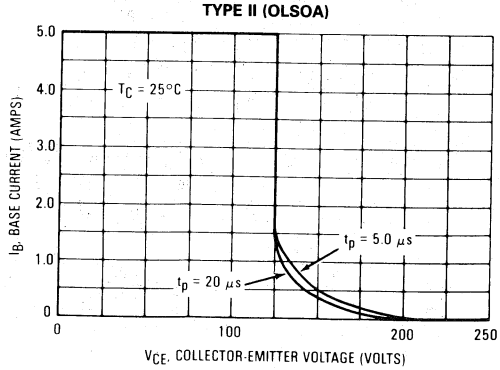


FIGURE 43 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transitor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 32, 34, and 36 are based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on these figures may be found at any case temperature by using the appropriate curve on Figure 28.

$T_{J(pk)}$ may be calculated from the data in Figure 31. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figures 33, 35 and 37 give the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in these figures adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figures 38, 40 and 42 depict the Type I OLSOA rating for these devices. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, these figures define the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 44) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figures 39, 41 and 43 are measured in the circuit shown in Figure 45, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

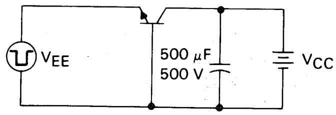
There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NON-REPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for these devices is 100 occurrences. Another factor is the form of turn-off bias. For these devices, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5.0$ V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

3

OVERLOAD SAFE OPERATING TEST CIRCUITS

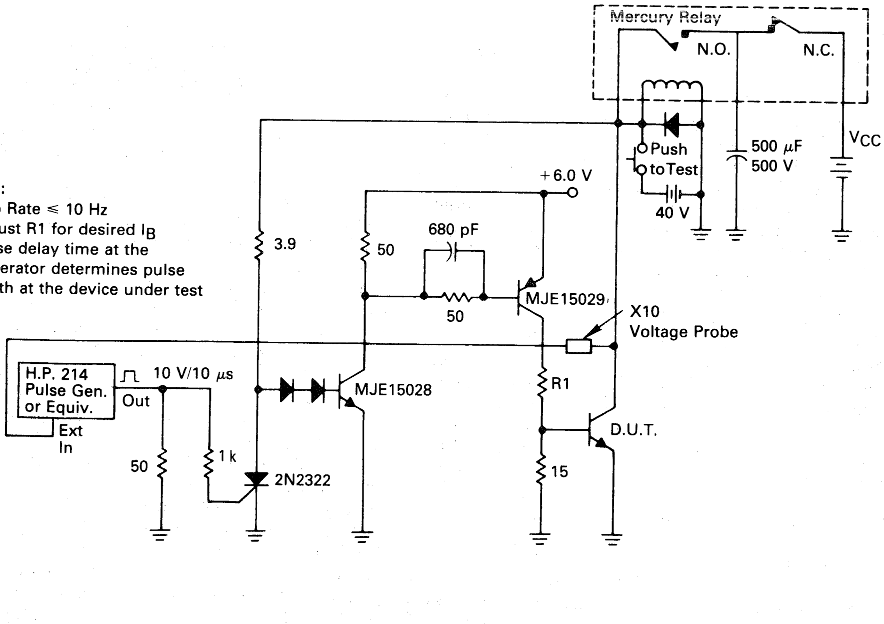
FIGURE 44 — OVERLOAD SOA TEST CIRCUIT
TYPE I (OLSOA)



Notes:
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

FIGURE 45 — OVERLOAD SOA TEST CIRCUIT
TYPE II (OLSOA)

Notes:
- Rep Rate ≤ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test



3

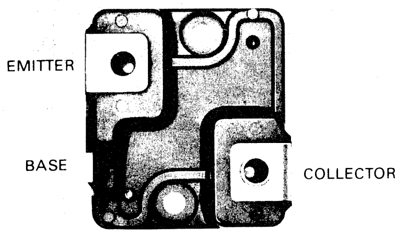
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

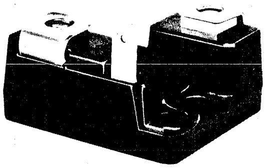
MJ10042
MJ10045
MJ10048

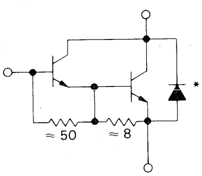
Designer's Data Sheet

25 KVA ENERGY MANAGEMENT SERIES SWITCHMODE DARLINGTON TRANSISTORS
25, 50 and 100 Ampere Operating Current

These Darlington transistors are designed for industrial service under practical operating environments found in switching high power inductive loads off 120, 230 and 460 Volt lines.





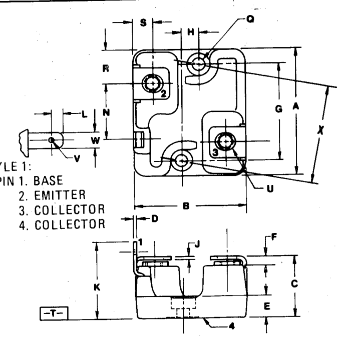


*Emitter-Collector Diode is a high power diode.

25, 50, and 100 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
250, 450 and 850 VOLTS
250 WATTS

Designer's Data for "Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.



STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. COLLECTOR

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   | ⌖ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ | B Ⓜ |
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
4. CONTROLLING DIMENSION: INCH EXCEPT FOR METRICALLY THREADED INSERTS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	39.11	40.13	1.540	1.580
B	33.93	34.95	1.336	1.376
C	–	20.32	–	0.800
D	0.68	0.83	0.027	0.033
E	8.30	8.81	0.327	0.347
F	–	4.44	–	0.175
G	29.67 BSC		1.168 BSC	
H	5.08 BSC		0.200 BSC	
J	0.93	1.09	0.037	0.043
K	—	25.40	–	1.000
L	2.92	3.30	0.115	0.130
N	17.14	17.39	0.675	0.685
Q	3.73	3.88	0.147	0.153
R	10.41	10.79	0.410	0.425
S	5.84	6.35	0.230	0.250
U	M5 .8 (METRIC THRD)			
V	1.27	1.52	0.050	0.060
W	4.69	4.85	0.185	0.191
X	30.15 BSC		1.187 BSC	

CASE 353-01

MAXIMUM RATINGS

Mechanical Ratings

Rating	Value	Unit
Mounting Torque (To heat sink with 6-32 Screw) (Note 1)	8.0	in.-lb
Lead Torque (Lead to bus with 5 mm Screw) (Note 2)	20	in.-lb
Per Unit Weight	41	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.5	°C/W

Mica Insulators available as separate items.
0.003" thick. Motorola Part Number 14CSB12387B003.

Notes:
1. A Belleville washer of 0.281" O.D., 0.138" I.D., 0.013" thick and 43 pounds flat is recommended.
2. The maximum penetration of the screw should be limited to 0.50".
3. To adapt the collector and emitter terminals to quick connect terminals, AMP 250 Series Faston tab P/N 61499-1 is suggested.
4. The mounting holes of this package are compatible with TO-204 (formerly TO-3) mounting holes.

3

MAXIMUM RATINGS (Continued) (T_C = 25°C unless otherwise noted.)

Rating	Symbol	MJ10042	MJ10045	MJ10048	Unit
Collector-Emitter Voltage (I_B = 0)	V_{CEO}	850	450	250	Vdc
Collector-Emitter Voltage (R_{BE} = 10 Ohms)	V_{CER}	900	500	300	Vdc
Collector-Base Voltage	V_{CB}	900	500	300	Vdc
Emitter-Base Voltage	V_{EB}	8.0			Vdc
Collector Current — Operating (T_C = 115°C) (T_C = 85°C) (T_C = 85°C)	$I_{C(op)}$	25 — —	— 50 —	— — 100*	A
Collector Current — Continuous — Peak Repetitive — Peak Nonrepetitive	I_C	37.5 75 125	75 150 250	100 300 500	A
Base Current — Continuous — Peak Nonrepetitive	I_B	25 50			A
Total Device Dissipation Derate above T_C = 25°C For 1-minute overload	P_D	250 2.0 333			Watts W/°C Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}	-55 to +150 -55 to 200			°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 125 mAdc) MJ10042 MJ10045 MJ10048	$V_{CEO(sus)}$	850 450 250	— — —	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	— —	2.0 10	mA
Collector Cutoff Current (V_{CE} = Rated V_{CER}, R_{BE} = 10 Ω, T_C = 100°C)	I_{CER}	—	10	mA
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	350	mA
SAFE OPERATING AREA				
Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figures 32, 34 & 36		
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figures 33, 35 & 37		
Overload Safe Operating Area	OLSOA	See Figures 38, 39, 40, 41, 42 & 43		
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	2000	pF

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤2.0%.
* This rating is with a 50% duty cycle, and is limited by power dissipation. Higher operating currents are allowable at lower duty cycles.

3

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
MJ10042				
DC Current Gain (I_C = 25 Adc, V_{CE} = 5.0 Vdc) (I_C = 25 Adc, V_{CE} = 10 Vdc)	h_{FE}	 35 40	 — —	
Collector-Emitter Saturation Voltage (I_C = 25 Adc, I_B = 2.0 Adc) (I_C = 37.5 Adc, I_B = 7.5 Adc) (I_C = 25 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 2.0 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 25 Adc, I_B = 2.0 Adc) (I_C = 25 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 3.0 3.0	Vdc
MJ10045				
DC Current Gain (I_C = 50 Adc, V_{CE} = 5.0 Vdc) (I_C = 50 Adc, V_{CE} = 10 Vdc)	h_{FE}	 50 60	 — —	
Collector-Emitter Saturation Voltage (I_C = 50 Adc, I_B = 1.67 Adc) (I_C = 75 Adc, I_B = 6.0 Adc) (I_C = 50 Adc, I_B = 1.67 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 2.0 3.3 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 50 Adc, I_B = 1.67 Adc) (I_C = 50 Adc, I_B = 1.67 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 3.0 3.0	Vdc
MJ10048				
DC Current Gain (I_C = 100 Adc, V_{CE} = 5.0 Vdc) (I_C = 100 Adc, V_{CE} = 10 Vdc)	h_{FE}	 75 90	 — —	
Collector-Emitter Saturation Voltage (I_C = 100 Adc, I_B = 2.75 Adc) (I_C = 100 Adc, I_B = 2.75 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — —	 2.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 100 Adc, I_B = 2.75 Adc) (I_C = 100 Adc, I_B = 2.75 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 3.0 3.0	Vdc

(1) Pulse Test: Pulse width of 300 μs, duty cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
MJ10042							
Resistive Load							
Delay Time	(V_{CC} = 300 Vdc, I_C = 25 A, I_{B1} = 2.0 A, R_{BE} = 10 Ω, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.03	0.25	μs
Rise Time			t_r	—	1.2	5.0	
Storage Time			t_s	—	35	100	
Fall Time			t_f	—	8.5	35	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 25 A, V_{CEM} = 350 V, R_{BE} = 10 Ω, I_{B1} = 2.0 A)	T_J = 100°C	t_{sv}	—	50	150	μs
Crossover Time			t_c	—	20	60	
Storage Time		T_J = 25°C	t_{sv}	—	35	100	
Crossover Time			t_c	—	10	35	
MJ10045							
Resistive Load							
Delay Time	(V_{CC} = 250 Vdc, I_C = 50 A, I_{B1} = 1.67 A, R_{BE} = 10 Ω, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.03	0.25	μs
Rise Time			t_r	—	0.9	3.0	
Storage Time			t_s	—	10	25	
Fall Time			t_f	—	3.0	10	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 50 A, V_{CEM} = 250 V, R_{BE} = 10 Ω, I_{B1} = 1.67 A)	T_J = 100°C	t_{sv}	—	15	50	μs
Crossover Time			t_c	—	4.0	15	
Storage Time		T_J = 25°C	t_{sv}	—	10	25	
Crossover Time			t_c	—	2.7	10	
MJ10048							
Resistive Load							
Delay Time	(V_{CC} = 150 Vdc, I_C = 100 A, I_{B1} = 2.75 A, R_{BE} = 10 Ω, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.035	0.25	μs
Rise Time			t_r	—	1.2	4.0	
Storage Time			t_s	—	6.3	20	
Fall Time			t_f	—	2.5	8.0	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 100 A, V_{CEM} = 150 V, R_{BE} = 10 Ω, I_{B1} = 2.75 A)	T_J = 100°C	t_{sv}	—	9.0	30	μs
Crossover Time			t_c	—	3.3	12	
Storage Time		T_J = 25°C	t_{sv}	—	6.5	20	
Crossover Time			t_c	—	2.3	8.0	
C-E DIODE CHARACTERISTICS							
Power Dissipation (I_B = 0)			P_D	—	—	125	W
Single Cycle Surge Current (60 Hz)			I_{FSM}	—	—	250	Apk
Forward Voltage (1)			V_F				Vdc
(I_F = 25 Adc)	MJ10042			—	—	1.5	
(I_F = 50 Adc)	MJ10045			—	—	1.5	
(I_F = 100 Adc)	MJ10048			—	—	2.0	
Reverse Recovery Time (d_i/d_t = 25 A/μs)			t_{rr}				μs
(I_F = 25 Adc)	MJ10042			—	4.0	12	
(I_F = 50 Adc)	MJ10045			—	3.3	10	
(I_F = 100 Adc)	MJ10048			—	2.5	8.0	
Forward Turn-On Time (Compliance Voltage = 250 V)			t_{on}				μs
(I_F = 25 Adc)	MJ10042			—	0.3	1.2	
(I_F = 50 Adc)	MJ10045			—	0.3	1.0	
(I_F = 100 Adc)	MJ10048			—	1.0	3.5	

(1) Pulse Test: Pulse width of 300 μs, duty cycle ≤2.0%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

MJ10042

FIGURE 1 — DC CURRENT GAIN

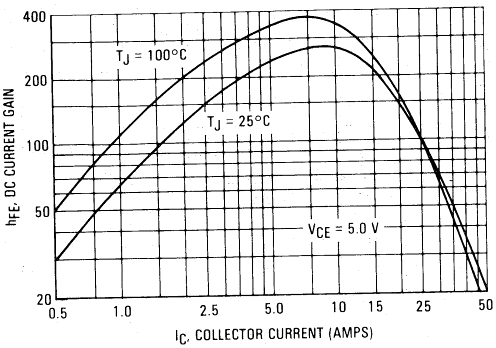
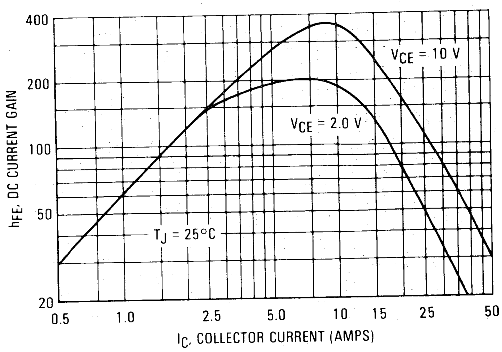


FIGURE 2 — DC CURRENT GAIN



MJ10045

FIGURE 3 — DC CURRENT GAIN

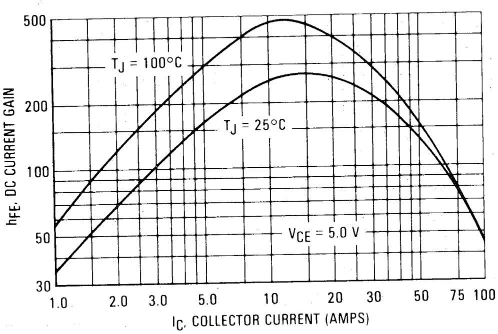
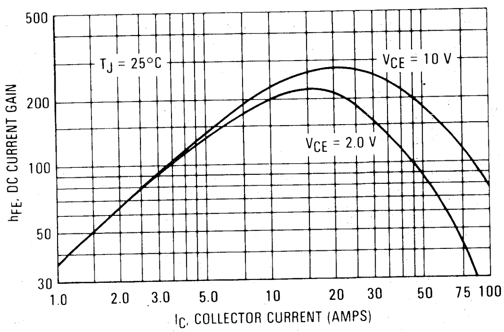


FIGURE 4 — DC CURRENT GAIN



MJ10048

FIGURE 5 — DC CURRENT GAIN

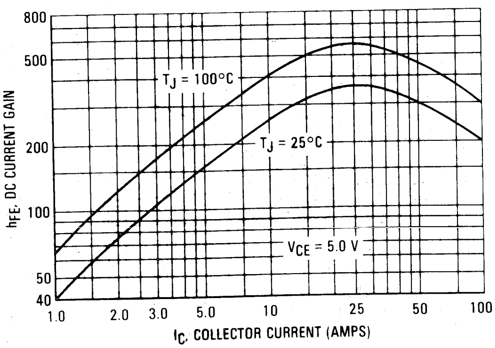
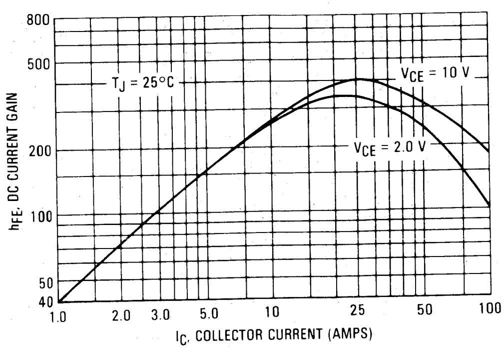


FIGURE 6 — DC CURRENT GAIN



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TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10042

FIGURE 7 — DC CURRENT GAIN

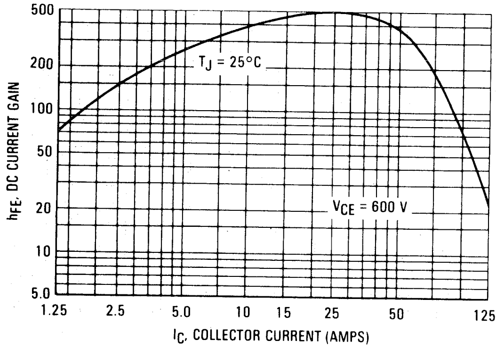
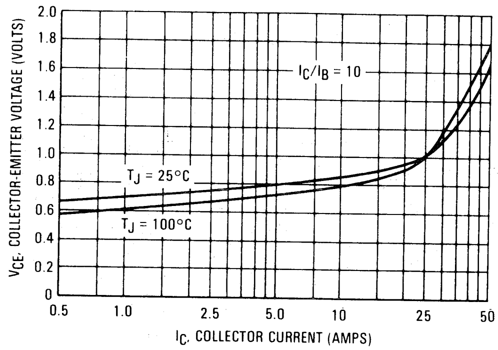


FIGURE 8 — COLLECTOR SATURATION VOLTAGE



MJ10045

FIGURE 9 — DC CURRENT GAIN

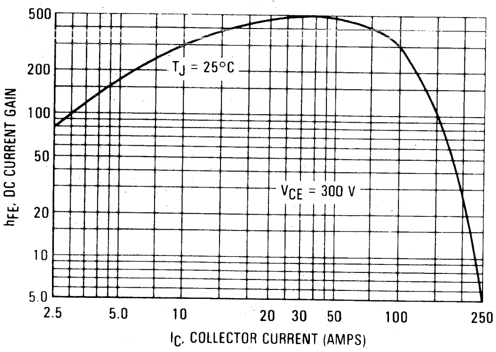
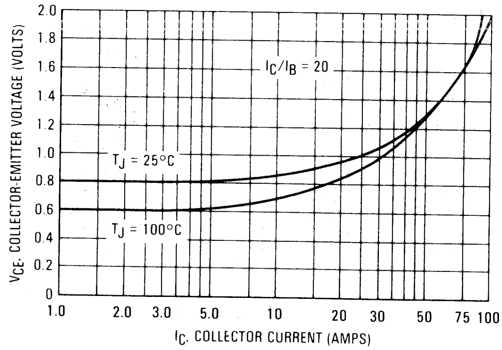


FIGURE 10 — COLLECTOR SATURATION REGION



MJ10048

FIGURE 11 — DC CURRENT GAIN

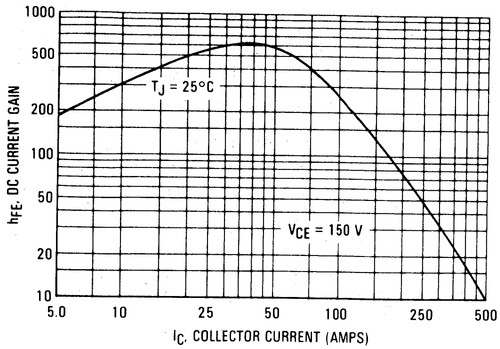
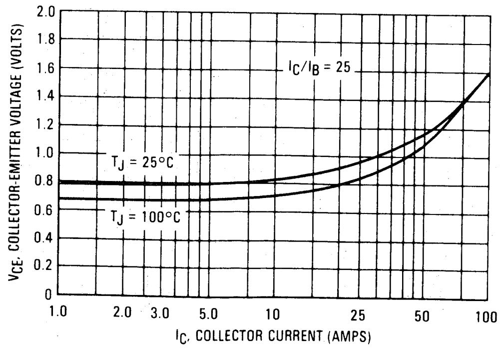


FIGURE 12 — COLLECTOR SATURATION REGION



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10042

FIGURE 13 — BASE-EMITTER SATURATION VOLTAGE

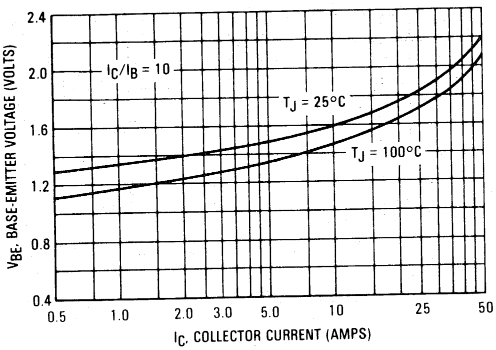
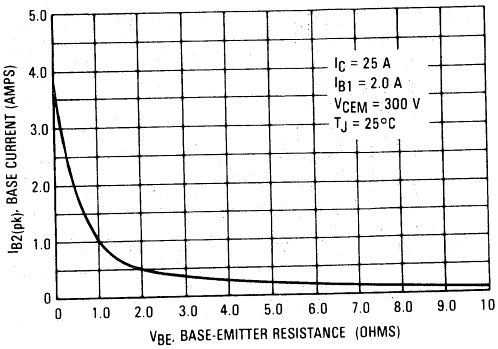


FIGURE 14 — TYPICAL PEAK REVERSE BASE CURRENT



MJ10045

FIGURE 15 — BASE-EMITTER SATURATION VOLTAGE

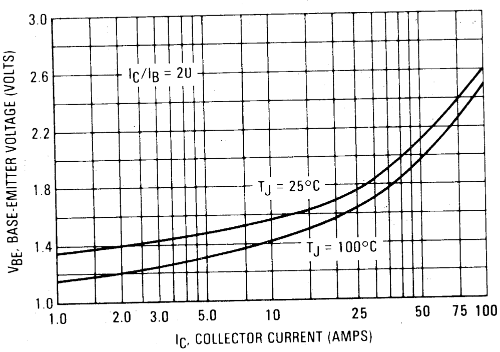
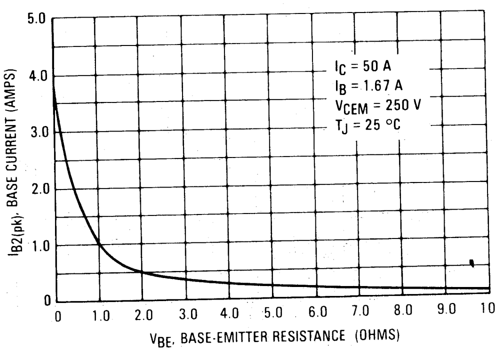


FIGURE 16 — TYPICAL PEAK REVERSE BASE CURRENT



MJ10048

FIGURE 17 — BASE-EMITTER SATURATION VOLTAGE

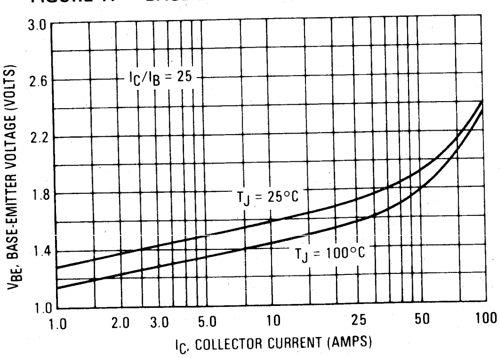
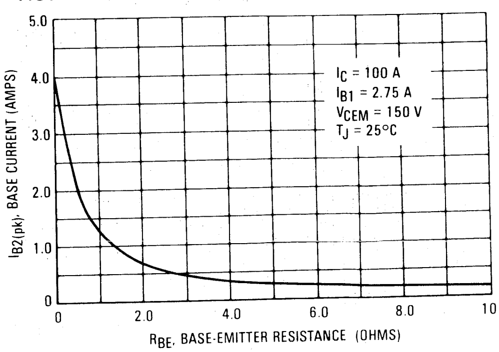


FIGURE 18 — TYPICAL PEAK REVERSE BASE CURRENT



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TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10042

FIGURE 19 — TYPICAL INDUCTIVE SWITCHING TIMES

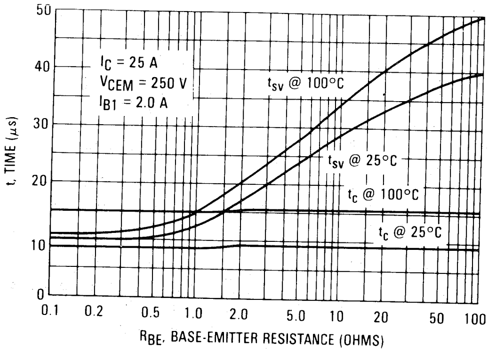
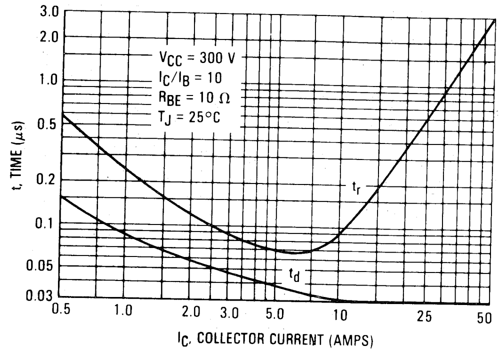


FIGURE 20 — TYPICAL TURN-ON SWITCHING TIMES



MJ10045

FIGURE 21 — TYPICAL INDUCTIVE SWITCHING TIMES

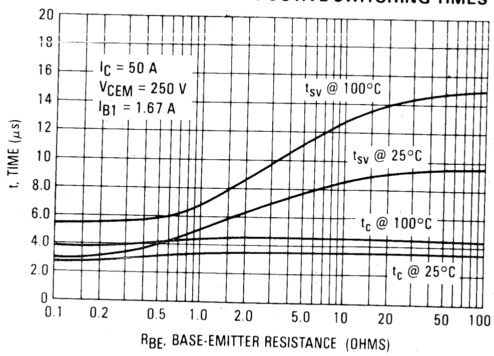
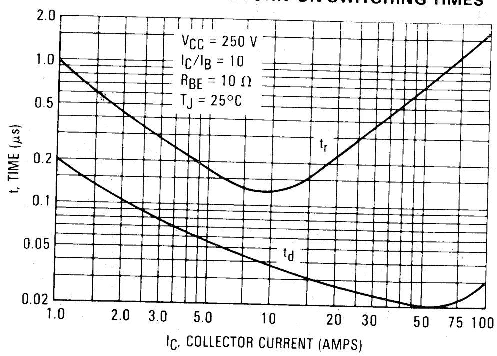


FIGURE 22 — TYPICAL TURN-ON SWITCHING TIMES



MJ10048

FIGURE 23 — TYPICAL INDUCTIVE SWITCHING TIMES

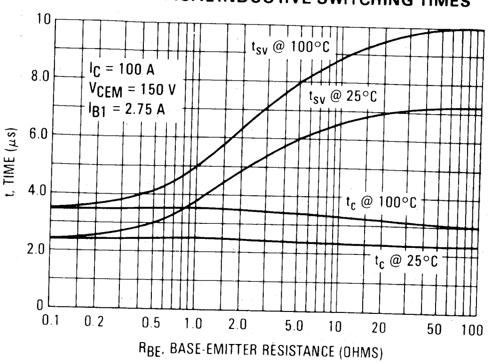
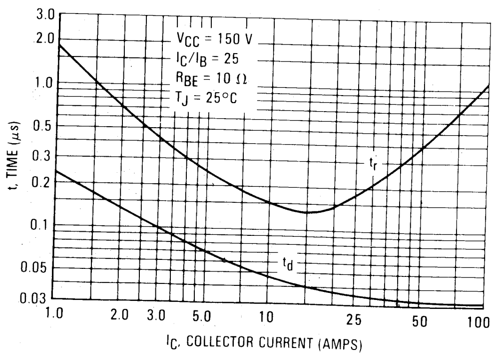


FIGURE 24 — TYPICAL TURN-ON SWITCHING TIMES



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 25 — TYPICAL TURN-OFF SWITCHING TIMES
MJ10042

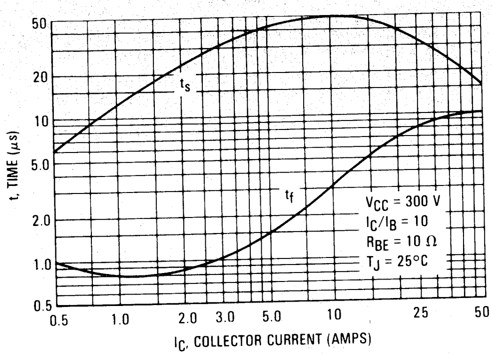


FIGURE 26 — EMITTER-COLLECTOR DIODE
FORWARD VOLTAGE

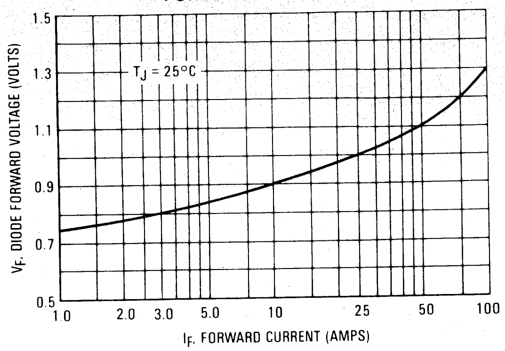


FIGURE 27 — TYPICAL TURN-OFF SWITCHING TIMES
MJ10045

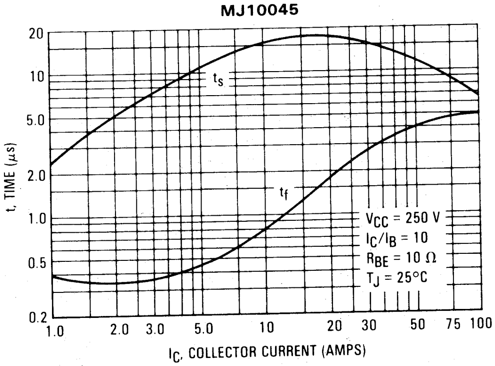


FIGURE 28 — POWER DERATING

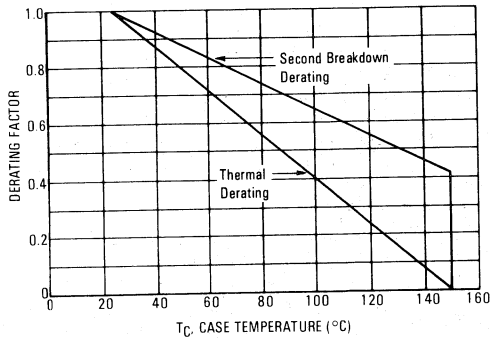
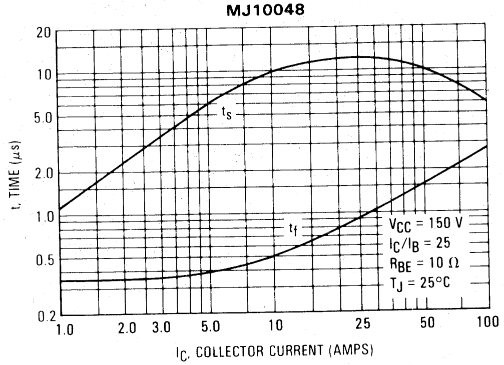
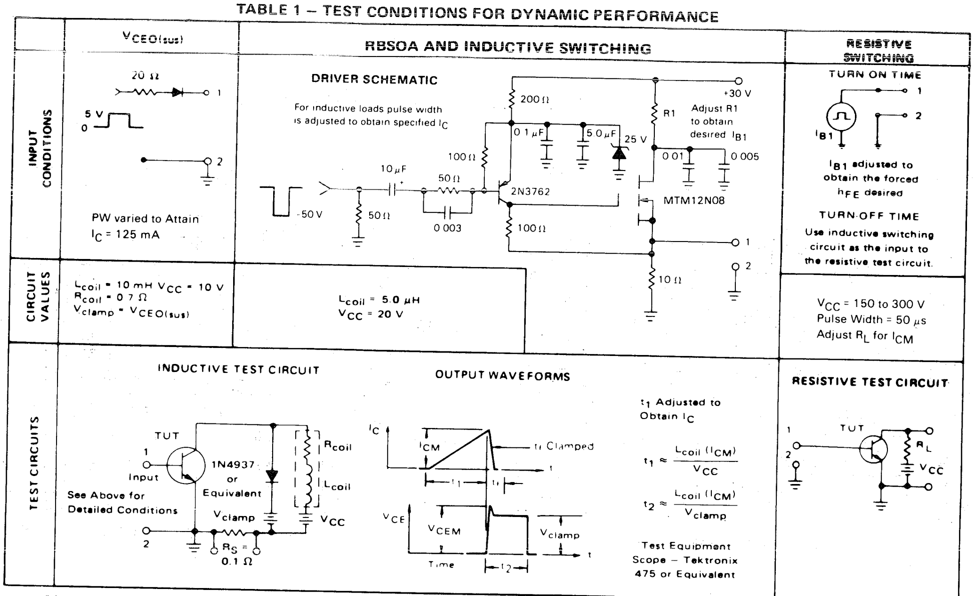


FIGURE 29 — TYPICAL TURN-OFF SWITCHING TIMES
MJ10048



3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust — V such that $V_{BE(off)}$ = 5.0 V except as required for RBSOA.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 30 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 30 — INDUCTIVE SWITCHING MEASUREMENTS

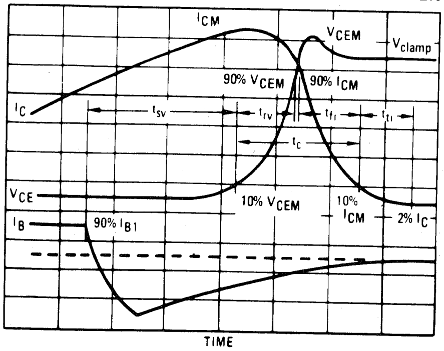
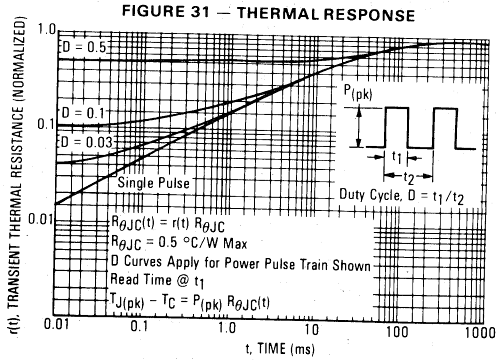


FIGURE 31 — THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

MJ10042

FIGURE 32 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

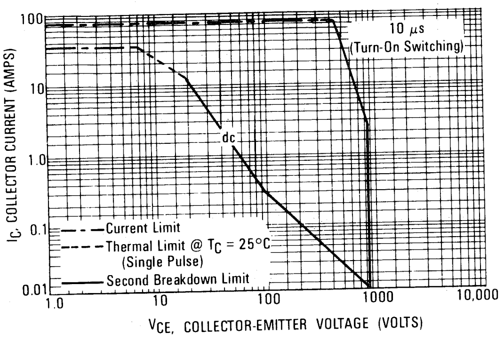
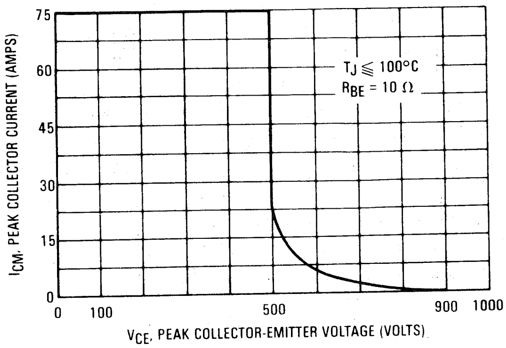


FIGURE 33 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



MJ10045

FIGURE 34 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

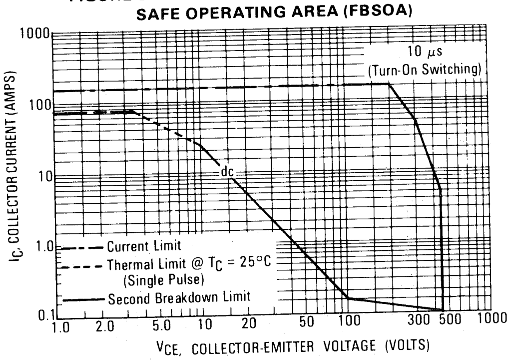
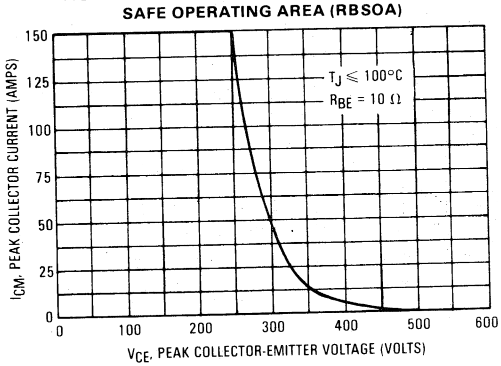


FIGURE 35 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



MJ10048

FIGURE 36 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

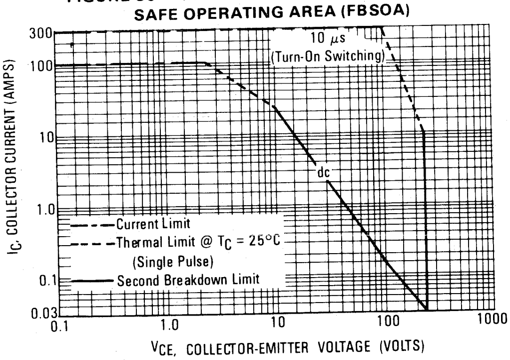
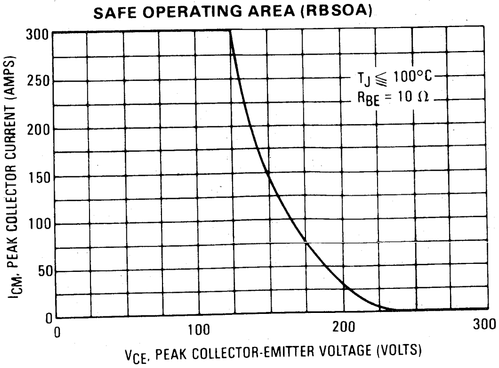


FIGURE 37 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



3

OVERLOAD CHARACTERISTICS

MJ10042

FIGURE 38 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

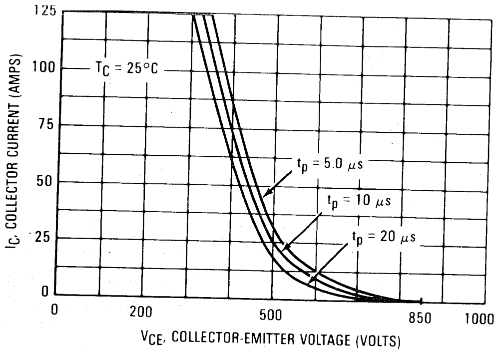
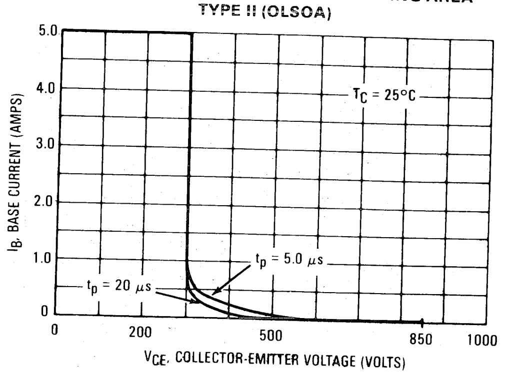


FIGURE 39 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



MJ10045

FIGURE 40 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

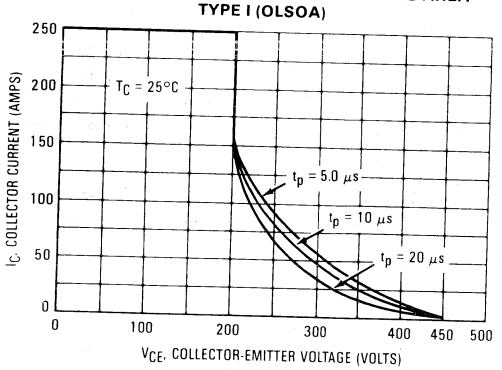
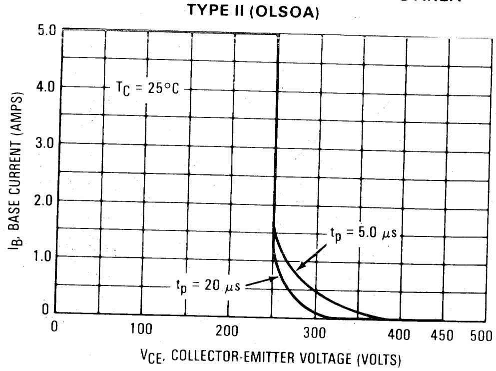


FIGURE 41 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



MJ10048

FIGURE 42 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

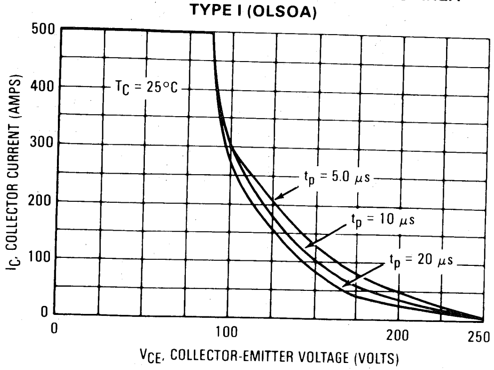
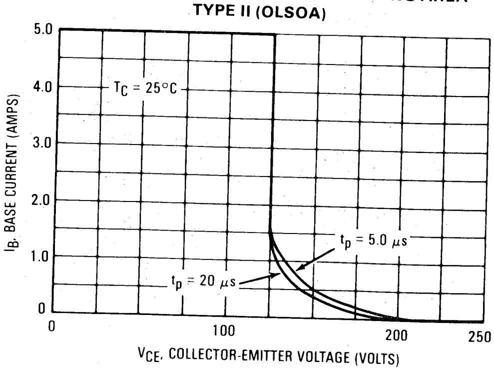


FIGURE 43 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 32, 34 and 36 are based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on these figures may be found at any case temperature by using the appropriate curve on Figure 28.

$T_{J(pk)}$ may be calculated from the data in Figure 31. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figures 33, 35 and 37 give the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in these figures adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figures 38, 40 and 42 depict the Type I OLSOA rating for these devices. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, these figures define the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 44) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figures 39, 41 and 43 are measured in the circuit shown in Figure 45, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

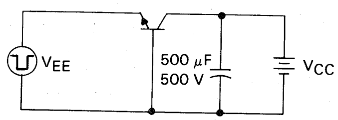
There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NON-REPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for these devices is 100 occurrences. Another factor is the form of turn-off bias. For these devices, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from I_{B2} = 0 (soft) to $V_{BE(off)}$ = 5 V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

3

OVERLOAD SAFE OPERATING TEST CIRCUITS

FIGURE 44 — OVERLOAD SOA TEST CIRCUIT
TYPE I (OLSOA)



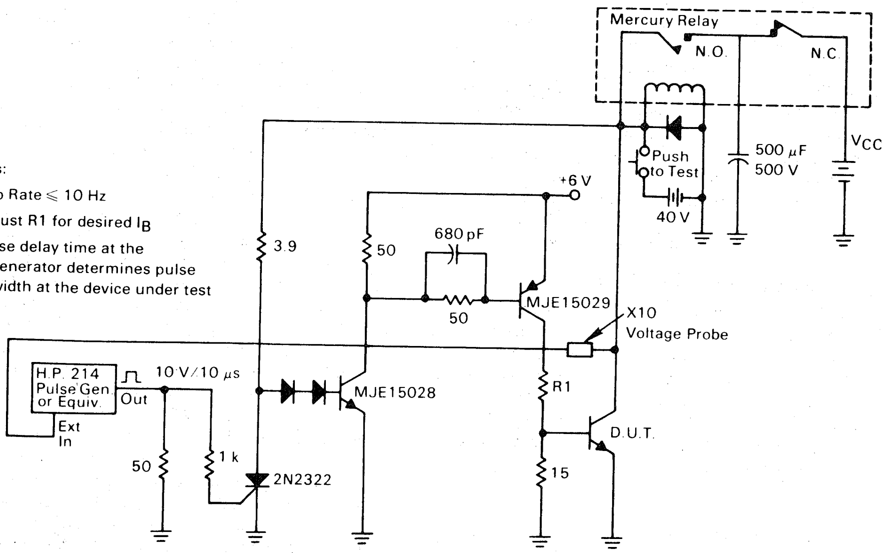
Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

FIGURE 45 — OVERLOAD SOA TEST CIRCUIT
TYPE II (OLSOA)

Notes:

- Rep Rate ⩽ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP	NPN
MJ11011	**MJ11012**
MJ11013	**MJ11014**
MJ11015	**MJ11016**

HIGH-CURRENT COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – h_{FE} = 1000 (Min) @ I_C = 20 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor
- Junction Temperature to +200°C

30 AMPERE

DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

60-120 VOLTS
200 WATTS

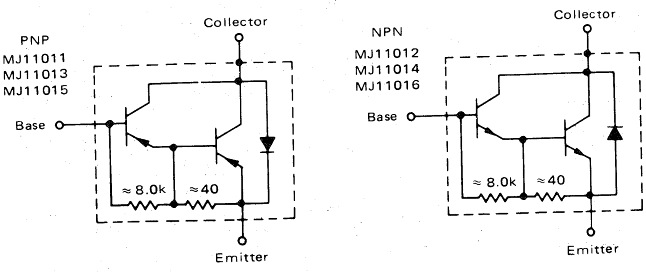
MAXIMUM RATINGS

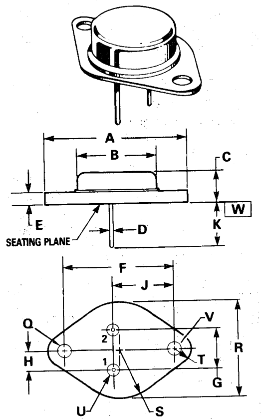
Rating	Symbol	MJ11011 MJ11012	MJ11013 MJ11014	MJ11015 MJ11016	Unit
Collector-Emitter Voltage	V_{CEO}	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector Current	I_C	30			Adc
Base Current	I_B	1			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C @ T_C = 100°C	P_D	200 1.15			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.87	°C/W
Maximum Lead Temperature for Soldering Purposes for ≤ 10 Seconds.	T_L	275	°C

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC





NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   | ⌖ | ϕ 0.25 (0.010) Ⓜ | W | V Ⓜ |
3. POSITIONAL TOLERANCE FOR LEADS:
   | ⌖ | ϕ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ |

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ11011,MJ11012	$V_{(BR)CEO}$	60	—	Vdc
	MJ11013,MJ11014		90	—	
	MJ11015,MJ11016		120	—	
Collector Emitter Leakage Current (V_{CE} = 60 Vdc, R_{BE} = 1 k ohm)	MJ11011,MJ11012	I_{CER}	—	1	mAdc
(V_{CE} = 90 Vdc, R_{BE} = 1 k ohm)	MJ11013,MJ11014		—	1	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm)	MJ11015,MJ11016		—	1	
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11011,MJ11012		—	5	
(V_{CE} = 90 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11013,MJ11014		—	5	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11015,MJ11016		—	5	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	5	mAdc
Collector-Emitter Leakage Current (V_{CE} = 50 Vdc, I_B = 0)		I_{CEO}	—	1	mAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 20 Adc, V_{CE} = 5 Vdc)		h_{FE}	1000	—	—
(I_C = 30 Adc, V_{CE} = 5 Vdc)			200	—	
Collector-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)		$V_{CE(sat)}$	—	3	Vdc
(I_C = 30 Adc, I_B = 300 mAdc)			—	4	
Base-Emitter Saturation Voltage I_C = 20 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	—	3.5	Vdc
I_C = 30 Adc, I_B = 300 mAdc)			—	5	
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3 Vdc, f = 1 MHz)		$\|h_{fe}\|$	4	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — DC CURRENT GAIN (1)

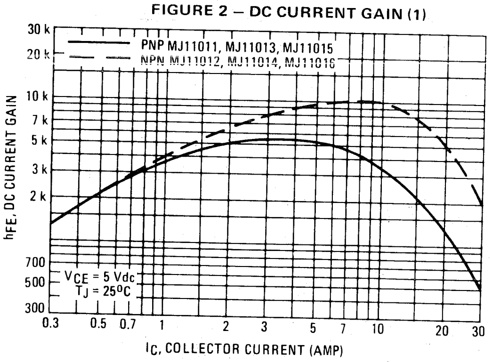


FIGURE 3 — SMALL-SIGNAL CURRENT GAIN

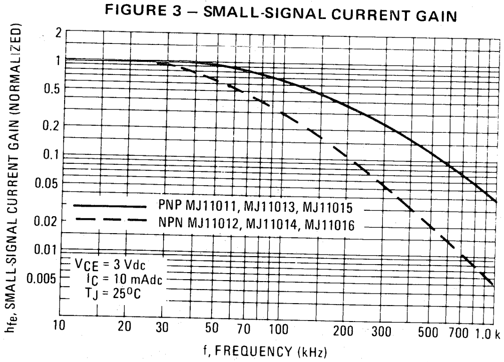


FIGURE 4 — "ON" VOLTAGES (1)

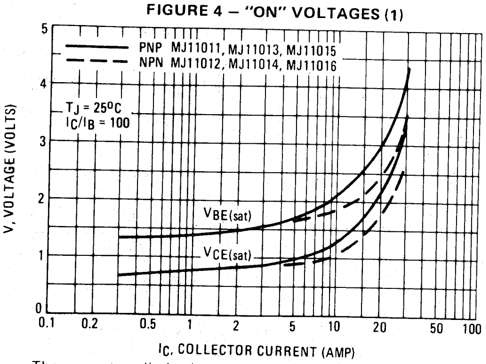
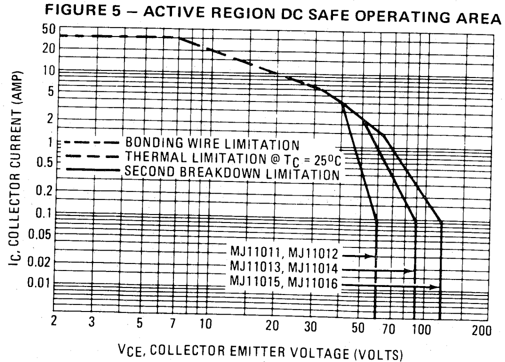


FIGURE 5 — ACTIVE REGION DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP	NPN
MJ11017	**MJ11018**
MJ11019	**MJ11020**
MJ11021	**MJ11022**

COMPLEMENTARY DARLINGTON SILICON POWER TRANSISTORS

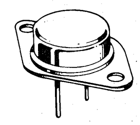
. . . designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High dc Current Gain @ 10 Adc — h_{FE} = 400 Min (All Types)
- Collector-Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 150 Vdc (Min) — MJ11018, 17
  = 200 Vdc (Min) — MJ11020, 19
  = 250 Vdc (Min) — MJ11022, 21
- Low Collector-Emitter Saturation
  $V_{CE(sat)}$ = 1.0 V (Typ) @ I_C = 5.0 A
  = 1.8 V (Typ) @ I_C = 10 A
- Monolithic Construction
- 100% SOA Tested @ V_{CE} = 44 V, I_C = 4.0 A, t = 250 ms.

15 AMPERE

DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

150, 200, 250 VOLTS
175 WATTS



MAXIMUM RATINGS

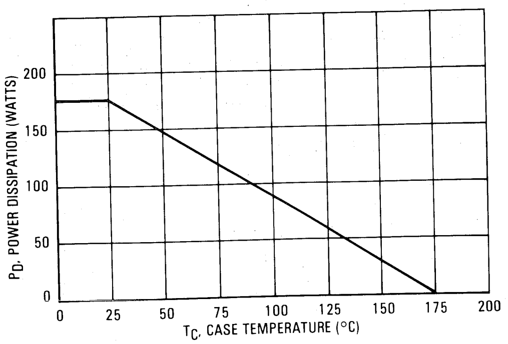
Rating	Symbol	MJ11018 MJ11017	MJ11020 MJ11019	MJ11022 MJ11021	Unit
Collector-Emitter Voltage	V_{CEO}	150	200	250	Vdc
Collector-Base Voltage	V_{CB}	150	200	250	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	15 30			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	175 1.16			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175 -65 to +200			°C °C

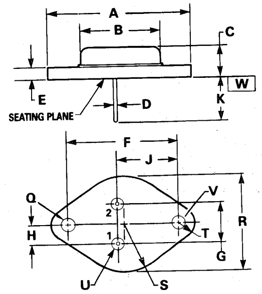
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.86	°C/W

(1) Pulse Test: Pulse Width 5.0 ms, Duty Cycle ≤ 10%

FIGURE 1 — POWER DERATING





NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⌖ φ 0.25 (0.010) Ⓜ W V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⌖ φ 0.30 (0.012) Ⓜ W V Ⓜ Q Ⓜ

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C Unless Otherwise Noted)

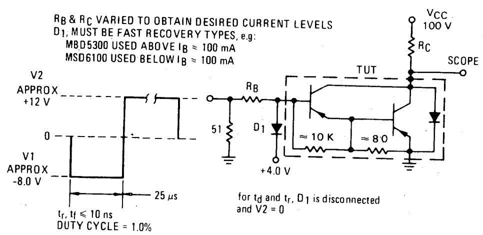
Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0) MJ11017, MJ11018	$V_{CEO(sus)}$	150	—	Vdc
MJ11019, MJ11020		200	—	
MJ11021, MJ11022		250	—	
Collector Cutoff Current (V_{CE} = 75, I_B = 0) MJ11017, MJ11018	I_{CEO}	—	1.0	mAdc
(V_{CE} = 100, I_B = 0) MJ11019, MJ11020		—	1.0	
(V_{CE} = 125, I_B = 0) MJ11021, MJ11022		—	1.0	
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	0.5	mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_J = 150°C)		—	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	400	15,000	—
(I_C = 15 Adc, V_{CE} = 5.0 Vdc)		100	—	
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 100 mA)	$V_{CE(sat)}$	—	2.0	Vdc
(I_C = 15 Adc, I_B = 150 mA)		—	3.4	
Base-Emitter On Voltage I_C = 10 A, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
Base-Emitter Saturation Voltage (I_C = 15 Adc, I_B = 150 mA)	$V_{BE(sat)}$	—	3.8	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common Emitter Small Signal Short Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$\lvert h_{fe} \rvert$	3.0	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJ11018, MJ11020, MJ11022	C_{ob}	—	400	pF
MJ11017, MJ11019, MJ11021		—	600	
Small-Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz	h_{fe}	100	—	—

SWITCHING CHARACTERISTICS

Characteristics		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	(V_{CC} = 100 V, I_C = 10 A, I_B = 100 mA $V_{BE(off)}$ = 5.0 V) (See Figure 2.)	t_d	150	75	ns
Rise Time		t_r	1.2	0.5	μs
Storage Time		t_s	4.4	2.7	μs
Fall Time		t_f	10.0	2.5	μs

(1)Pulsed Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 — THERMAL RESPONSE

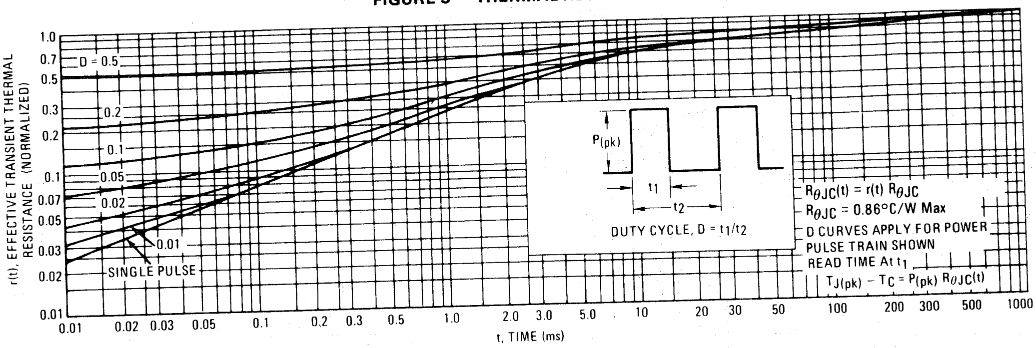
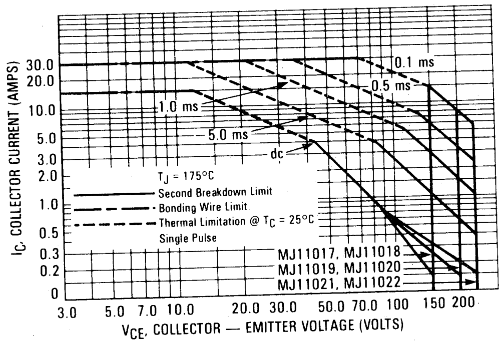


FIGURE 4 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (FBSOA)

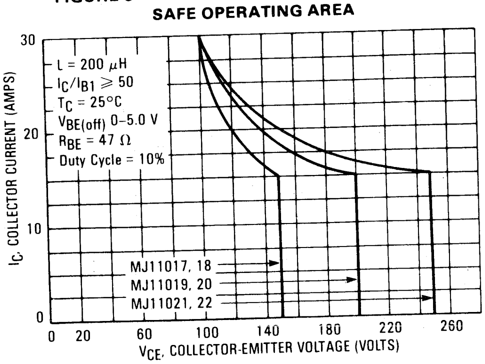


FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 175°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 175°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 5 — MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives RBSOA characteristics.

FIGURE 6 — DC CURRENT GAIN

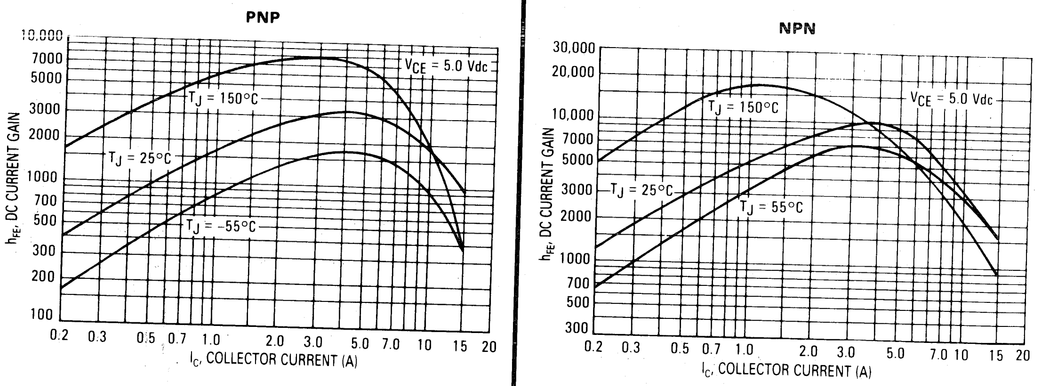


FIGURE 7 — COLLECTOR SATURATION REGION

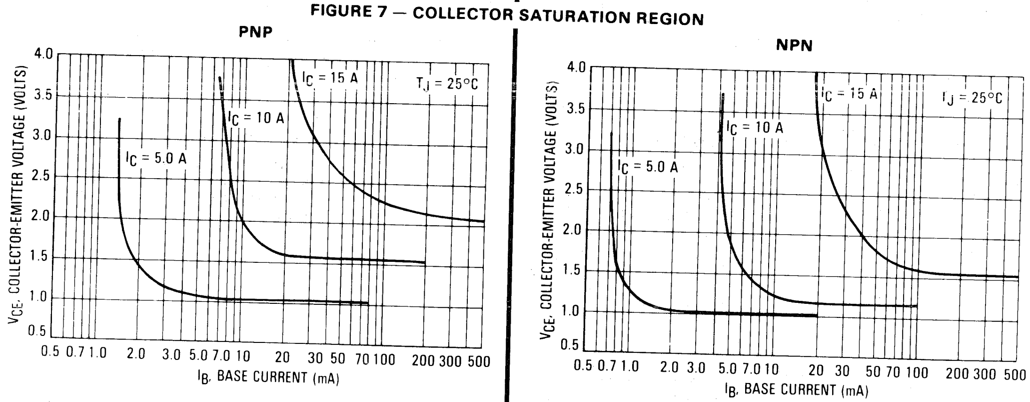
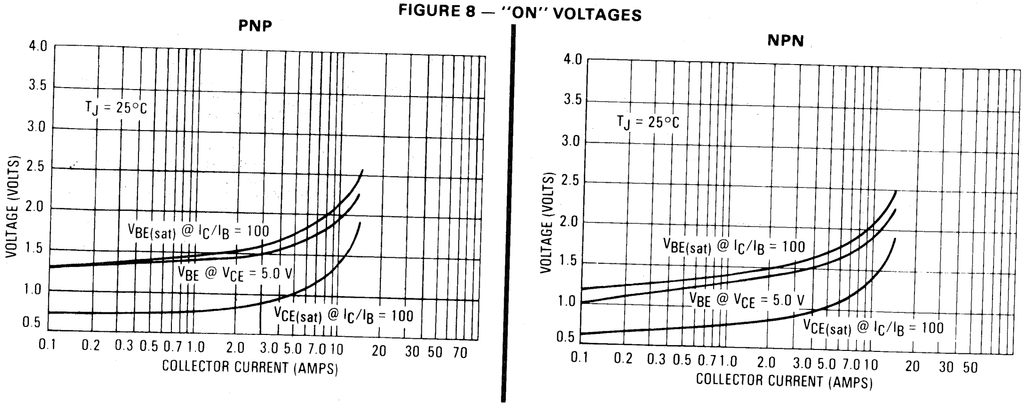


FIGURE 8 — "ON" VOLTAGES



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
MJ11028	**MJ11029**
MJ11030	**MJ11031**
MJ11032	**MJ11033**

HIGH-CURRENT COMPLEMENTARY SILICON TRANSISTORS

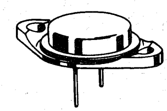
. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 1000 (Min) @ I_C = 25 Adc
  h_{FE} = 400 (Min) @ I_C = 50 Adc
- Curves to 100 A (Pulsed)
- Diode Protection to Rated I_C
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor
- Junction Temperature to +200°C

50 AMPERE

COMPLEMENTARY SILICON DARLINGTON POWER TRANSISTOR

60–120 VOLTS
300 WATTS



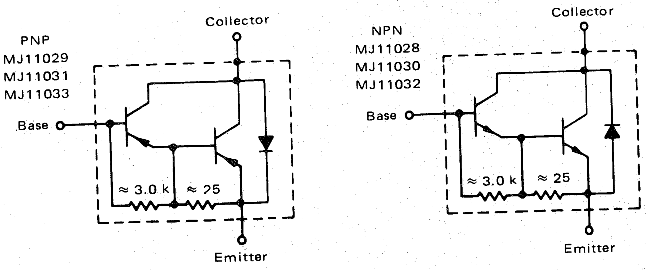
MAXIMUM RATINGS

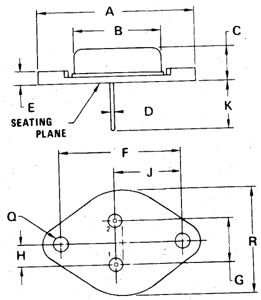
Rating	Symbol	MJ11028 MJ11029	MJ11030 MJ11031	MJ11032 MJ11033	Unit
Collector-Emitter Voltage	V_{CEO}	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}		5		Vdc
Collector Current—Continuous Peak	I_C I_{CM}		50 100		Adc
Base Current—Continuous	I_B		2		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C @ T_C = 100°C	P_D		300 1.71		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Maximum Lead Temperature for Soldering Purposes for ≤ 10 seconds	T_L	275	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.584	°C

FIGURE 1 — DARLINGTON CIRCUIT SCHEMATIC





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

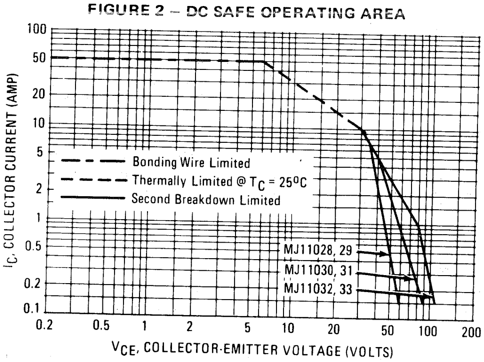
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 100 mAdc, I_B = 0)	MJ11028 MJ11029 MJ11030 MJ11031 MJ11032 MJ11033	$V_{(BR)CEO}$	60 90 120	— — —	Vdc
Collector-Emitter Leakage Current (V_{CE} = 60 Vdc, R_{BE} = 1 k ohm) (V_{CE} = 90 Vdc, R_{BE} = 1 k ohm) (V_{CE} = 120 Vdc, R_{BE} = 1 k ohm) (V_{CE} = 60 Vdc, R_{BE} = 1 k ohm, T_C = 150°C) (V_{CE} = 90 Vdc, R_{BE} = 1 k ohm, T_C = 150°C) (V_{CE} = 120 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11028 MJ11029 MJ11030 MJ11031 MJ11032 MJ11033 MJ11028 MJ11029 MJ11030 MJ11031 MJ11032 MJ11033	I_{CER}	— — — — — —	2 2 2 10 10 10	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	5	mAdc
Collector-Emitter Leakage Current (V_{CE} = 50 Vdc, I_B = 0)		I_{CEO}	—	2	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 25 Adc, V_{CE} = 5 Vdc) (I_C = 50 Adc, V_{CE} = 5 Vdc)		h_{FE}	1 k 400	18 k —	—
Collector-Emitter Saturation Voltage (I_C = 25 Adc, I_B = 250 mAdc) (I_C = 50 Adc, I_B = 500 mAdc)		$V_{CE(sat)}$	— —	2.5 3.5	Vdc
Base-Emitter Saturation Voltage (I_C = 25 Adc, I_B = 200 mAdc) (I_C = 50 Adc, I_B = 300 mAdc)		$V_{BE(sat)}$	— —	3.0 4.5	Vdc

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — DC SAFE OPERATING AREA



There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 3 — DC CURRENT GAIN

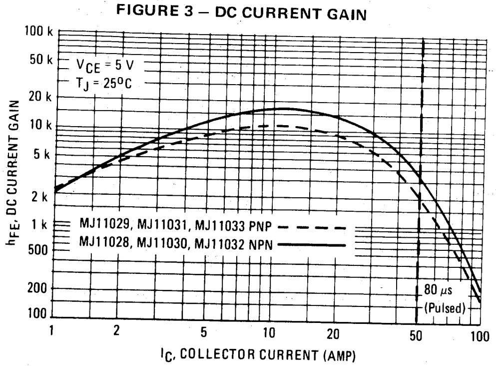
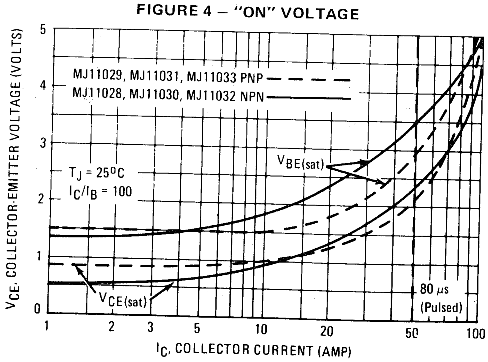


FIGURE 4 — "ON" VOLTAGE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ12002

Designer's Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage —
  V_{CEX} = 1500 Volts
- Glassivated Base-Collector Junction
- Forward Bias Safe Operating Area @ 50 μs = 15 A, 300 V
- Switching Times with Inductive Loads —
  t_f = 0.65 μs (Typ) @ I_C = 2.0 A

2.5 AMPERE
NPN SILICON
POWER TRANSISTOR

1500 VOLTS
75 WATTS

Designer's Data for "Worst Case" Conditions

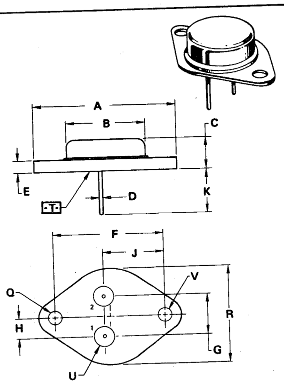
The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous	I_C	2.5	Adc
Base Current — Continuous	I_B	2.0	Adc
Emitter Current — Continuous	I_E	4.5	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	75 30 0.6	Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [-T-] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   | ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ |
   FOR LEADS:
   | ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

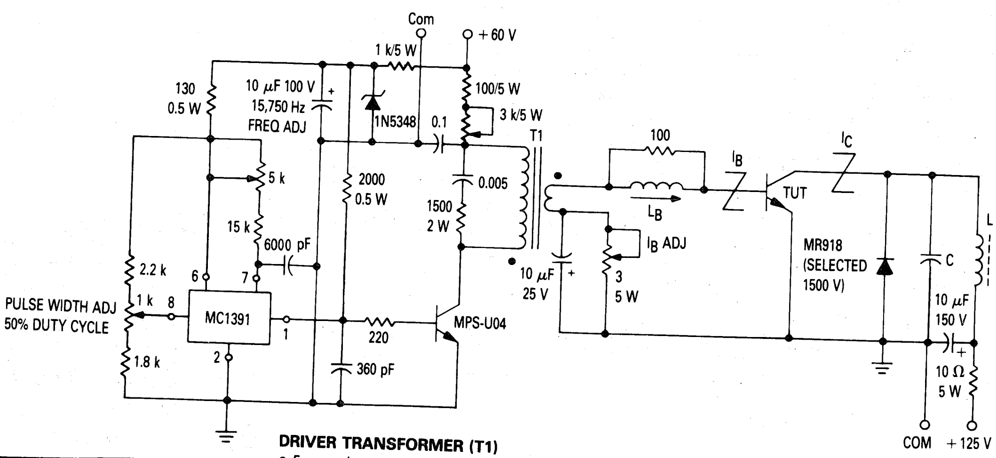
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	—	—	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	—	—	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	—	0.1	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.8 Adc)	$V_{CE(sat)}$	—	—	5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.8 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
Second Breakdown Collector Current with Base-Forward Biased	$I_{S/B}$		See Figure 14		—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	50	—	pF
Current Gain — Bandwidth Product (1) (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	—	4.0	—	MHz
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 2.0 Adc, I_{B1} = 1.0 Adc, L_B = 12 µH, See Figure 1)	t_f	—	0.65	1.0	µs

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle = 2%.

Figure 1. Switching Times Test Circuit



I_C	L	C
0.75 A	4.25 mH	.003 µF
1.5	2.18 mH	.006 µF
2.0	1.6 mH	.008 µF

DRIVER TRANSFORMER (T1)
- Ferrox cube pot core #4229P-L00-3C8
- Adjust gap for primary inductance L_P = 70 mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than 3 µH
- Use 3 mil mylar tape between each winding layer

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst case component variations and maximum high voltage loading must also be taken into account.

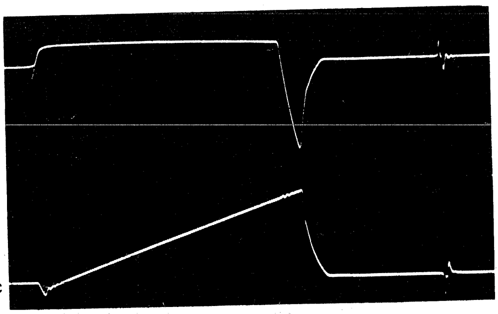
If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when I_{B1} h_{FE} = I_{CM}, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the I_{B1} h_{FE} = I_{CM} point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation I_{B1} h_{FE} = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

TEST CIRCUIT WAVEFORMS

FIGURE 2

I_B

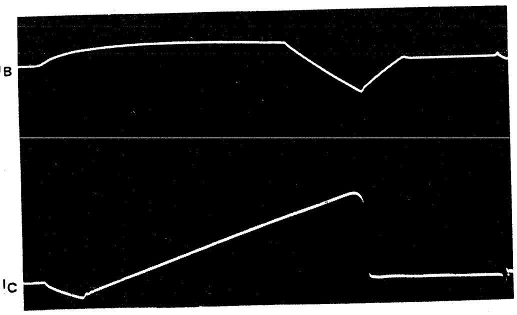


I_C

(time)

FIGURE 3

I_B



I_C

(time)

3

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 — OPTIMIZING DRIVE @ I_C = 0.75 A

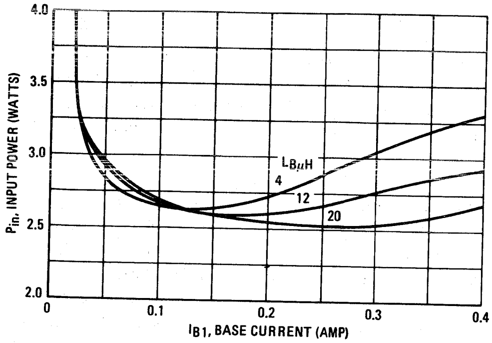


FIGURE 5 — OPTIMIZING DRIVE @ I_C = 1.5 A

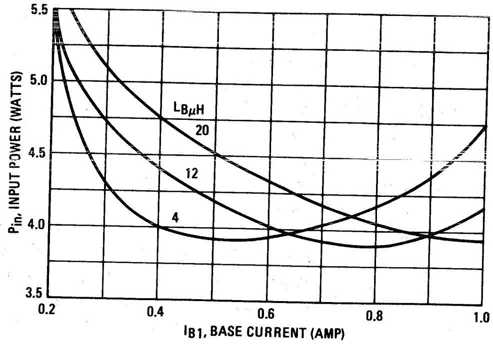


FIGURE 6 — OPTIMIZING DRIVE @ I_C = 2.0 A

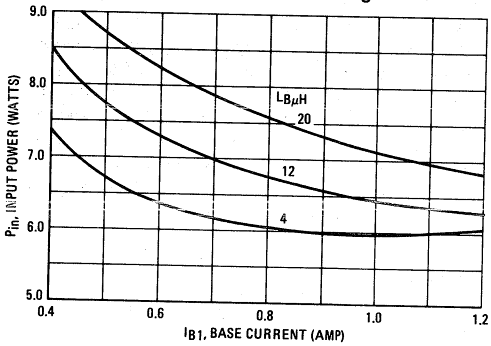


FIGURE 7 — SWITCHING BEHAVIOR versus TEMPERATURE

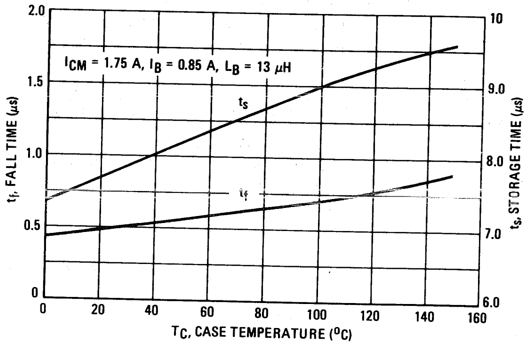


FIGURE 8 — OPTIMUM DRIVE CONDITIONS

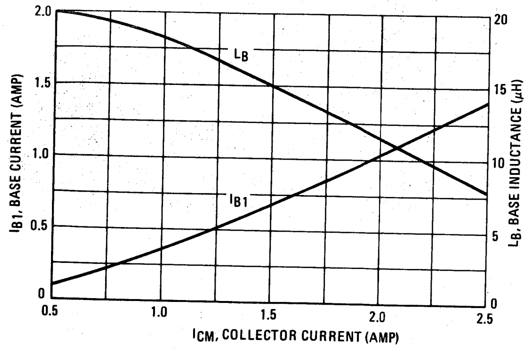
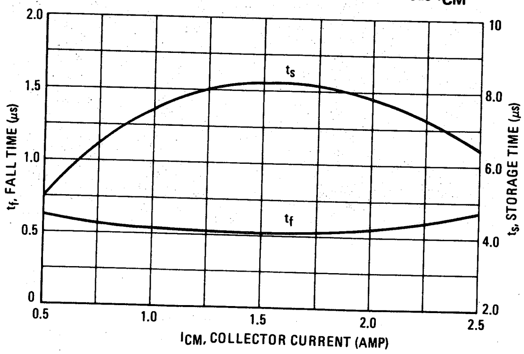


FIGURE 9 — SWITCHING BEHAVIOR versus I_{CM}



3

FIGURE 10 – THERMAL RESPONSE

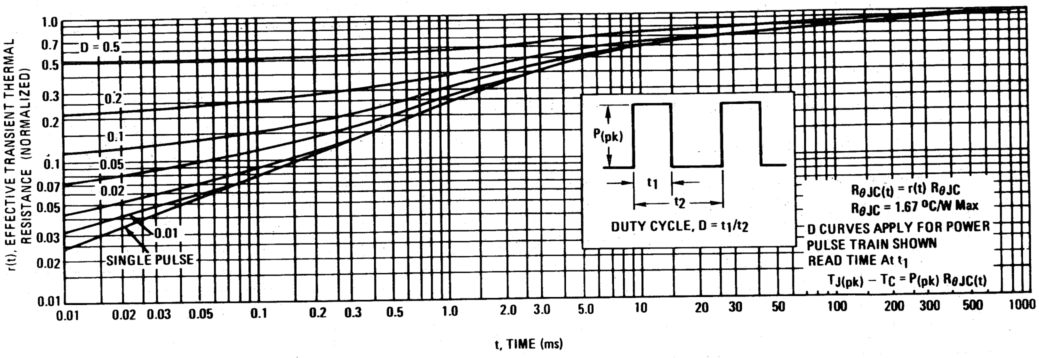


FIGURE 11 – COLLECTOR SATURATION REGION

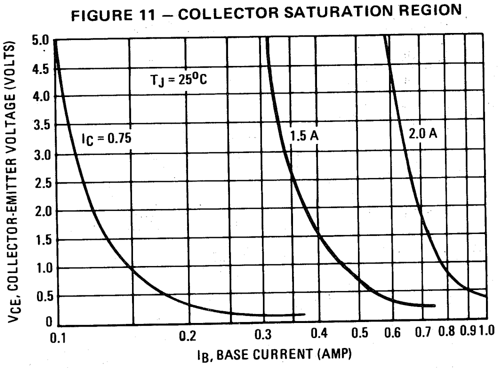


FIGURE 12 – DC CURRENT GAIN

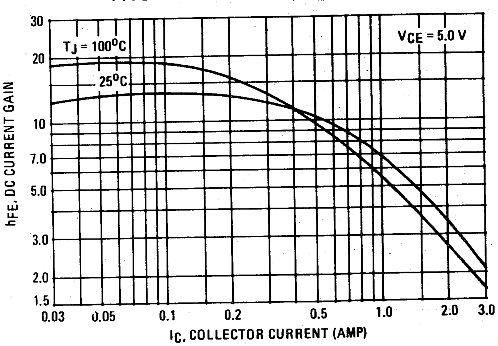


FIGURE 13 – "ON" VOLTAGES

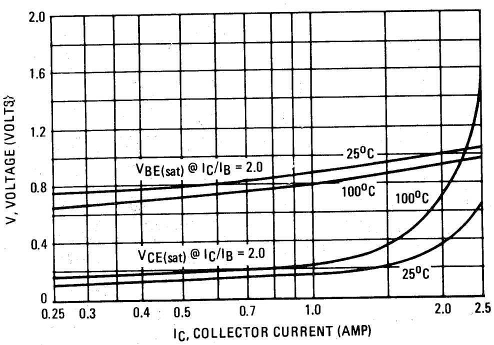
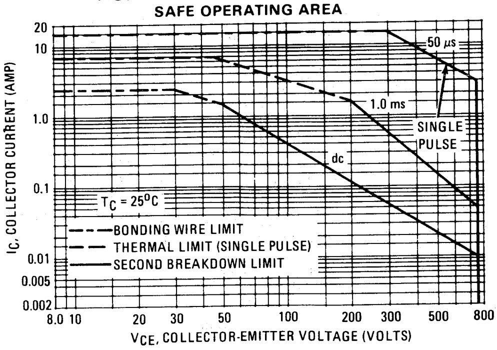


FIGURE 14-MAXIMUM FORWARD BIAS SAFE OPERATING AREA



NOTE:
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 μs SB curve is beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ12003

HORIZONTAL DEFLECTION TRANSISTOR

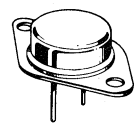
. . . specifically designed for use in CRT deflection circuits.

- Collector-Emitter Voltage — V_{CEX} = 1500 Volts
- Glassivated Base-Collector Junction
- Forward Bias Safe Operating Area @ 50 μs = 20 A, 300 V
- Switching Times with Inductive Loads — t_f = 0.5 μs (Typ) @ I_C = 3.0 A

4 AMPERE

NPN SILICON POWER TRANSISTOR

1500 VOLTS
100 WATTS

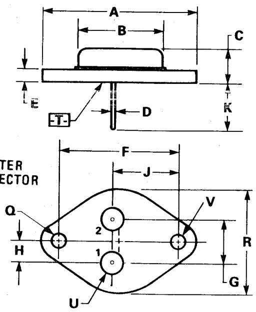


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector-Current — Continuous	I_C	4.0	Adc
Base Current — Continuous	I_B	3.0	Adc
Emitter Current — Continuous	I_E	7.0	Adc
Total Power Dissipation @ T_C = 25°C T_C = 100°C Derate above 25°C	P_D	100 40 0.8	Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

| ⌖ | ∅0.13 (0.005) Ⓜ | T | V Ⓜ |

FOR LEADS:

| ⌖ | ∅0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |

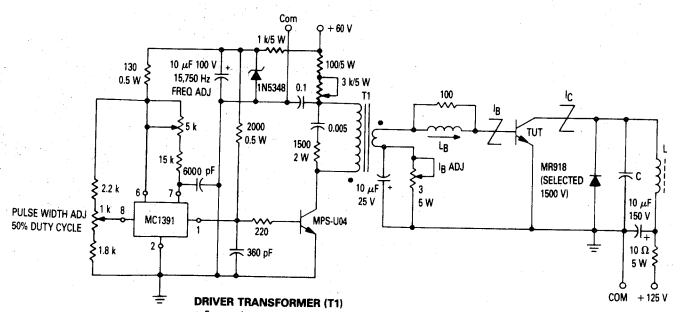
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

FIGURE 1 — TEST CIRCUIT



I_C A	L mH	C μF
3.0	1.00	0.012

DRIVER TRANSFORMER (T1)
- Ferrox cube pot core #4229P-L00-3C8
- Adjust gap for primary inductance Lp = 70 mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than 3 μH
- Use 3 mil mylar tape between each winding layer

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 1.2 Adc)	$V_{CE(sat)}$	–	–	5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 1.2 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 5			–
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	–	4	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	90	–	pF
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 3.0 Adc, I_{B1} = 1.2 Adc, L_B = 8.0 μH, See Figure 1)	t_f	–	0.5	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 2 — DC CURRENT GAIN

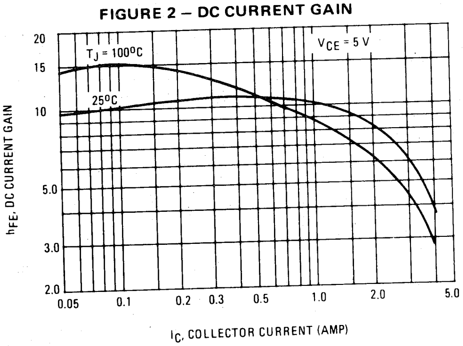


FIGURE 3 — COLLECTOR SATURATION REGION

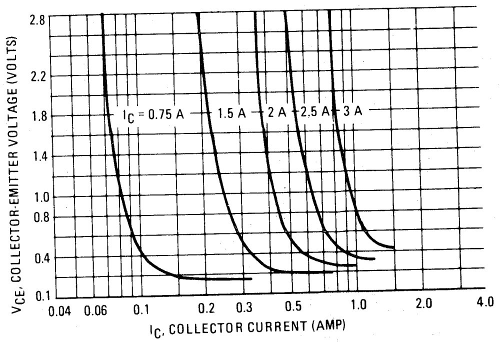


FIGURE 4 — "ON" VOLTAGES

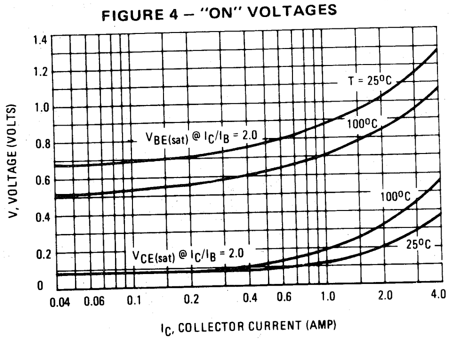
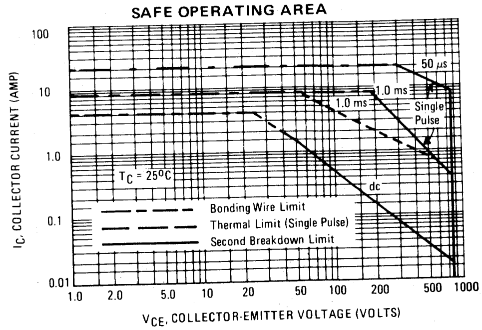


FIGURE 5 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



NOTE:
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The 50 μs and 1 ms curves are beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ12004
MJH12004

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage — V_{CEX} = 1500 Vdc
- Glassivated Base-Collector Junction
- Safe Operating Area @ 50 μs = 20 A, 400 V
- Switching Times with Inductive Loads — t_f = 0.4 μs (Typ) @ I_C = 4.5 A

5.0 AMPERE

NPN SILICON POWER TRANSISTORS

1500 VOLTS
100 WATTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	5.0	Adc
Base Current — Continuous	I_B	4.0	Adc
Emitter Current — Continuous	I_E	9.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	100 40 0.8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

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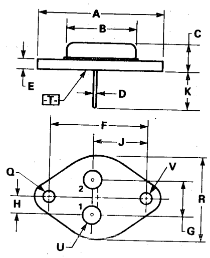
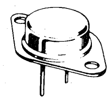
MJ12004





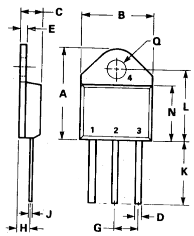
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

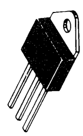
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ 0.13 (0.005) Ⓜ T V Ⓜ
   FOR LEADS:
   ⌖ 0.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

CASE 1-05
TO-204AA

MJH12004





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

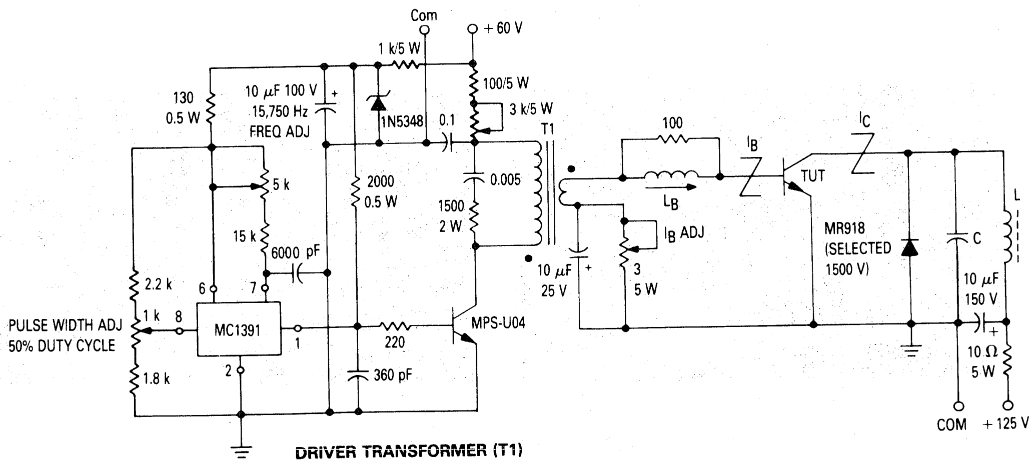
CASE 340-01
TO-218AC

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 1.8 Adc) (I_C = 3.5 Adc, I_B = 1.5 Adc)	$V_{CE(sat)}$	– –	– –	5.0 5.0	Vdc
Base Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 1.8 Adc) (I_C = 3.5 Adc, I_B = 1.5 Adc)	$V_{BE(sat)}$	– –	– –	1.5 1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14			
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1 MHz)	f_T	–	4	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	125	–	pF
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 4.5 Adc, I_{B1} = 1.8 Adc, L_B = 8.0 μH, See Figure 1) T_C = 25°C / T_C = 100°C	t_f	– –	0.4 0.6	1.0 –	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

Figure 1. Switching Times Test Circuit



I_C A	L mH	C μF
3.5	0.87	0.013
4.5	0.67	0.017

DRIVER TRANSFORMER (T1)

- Ferrox cube pot core #4229P-L00-3C8
- Adjust gap for primary inductance Lp = 70 mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than 3 μH
- Use 3 mil mylar tape between each winding layer

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1}\ h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1}\ h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor *initiation* of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation $I_{B1}\ h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

3

TEST CIRCUIT WAVEFORMS

FIGURE 2

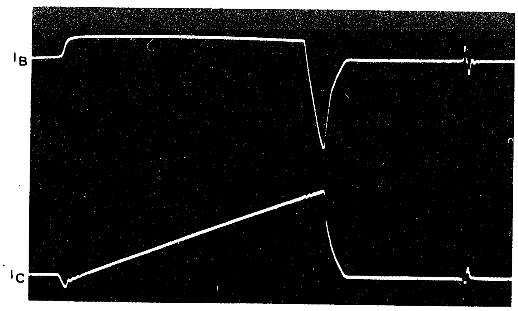
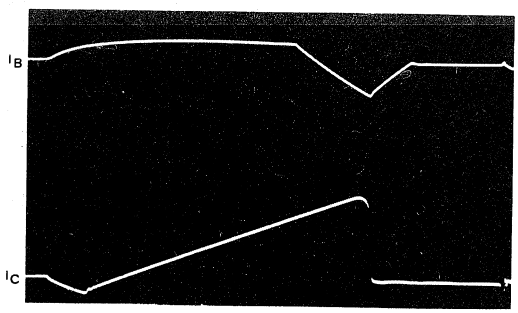


FIGURE 3



TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 – OPTIMIZING DRIVE @ 3.5 A

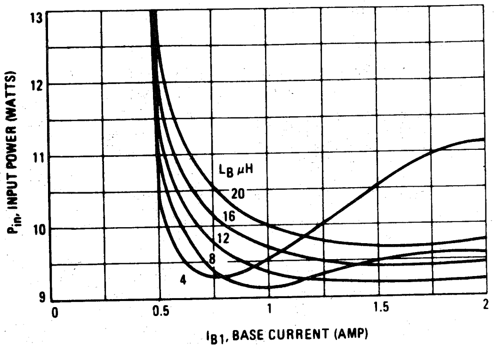


FIGURE 5 – OPTIMIZING DRIVE @ 4.5 A

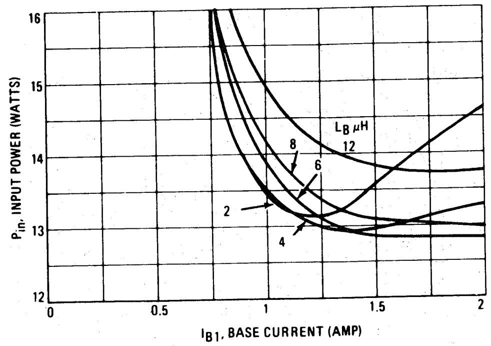


FIGURE 6 – SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 3.5 A, I_B = 1.5 A, L_B = 14 μH

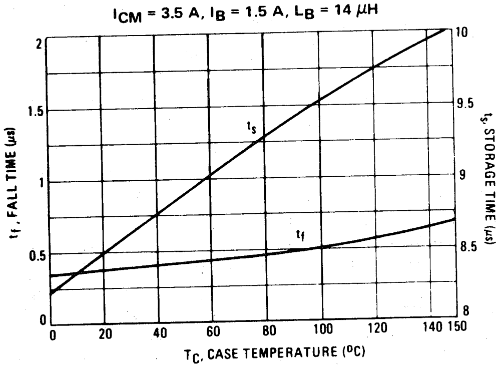


FIGURE 7 – SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 4.5 A, I_B = 1.75 A, L_B = 8 μH

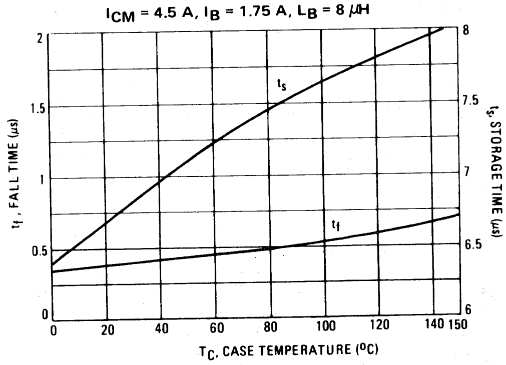


FIGURE 8 – OPTIMUM DRIVE CONDITIONS

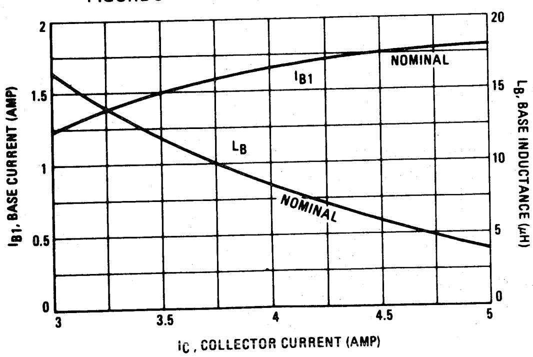
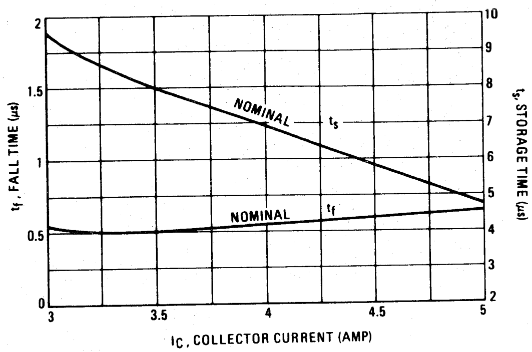


FIGURE 9 – SWITCHING BEHAVIOR versus I_{CM}



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TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 10 — DC CURRENT GAIN

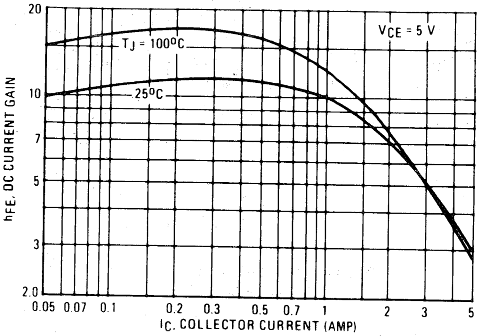
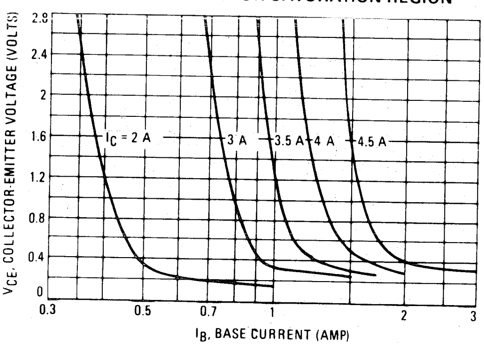
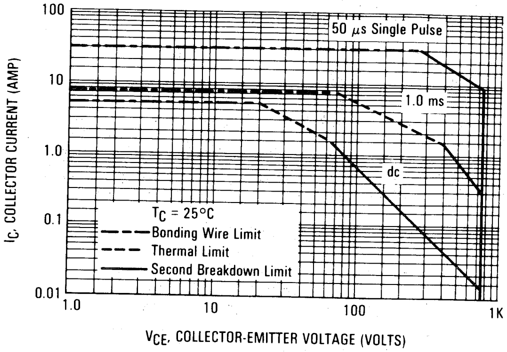


FIGURE 12 — COLLECTOR SATURATION REGION



SAFE OPERATING AREA INFORMATION

FIGURE 11 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

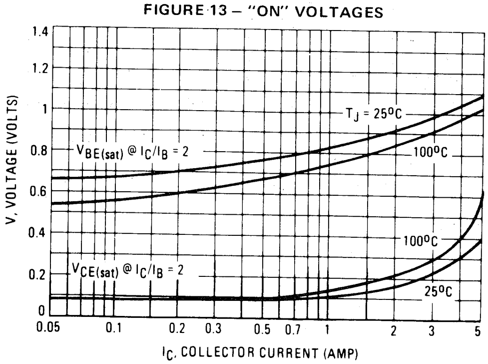


NOTE:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 μs SB curve is beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

FIGURE 13 — "ON" VOLTAGES



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THERMAL RESPONSE

FIGURE 14 — MJ12004

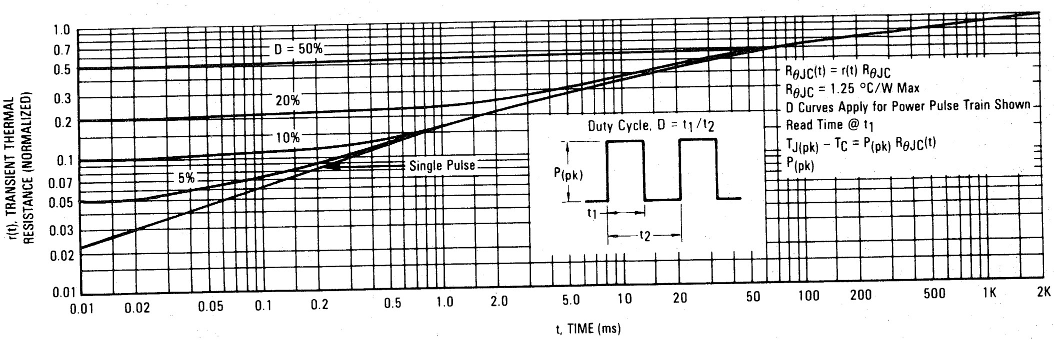
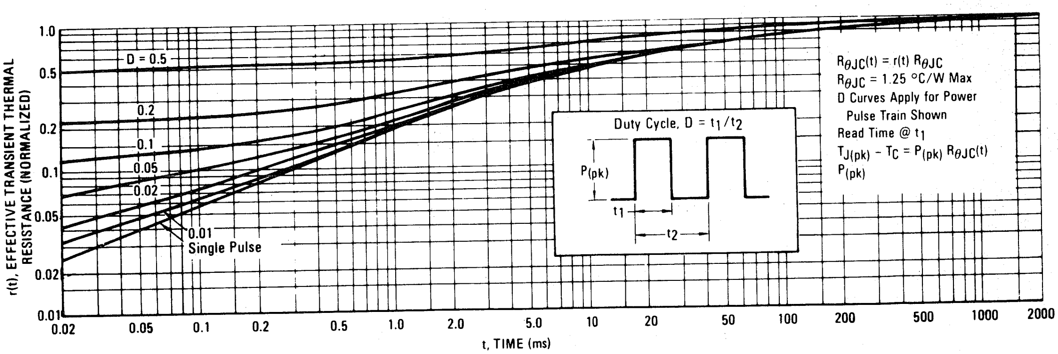


FIGURE 15 — MJH12004



3

MJ12005

HORIZONTAL DEFLECTION TRANSISTOR

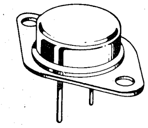
. . . specifically designed for use in deflection circuits.

- V_{CEX} = 1500 V
- Glassivated Base-Collector Junction
- Safe Operating Area @ 50 μs = 20 A, 400 V

8 AMPERE

NPN SILICON POWER TRANSISTOR

1500 VOLTS
100 WATTS

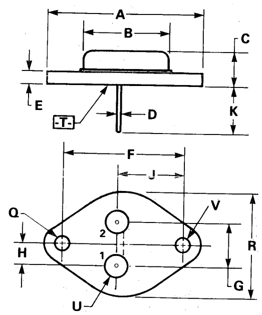


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
Base Current — Continuous	I_B	4.0	Adc
Emitter Current — Continuous	I_E	12	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C



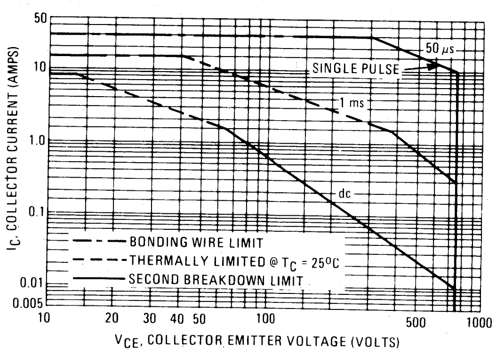
NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ 0.13 (0.005) Ⓜ T V Ⓜ
   FOR LEADS:
   ⌖ 0.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA

FIGURE 1 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (V_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	—	—	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	—	—	0.25	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	—	0.1	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	—	—	5.0	Vdc
Base Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	—	—	See Figure 1	
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 5.0 Adc, I_{B1} = 1.0 Adc, L_B = 8.0 μH)	t_f	—	0.4	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 2 — DC CURRENT GAIN

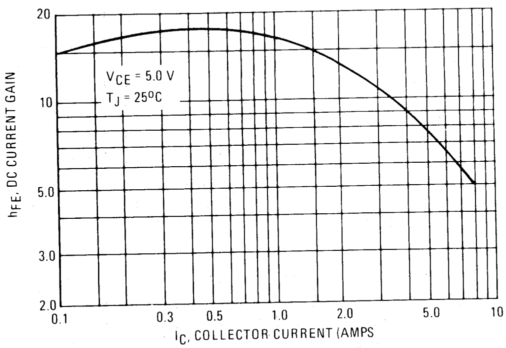
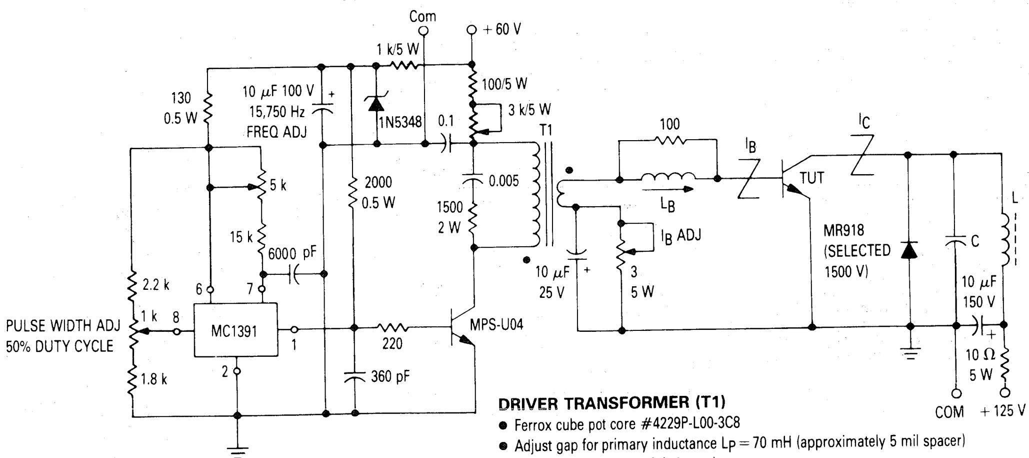


FIGURE 3 — SWITCHING TIMES TEST CIRCUIT



I_C A	L mH	C μF
5.0	0.575	0.018

DRIVER TRANSFORMER (T1)

- Ferrox cube pot core #4229P-L00-3C8
- Adjust gap for primary inductance Lp = 70 mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than 3 μH
- Use 3 mil mylar tape between each winding layer

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ12005D

Designers Data Sheet

8.0 AMPERE

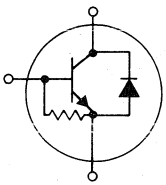
NPN SILICON POWER TRANSISTORS

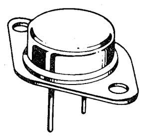
1500 VOLTS
100 WATTS

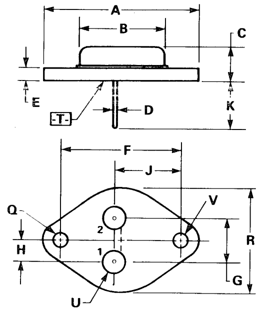
NPN HORIZONTAL DEFLECTION TRANSISTOR WITH INTEGRATED DAMPER DIODE

. . . specifically designed for use in large-screen color-deflection circuits.

- Collector-Emitter Voltage — V_{CEX} = 1500 Vdc
- Glassivated Base-Collector Junction
- Safe Operating Area @ 50 μs = 20 A, 400 V
- Switching Times with Inductive Loads — t_f = 0.4 μs (Typ) @ I_C = 5.0 A
- C-E Diode Forward Voltage Specified







NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ 0.13 (0.005) Ⓜ T V Ⓜ
   FOR LEADS:
   ⌖ 0.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MJ12005D	Unit
Collector-Emitter Voltage	V_{CEO}	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
Base Current — Continuous	I_B	4.0	Adc
Emitter Current — Continuous	I_E	12	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	100 40 0.8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

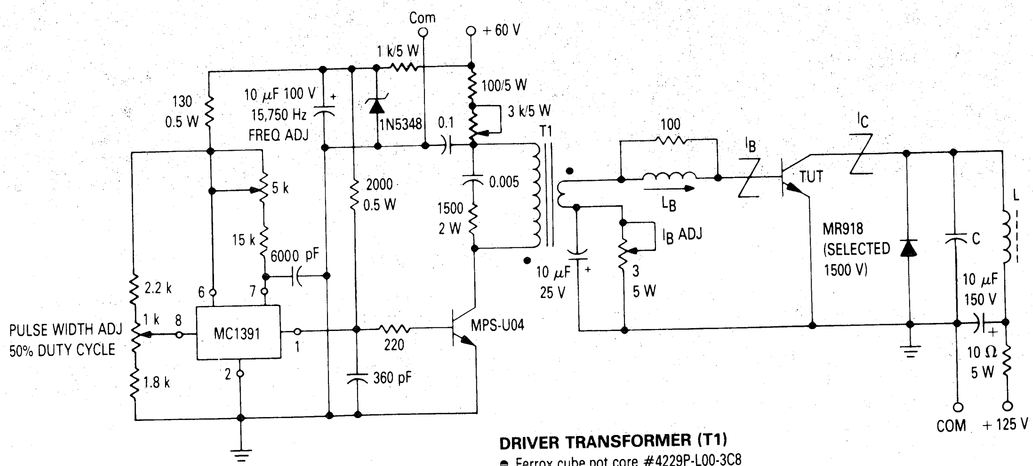
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	—	—	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	—	—	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	—	200	mAdc
ON CHARACTERISTICS (1)					
Diode Forward Voltage (I_F = 8.0 Amps)	$V_{F(VEC)}$	—	—	2.5	Vdc
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 8.0 Adc, I_B = 2.5 Adc)	$V_{CE(sat)}$	— —	— —	5.0 5.0	Vdc
Base Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 8.0 Adc, I_B = 2.5 Adc)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14			
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	—	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	150	—	pF
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 5.0 Adc, I_{B1} = 1.5 Adc, L_B = 8.0 μH, See Figure 1) T_C = 25°C T_C = 100°C	t_f	— —	0.4 0.6	1.0 —	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%.

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



I_C A	L mH	C μF
5.0	0.57	0.018
7.0	0.45	0.025

DRIVER TRANSFORMER (T1)

- Ferrox cube pot core #4229P-L00-3C8
- Adjust gap for primary inductance Lp = 70 mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than 3 μH
- Use 3 mil mylar tape between each winding layer

3

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst-case component variations and maximum high voltage loading must also be taken into account.

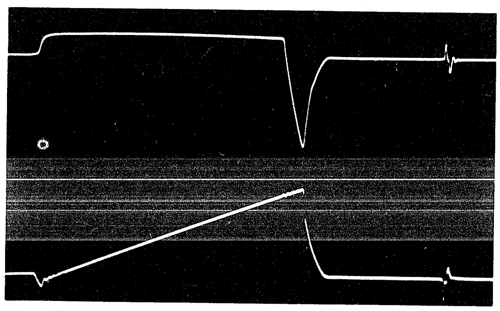
If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1}\ h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the I_{B1} $h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor *initiation* of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation $I_{B1}\ h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

TEST CIRCUIT WAVEFORMS

FIGURE 2

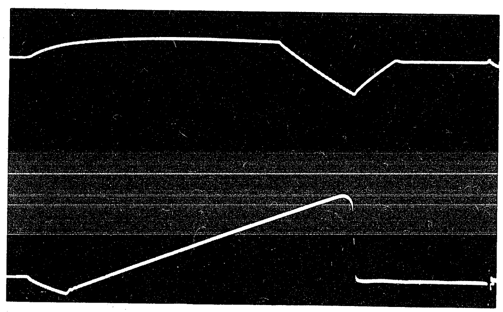
I_B



I_C

(time)

FIGURE 3



(time)

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 — OPTIMIZING DRIVE @ 5.0 A

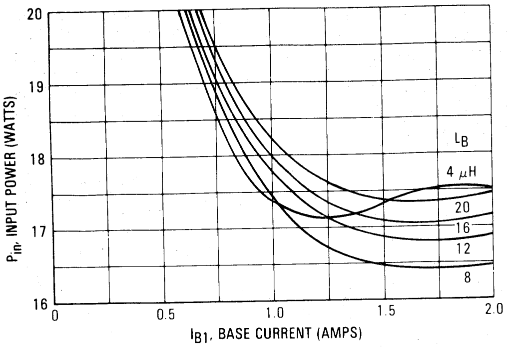


FIGURE 5 — OPTIMIZING DRIVE @ 7.0 A

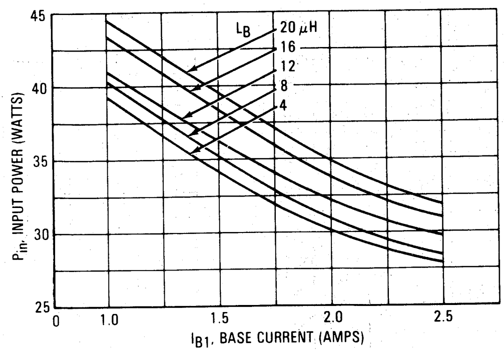


FIGURE 6 — SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 5.0 A, I_B = 1.5 A, L_B = 8.0 μH

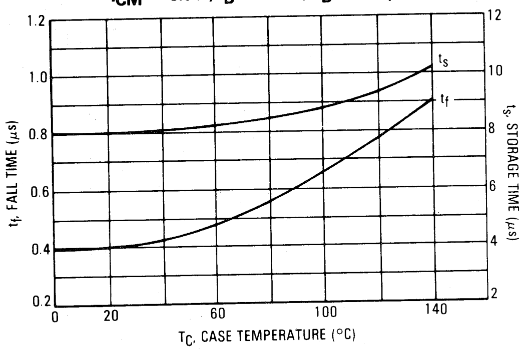


FIGURE 7 — SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 7.0 A, I_B = 2.0 A, L_B = 4.0 μH

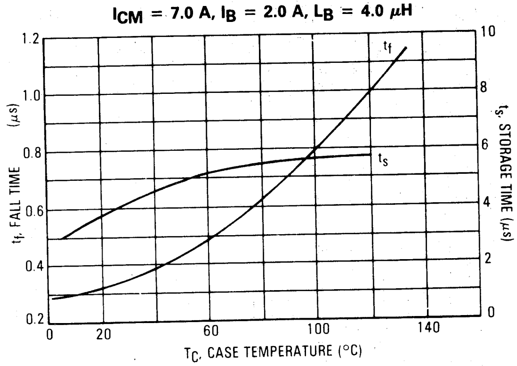


FIGURE 8 — OPTIMUM DRIVE CONDITIONS

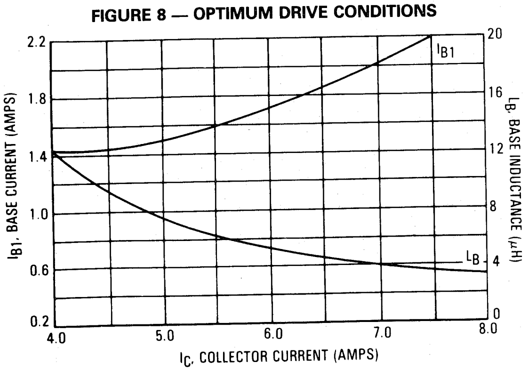
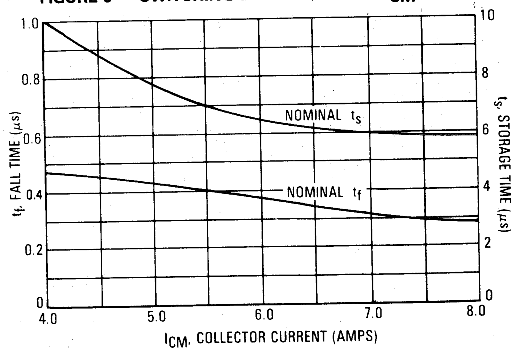


FIGURE 9 — SWITCHING BEHAVIOR versus I_{CM} AT 25°C



3

FIGURE 10 — THERMAL RESPONSE

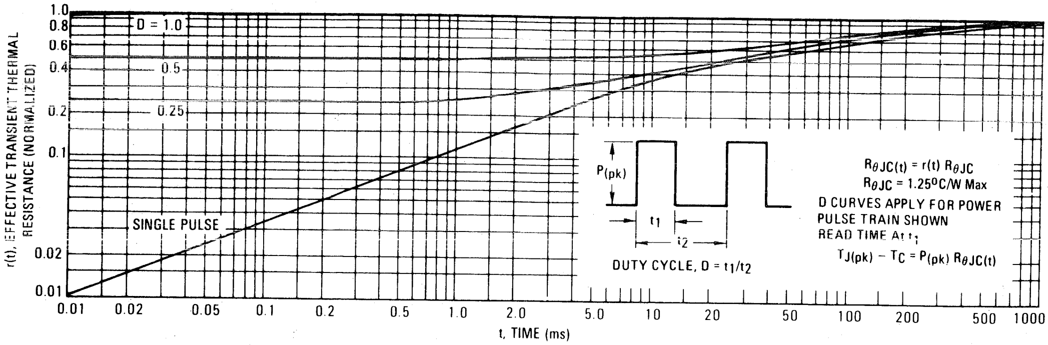


FIGURE 11 — COLLECTOR SATURATION REGION

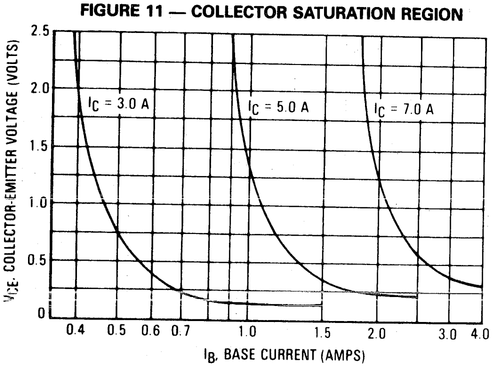


FIGURE 12 — DC CURRENT GAIN versus COLLECTOR CURRENT

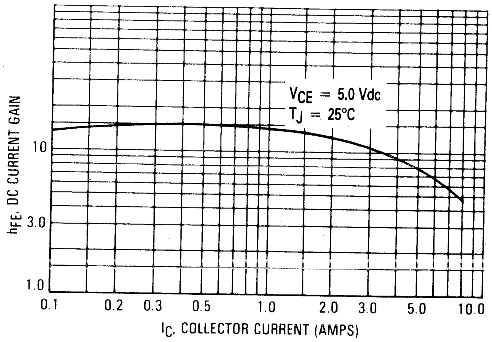


FIGURE 13 — "ON" VOLTAGES

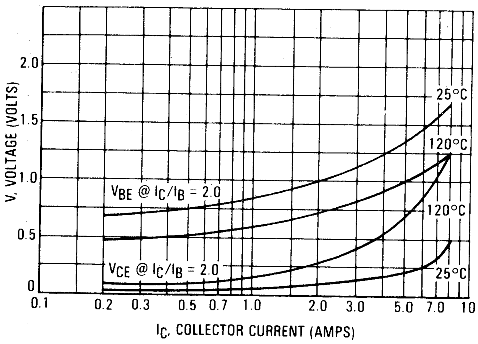


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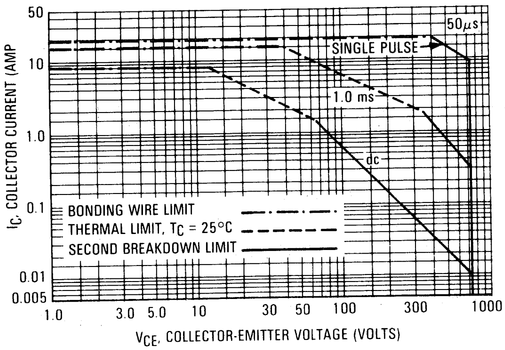
FIGURE 14 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



NOTE:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 μs SB curve is beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without falling.

3

MJ12010

HORIZONTAL DEFLECTION TRANSISTOR

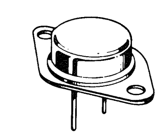
. . . specifically designed for use in CRT deflection circuits.

- Collector-Emitter Voltage — V_{CEX} = 950 Volts
- Glassivated Base-Collector Junction
- Forward Bias Safe Operating Area @ 50 μs = 30 A, 300 V
- Switching Times with Inductive Loads — t_f = 0.5 μs (Typ) @ I_C = 5.0 A

10 AMPERE

NPN SILICON POWER TRANSISTOR

950 VOLTS
100 WATTS

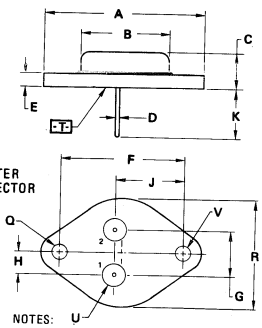


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	400	Vdc
Collector-Emitter Voltage	V_{CEX}	950	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector-Current — Continuous	I_C	10	Adc
Base Current — Continuous	I_B	5.0	Adc
Emitter Current — Continuous	I_E	15	Adc
Total Power Dissipation @ T_C = 25°C T_C = 100°C Derate above 25°C	P_D	100 40 0.8	Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C



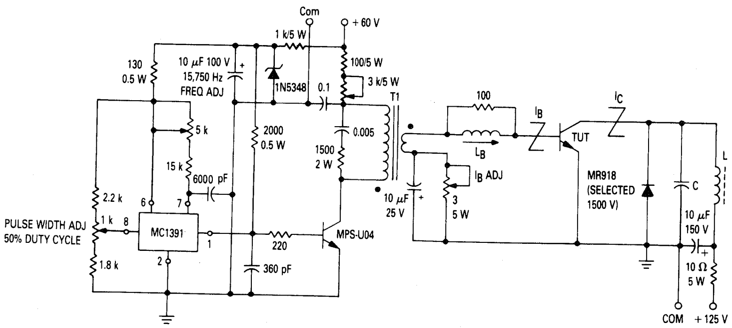
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE-COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
⌖ ϕ.13 (0.005) Ⓜ T V Ⓜ
FOR LEADS:
⌖ ϕ.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

FIGURE 1 — TEST CIRCUIT



I_C A	L mH	C μF
5.0	0.57	0.039

DRIVER TRANSFORMER (T1)
- Ferrox cube pot core #4229P-L00-3C8
- Adjust gap for primary inductance L_P = 70 mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than 3 μH
- Use 3 mil mylar tape between each winding layer

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	400	–	–	Vdc
Collector Cutoff Current (V_{CE} = 950 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.2 Adc)	$V_{CE(sat)}$	–	–	5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.2 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 5			–
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	–	6.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	150	–	pF
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 5.0 Adc, I_{B1} = 1.2 Adc, L_B = 8.0 μH, See Figure 1)	t_f	–	0.5	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 2 — DC CURRENT GAIN

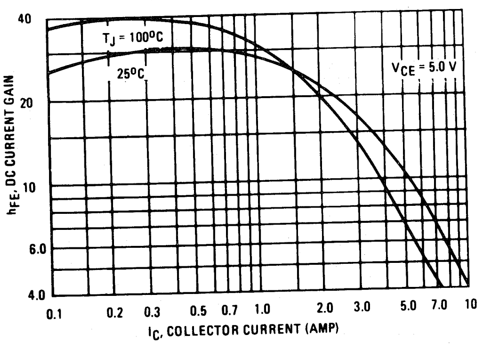


FIGURE 3 — COLLECTOR SATURATION REGION

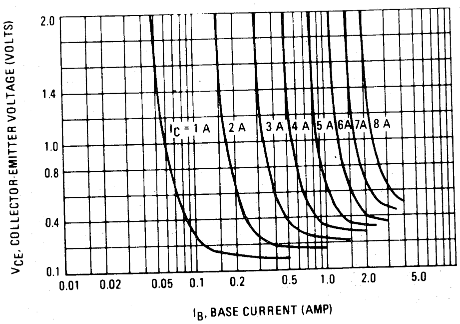


FIGURE 4 — "ON" VOLTAGES

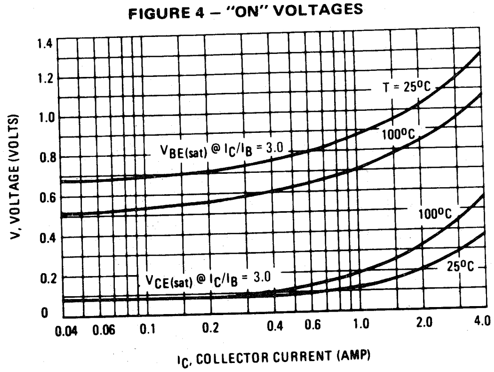
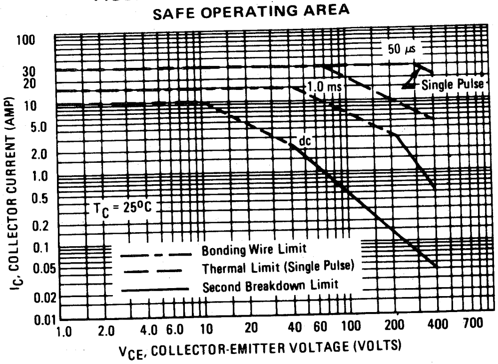


FIGURE 5 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



NOTE:
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The 50 μs and 1 ms curves are beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ12020
MJ12021
MJ12022

Designer's Data Sheet

HIGH PERFORMANCE NPN DEFLECTION TRANSISTORS

These transistors are designed for high resolution video systems, such as, high density graphic displays, data terminals, video scanners . . . wherever high frequency deflection is required.

- Fast Turn-Off Times
- Maximum Storage and Fall Times Specified at 100°C
- Operating Junction Temperature Range -65°C to +200°C
- High f_T of 15 MHz

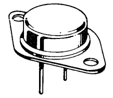
5.0, 8.0 and 15 AMPERE

NPN SILICON DEFLECTION POWER TRANSISTORS

850 VOLTS
125, 150 and 175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



3

MAXIMUM RATINGS

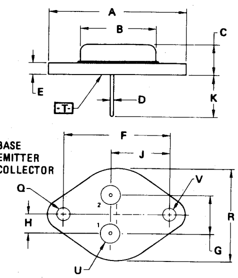
Rating	Symbol	MJ12020	MJ12021	MJ12022	Unit
Collector-Emitter Voltage	V_{CEO}	450			Vdc
Collector-Emitter Voltage	V_{CEV}	850			Vdc
Emitter Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 10	8.0 16	15 20	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4.0 8.0	6.0 12	10 15	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	 125 71.5 0.714	 150 85.5 0.86	 175 100 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	1.17	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275			°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA (TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)		$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figures 19, 21 or 23			
Turn-Off SOA with Base Reverse Biased		RBSOA	See Figures 20, 22 or 24			
ON CHARACTERISTICS (1)						
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)	 MJ12020 MJ12021 MJ12022	$V_{CE(sat)}$	 — — —	 — — —	 1.2 1.2 1.2	Vdc
Base Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)	 MJ12020 MJ12021 MJ12022	$V_{BE(sat)}$	 — — —	 — — —	 1.5 1.5 1.5	Vdc
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)	 MJ12020 MJ12021 MJ12022	h_{FE}	 5.0 5.0 5.0	 — — —	 — — —	—
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth Product (I_C = 0.3 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz) (I_C = 1.3 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	 MJ12020 MJ12021 MJ12022	f_T	 15 15 15	 — — —	 — — —	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 kHz)	 MJ12020 MJ12021 MJ12022	C_{ob}	 — — —	 — — —	 200 350 400	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
MJ12020							
Inductive Switching, Clamped Drive							
Storage Time	(I_C = 3.0 Adc, I_B = 0.6 Adc, V_{CC} = 40 Vdc, $V_{BE(off)}$ = 4.0 Vdc, Pulse Width = 8.0 μs, Duty Cycle ≤ 2%) See Table 1	T_J = 25°C	t_s	—	440	1200	ns
Fall Time			t_f	—	130	300	
Storage Time		T_J = 100°C	t_s	—	550	1500	
Fall Time			t_f	—	200	500	
Inductive Switching, Series Base Inductance							
Fall Time (I_C = 3.0 Adc, I_B = 0.6 Adc, L_B = 24 μH) See Table 2			t_f	—	175	—	ns
MJ12021							
Inductive Switching, Clamped Drive							
Storage Time	(I_C = 5.0 Adc, I_B = 1.0 Adc, V_{CC} = 60 Vdc, $V_{BE(off)}$ = 4.0 Vdc, Pulse Width = 8.0 μs, Duty Cycle ≤ 2%) See Table 1	T_J = 25°C	t_s	—	550	1200	ns
Fall Time			t_f	—	100	300	
Storage Time		T_J = 100°C	t_s	—	750	1600	
Fall Time			t_f	—	180	500	
Inductive Switching, Series Base Inductance							
Fall Time (I_C = 5.0 Adc, I_B = 1.0 Adc, L_B = 24 μH) See Table 2			t_f	—	300	—	ns
MJ12022							
Inductive Switching, Clamped Drive							
Storage Time	(I_C = 10 Adc, I_B = 2.0 Adc, V_{CC} = 120 Vdc, $V_{BE(off)}$ = 4.0 Vdc, Pulse Width = 8.0 μs, Duty Cycle ≤ 2%) See Table 1	T_J = 25°C	t_s	—	820	1800	ns
Fall Time			t_f	—	100	300	
Storage Time		T_J = 100°C	t_s	—	1100	2500	
Fall Time			t_f	—	130	400	
Inductive Switching, Series Base Inductance							
Fall Time (I_C = 10 Adc, I_B = 2.0 Adc, L_B = 24 μH) See Table 2			t_f	—	350	—	ns

TYPICAL ELECTRICAL CHARACTERISTICS

MJ12020

FIGURE 1 — DC CURRENT GAIN

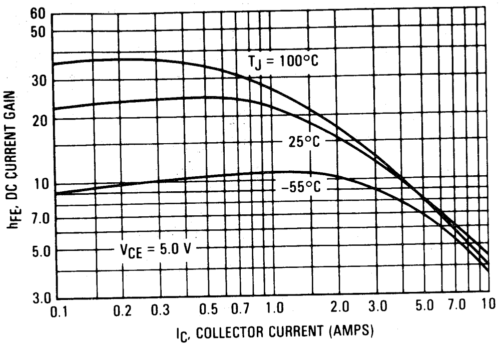
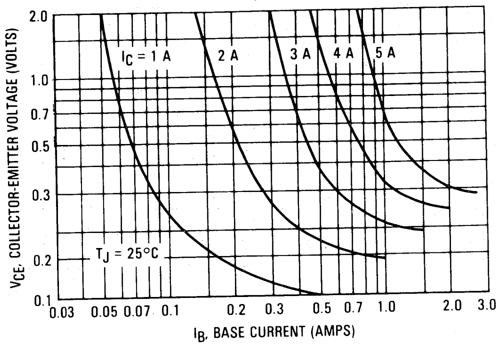


FIGURE 2 — COLLECTOR SATURATION REGION



MJ12021

FIGURE 3 — DC CURRENT GAIN

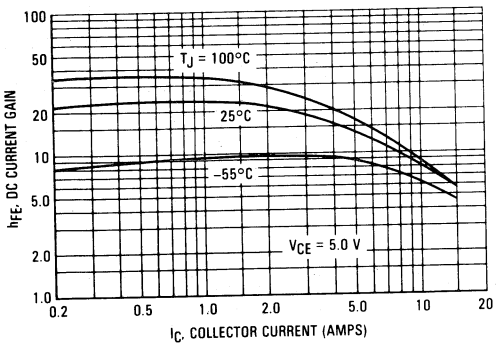
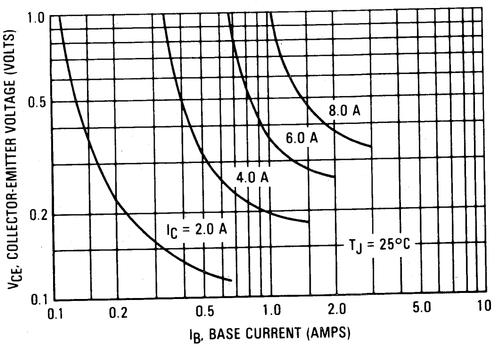


FIGURE 4 — COLLECTOR SATURATION REGION



MJ12022

FIGURE 5 — DC CURRENT GAIN

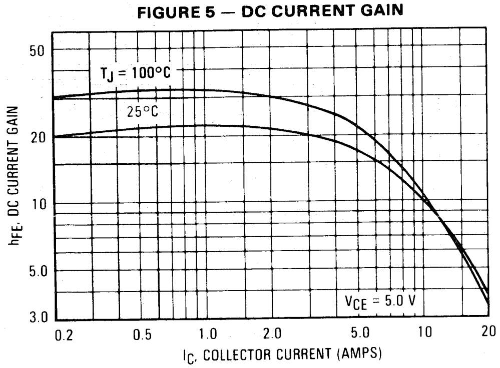
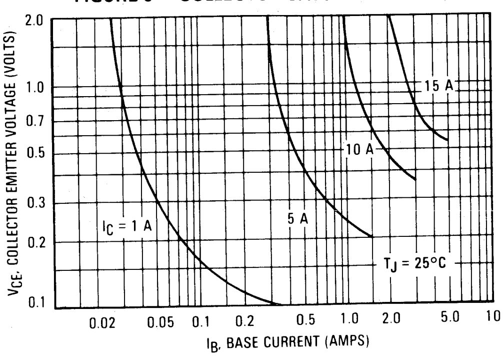


FIGURE 6 — COLLECTOR SATURATION REGION



TYPICAL ELECTRICAL CHARACTERISTICS

MJ12020

FIGURE 7 — COLLECTOR-EMITTER SATURATION VOLTAGE

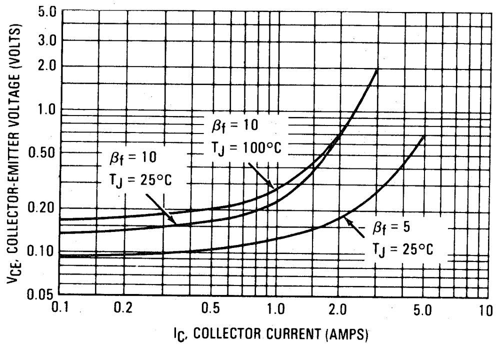
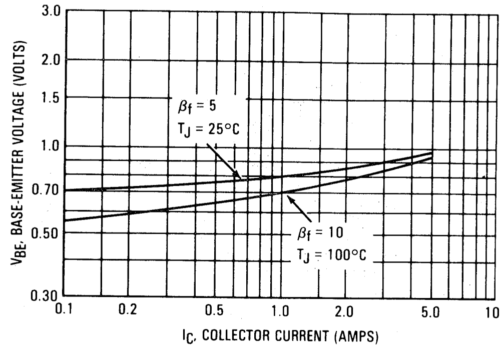


FIGURE 8 — BASE-EMITTER VOLTAGE



MJ12021

FIGURE 9 — COLLECTOR-EMITTER SATURATION VOLTAGE

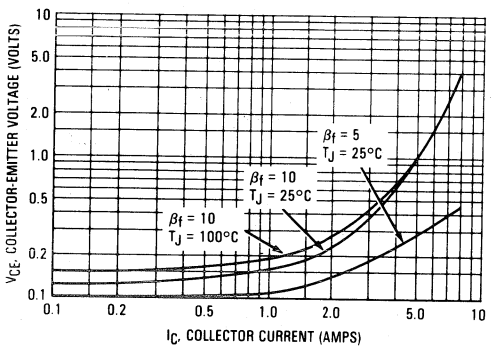
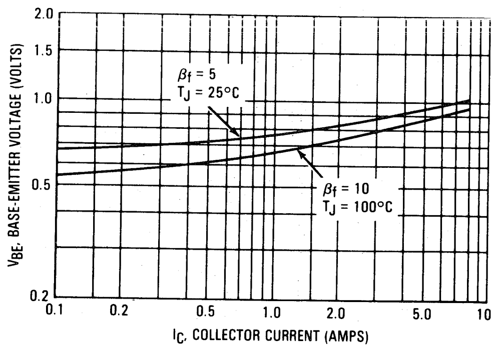


FIGURE 10 — BASE-EMITTER VOLTAGE



MJ12022

FIGURE 11 — COLLECTOR-EMITTER SATURATION VOLTAGE

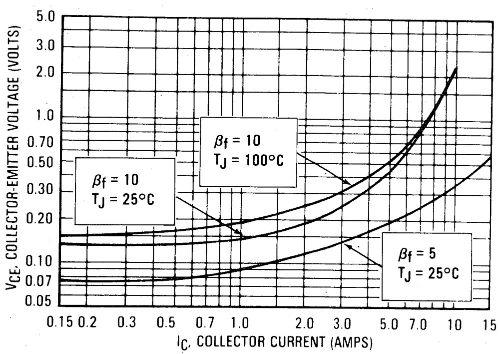
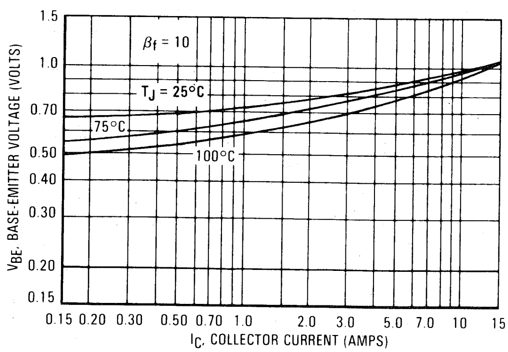


FIGURE 12 — BASE-EMITTER VOLTAGE



3

TYPICAL DYNAMIC CHARACTERISTICS

MJ12020

FIGURE 13 — STORAGE TIME

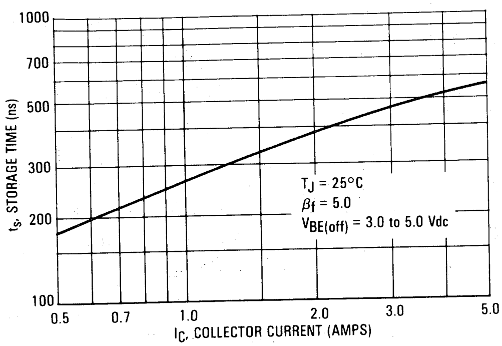
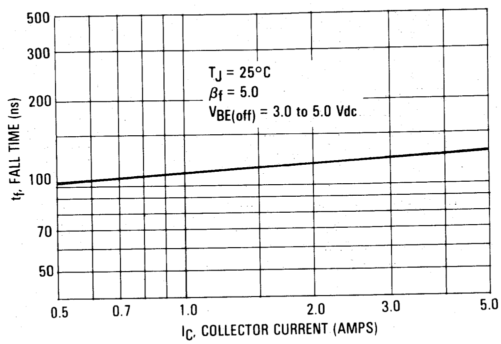


FIGURE 14 — FALL TIME



MJ12021

FIGURE 15 — STORAGE TIME

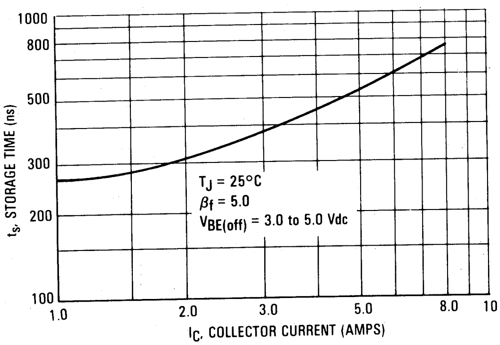
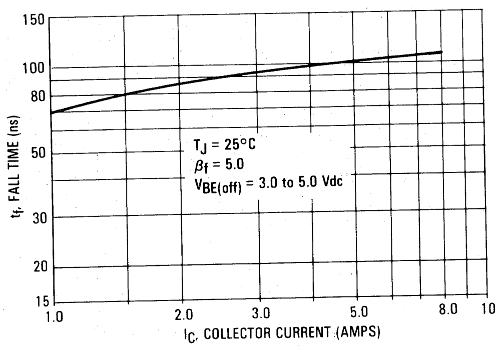


FIGURE 16 — FALL TIME



MJ12022

FIGURE 17 — STORAGE TIME

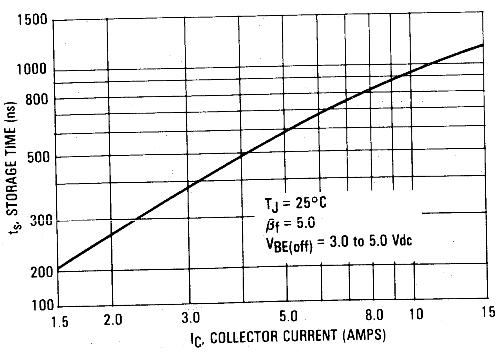
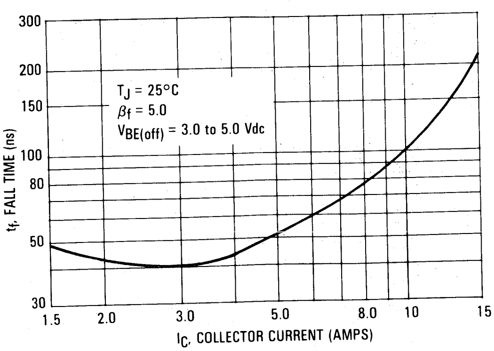


FIGURE 18 — FALL TIME



SAFE OPERATING AREA INFORMATION

MJ12020

FIGURE 19 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

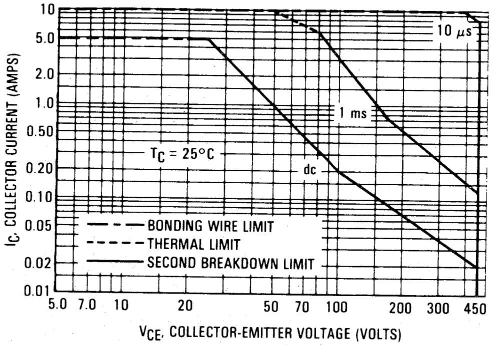
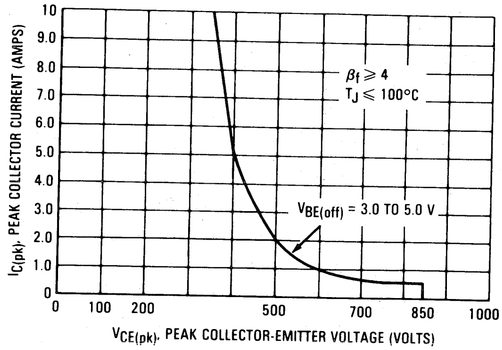


FIGURE 20 — MAXIMUM RATED TURN-OFF SAFE OPERATING AREA



MJ12021

FIGURE 21 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

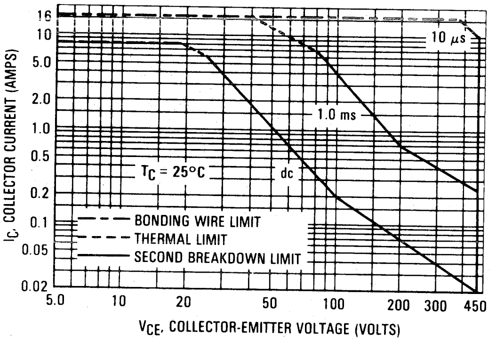
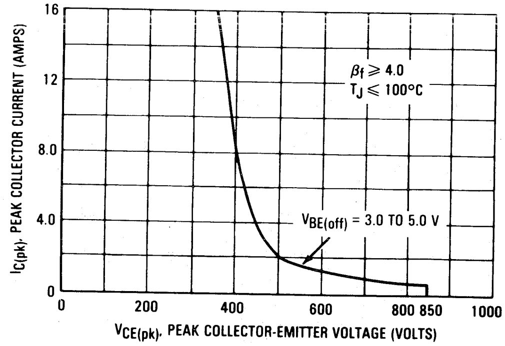


FIGURE 22 — MAXIMUM RATED TURN-OFF SAFE OPERATING AREA



MJ12022

FIGURE 23 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

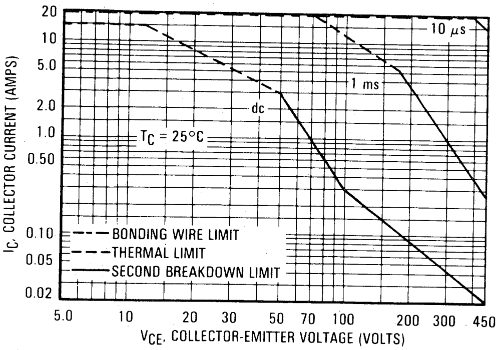
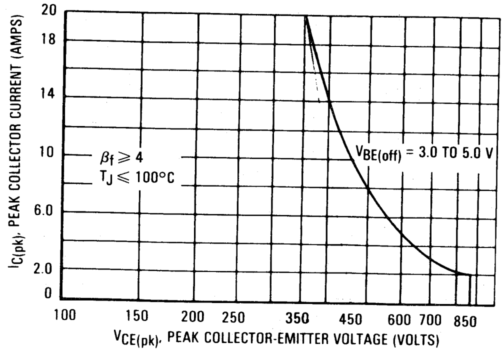


FIGURE 24 — MAXIMUM RATED TURN-OFF SAFE OPERATING AREA



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SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 19, 21 and 23 are based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 19, 21 and 23 may be found at any case temperature by using the appropriate curve on Figure 28.

$T_{J(pk)}$ may be calculated from the data in Figures 29, 30 or 31. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TURN-OFF

In deflection circuits, high voltage and high current normally do not occur simultaneously during turn-off with the base-emitter reverse biased. The safe level of operating these devices is specified as the Turn-Off Safe Operating Area, and represents the area the lead line may traverse during reverse biased turn off. For reliable operation, all abnormal operating conditions should be checked for operation within this area.

FIGURE 25 — CAPACITANCE VARIATION
MJ12020

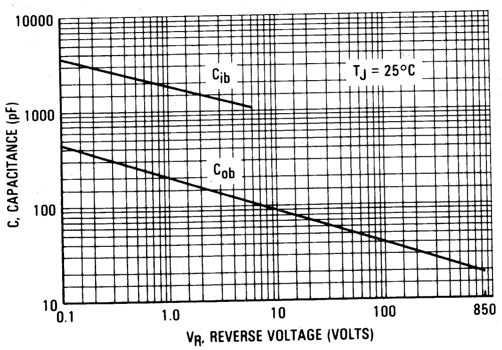


FIGURE 26 — CAPACITANCE VARIATION
MJ12021

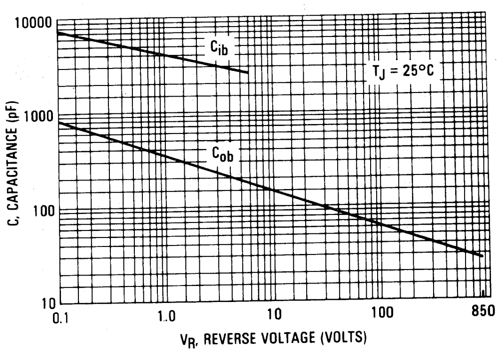


FIGURE 27 — CAPACITANCE VARIATION
MJ12022

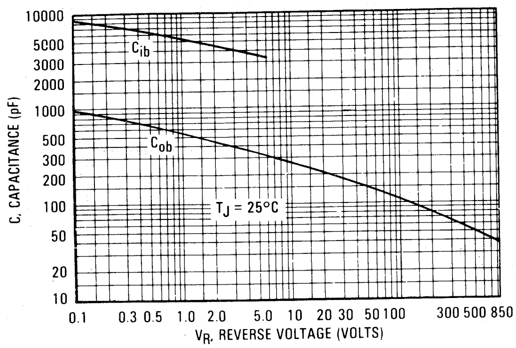
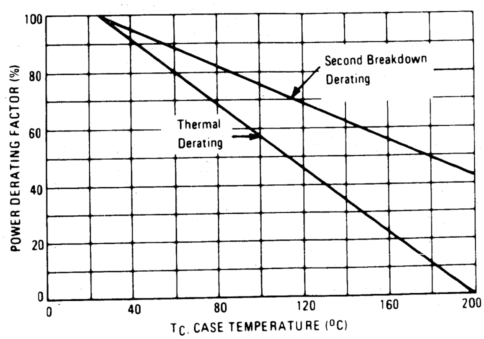


FIGURE 28 — POWER DERATING



3

THERMAL RESPONSE

FIGURE 29 — MJ12020

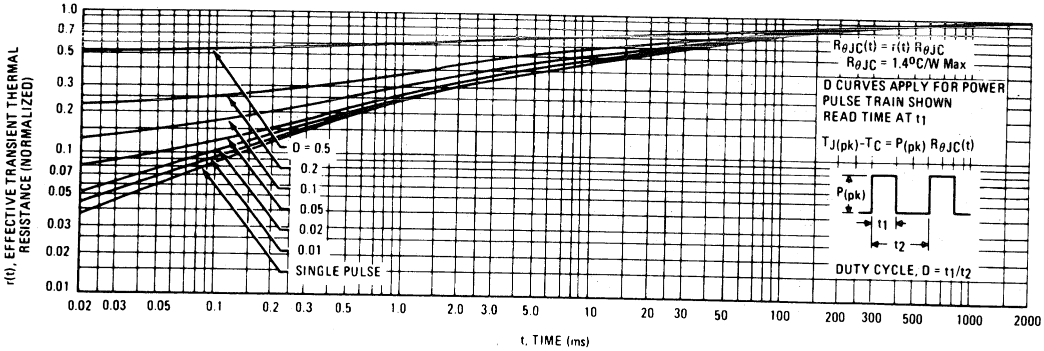


FIGURE 30 — MJ12021

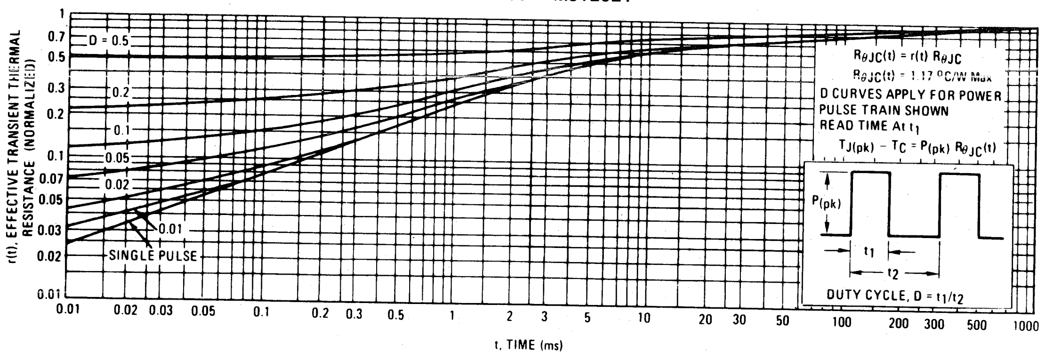


FIGURE 31 — MJ12022

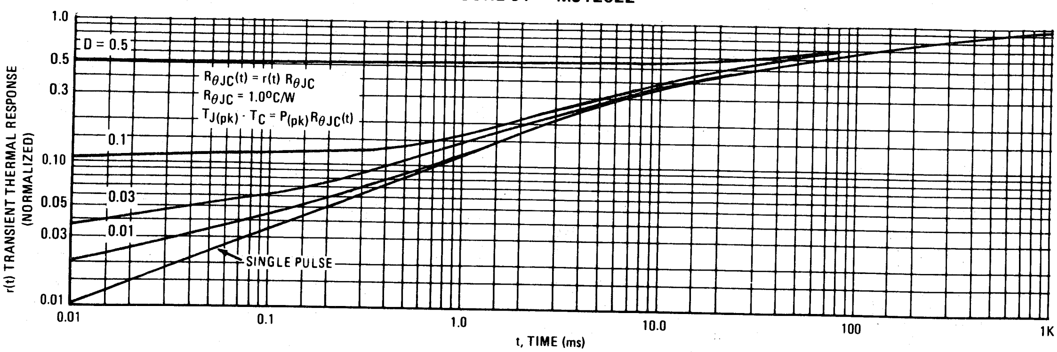
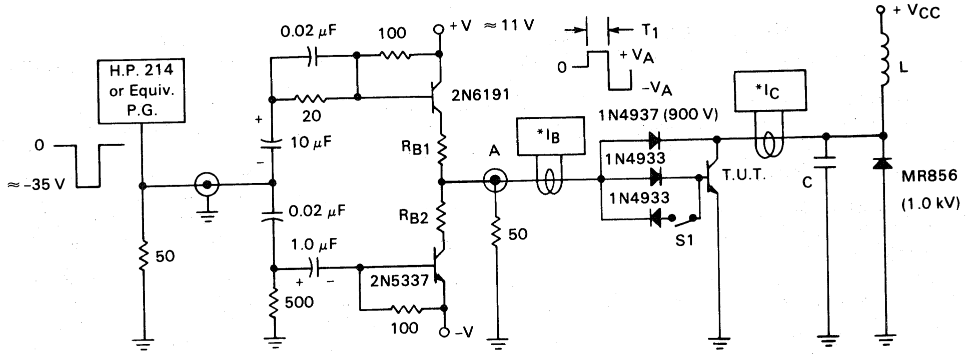


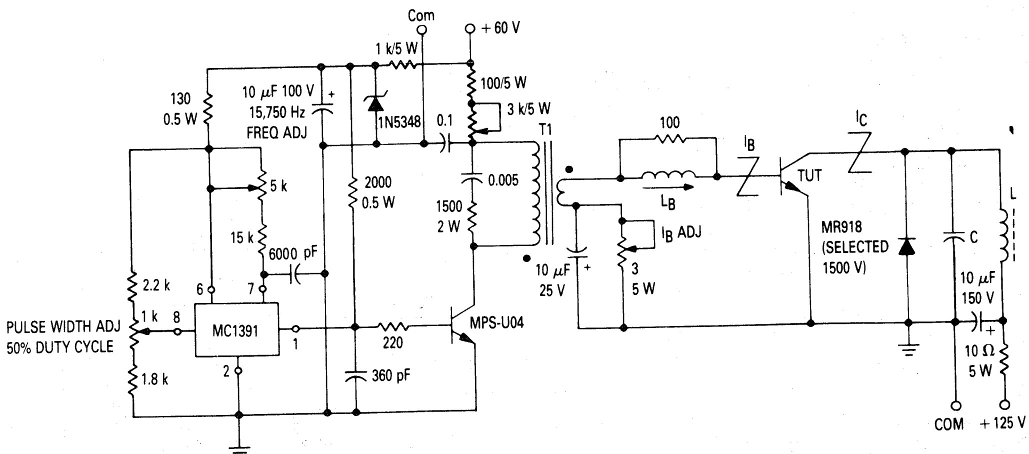
TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



T_1 adjusted to obtain $I_{C(pk)}$
$-V_A$ adjusted to obtain $V_{BE(off)}$

$V_{CEO(sus)}$	Inductive Switching, Clamped Drive			Turn-Off SOA		
	MJ12020	MJ12021	MJ12022	MJ12020	MJ12021	MJ12022
L = 10 mH $R_{B2} = \infty$ V_{CC} = 20 Vdc S1 — Open *Tektronix P-6042 or Equivalent	C = 0.003 µF V_{CC} = 40 Vdc	C = 0.020 µF V_{CC} = 60 Vdc	C = 0.036 µF V_{CC} = 120 Vdc	C = 0.003 µF V_{CC} = 20 Vdc	C = 0.020 µF V_{CC} = 35 Vdc	C = 0.037 µF V_{CC} = 55 Vdc
	L = 100 µH, S1 — Closed R_{B2} = 0, R_{B1} selected for required I_{B1} Scope — Tektronix 7403 or Equivalent			L = 100 µH R_{B2} = 0, R_{B1} selected for required I_{B1} S1 — Closed		

TABLE 2 — TEST CIRCUIT FOR INDUCTIVE SWITCHING WITH BASE INDUCTANCE



Device	V_{CC} (Volts)	$I_{C(pk)}$ (Amp)	C (µF)
MJ12020	20	3.0	0.003
MJ12021	35	5.0	0.;020
MJ12022	55	10	0.036

DRIVER TRANSFORMER (T1)

- Ferrox cube pot core #4229P-L00-3C8
- Adjust gap for primary inductance Lp = 70 mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than 3 µH
- Use 3 mil mylar tape between each winding layer

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

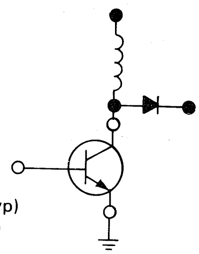
MJ13014
MJ13015

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ13014 and MJ13015 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn - Off Times:
- 60 ns Inductive Fall Time @ 25°C (Typ)
- 120 ns Inductive Crossover Time @ 25°C (Typ)
- 800 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

10 AMPERE

NPN SILICON POWER TRANSISTORS

350 AND 400 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

3

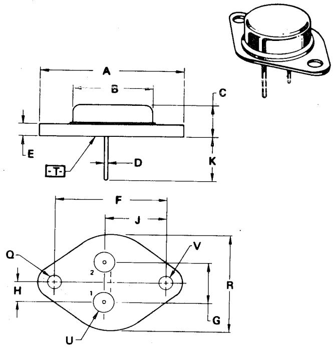
MAXIMUM RATINGS

Rating	Symbol	MJ13014	MJ13015	Unit
Collector-Emitter Voltage	V_{CEO}	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	550	600	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	10		Adc
— Peak (1)	I_{CM}	20		
Base Current — Continuous	I_B	5.0		Adc
— Peak (1)	I_{BM}	10		
Total Power Dissipation @ $T_C = 25°C$	P_D	150		Watts
@ $T_C = 100°C$		85.5		
Derate above 25°C		0.86		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅0.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100$ mA, $I_B = 0$) MJ13014	$V_{CEO(sus)}$	350	–	–	Vdc
MJ13015		400	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc)	I_{CEV}	–	–	0.5	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)} = 1.5$ Vdc, $T_C = 150°C$)		–	–	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $R_{BE} = 50\ \Omega$, $T_C = 100°C$)	I_{CER}	–	–	3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0$ Vdc, $I_C = 0$)	I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 2.5$ Adc, $V_{CE} = 5$ Vdc)	h_{FE}	12	–	40	–
Collector-Emitter Saturation Voltage ($I_C = 5$ Adc, $I_B = 1.0$ Adc)	$V_{CE(sat)}$	–	–	1.4	Vdc
($I_C = 10$ Adc, $I_B = 2.0$ Adc)		–	–	5.0	
($I_C = 5$ Adc, $I_B = 1.0$ Adc, $T_C = 100°C$)		–	–	2.4	
Base-Emitter Saturation Voltage ($I_C = 5$ Adc, $I_B = 1.0$ Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
($I_C = 5$ Adc, $I_B = 1.0$ Adc, $T_C = 100°C$)		–	–	1.5	
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f_{test} = 1.0$ kHz)	C_{ob}	50	–	350	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — ($V_{CC} = 250$ Vdc, $I_C = 5.0$ A, $I_{B1} = 1.0$ A, $t_p = 25\ \mu s$, Duty Cycle ≤ 2%)	t_d	–	0.01	0.1	μs
Rise Time	t_r	–	0.085	0.5	μs
Storage Time — ($V_{CC} = 250$ Vdc, $I_C = 5.0$ A, $I_{B1} = 1.0$ A, $V_{BE(off)} = 5.0$ Vdc, $t_p = 25\ \mu s$, Duty Cycle ≤ 2%)	t_s	–	0.8	2.0	μs
Fall Time	t_f	–	0.095	0.5	μs
Inductive Load, Clamped (Table 1)					
Storage Time — ($I_C = 5$ A(pk), $V_{clamp} = 250$ Vdc, $I_{B1} = 1.0$ A, $V_{BE(off)} = 5$ Vdc, $T_C = 100°C$)	t_{sv}	–	1.5	3.5	μs
Crossover Time	t_c	–	0.25	1.0	μs
Fall Time	t_{fi}	–	0.12	–	μs
Storage Time — ($I_C = 5$ A (pk), $V_{clamp} = 250$ Vdc, $I_{B1} = 1.0$ A, $V_{BE(off)} = 5$ Vdc, $T_C = 25°C$)	t_{sv}	–	0.8	–	μs
Crossover Time	t_c	–	0.12	–	μs
Fall Time	t_{fi}	–	0.06	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

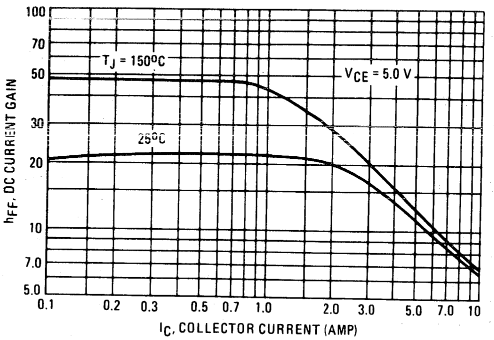


FIGURE 2 — COLLECTOR SATURATION REGION

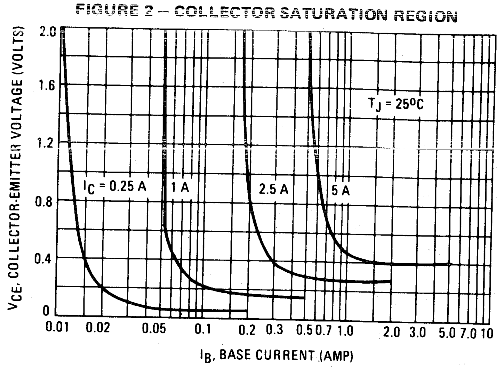


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

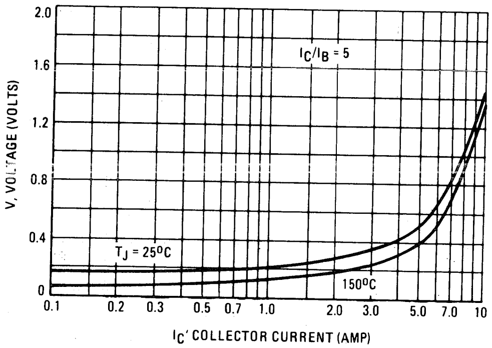


FIGURE 4 — BASE-EMITTER VOLTAGE

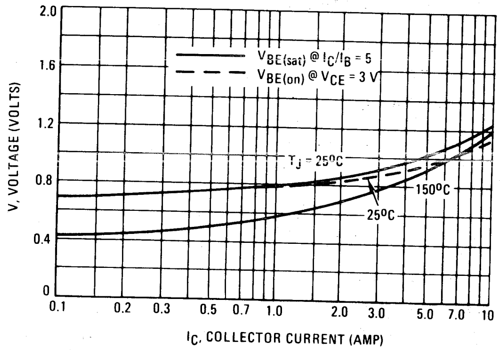


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FIGURE 5 — COLLECTOR CUTOFF REGION

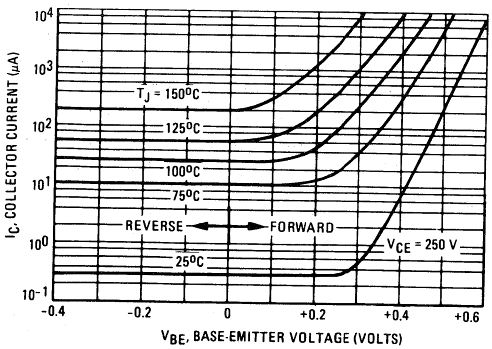


FIGURE 6 — CAPACITANCE

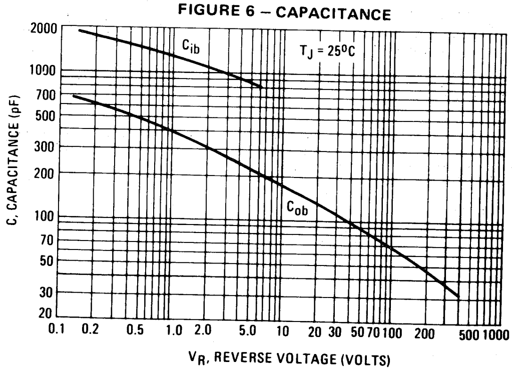
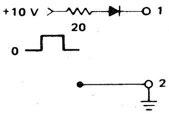
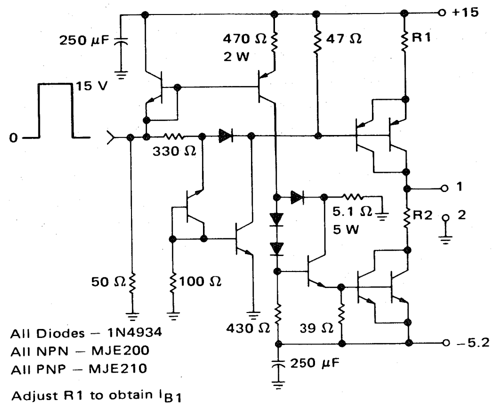
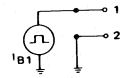


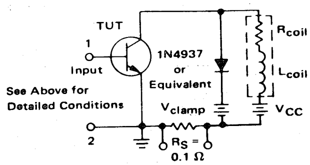
TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

<table>
<tr><th></th><th>$V_{CEO(sus)}$</th><th>RBSOA AND INDUCTIVE SWITCHING</th><th>RESISTIVE SWITCHING</th></tr>
<tr><td>INPUT CONDITIONS</td>
<td>

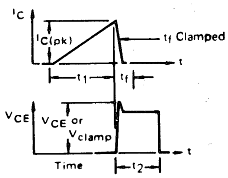
PW Varied to Attain I_C = 100 mA</td>
<td>

All Diodes – 1N4934
All NPN – MJE200
All PNP – MJE210

Adjust R1 to obtain I_{B1}
For switching and RB_{SOA}, R2 = 0
For $V_{CEO(sus)}$, R2 = ∞</td>
<td>TURN-ON TIME


I_{B1} adjusted to obtain the forced h_{FE} desired
TURN-OFF TIME
Use inductive switching driver as the input to the resistive test circuit.</td></tr>
<tr><td>CIRCUIT VALUES</td>
<td>L_{coil} = 80 mH V_{CC} = 10 V
R_{coil} = 0.7 Ω</td>
<td>L_{coil} = 180 μH
R_{coil} = 0.05 Ω
V_{CC} = 20 V
V_{clamp} = 250 V
R_B adjusted to attain desired I_{B1}</td>
<td>V_{CC} = 250 V
R_L = 50 Ω
Pulse Width = 10 μs</td></tr>
<tr><td>TEST CIRCUITS</td>
<td colspan="2">INDUCTIVE TEST CIRCUIT


See Above for Detailed Conditions

OUTPUT WAVEFORMS


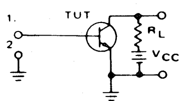
t_1 Adjusted to Obtain I_C
$t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$
$t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$
Test Equipment
Scope – Tektronix
475 or Equivalent</td>
<td>RESISTIVE TEST CIRCUIT

</td></tr>
</table>

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FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

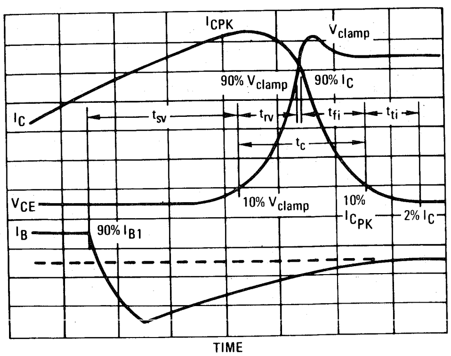
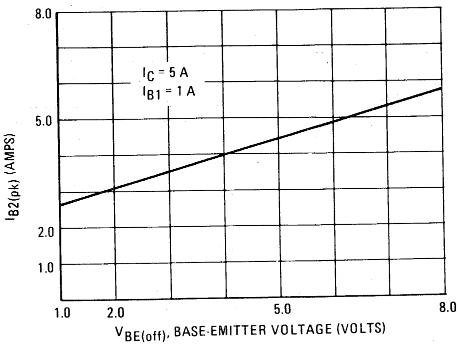


FIGURE 8 – PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

FIGURE 9 — TURN-ON SWITCHING TIMES

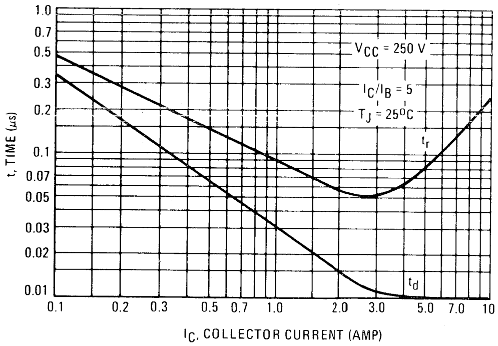


FIGURE 10 — TURN-OFF TIME

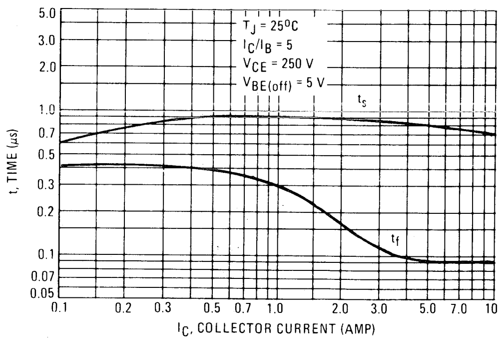


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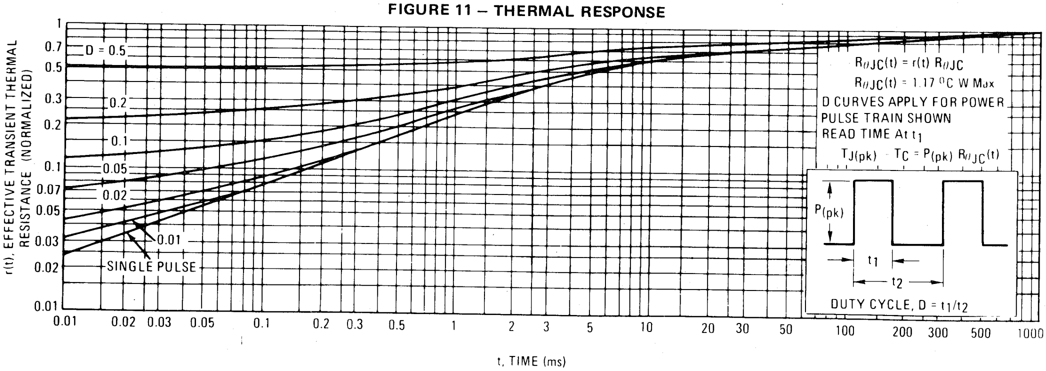
FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

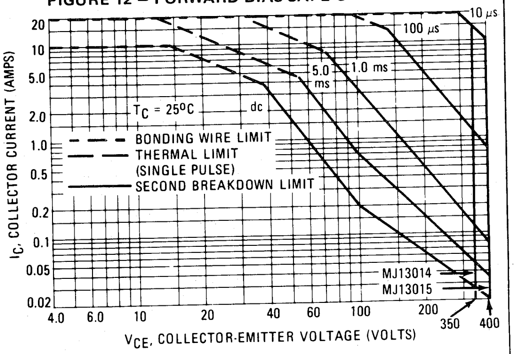
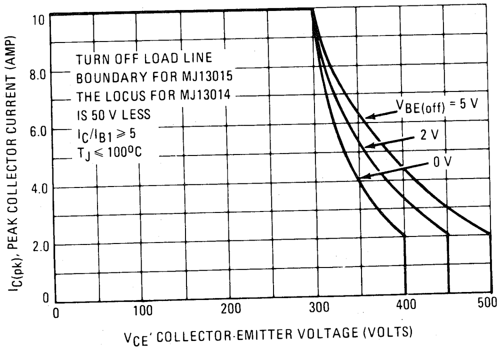


FIGURE 13 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

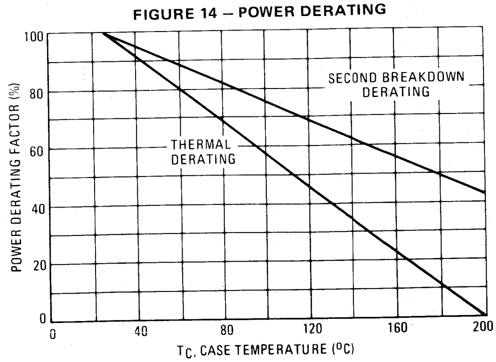
$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

3

FIGURE 14 – POWER DERATING



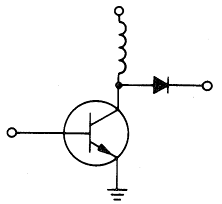
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ13070
MJ13071

Designer's Data Sheet

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The MJ13070 and MJ13071 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:



- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 100 ns Inductive Fall Time @ 25°C (Typ)
- 150 ns Inductive Crossover Time @ 25°C (Typ)
- 400 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range −65 to +200°C

100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

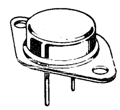
5 AMPERE

NPN SILICON POWER TRANSISTORS

400 AND 450 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



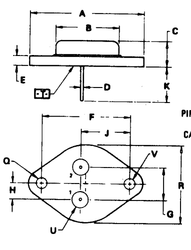
MAXIMUM RATINGS

Rating	Symbol	MJ13070	MJ13071	Unit
Collector-Emitter Voltage	V_{CEO}	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	750	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 8.0		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.0 4.0		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	125 71.5 0.714		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   | ⌖ | ⌀0.13 (0.005) Ⓜ | T | V Ⓜ |
   FOR LEADS:
   | ⌖ | ⌀0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ13070	$V_{CEO(sus)}$	400	—	—	Vdc
MJ13071		450	—	—	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.5	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 5.0 Vdc	h_{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)	$V_{CE(sat)}$	—	—	1.0	Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)		—	—	3.0	
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		—	—	2.0	
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	250	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	(V_{CC} = 250 Adc, I_C = 3.0 Adc, I_{B1} = 0.4 Adc, t_p = 30 μs, Duty Cycle ≤2%, $V_{BE(off)}$ = 5.0 Vdc)	t_d	—	0.03	0.05	μs
Rise Time		t_r	—	0.10	0.40	
Storage Time		t_s	—	0.40	1.50	
Fall Time		t_f	—	0.175	0.50	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)}$ = 3.0 A, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V)	(T_J = 100°C)	t_{sv}	—	0.70	2.0	μs
Crossover Time			t_c	—	0.28	0.50	
Fall Time			t_{fi}	—	0.15	0.30	
Storage Time		(T_J = 25°C)	t_{sv}	—	0.40	—	
Crossover Time			t_c	—	0.15	—	
Fall Time			t_{fi}	—	0.10	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$\beta_f = \frac{I_C}{I_B}$

3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

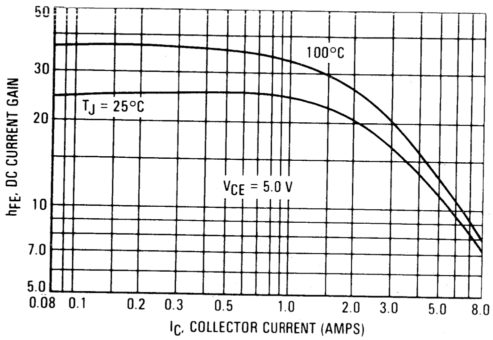


FIGURE 2 — COLLECTOR SATURATION REGION

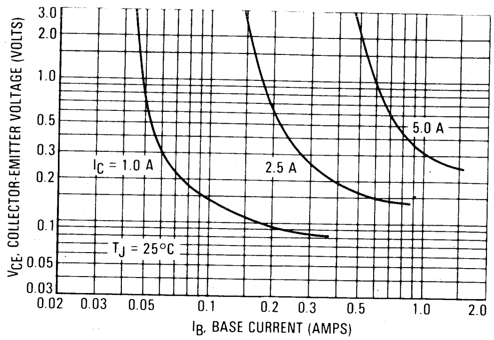


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

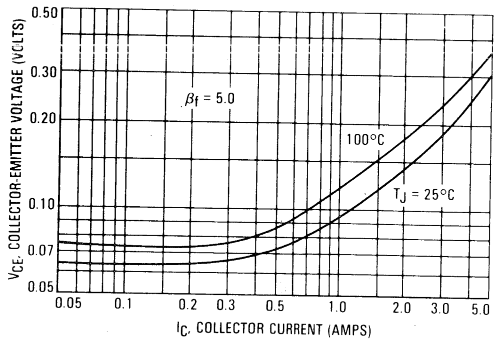


FIGURE 4 — BASE-EMITTER VOLTAGE

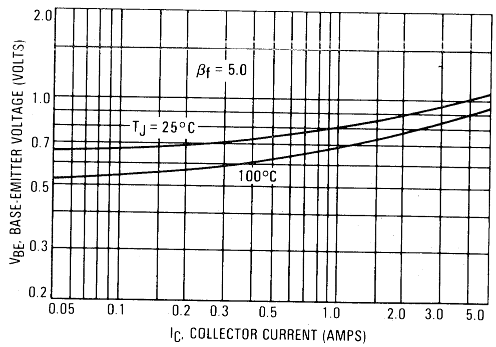


FIGURE 5 — COLLECTOR CUTOFF REGION

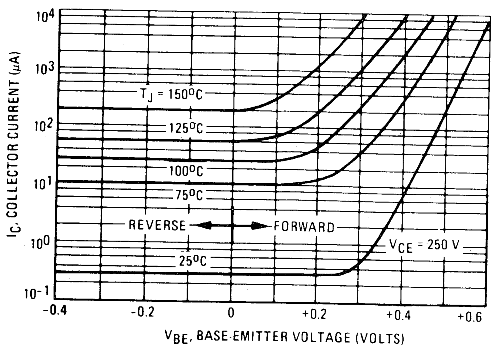


FIGURE 6 — CAPACITANCE

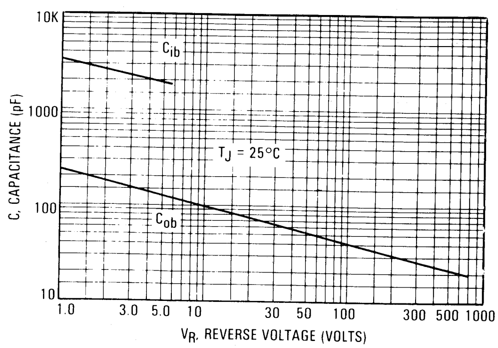


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TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

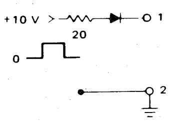
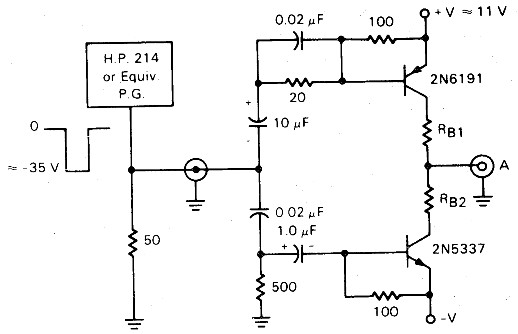
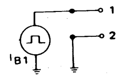
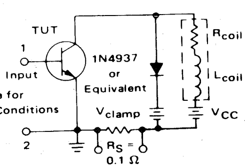
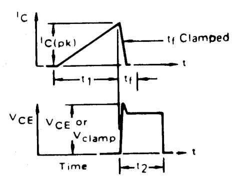
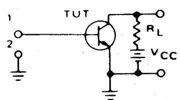
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $V_{CEO(sus)}$, R2 = ∞	TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT See Above for Detailed Conditions 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

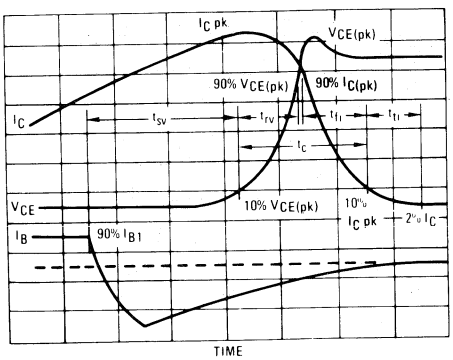
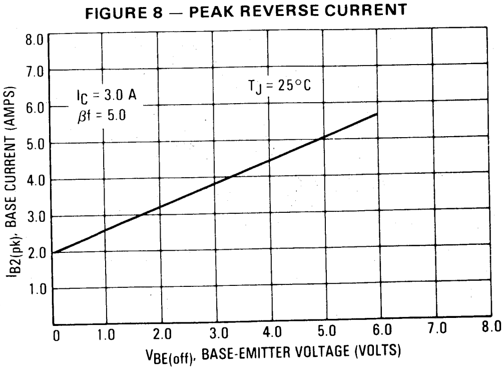


FIGURE 8 — PEAK REVERSE CURRENT



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SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

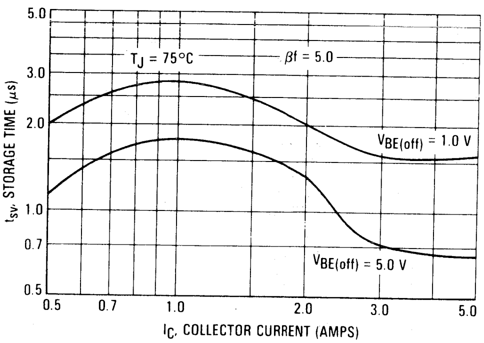


FIGURE 10 — CROSSOVER AND FALL TIMES

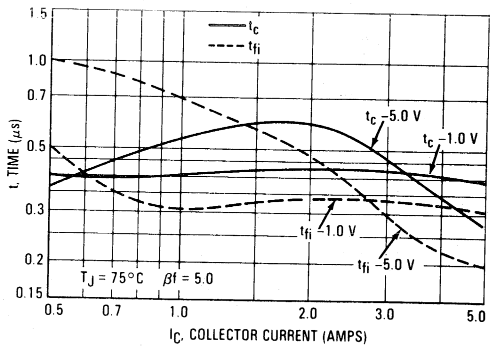
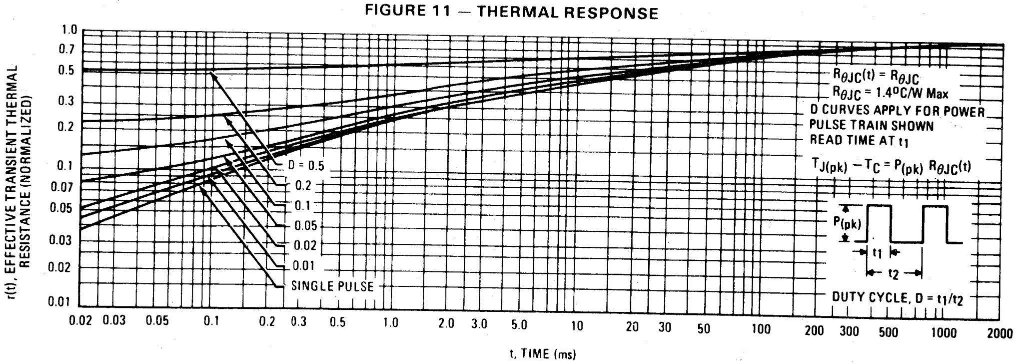


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

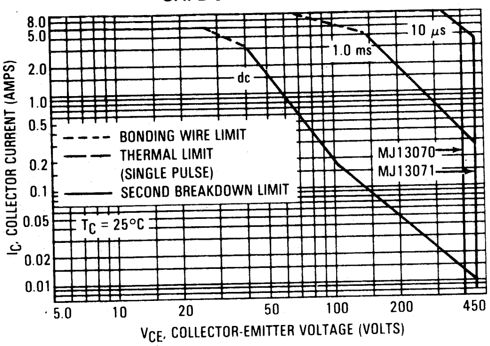
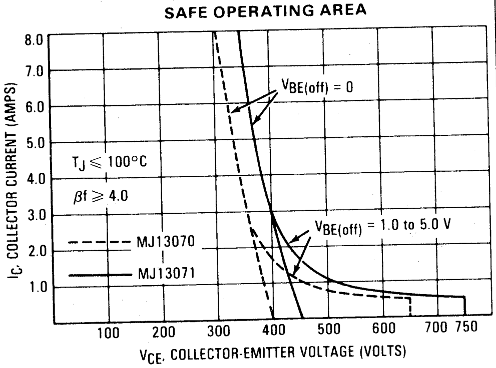


FIGURE 13 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

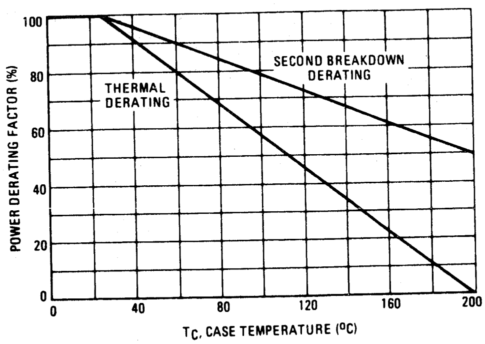
The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 14 — POWER DERATING



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

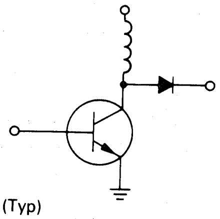
MJ13080
MJ13081

Designer's Data Sheet

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The MJ13080 and MJ13081 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
- 100 ns Inductive Fall Time @ 25°C (Typ)
- 150 ns Inductive Crossover Time @ 25°C (Typ)
- 400 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range −65 to +200°C

100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

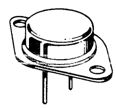
8 AMPERE

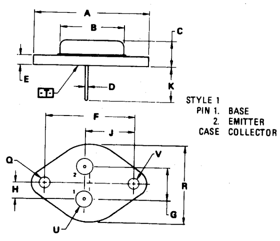
NPN SILICON POWER TRANSISTORS

400 AND 450 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.





NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [-T-] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   | ⌖ | ⌀.13 (0.005) Ⓜ | T | V Ⓜ |

   FOR LEADS:
   | ⌖ | ⌀.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MJ13080	MJ13081	Unit
Collector-Emitter Voltage	V_{CEO}	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	750	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8.0 12		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	3.0 6.0		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	150 85.5 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ13080 / MJ13081	$V_{CEO(sus)}$	400 / 450	— / —	— / —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) / (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— / —	— / —	0.5 / 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc	h_{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc) / (I_C = 8.0 Adc, I_B = 1.6 Adc) / (I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	— / — / —	— / — / —	1.0 / 3.0 / 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc) / (I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	— / —	— / —	1.5 / 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	300	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	(V_{CC} = 250 Vdc, I_C = 5.0 Adc, I_{B1} = 0.7 Adc, t_p = 30 μs, Duty Cycle ≤2%, $V_{BE(off)}$ = 5.0 Vdc)	t_d	—	0.025	0.05	μs
Rise Time		t_r	—	0.10	0.50	
Storage Time		t_s	—	0.50	1.50	
Fall Time		t_f	—	0.15	0.50	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)}$ = 5.0 A, I_{B1} = 0.7 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V)	(T_J = 100°C)	t_{sv}	—	0.75	2.20	μs
Crossover Time			t_c	—	0.22	0.40	
Fall Time			t_{fi}	—	0.175	0.35	
Storage Time		(T_J = 25°C)	t_{sv}	—	0.40	—	
Crossover Time			t_c	—	0.15	—	
Fall Time			t_{fi}	—	0.10	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$\beta_f = \frac{I_C}{I_B}$

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TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

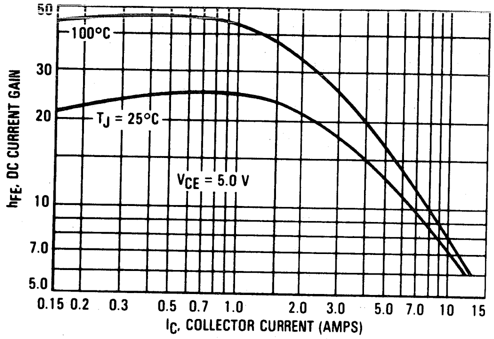

FIGURE 2 — COLLECTOR SATURATION REGION

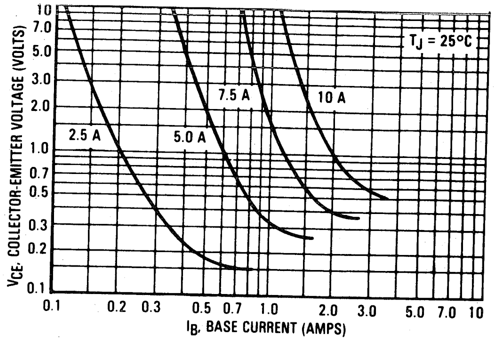

FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

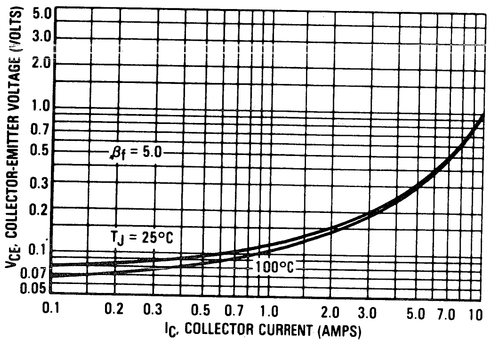

FIGURE 4 — BASE-EMITTER VOLTAGE

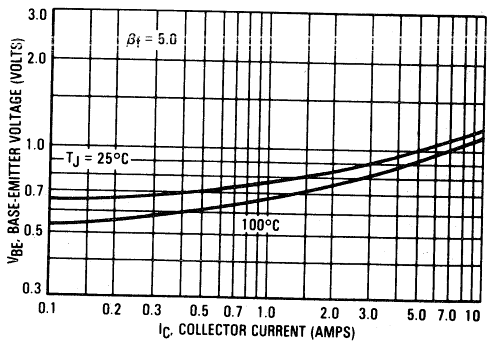

FIGURE 5 — COLLECTOR CUTOFF REGION

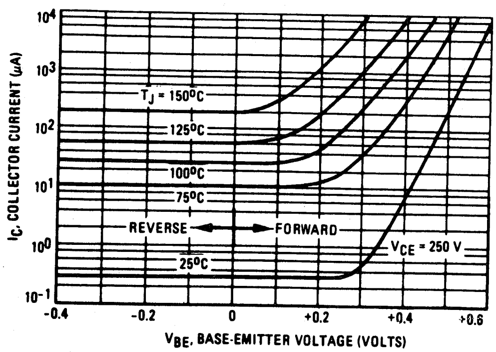

FIGURE 6 — CAPACITANCE

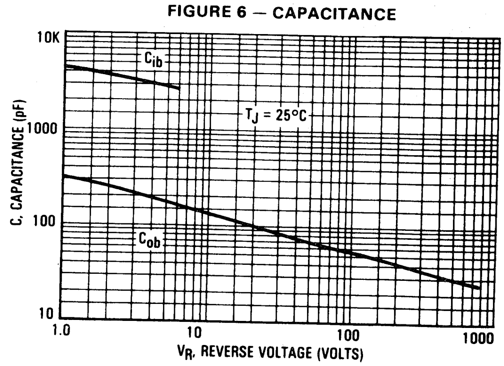

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TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

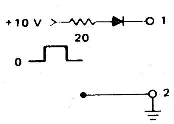
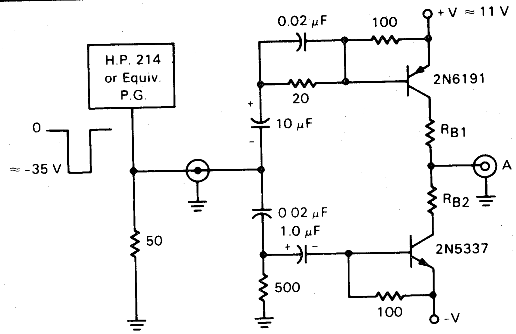
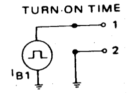
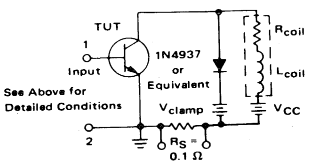
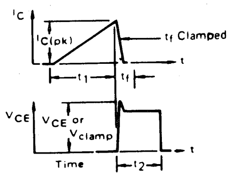
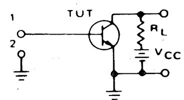
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $V_{CEO(sus)}$, R2 = ∞	TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 30 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

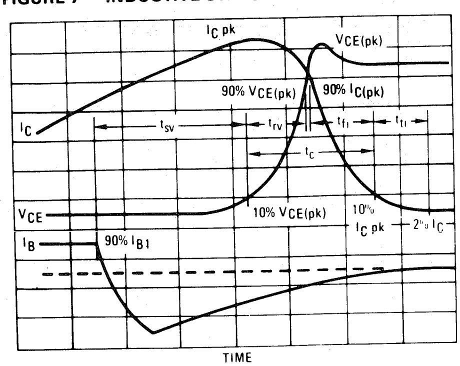
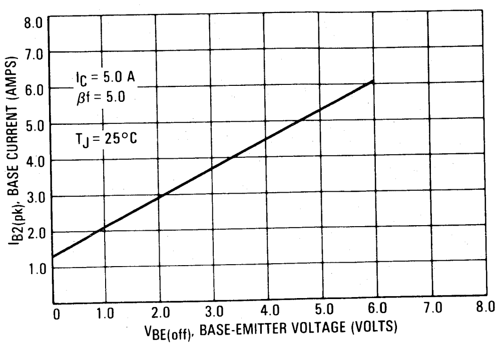


FIGURE 8 — PEAK REVERSE CURRENT



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SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

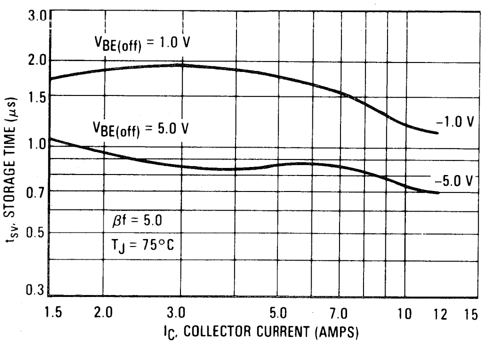


FIGURE 10 — CROSSOVER AND FALL TIMES

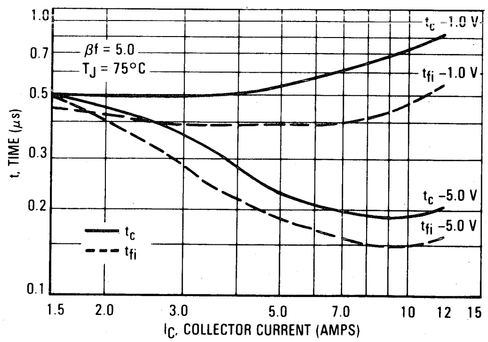
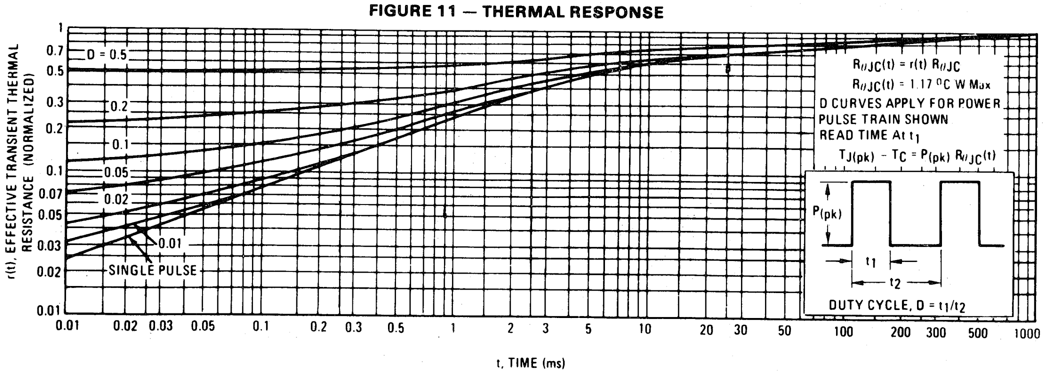


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

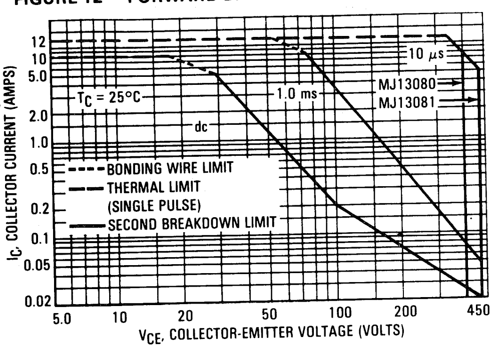
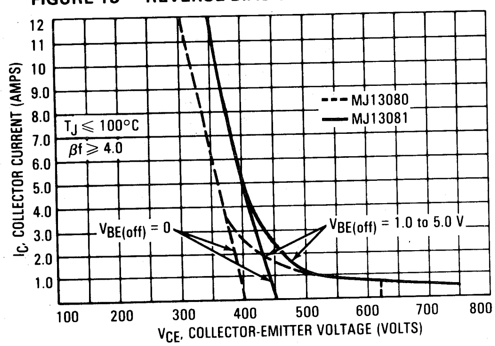


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

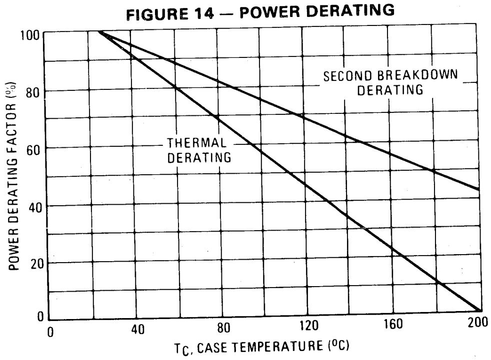
$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

3

FIGURE 14 — POWER DERATING



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

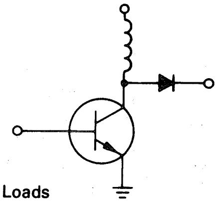
MJ13090 MJH13090
MJ13091 MJH13091

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads — 150 ns Inductive Fall Time (Typ)
- Saturation Voltages
- Leakage Currents

15 AMPERE

NPN SILICON POWER TRANSISTORS

400 AND 450 VOLTS
125 and 175 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJ13090	MJ13091	MJH13090	MJH13091	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	750	650	750	Vdc
Emitter-Base Voltage	V_{EB}	6.0				Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20				Adc
Base Current — Continous — Peak (1)	I_B I_{BM}	5.0 10				Adc
Total Device Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	175 100 1.0		125 50 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200		-55 to 150		°C

THERMAL CHARACTERISTICS

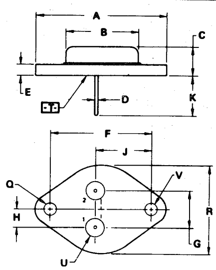
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds.	T_L	275	°C

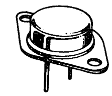
(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MJ13090
MJ13091





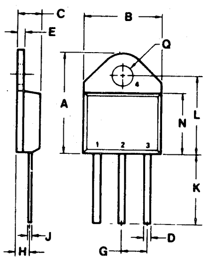
STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

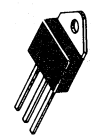
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ϕ0.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ϕ0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

CASE 1-05
TO-204AA

MJH13090
MJH13091





1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ13090, MJH13090 / MJ13091, MJH13091	$V_{CEO(sus)}$	400 450	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) / (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	— —	0.5 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figures 12 and 13			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 14			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) / (I_C = 15 Adc, I_B = 3.0 Adc) / (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	— — —	1.0 3.0 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) / (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	350	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 Adc, I_{B1} = 1.25 Adc, t_p = 30 μs, Duty Cycle ≤2%, $V_{BE(off)}$ = 5.0 Vdc)		t_d	—	0.03	0.05	μs
Rise Time			t_r	—	0.13	0.50	
Storage Time			t_s	—	0.55	2.50	
Fall Time			t_f	—	0.10	0.50	
Inductive Load, Clamped (Table 1)							
Storage Time	($I_{C(pk)}$ = 10 A, I_{B1} = 1.25 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V)	(T_J = 100°C)	t_{sv}	—	0.80	3.00	μs
Crossover Time			t_c	—	0.175	0.40	
Fall Time			t_{fi}	—	0.15	0.30	
Storage Time		(T_J = 25°C)	t_{sv}	—	0.50	—	
Crossover Time			t_c	—	0.15	—	
Fall Time			t_{fi}	—	0.10	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

$*\beta_f = \frac{I_C}{I_B}$

3

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

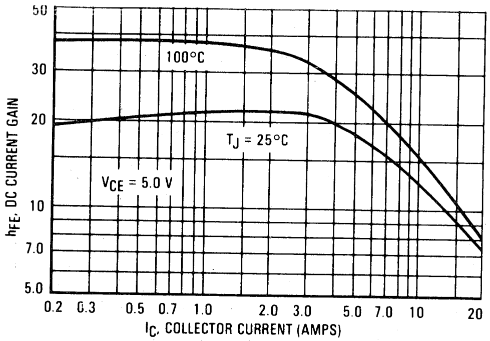


FIGURE 2 — COLLECTOR SATURATION REGION

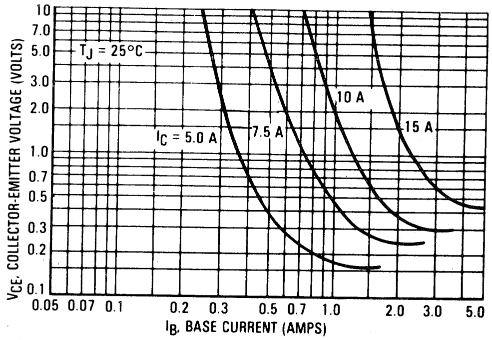


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

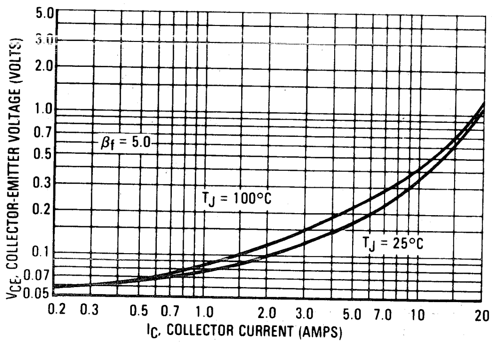


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

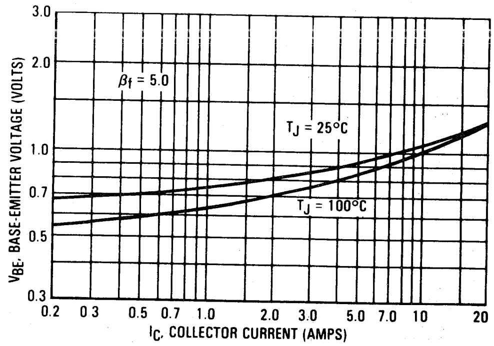


FIGURE 5 — COLLECTOR CUTOFF REGION

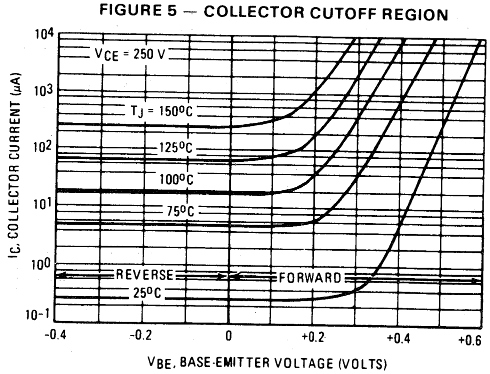


FIGURE 6 — CAPACITANCE

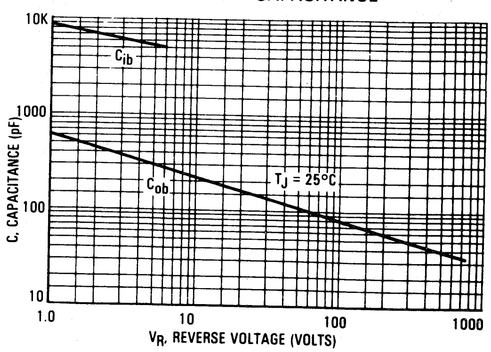


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

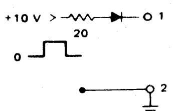
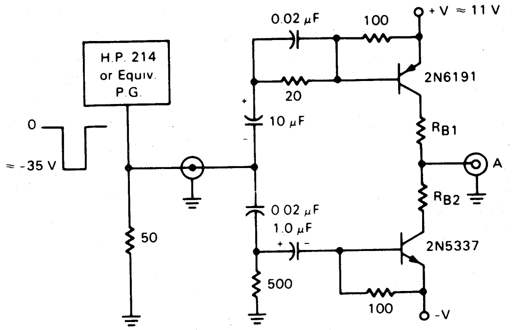
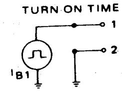
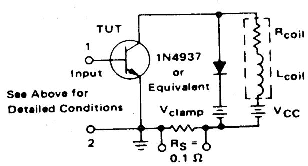
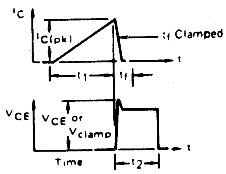
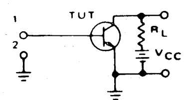
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Connect Point A to base of TUT Adjust −V to obtain desired $V_{BE(off)}$ at Point A Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $V_{CEO(sus)}$ R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_{B1} adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 30 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

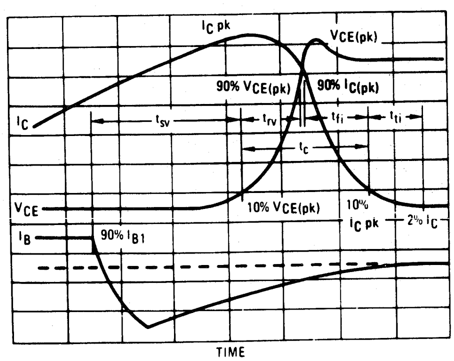
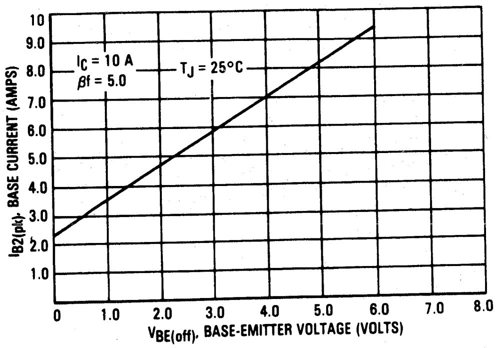


FIGURE 8 — PEAK REVERSE CURRENT



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In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

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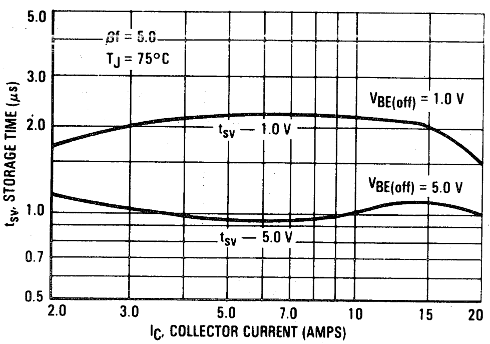
INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME



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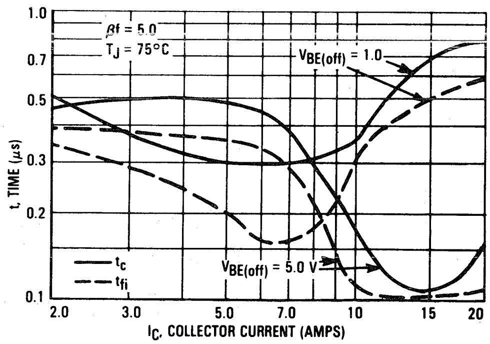

FIGURE 11 — THERMAL RESPONSE

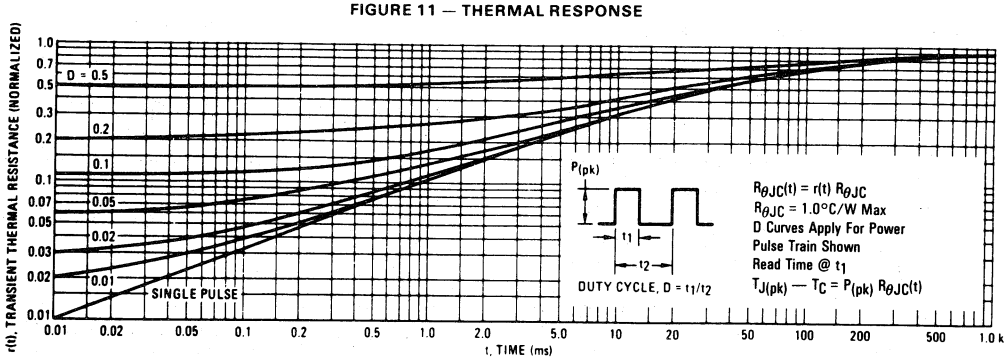

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FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA
MJ13090 and MJ13091

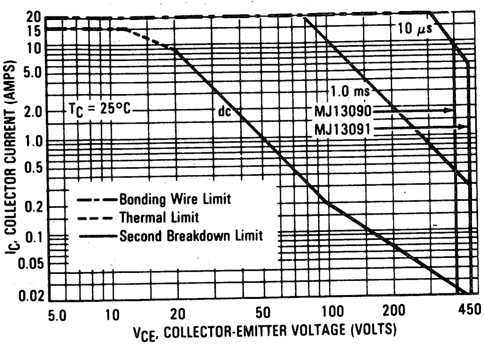
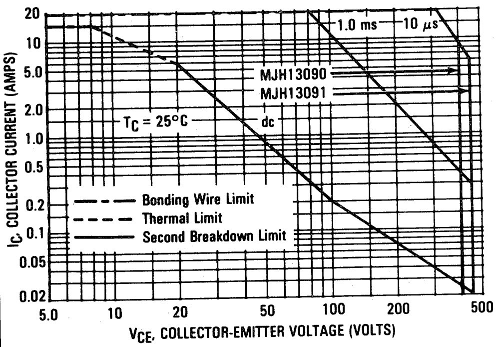


FIGURE 13 — FORWARD BIAS SAFE OPERATING AREA
MJH13090 and MJH13091



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

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$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives RBSOA characteristics.

3

FIGURE 14 — REVERSE BIAS SAFE OPERATING AREA

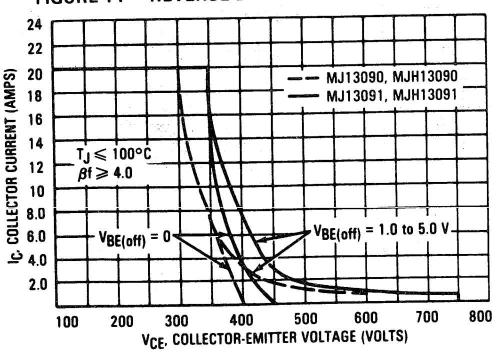
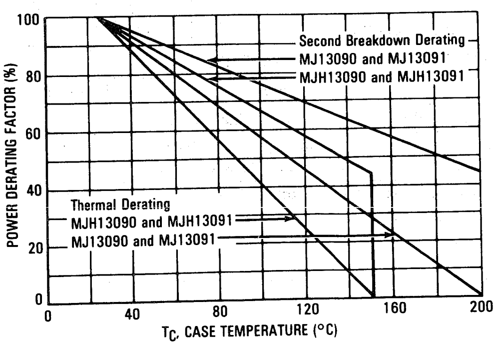


FIGURE 15 — POWER DERATING



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

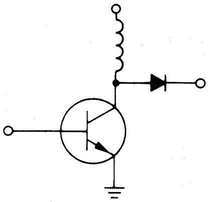
MJ13101

Designer's Data Sheet

SWITCHMODE II SERIES NPN SILICON POWER TRANSISTOR

The MJ13101 transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
- 30 ns Inductive Fall Time @ 25°C (Typ)
- 50 ns Inductive Crossover Time @ 25°C (Typ)
- 900 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

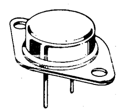
20 AMPERE

NPN SILICON POWER TRANSISTOR

450 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



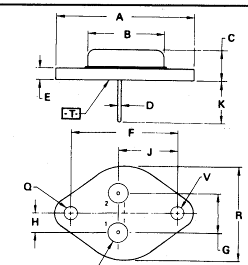
MAXIMUM RATINGS

Rating	Symbol	MJ13101	Unit
Collector-Emitter Voltage	V_{CEO}	450	Vdc
Collector-Emitter Voltage	V_{CEV}	750	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ⩽ 10%.



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [-T-] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅ 0.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅ 0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ13101	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.5	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 15 Adc, V_{CE} = 3.0 Vdc	h_{FE}	8.0	—	40	—
Collector-Emitter Saturation Voltage (I_C = 15 Adc, I_B = 3.0 Adc)	$V_{CE(sat)}$	—	—	1.0	Vdc
(I_C = 20 Adc, I_B = 4.0 Adc)		—	—	3.0	
(I_C = 15 Adc, I_B = 3.0 Adc, T_C = 100°C)		—	—	2.0	
Base-Emitter Saturation Voltage (I_C = 15 Adc, I_B = 3.0 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 15 Adc, I_B = 3.0 Adc, T_C = 100°C)		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	450	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	V_{CC} = 250 Vdc, I_C = 15 Adc, I_{B1} = 2.0 Adc, t_p = 30 μs, Duty Cycle ≤2%, $V_{BE(off)}$ = 5.0 Vdc)	t_d	—	0.02	0.05	μs
Rise Time		t_r	—	0.13	0.50	
Storage Time		t_s	—	0.90	3.5	
Fall Time		t_f	—	0.10	0.50	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	($I_{C(pk)}$ = 15 A, I_{B1} = 2.0 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V)	(T_J = 100°C)	t_{sv}	—	1.25	4.0	μs
Crossover Time			t_c	—	0.15	0.50	
Fall Time			t_{fi}	—	0.13	0.40	
Storage Time		(T_J = 25°C)	t_{sv}	—	0.90	—	
Crossover Time			t_c	—	0.05	—	
Fall Time			t_{fi}	—	0.03	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$*\beta_f = \frac{I_C}{I_B}$

3

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

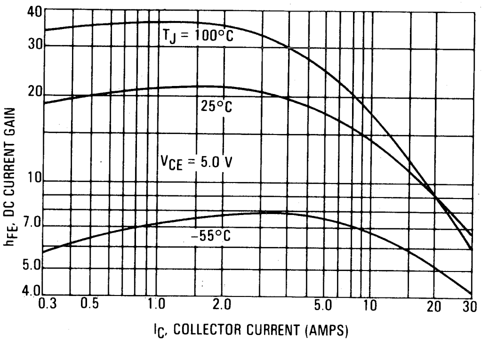


FIGURE 2 — COLLECTOR SATURATION REGION

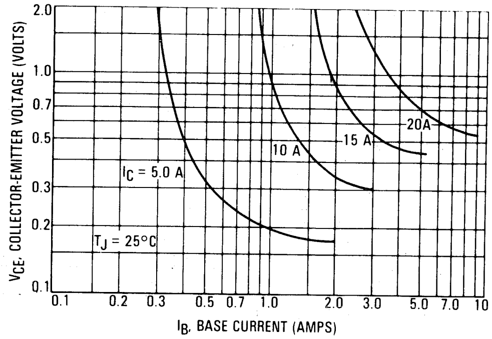


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

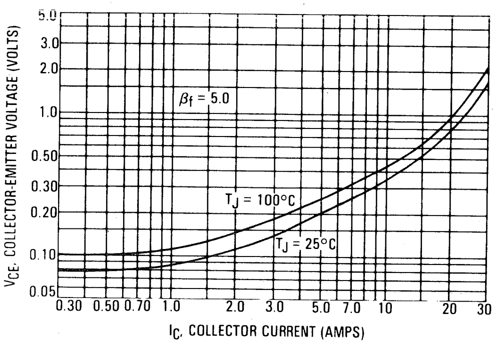


FIGURE 4 — BASE-EMITTER VOLTAGE

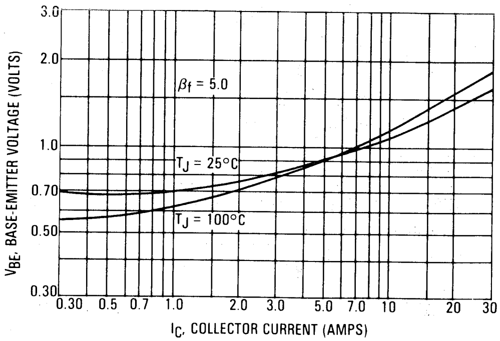


FIGURE 5 — COLLECTOR CUTOFF REGION

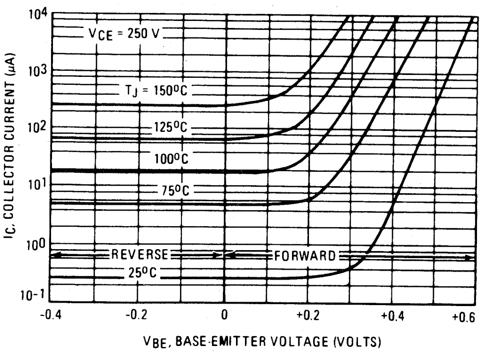


FIGURE 6 — CAPACITANCE

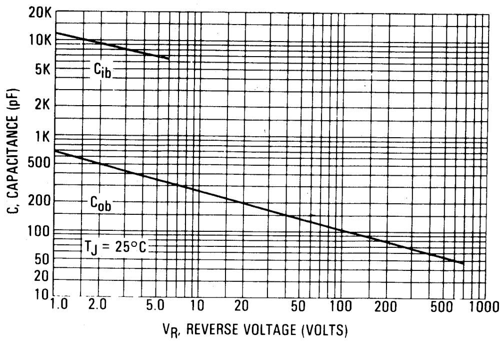


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TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

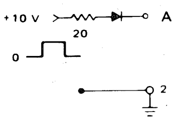
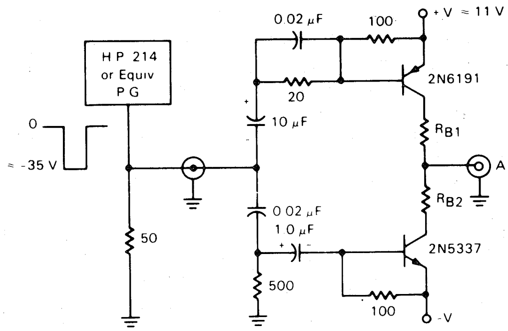
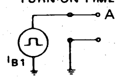
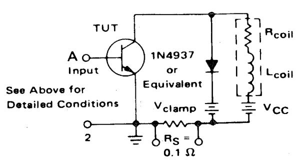
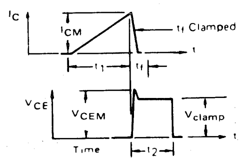
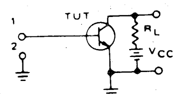
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $V_{CEO(sus)}$, R2 = ∞	TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 16.6 Ω Pulse Width = 30 μs
TEST CIRCUITS		INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

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FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

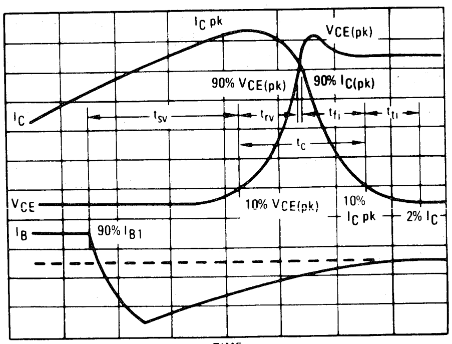
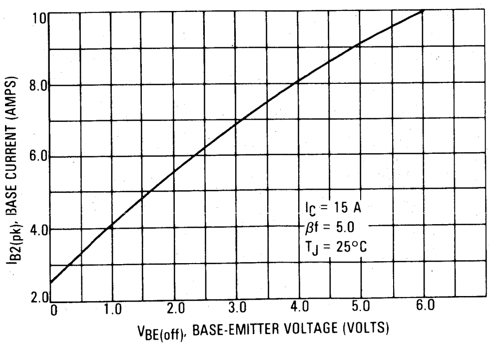


FIGURE 8 — PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

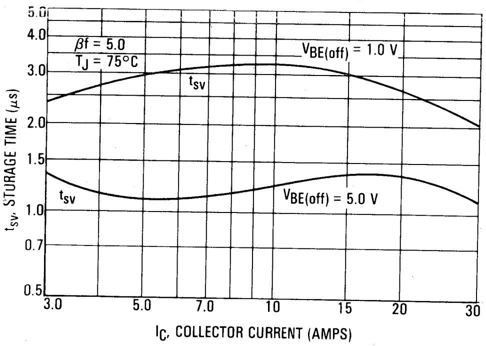


FIGURE 10 — CROSSOVER AND FALL TIMES

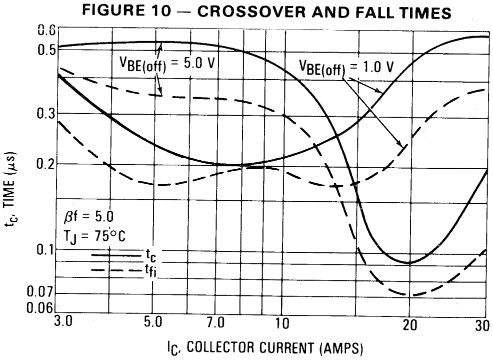
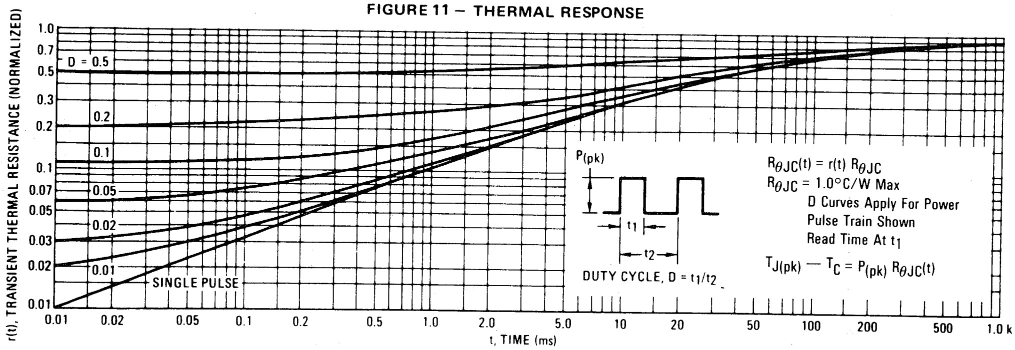


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in figure 12 and 13 are specified for these devices under the test conditions shown

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

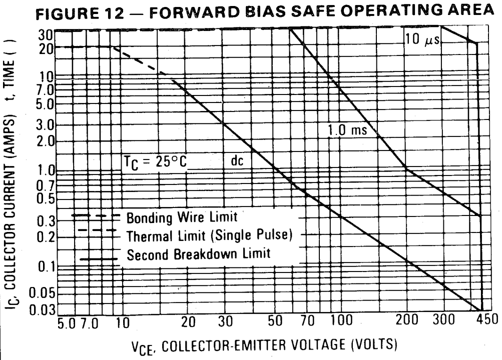
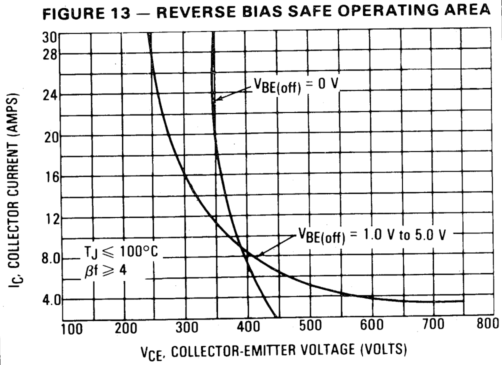


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

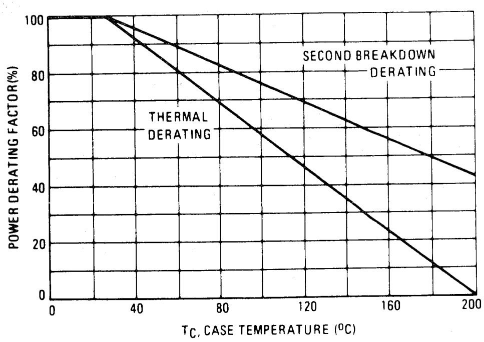
The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

FIGURE 14 — POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

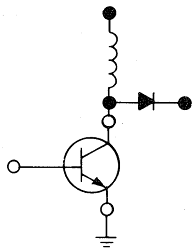
MJ13330
MJ13331

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ13330 and MJ13331 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Time
75 ns Inductive Fall Time–25°C (Typ)
150 ns Inductive Crossover Time–25°C (Typ)
900 ns Inductive Storage Time–25°C (Typ)
Operating Temperature Range −65 to +200°C
100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

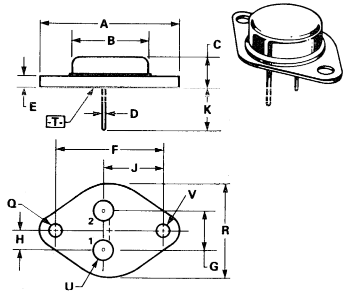
20 AMPERE

NPN SILICON POWER TRANSISTORS

200 and 250 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
⊕ 0.13 (0.005) Ⓜ T V Ⓜ
FOR LEADS:
⊕ 0.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
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D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MJ13330	MJ13331	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Emitter Voltage	V_{CEV}	400	450	Vdc
Emitter Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 20		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Similar device types with higher V_{CEO} ratings are: MJ13332 (350 V) thru MJ13335 (500 V).

3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ13330		$V_{CEO(sus)}$	200	–	–	Vdc
MJ13331			250	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	–	0.25	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 150^oC$)			–	–	5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, $T_C = 100^oC$)		I_{CER}	–	–	5	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)		I_{EBO}	–	–	0.5	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with base reverse biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)		h_{FE}	15	–	75	–
(I_C = 10 Adc, V_{CE} = 5 Vdc)			8.0	–	40	
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.5 Adc)		$V_{CE(sat)}$	–	–	1.5	Vdc
(I_C = 20 Adc, I_B = 5 Adc)			–	–	3.5	
(I_C = 10 Adc, I_B = 1.8 Adc, $T_C = 100^oC$)			–	–	2.5	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.5 Adc)		$V_{BE(sat)}$	–	–	1.8	Vdc
(I_C = 10 Adc, I_B = 1.8 Adc, $T_C = 100^oC$)			–	–	1.8	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 300 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	5	–	40	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	100	–	400	pF
SWITCHING CHARACTERSITICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 175 Vdc, I_C = 10 A, I_{B1} = 1.5 Adc, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%)	t_d	–	0.08	0.20	μs
Rise Time		t_r	–	0.55	1.0	μs
Storage Time		t_s	–	0.70	3.5	μs
Fall Time		t_f	–	0.11	0.7	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 10 A(pk), V_{clamp} = 200 Vdc, I_{B1} = 1.8 Adc, $V_{BE(off)}$ = 5 Vdc, $T_C = 100^oC$)	t_{sv}	–	1.35	4.5	μs
Crossover Time		t_c	–	0.45	1.8	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = 200 Vdc, I_{B1} = 1.5 Adc, $V_{BE(off)}$ = 5 Vdc, $T_C = 25^oC$)	t_{sv}	–	0.90	–	μs
Crossover Time		t_c	–	0.15	–	μs
Fall Time		t_{fi}	–	0.075	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

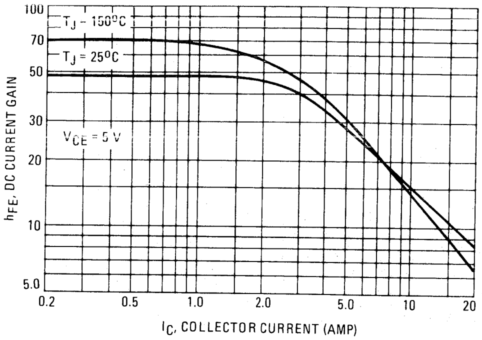

FIGURE 2 — COLLECTOR SATURATION REGION

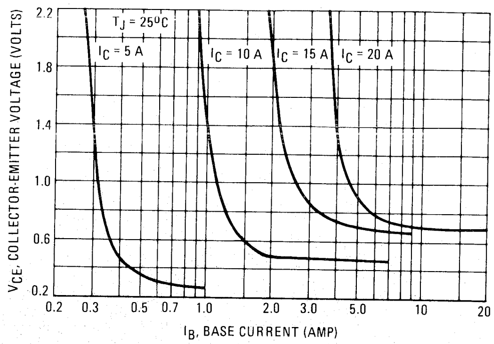

FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

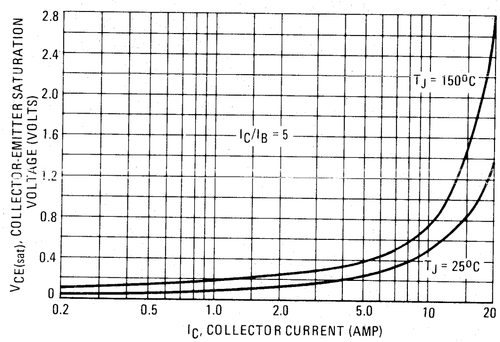

FIGURE 4 — BASE-EMITTER VOLTAGE

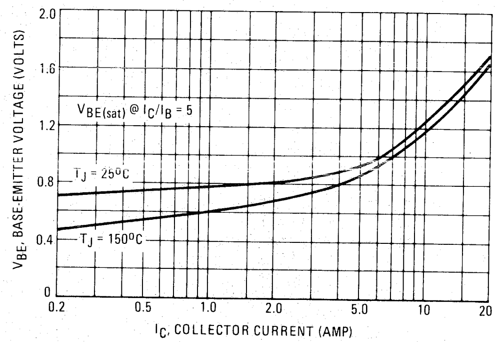

FIGURE 5 — COLLECTOR CUTOFF REGION

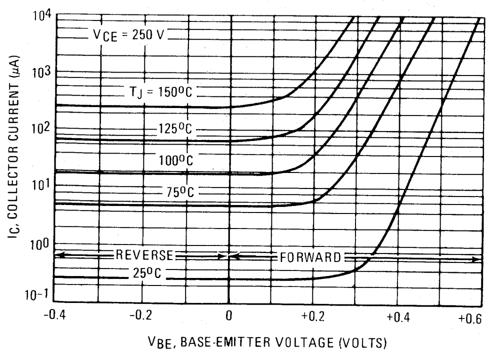

FIGURE 6 — OUTPUT CAPACITANCE

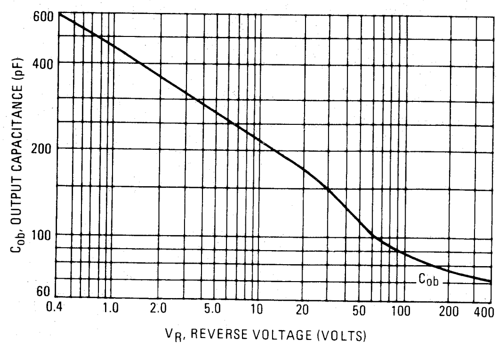

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FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

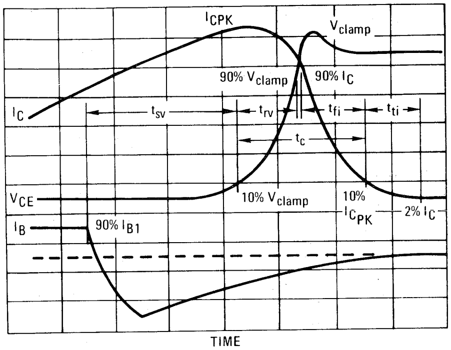
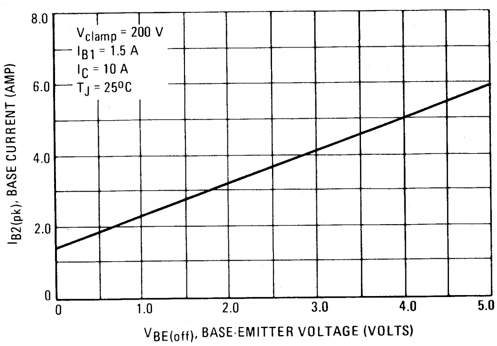


FIGURE 8 — REVERSE BASE CURRENT versus BASE EMITTER VOLTAGE



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

FIGURE 9 — TURN-ON TIME

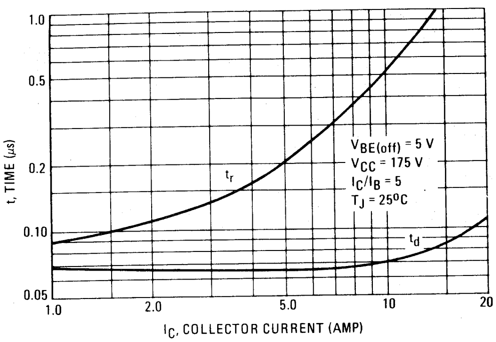


FIGURE 10 — TURN-OFF TIME

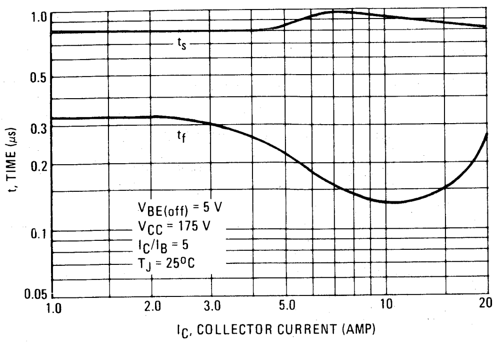


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TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

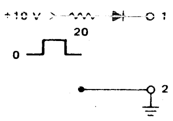
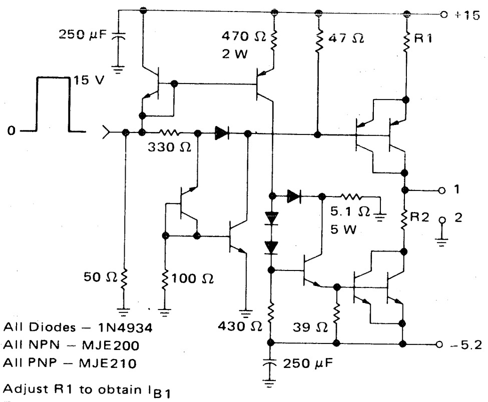
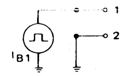
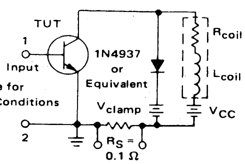
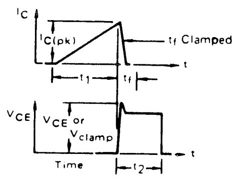
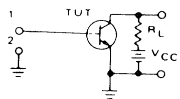
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For $V_{CEO(sus)}$, R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 200 V	V_{CC} = 175 V R_L = 17.5 Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

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FIGURE 11 – THERMAL RESPONSE

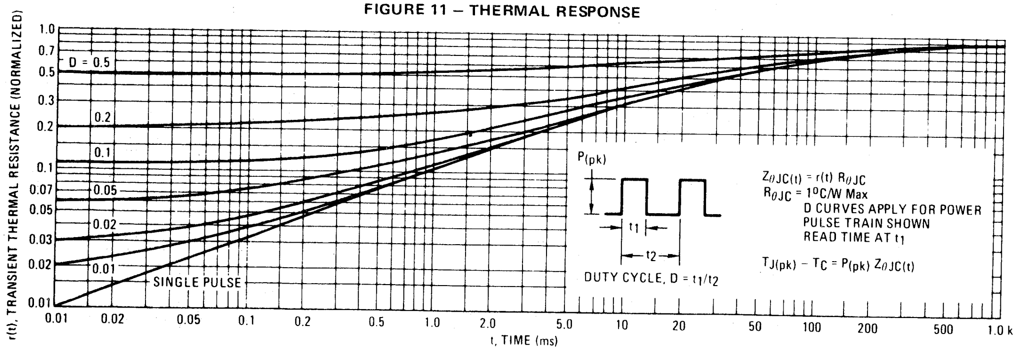


FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

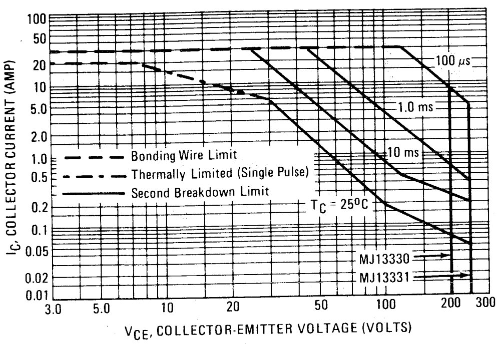
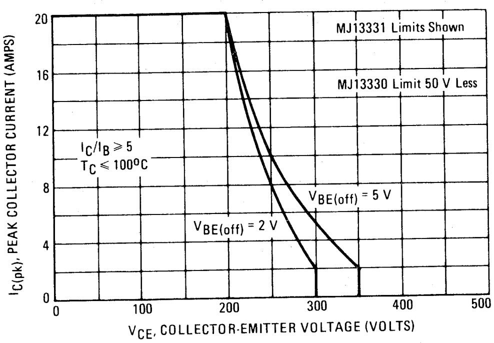


FIGURE 13 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

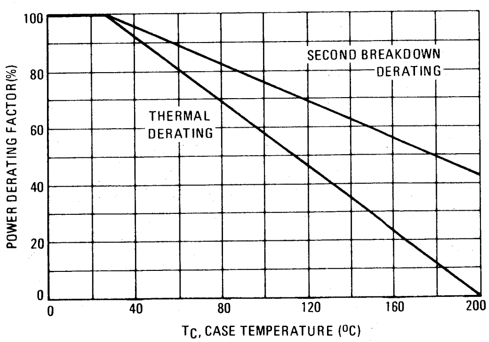
The data of Figure 12 is based on $T_C = 25^\circ C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 — POWER DERATING



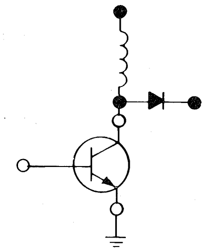
MJ13333
MJ13335

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ13333 and MJ13335 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
- 200 ns Inductive Fall Time—25°C (Typ)
- 1.8 µs Inductive Storage Time—25°C (Typ)

Operating Temperature Range −65 to +200°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

20 AMPERE

NPN SILICON POWER TRANSISTORS

400–500 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

MAXIMUM RATINGS

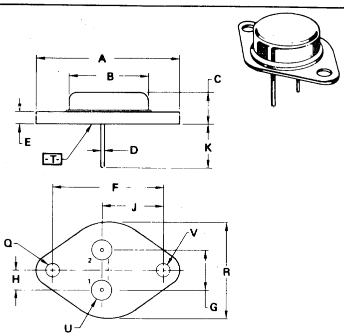
Rating	Symbol	MJ13333	MJ13335	Unit
Collector-Emitter Voltage	V_{CEO}	400	500	Vdc
Collector-Emitter Voltage	V_{CEV}	700	800	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Similar device types available with lower V_{CEO} ratings, see the MJ13330 (200 V) and MJ13331 (250 V).



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⌖	∅0.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	∅0.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ13335	$V_{CEO(sus)}$	500	–	–	Vdc
MJ13333		400	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	0.25	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	–	5.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	60	–
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	–	–	1.8	Vdc
(I_C = 20 Adc, I_B = 6.7 Adc)		–	–	5.0	
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)		–	–	2.4	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	–	–	1.8	Vdc
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)		–	–	1.8	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	125	–	500	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — (V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 10 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.02	0.1	μs
Rise Time	t_r	–	0.3	0.7	μs
Storage Time	t_s	–	1.6	4.0	μs
Fall Time	t_f	–	0.3	0.7	μs
Inductive Load, Clamped (Table 1)					
Storage Time — (I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	2.5	5.0	μs
Crossover Time	t_c	–	0.8	2.0	μs
Storage Time — (I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	1.8	–	μs
Crossover Time	t_c	–	0.4	–	μs
Fall Time	t_{fi}	–	0.2	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

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FIGURE 1 — DC CURRENT GAIN

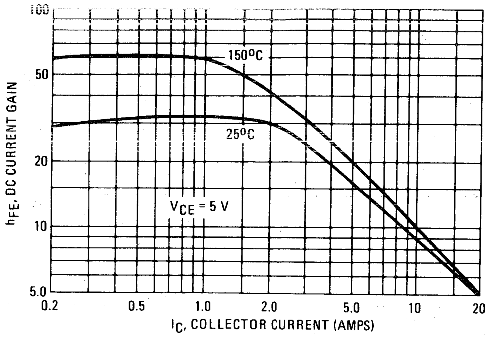


FIGURE 2 — COLLECTOR SATURATION REGION

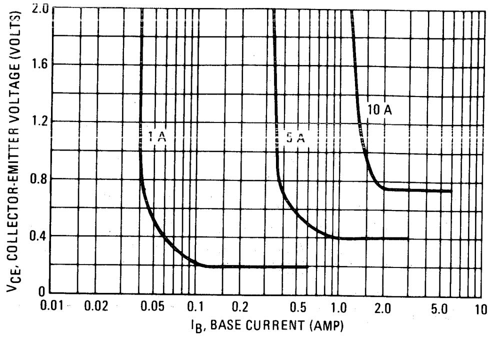


FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION

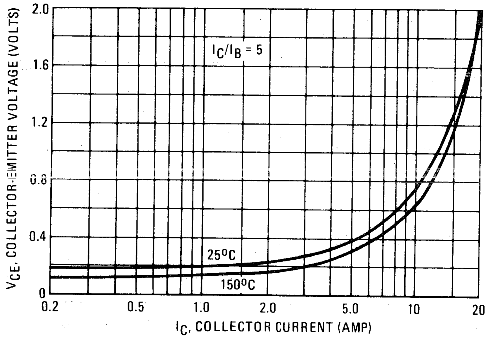
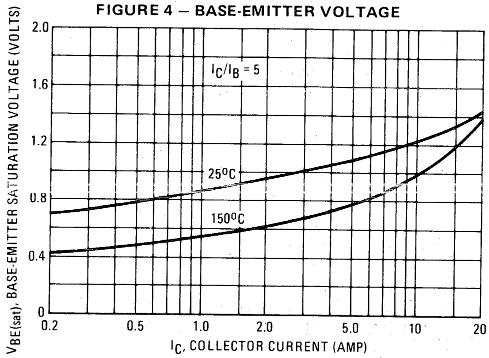


FIGURE 4 — BASE-EMITTER VOLTAGE



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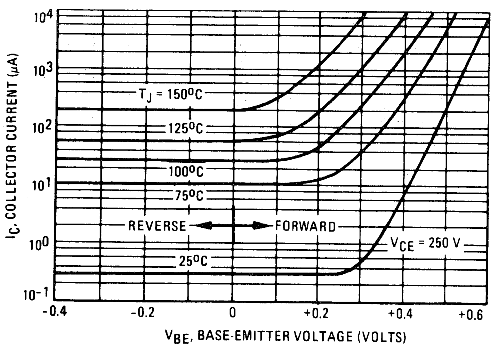

FIGURE 6 — CAPACITANCE

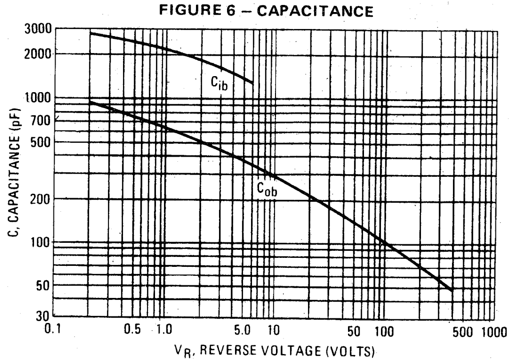

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FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

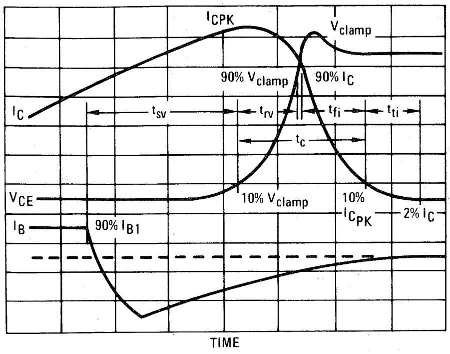
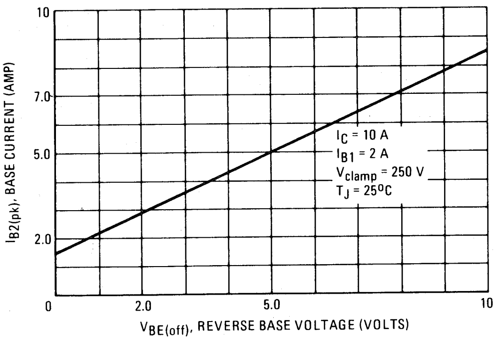


FIGURE 8 — REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



SWITCHING TIMES NOTE

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t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

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$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 — TURN-ON SWITCHING TIMES

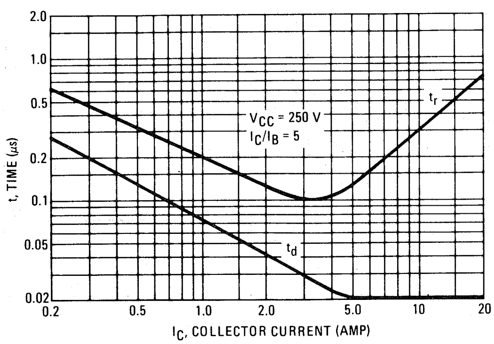

FIGURE 10 — TURN-OFF SWITCHING TIMES

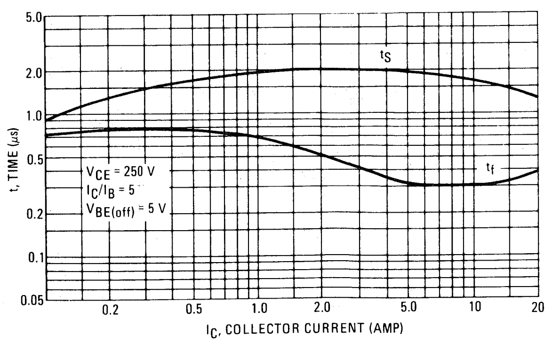

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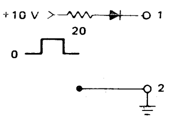
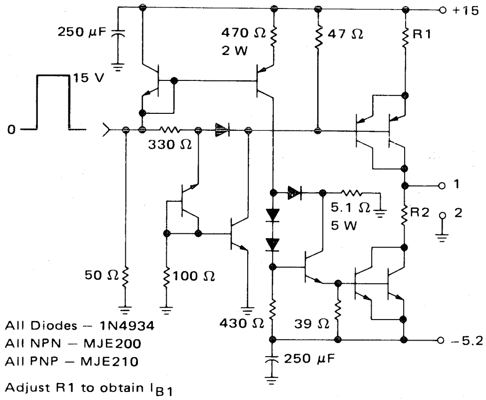
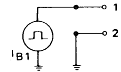
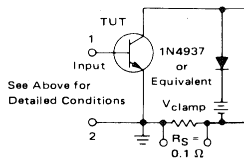
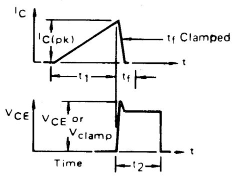
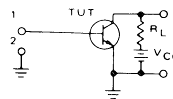
TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes — 1N4934 All NPN — MJE200 All PNP — MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $V_{CEO(sus)}$, R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

3

FIGURE 11 — THERMAL RESPONSE

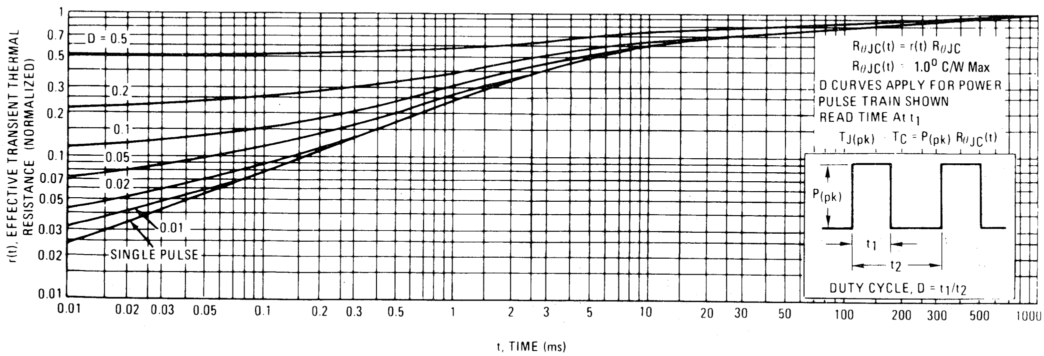


FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

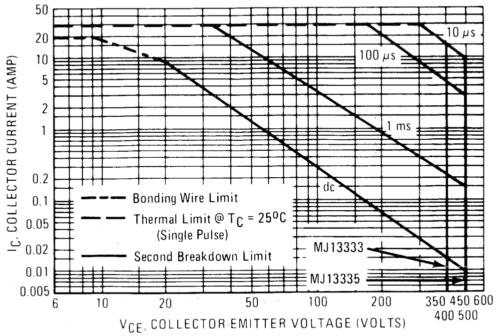
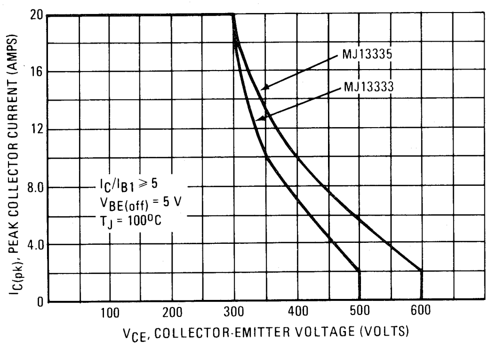


FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

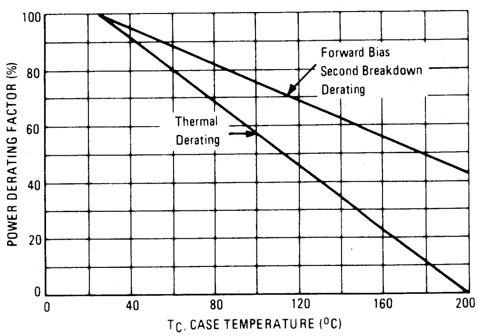
The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 — POWER DERATING



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
MJ14000, MJ14002
PNP
MJ14001, MJ14003

HIGH-CURRENT COMPLEMENTARY SILICON POWER TRANSISTORS

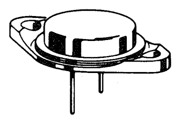
. . . designed for use in high-power amplifier and switching circuit applications.

- High Current Capability — I_C Continuous = 60 Amperes
- DC Current Gain — h_{FE} = 15-100 @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C = 50 Adc

60 AMPERES

COMPLEMENTARY SILICON POWER TRANSITORS

60-80 VOLTS
300 WATTS



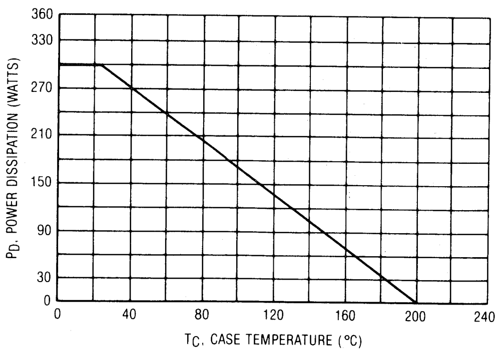
MAXIMUM RATINGS

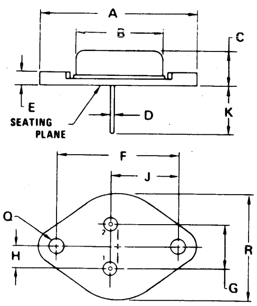
Rating	Symbol	MJ14000 MJ14001	MJ14002 MJ14003	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CBO}	60	80	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector Current — Continuous	I_C	60		Adc
Base Current — Continuous	I_B	15		Adc
Emitter Current — Continuous	I_E	75		
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.7		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.584	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

3

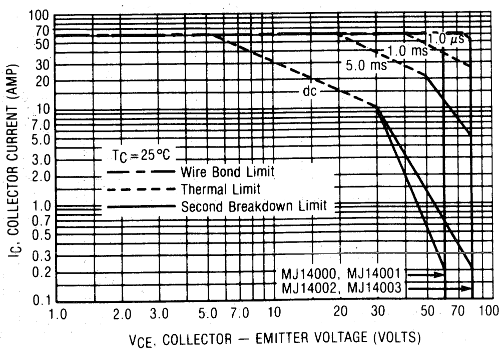
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	MJ14000, MJ14001 MJ14002, MJ14003	$V_{CEO(sus)}$	60 80	– –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	MJ14000, MJ14001 MJ14402, MJ14003	I_{CEO}	– –	1.0 1.0	mA
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 V) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 V)	MJ14000, MJ14001 MJ14002, MJ14003	I_{CEX}	– –	1.0 1.0	mA
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	MJ14000, MJ14001 MJ14002, MJ14003	I_{CBO}	– –	1.0 1.0	mA
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	–	1.0	mA
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 25 Adc, V_{CE} = 3.0 V) (I_C = 50 Adc, V_{CE} = 3.0 V) (I_C = 60 Adc, V_{CE} = 3.0 V)		h_{FE}	30 15 5	– 100 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 25 Adc, I_B = 2.5 Adc) (I_C = 50 Adc, I_B = 5.0 Adc) (I_C = 60 Adc, I_B = 12 Adc)		$V_{CE(sat)}$	– – –	1 2.5 3	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 25 Adc, I_B = 2.5 Adc) (I_C = 50 Adc, I_B = 5.0 Adc) (I_C = 60 Adc, I_B = 12 Adc)		$V_{BE(sat)}$	– – –	2 3 4	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	2000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 2 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

TYPICAL ELECTRICAL CHARACTERISTICS

NPN
MJ14000, MJ14002

FIGURE 3 — DC CURRENT GAIN

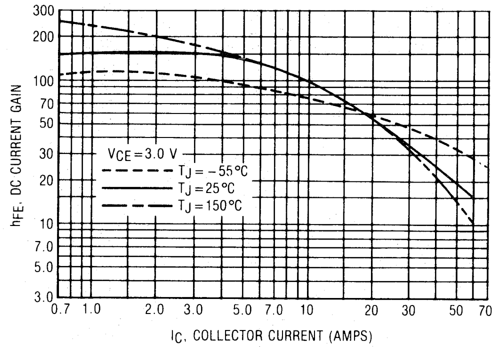


FIGURE 5 — COLLECTOR SATURATION REGION

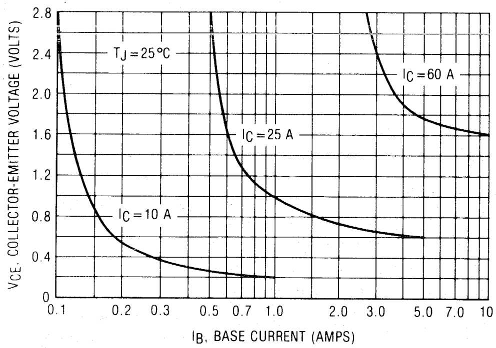
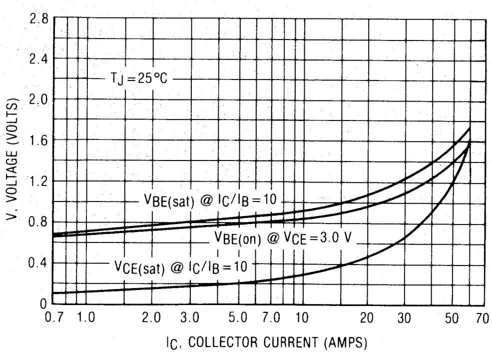


FIGURE 7 — "ON" VOLTAGES



PNP
MJ14001, MJ14003

FIGURE 4 — DC CURRENT GAIN

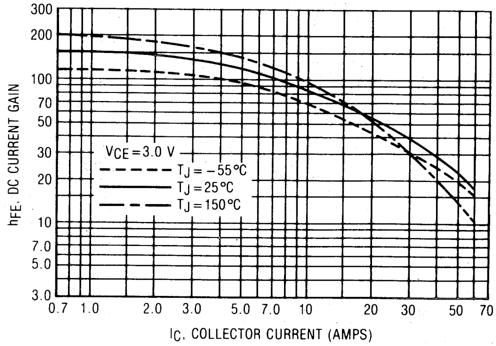


FIGURE 6 — COLLECTOR SATURATION REGION

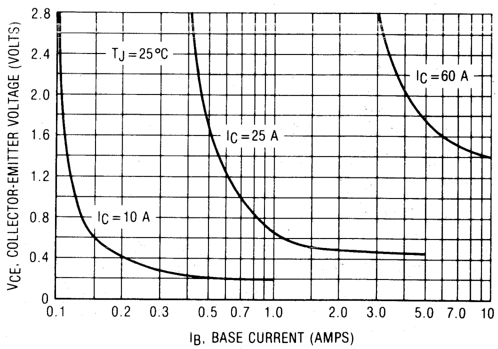
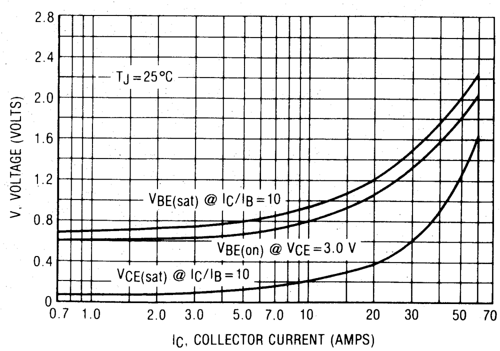


FIGURE 8 — "ON" VOLTAGES



3

FIGURE 9 — TURN-ON SWITCHING TIMES

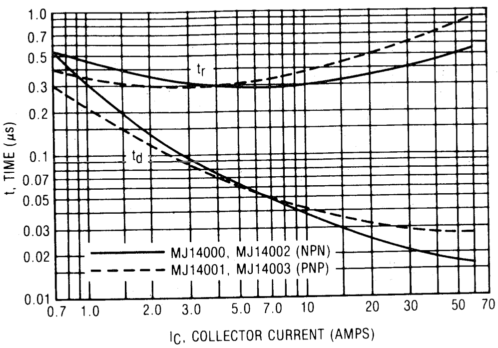


FIGURE 10 - TURN-OFF SWITCHING TIMES

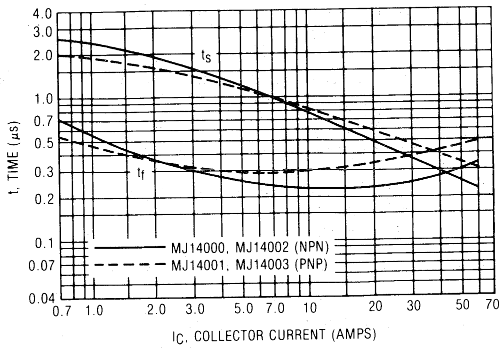


FIGURE 11 — CAPACITANCE VARIATION

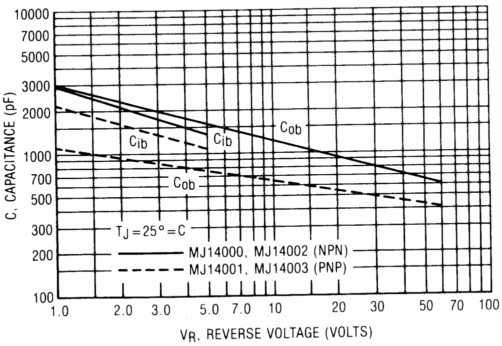
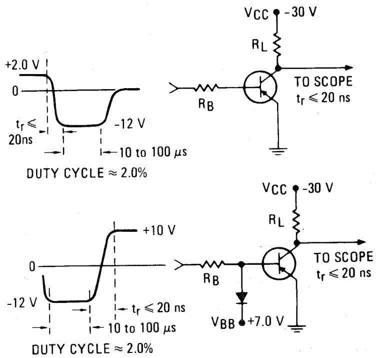
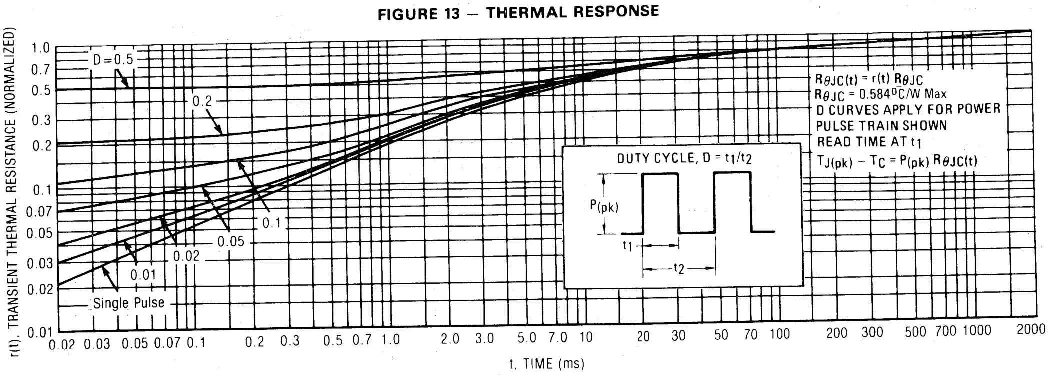


FIGURE 12 — SWITCHING TEST CIRCUIT



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

FIGURE 13 — THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

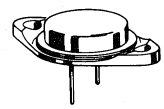
NPN MJ15001   PNP MJ15002

COMPLEMENTARY SILICON POWER TRANSISTORS

The MJ15001 and MJ15002 are EpiBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —
  200 W @ 40 V
  50 W @ 100 V
- For Low Distortion Complementary Designs
- High DC Current Gain —
  h_{FE} = 25 (Min) @ I_C = 4 Adc

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
140 VOLTS
200 WATTS



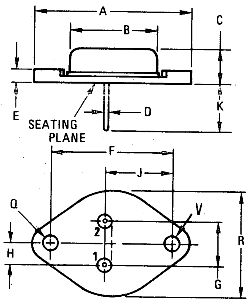
3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	140	Vdc
Collector-Base Voltage	V_{CBO}	140	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current — Continuous	I_B	5	Adc
Emitter Current — Continuous	I_E	20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for ≤10s.	T_L	265	°C



NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⊕ ∅ 0.25 (0.010) Ⓜ T V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⊕ ∅ 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

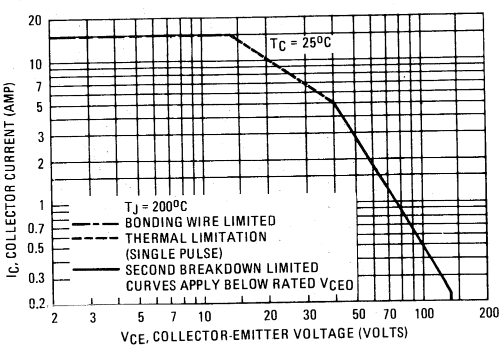
ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	–	100 2	μAdc mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	–	250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1 s (non-repetitive)) (V_{CE} = 100 Vdc, t = 1 s (non-repetitive)	$I_{S/b}$	5 0.5	– –	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	–
Collector-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	–	1	Vdc
Base-Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	–	2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	1000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 — CAPACITANCES

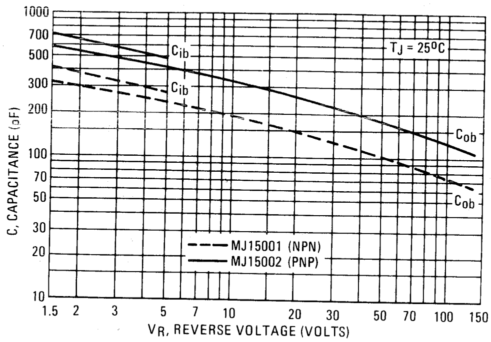


FIGURE 3 — CURRENT-GAIN — BANDWIDTH PRODUCT

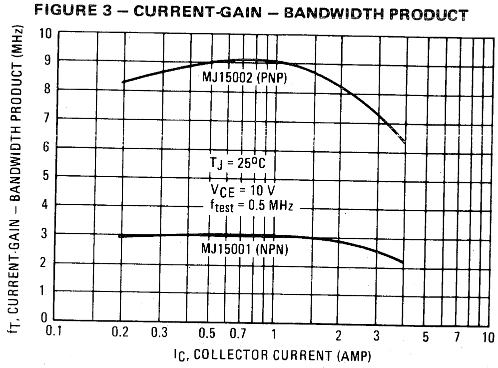


FIGURE 4 — DC CURRENT GAIN

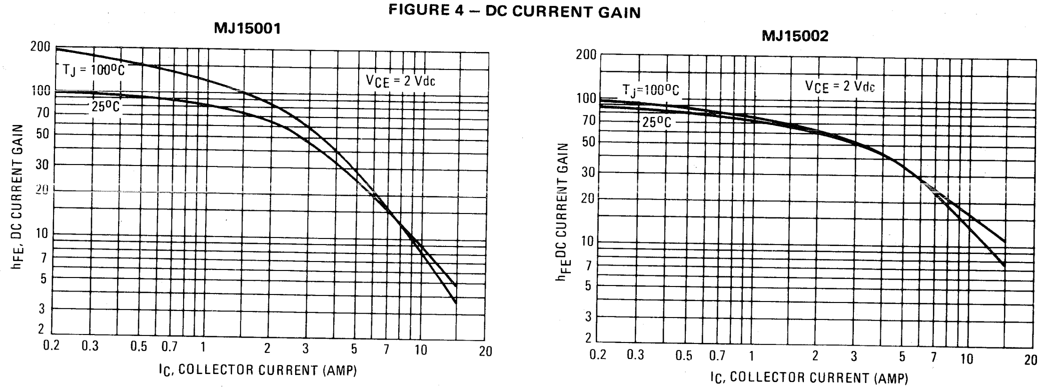
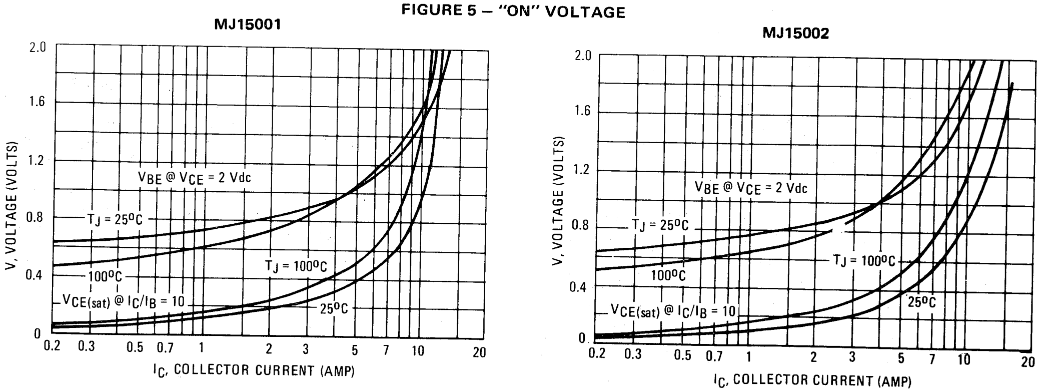


FIGURE 5 — "ON" VOLTAGE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
MJ15003
PNP
MJ15004

COMPLEMENTARY SILICON POWER TRANSISTORS

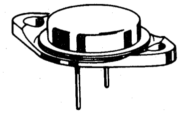
The MJ15003 and MJ15004 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) — 250 W @ 50 V
- For Low Distortion Complementary Designs
- High DC Current Gain — h_{FE} = 25 (Min) @ I_C = 5 Adc

20 AMPERE

POWER TRANSISTORS
COMPLEMENTARY SILICON

140 VOLTS
250 WATTS

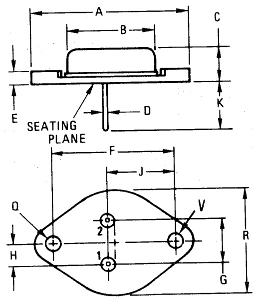


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	140	Vdc
Collector-Base Voltage	V_{CBO}	140	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current — Continuous	I_C	20	Adc
Base Current — Continuous	I_B	5	Adc
Emitter Current — Continuous	I_E	25	Adc
Total Power Dissipation @ $T_C = 25^{\circ}C$ Derate above $25^{\circ}C$	P_D	250 1.43	Watts $W/^{\circ}C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^{\circ}C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	$^{\circ}C/W$
Maximum Lead Temperature for Soldering Purposes: 1/16″ from Case for ≤10s.	T_L	265	$^{\circ}C$



NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⊕ ∅ 0.25 (0.010) Ⓜ T V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⊕ ∅ 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

3

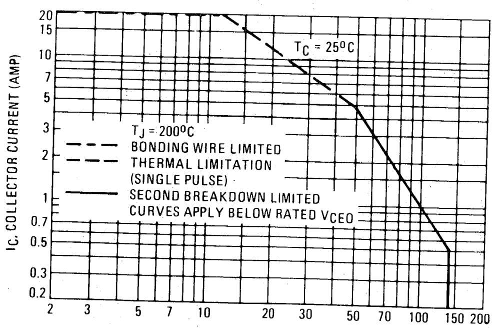
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	100 2	μAdc mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	–	250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non-repetitive)) (V_{CE} = 100 Vdc, t = 1 s (non-repetitive))	$I_{S/b}$	5 1	– –	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 5 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)	$V_{CE(sat)}$	–	1	Vdc
Base-Emitter On Voltage (I_C = 5 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	–	2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	1000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

3

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

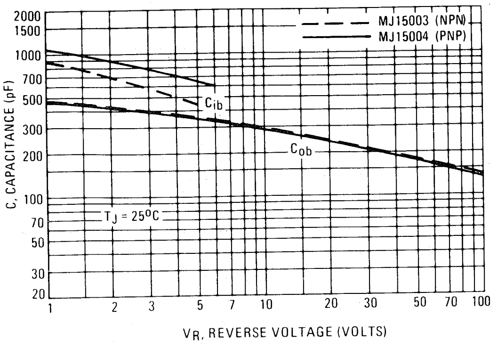


FIGURE 3 – CURRENT GAIN – BANDWIDTH PRODUCT

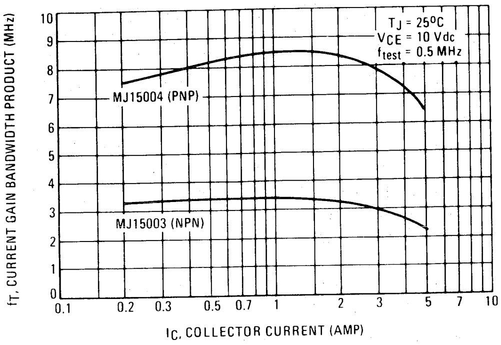
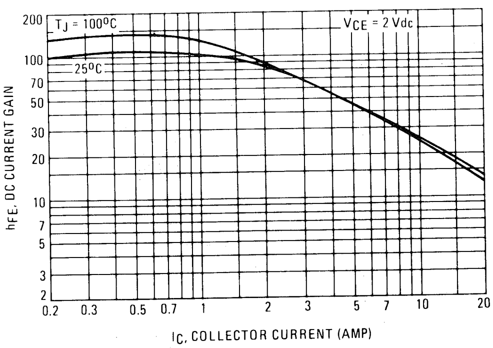


FIGURE 4 – DC CURRENT GAIN

MJ15003



MJ15004

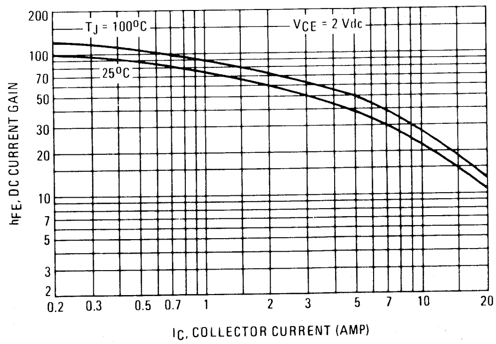
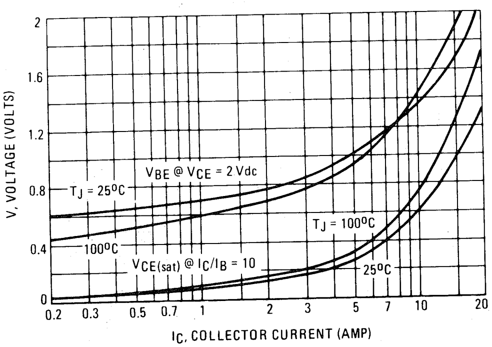
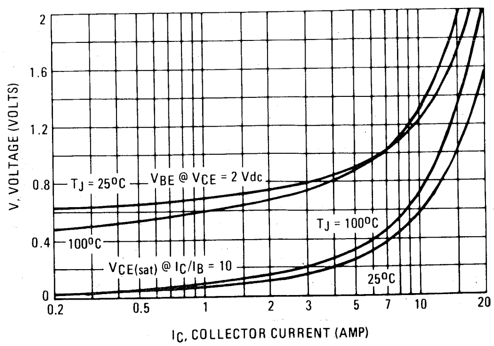


FIGURE 5 – "ON" VOLTAGE

MJ15003



MJ15004



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
MJ15011
PNP
MJ15012

Advance Information

COMPLEMENTARY SILICON POWER TRANSISTORS

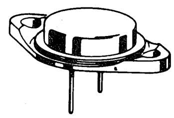
The MJ15011 and MJ15012 are PowerBase power transistors designed for high-power audio, disk head positioners, and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc-to-dc converters or inverters.

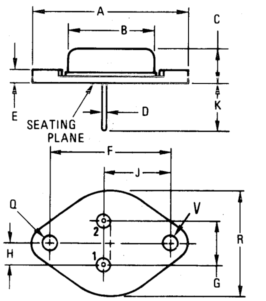
- High Safe Operating Area (100% Tested)
  1.2 A @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{FE} = 20 (Min) @ 2 A, 2 V
  $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 4 A, I_B = 0.4 A
- For Low Distortion Complementary Designs

10 AMPERE

COMPLEMENTARY POWER TRANSISTORS

250 VOLTS
200 WATTS





NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⊕ ϕ 0.25 (0.010) Ⓜ T V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⊕ ϕ 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	250	Vdc
Collector-Emitter Voltage	V_{CEX}	250	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 15	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 5	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes	T_L	265	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 100 mA)	$V_{(BR)CEO}$	250	–	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc)	I_{CEO}	–	1	mAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	500	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc)	I_{EBO}	–	500	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
(I_C = 2 Adc, V_{CE} = 2 Vdc)		20	100	
(I_C = 4 Adc, V_{CE} = 2 Vdc)		5	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 2 Adc, I_B = 0.2 Adc)		–	0.8	
(I_C = 4 Adc, I_B = 0.4 Adc)		–	2.5	
Base-Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	–	2	Vdc
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, f = 1 MHz)	C_{ob}	–	750	pF
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$			Adc
(V_{CE} = 40 Vdc, t = 0.5 s)		5	–	
(V_{CE} = 100 Vdc, t = 0.5 s)		1.4	–	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 1 – DC CURRENT GAIN

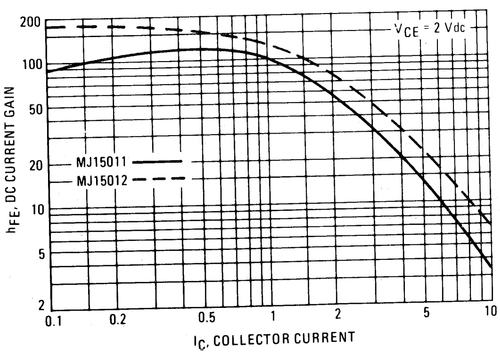
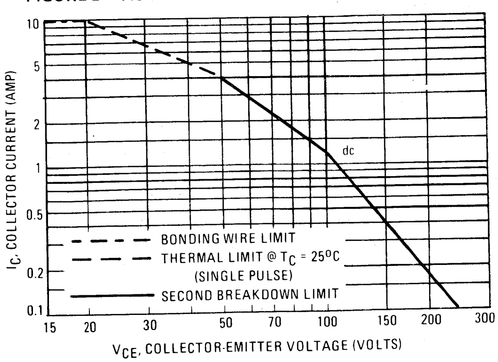


FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



MJ15015, MJ15016
See Page 3-9

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
MJ15022, MJ15024

SILICON POWER TRANSISTORS

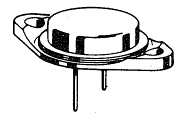
The MJ15022 and MJ15024 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) — 2 A @ 80 V
- High DC Current Gain — h_{FE} = 15 (Min) @ I_C = 8 Adc

16 AMPERE

SILICON POWER TRANSISTORS

200 and 250 VOLTS
250 WATTS



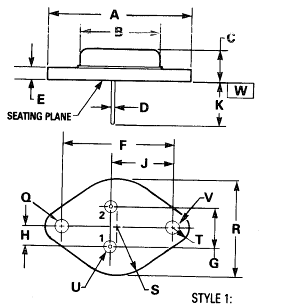
MAXIMUM RATINGS

Rating	Symbol	MJ15022	MJ15024	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Base Voltage	V_{CBO}	350	400	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector-Emitter Voltage	V_{CEX}	400		Vdc
Collector Current — Continuous Peak (1)	I_C	16 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⌖ φ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⌖ φ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA

3

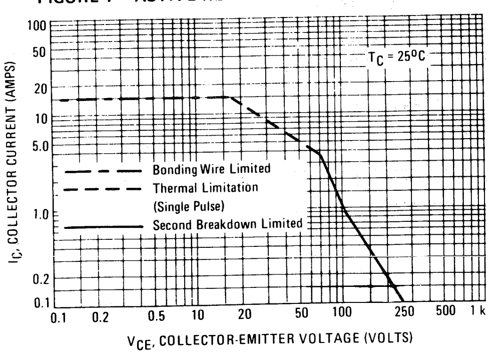
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	MJ15022 MJ15024	$V_{CEO(sus)}$	200 250	– –	
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15022 MJ15024	I_{CEX}	– –	250 250	μAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0)	MJ15022 MJ15024	I_{CEO}	– –	500 500	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_B = 0)		I_{EBO}	–	500	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 0.5 s (non-repetitive)) (V_{CE} = 80 Vdc, t = 0.5 s (non-repetitive))		$I_{S/b}$	5 2	– –	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)		h_{FE}	15 5	60 –	–
Collector-Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)		$V_{CE(sat)}$	– –	1.4 4.0	Vdc
Base-Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	–	2.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	–	500	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

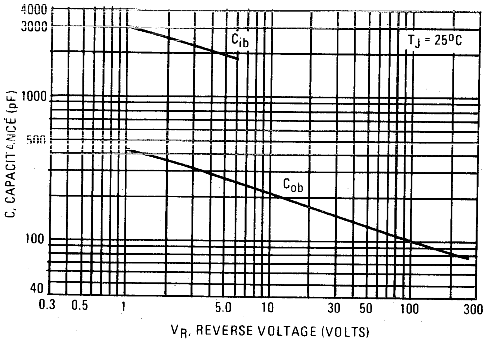


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

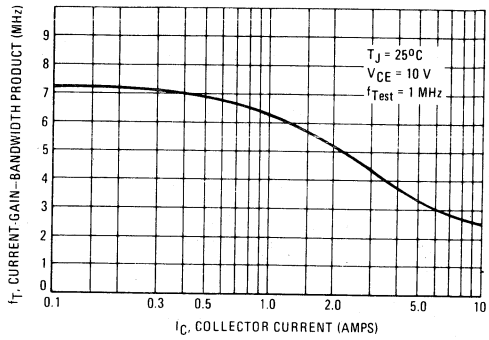


FIGURE 4 – DC CURRENT GAIN

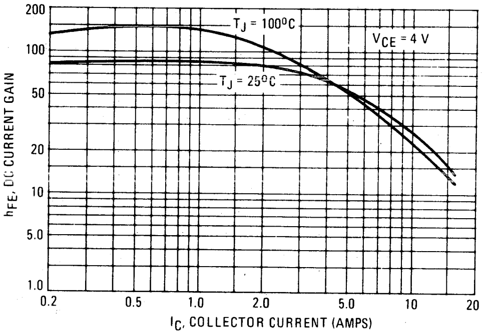


FIGURE 5 – "ON" VOLTAGE

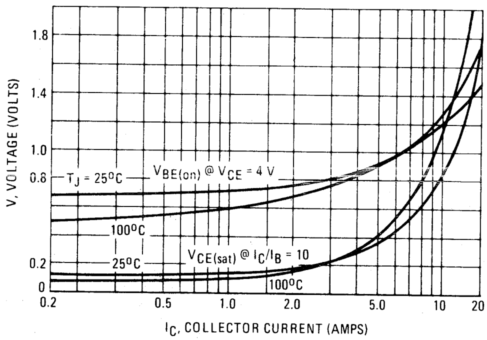
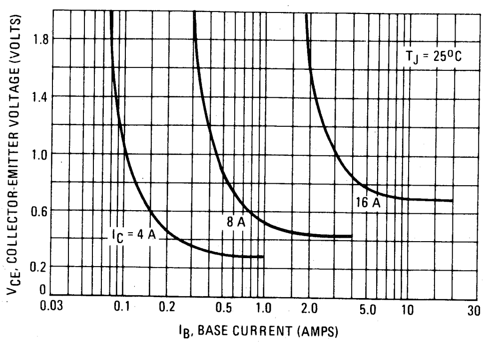


FIGURE 6 – COLLECTOR SATURATION REGION



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
MJ15023
MJ15025

SILICON POWER TRANSISTORS

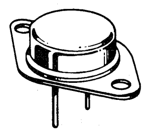
The MJ15023 and MJ15025 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) — 2 A @ 80 V
- High DC Current Gain — h_{FE} = 15 (Min) @ I_C = 8 Adc

16 AMPERE

SILICON
POWER TRANSISTORS

200 and 250 VOLTS
250 WATTS



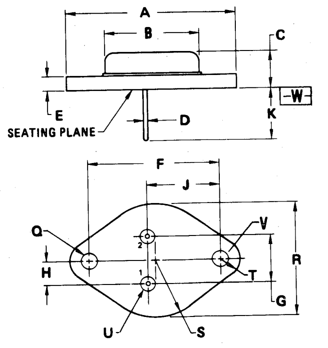
MAXIMUM RATINGS

Rating	Symbol	MJ15023	MJ15025	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Base Voltage	V_{CBO}	350	400	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector-Emitter Voltage	V_{CEX}	400		Vdc
Collector Current — Continuous Peak (1)	I_C	16 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

CASE 1-04
TO-204AA

3

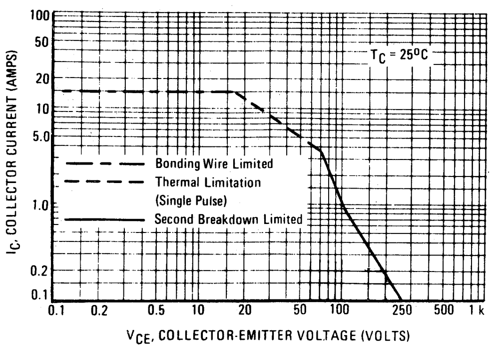
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	MJ15023 MJ15025	$V_{CEO(sus)}$	200 250	– –	
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15023 MJ15025	I_{CEX}	– –	250 250	μAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0)	MJ15023 MJ15025	I_{CEO}	– –	500 500	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_B = 0)	Both	I_{EBO}	–	500	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 0.5 s (non-repetitive)) (V_{CE} = 80 Vdc, t = 0.5 s (non-repetitive))		$I_{S/b}$	5 2	– –	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)		h_{FE}	15 5	60 –	–
Collector-Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)		$V_{CE(sat)}$	– –	1.4 4.0	Vdc
Base-Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	–	2.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	–	600	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

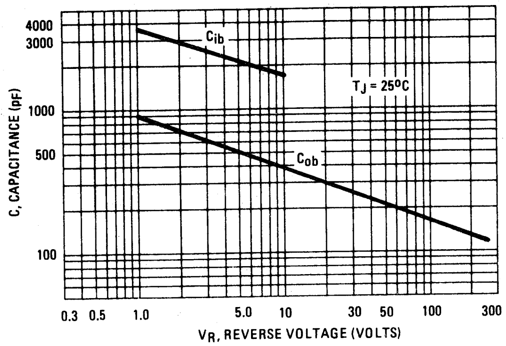


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

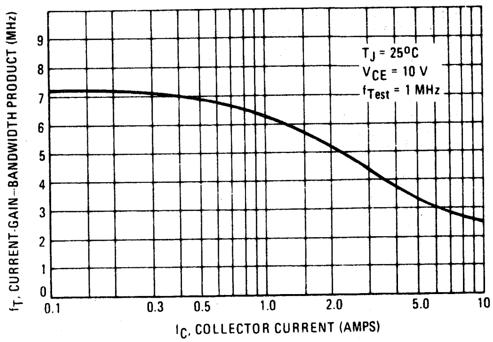


FIGURE 4 – DC CURRENT GAIN

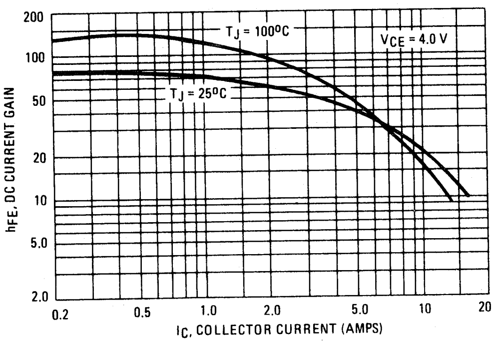
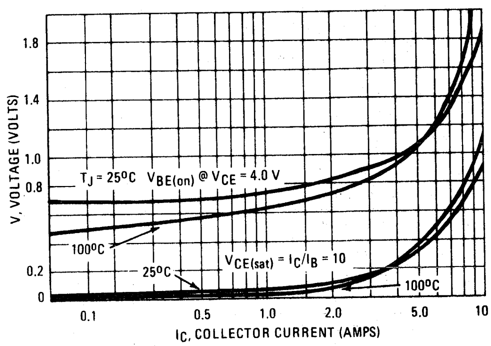


FIGURE 5 – "ON" VOLTAGE



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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ16002
MJ16004

Designers Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16004 is a selected high-gain version of the MJ16002 for applications where drive current is limited.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  - 50 ns Inductive Fall Time — 75°C (Typ)
  - 70 ns Inductive Crossover Time — 75°C (Typ)
  - 500 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

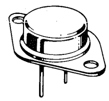
5 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



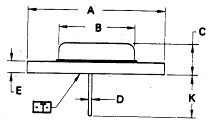
MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 10	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4.0 8.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	125 71.5 0.714	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

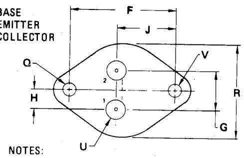
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR



NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ϕ.13 (0.005) Ⓜ | T | V Ⓜ

   FOR LEADS:
   ⌖ | ϕ.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

MJ16002

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 0.2 Adc) (I_C = 3.0 Adc, I_B = 0.4 Adc) (I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	— — —	1.0 2.5 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.4 Adc) (I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc	h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	200	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 0.8 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100	ns
Rise Time			t_r	—	100	300	
Storage Time			t_s	—	1000	3000	
Fall Time			t_f	—	60	300	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	400	—	
Fall Time			t_f	—	130	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	500	1600	ns
Fall Time			t_{fi}	—	100	200	
Crossover Time			t_c	—	120	250	
Storage Time		(T_J = 150°C)	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$$*\beta_f = \frac{I_C}{I_{B1}}$$

3

MJ16004

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.25	mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 0.15 Adc)	$V_{CE(sat)}$	—	—	1.0	Vdc
(I_C = 3.0 Adc, I_B = 0.3 Adc)		—	—	2.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc, T_C = 100°C)		—	—	2.5	
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 3.0 Adc, I_B = 0.3 Adc, T_C = 100°C)		—	—	1.5	
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc	h_{FE}	7.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	200	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.3 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 0.6 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100	ns
Rise Time			t_r	—	130	300	
Storage Time			t_s	—	800	2700	
Fall Time			t_f	—	80	350	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	250	—	
Fall Time			t_f	—	60	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.3 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	400	1300	ns
Fall Time			t_{fi}	—	80	150	
Crossover Time			t_c	—	90	200	
Storage Time		(T_J = 150°C)	t_{sv}	—	450	—	
Fall Time			t_{fi}	—	100	—	
Crossover Time			t_c	—	110	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$^*\beta_f = \frac{I_C}{I_{B1}}$

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

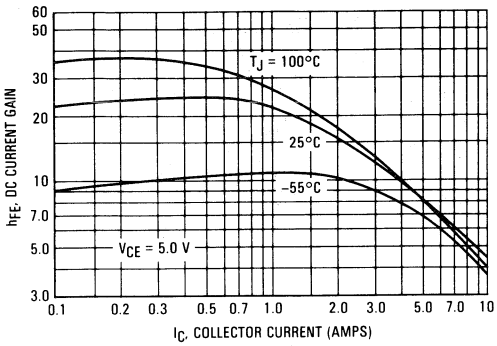


FIGURE 2 — COLLECTOR SATURATION REGION

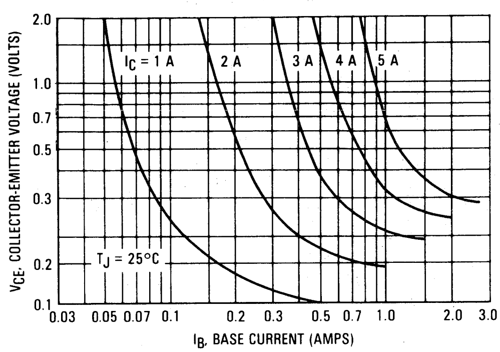


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

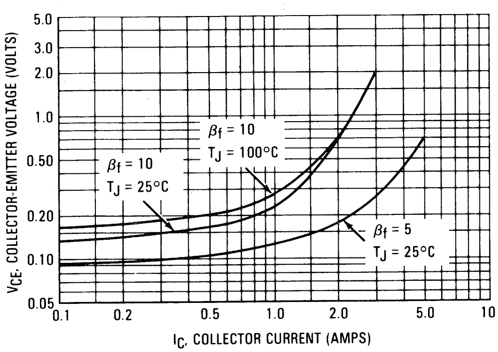


FIGURE 4 — BASE-EMITTER VOLTAGE

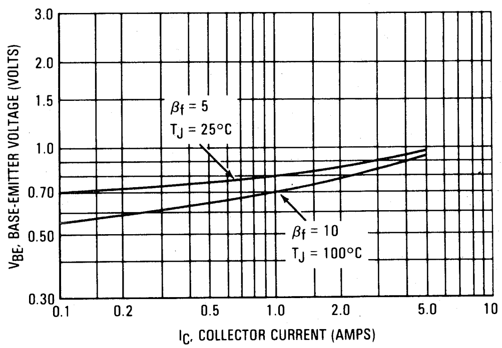


FIGURE 5 — COLLECTOR CUTOFF REGION

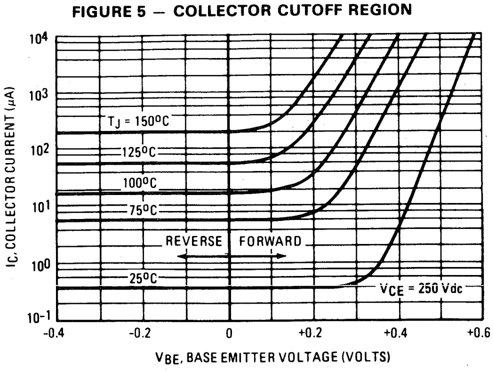
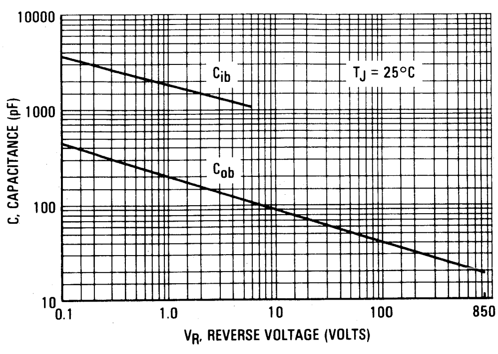


FIGURE 6 — CAPACITANCE



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TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

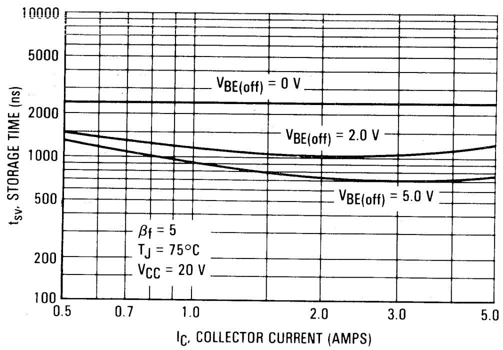

FIGURE 8 — STORAGE TIME

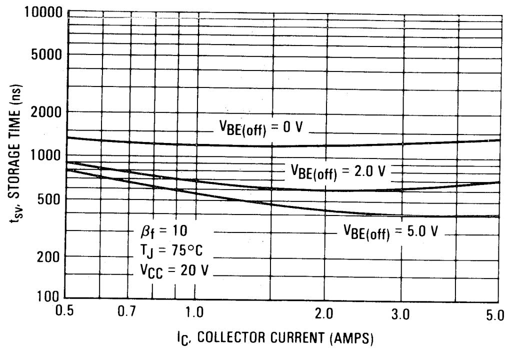

FIGURE 9 — COLLECTOR CURRENT FALL TIME

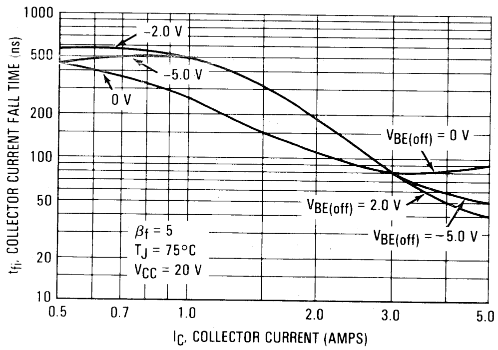

FIGURE 10 — COLLECTOR CURRENT FALL TIME

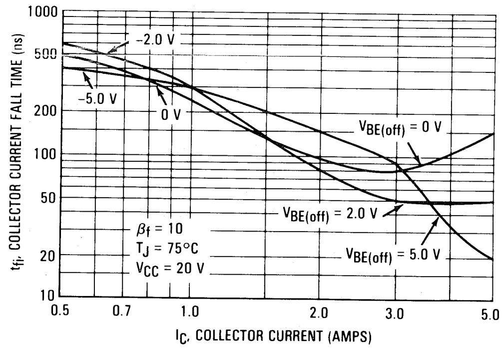

FIGURE 11 — CROSSOVER TIME

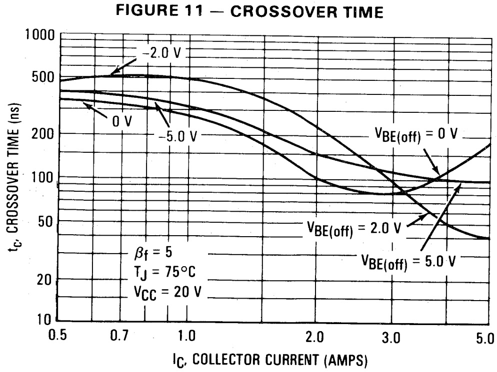

FIGURE 12 — CROSSOVER TIME

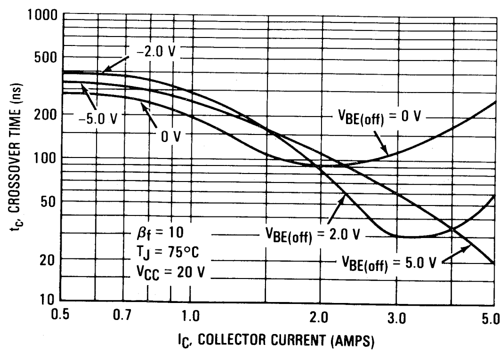

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FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

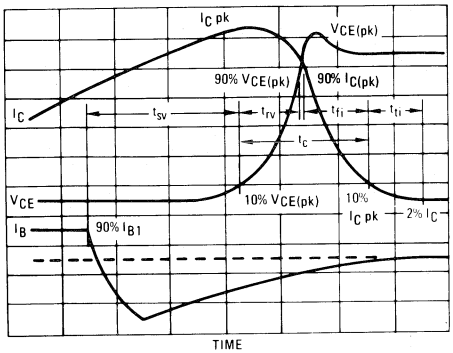
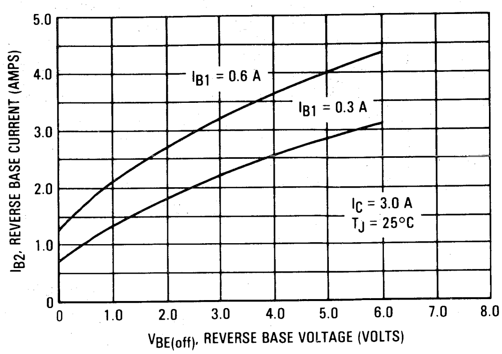


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

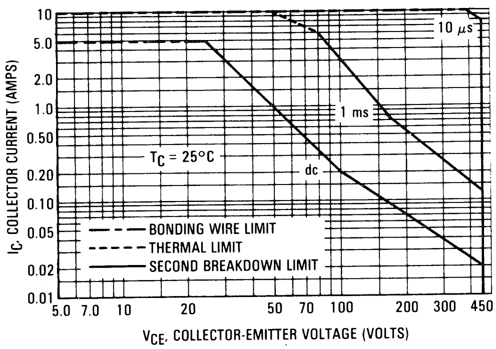
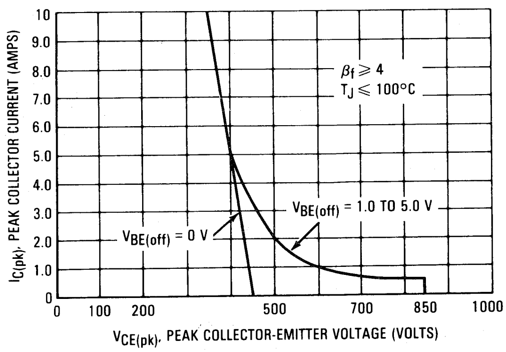


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



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SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

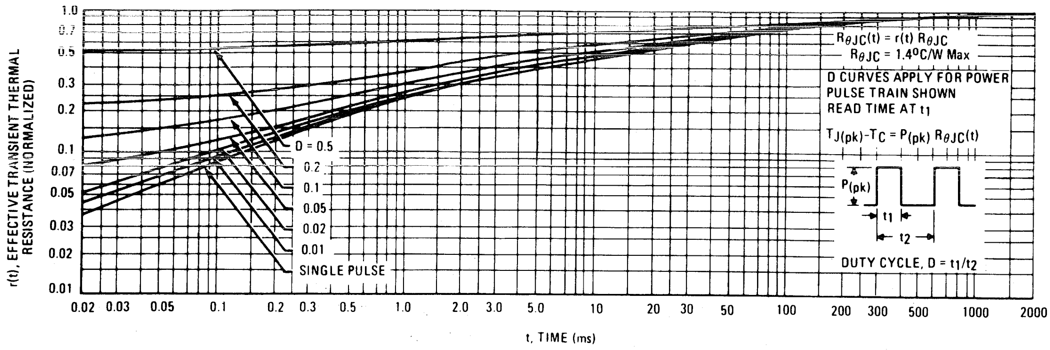


FIGURE 18 — POWER DERATING

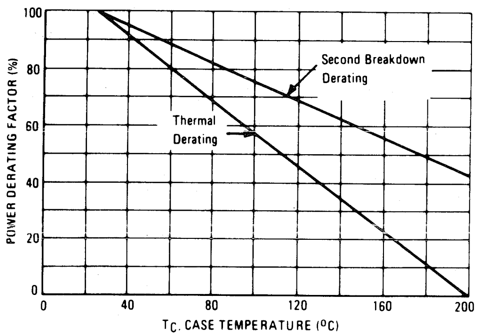
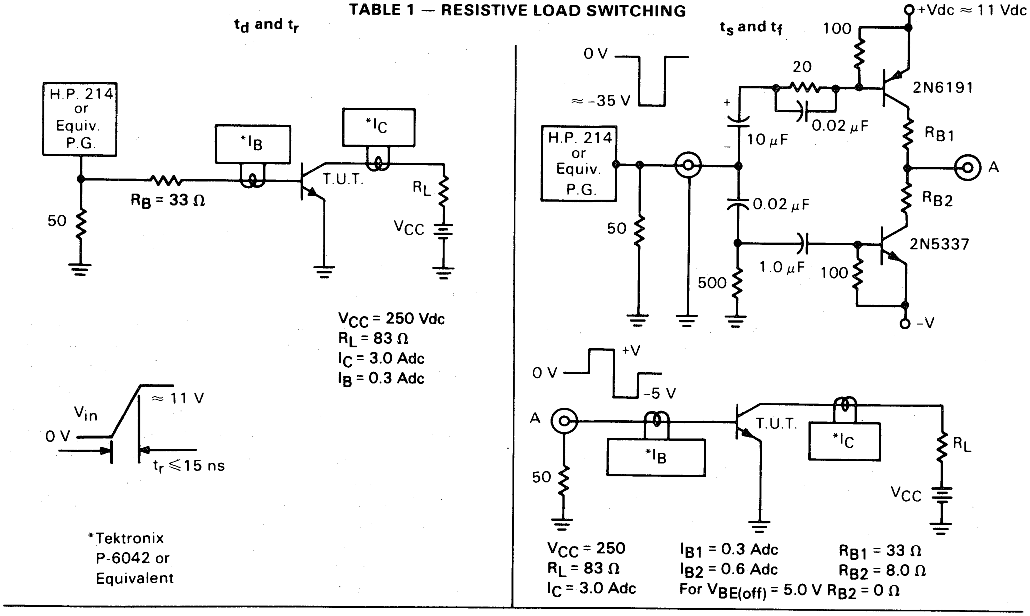


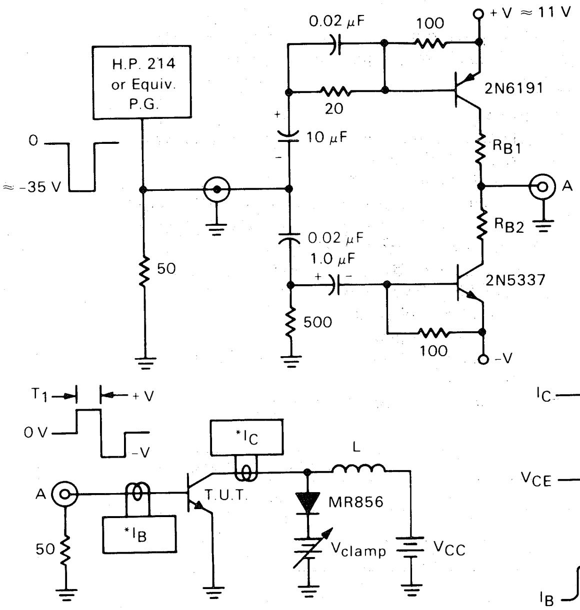
TABLE 1 — RESISTIVE LOAD SWITCHING

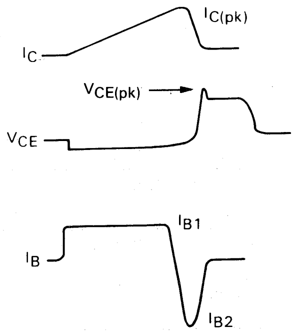


*Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

3

TABLE 2 — INDUCTIVE LOAD SWITCHING





$T_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{CEO(sus)}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

*Tektronix
P-6042 or
Equivalent

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

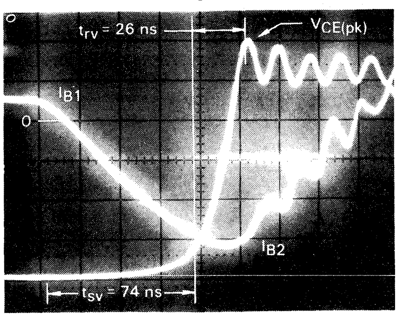
Scope - Tektronix
7403 or
Equivalent

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

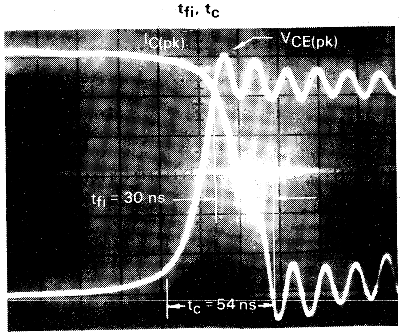
TYPICAL INDUCTIVE SWITCHING WAVEFORMS

t_{sv}



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.3 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 300 Volts
T_C = 25°C
Time Base =
20 ns/cm

t_{fi}, t_c



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.3 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 300 Volts
T_C = 25°C
Time Base =
20 ns/cm

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

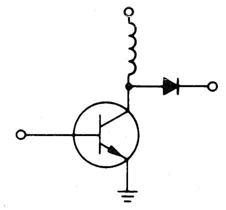
MJ16002A
MJH16002A

Designer's Data Sheet

NPN Silicon Power Transistors

1 kV Switchmode III Series

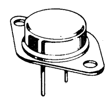
POWER TRANSISTORS
5 AMPERES
500 VOLTS
125 and 100 WATTS



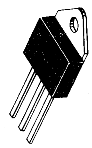
These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:
- Collector-Emitter Voltage — V_{CEV} = 1000 Vdc
- Fast Turn-Off Times
  100 ns Inductive Fall Time — 100°C (Typ)
  120 ns Inductive Crossover Time — 100°C (Typ)
  500 ns Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Load
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents
- Extended FBSOA Rating Using Ultra-fast Rectifiers
- Extremely High RBSOA Capability



CASE 1-05
TO-204AA
MJ16002A



CASE 340-01
TO-218AC
MJH16002A

MAXIMUM RATINGS

Rating	Symbol	MJ16002A	MJH16002A	Unit
Collector-Emitter Voltage	V_{CEO}	500		Vdc
Collector-Emitter Voltage	V_{CEV}	1000		Vdc
Emitter-Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	5 10		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	4 8		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	125 71.5 0.714	100 40 0.833	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.40	1.25	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS[1]					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	0.003 0.020	0.15 1.0	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	0.020	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	I_{EBO}	—	—	0.15	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14a or 14b			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 15			
ON CHARACTERISTICS[1]					
Collector-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 0.2 Adc) (I_C = 3 Adc, I_B = 0.4 Adc) (I_C = 3 Adc, I_B = 0.4 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	0.3 0.5 0.6	0.7 1 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 3 Adc, I_B = 0.4 Adc) (I_C = 3 Adc, I_B = 0.4 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	1 1	1.5 1.5	Vdc
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)	h_{FE}	5	8	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)	C_{ob}	—	—	200	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Inductive Load (Table 1)							
Storage Time	(I_C = 3 Adc, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	500	1600	ns
Fall Time			t_{fi}	—	100	200	
Crossover Time			t_c	—	120	250	
Storage Time		(T_J = 150°C)	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	
Resistive Load (Table 2)							
Delay Time	(I_C = 3 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ≤ 2%)	(I_{B2} = 0.8 Adc, R_{B2} = 8 Ω)	t_d	—	30	100	ns
Rise Time			t_r	—	100	300	
Storage Time			t_s	—	1000	3000	
Fall Time			t_f	—	60	300	
Storage Time		($V_{BE(off)}$ = 5 Vdc)	t_s	—	400	—	
Fall Time			t_f	—	130	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

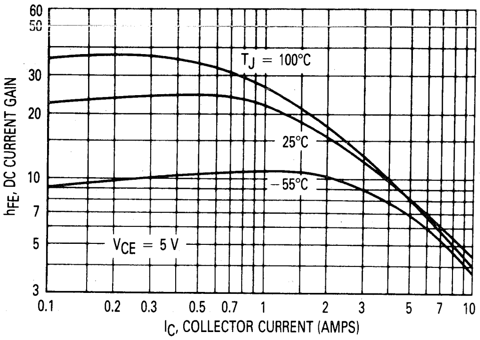


Figure 1. DC Current Gain

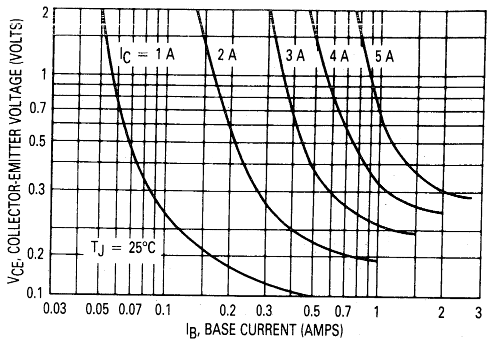


Figure 2. Collector Saturation Region

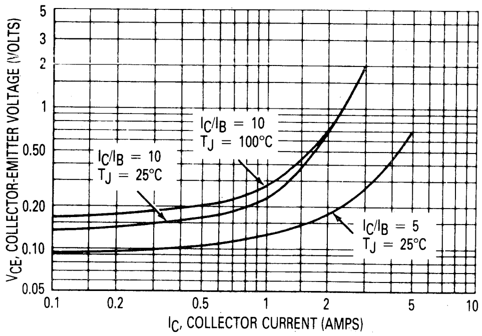


Figure 3. Collector-Emitter Saturation Region

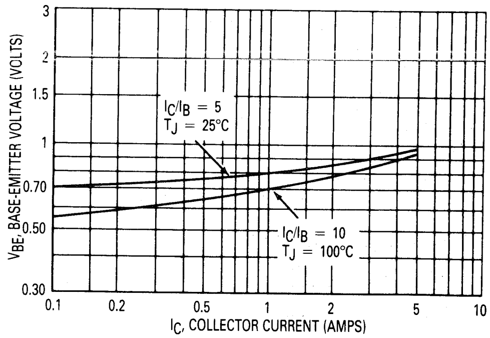


Figure 4. Base-Emitter Saturation Region

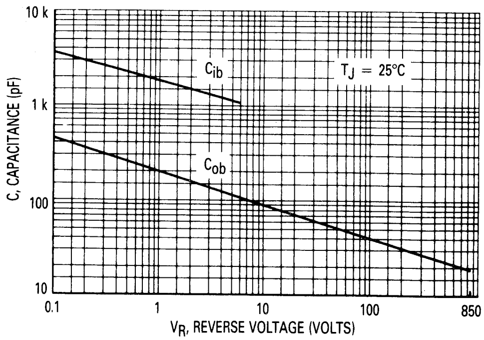


Figure 5. Capacitance

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TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

I_C/I_{B1} = 5, T_C = 75°C, $V_{CE(pk)}$ = 400 V

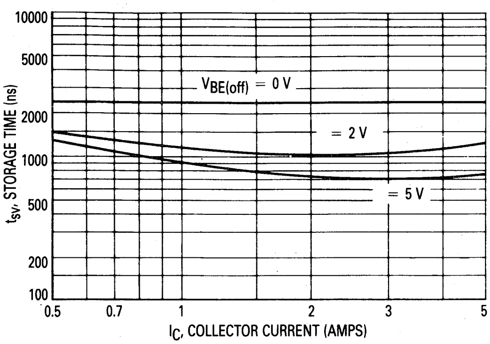


Figure 6. Storage Time

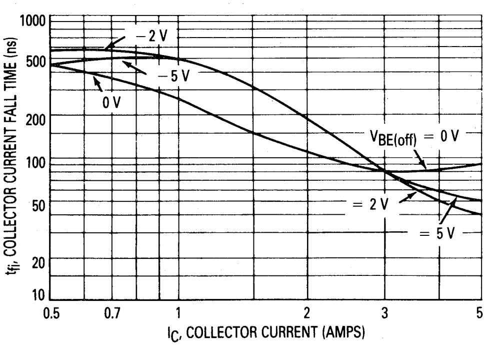


Figure 8. Collector Current Fall Time

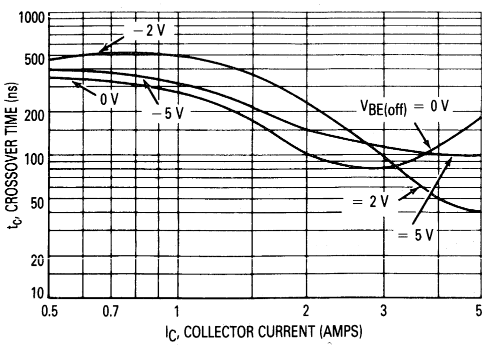


Figure 10. Crossover Time

I_C/I_{B1} = 10, T_C = 75°C, $V_{CE(pk)}$ = 400 V

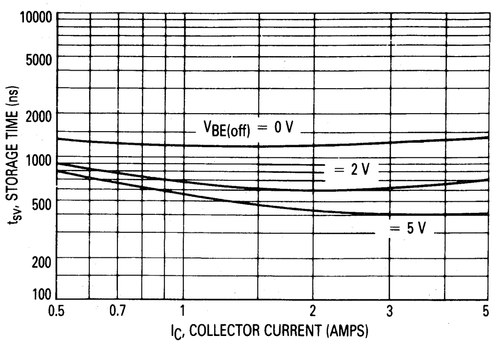


Figure 7. Storage Time

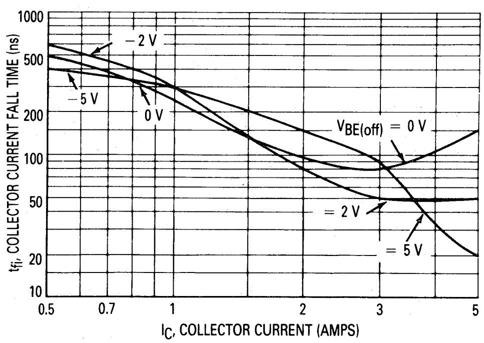


Figure 9. Collector Current Fall Time

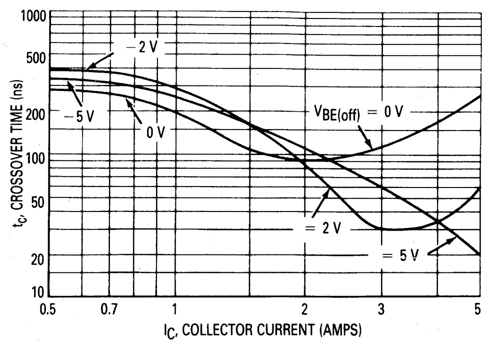
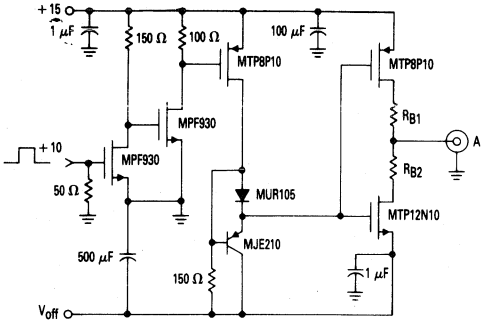


Figure 11. Crossover Time

Table 1. Inductive Load Switching

Drive Circuit



*Tektronix AM503 P6302 or Equivalent

Scope — Tektronix 7403 or Equivalent

$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

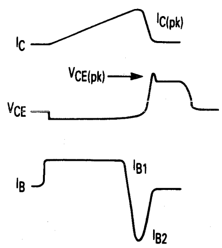
T_1 adjusted to obtain $I_{C(pk)}$

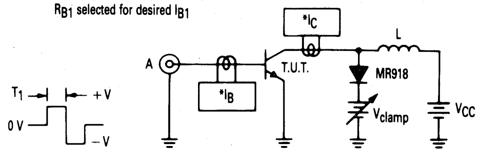
Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

$V_{CEO(sus)}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts
$I_{C(pk)}$ = 100 mA

Inductive Switching
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}





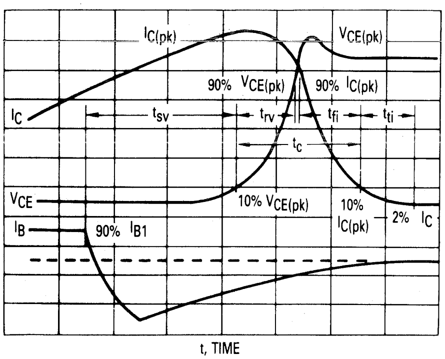


Figure 12. Inductive Switching Measurements

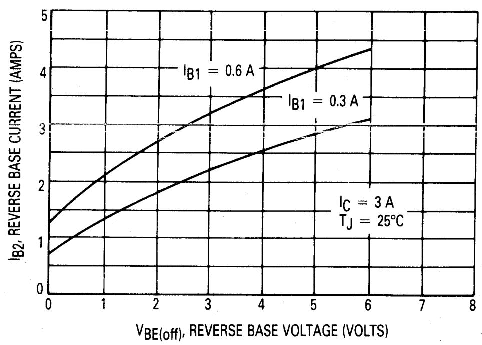
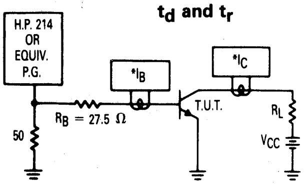


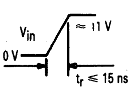
Figure 13. Peak Reverse Base Current

Table 2. Resistive Load Switching

t_d and t_r



V_{CC}	250 Vdc
R_L	83 Ω
I_C	3 Adc
I_B	0.4 Adc



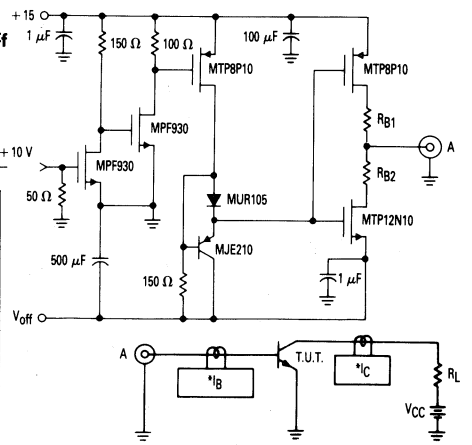
*Tektronix AM503 P6302 or Equivalent

t_s and t_f

$V_{(off)}$ adjusted to give specified off drive

V_{CC}	250 V
R_L	83 Ω
I_C	3 Adc
I_{B1}	0.4 Adc
I_{B2}	0.8 Adc
R_{B1}	37.5 Ω
R_{B2}	8 Ω

FOR $V_{BE(off)}$ = 5 V
R_{B2} = 0 Ω



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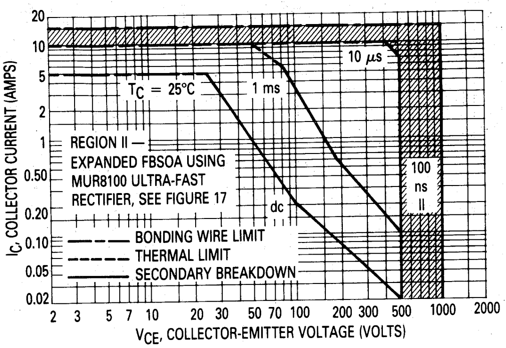
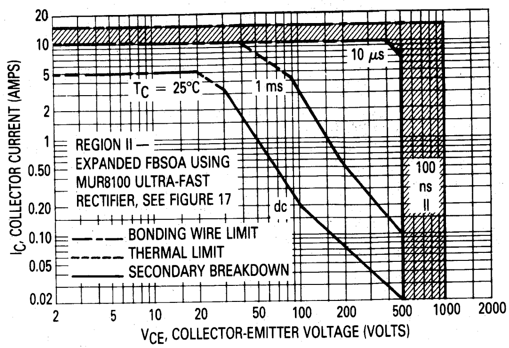
GUARANTEED OPERATING AREA INFORMATION



a. MJ16002A



b. MJH16002A

Figure 14. Maximum Rated Forward Biased Safe Operating Area

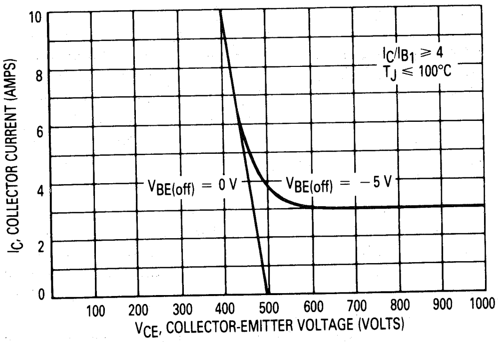


Figure 15. Maximum Reverse Biased Safe Operating Area

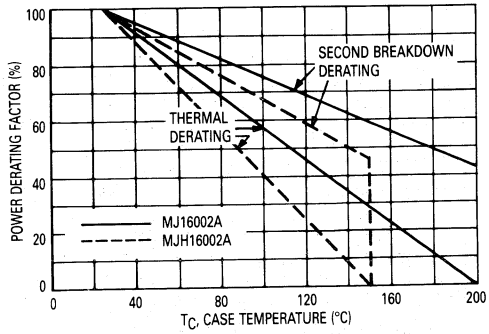


Figure 16. Power Derating

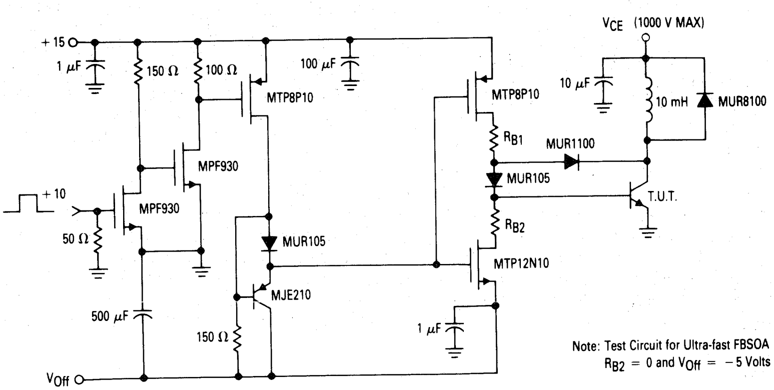


Figure 17. Switching Safe Operating Area

3

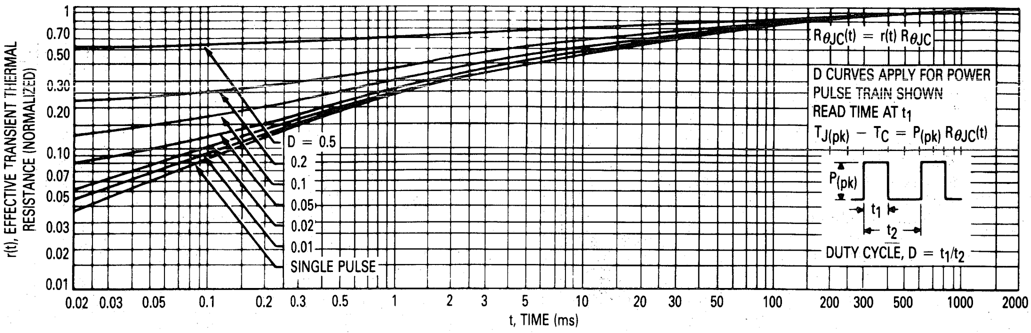


Figure 18. Thermal Response

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 14a or 14b is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 14a or 14b may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE III DESIGN CONSIDERATIONS

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector-emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{CEO(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN-ON —

Safe turn-on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra-fast recovery rectifiers, and are valid for turn-on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{CEO(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn-on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

3. TURN-OFF —

A bipolar transistor's ability to withstand turn-off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

SWITCHMODE III DESIGN CONSIDERATIONS (Cont.)

4. OPERATION ABOVE $V_{(BR)CEO(sus)}$ —

When bipolars are operated above collector-emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn-on, as a stiff negative bias is needed for safe turn-off. Any hiccup in the base-drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

5. RBSOA —

Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

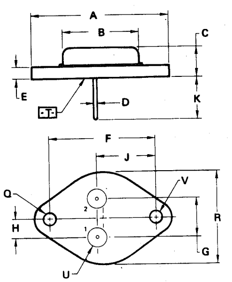
6. DESIGN SAMPLES —

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR4100 types are well-suited for higher drive requirements (see Article Reprint AR131).

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

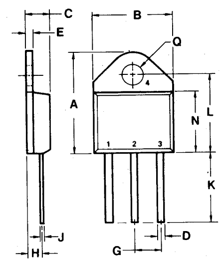
⌖	ϕ 0.13 (0.005) Ⓜ	T	V Ⓜ

FOR LEADS:

⌖	ϕ 0.13 (0.005) Ⓜ T	V Ⓜ	Q Ⓜ

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

CASE 1-05
TO-204AA
MJ16002A



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340-01
TO-218AC
MJH16002A

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

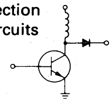
MJ16006 MJH16006
MJ16008 MJH16008

Designers Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16008 and MJH16008 are selected high gain versions of the MJ16006 and MJH16006 for applications where drive current is limited.

Typical Applications:
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits



Features:
- Fast Turn-Off Times
  - 70 ns Inductive Fall Time − 100°C (Typ)
  - 100 ns Inductive Crossover Time − 100°C (Typ)
  - 500 ns Inductive Storage Time − 100°C (Typ)
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Load
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

8.0 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
125 AND 150 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJ16006 MJ16008	MJH16006 MJH16008	Unit
Collector-Emitter Voltage	V_{CEO}	450		Vdc
Collector-Emitter Voltage	V_{CEV}	850		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	8.0		Adc
Collector Current — Peak (1)	I_{CM}	16		Adc
Base Current — Continuous	I_B	6.0		Adc
Base Current — Peak (1)	I_{BM}	12		Adc
Total Device Dissipation @ T_C = 25°C	P_D	150	125	Watts
@ T_C = 100°C		85.5	50	
Derate above 25°C		0.86	1.0	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	−55 to 150	°C

THERMAL CHARACTERISTICS

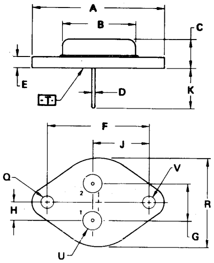
Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	1.0	°C/W
Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds.	T_L	275		°C

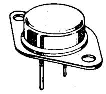
(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit Curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MJ16006
MJ16008





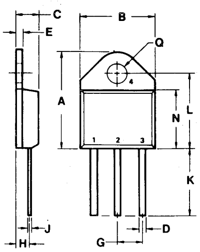
STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

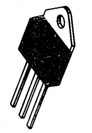
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ∅0.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ∅0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

CASE 1-05
TO-204AA

MJH16006
MJH16008





1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

3

MJ16006
MJH16006

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)							
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)			I_{CEV}	—	—	0.25	mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)				—	—	1.5	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 16			
ON CHARACTERISTICS (1)							
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.4 Adc)			$V_{CE(sat)}$	—	—	2.5	Vdc
(I_C = 5.0 Adc, I_B = 0.66 Adc)				—	—	3.0	
(I_C = 5.0 Adc, I_B = 0.66 Adc, T_C = 100°C)				—	—	3.0	
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.66 Adc)			$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 5.0 Adc, I_B = 0.66 Adc, T_C = 100°C)				—	—	1.5	
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 5.0 Vdc			h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	—	—	350	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(I_C = 5.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.66 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 1.3 Adc, R_{B2} = 4.0 Ω)	t_d	—	20	50	ns
Rise Time			t_r	—	85	250	
Storage Time			t_s	—	1000	2500	
Fall Time			t_f	—	70	250	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	500	—	
Fall Time			t_f	—	100	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 5.0 Adc, I_{B1} = 0.66 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	700	1800	ns
Fall Time			t_{fi}	—	80	200	
Crossover Time			t_c	—	150	250	
Storage Time		(T_J = 150°C)	t_{sv}	—	800	—	
Fall Time			t_{fi}	—	80	—	
Crossover Time			t_c	—	200	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

3

MJ16008
MJH16008

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc) (I_C = 5.0 Adc, I_B = 0.5 Adc) (I_C = 5.0 Adc, I_B = 0.5 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	— — —	2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc) (I_C = 5.0 Adc, I_B = 0.5 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 5.0 Vdc	h_{FE}	7.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	350	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 5.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.5 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 1.0 Adc, R_{B2} = 4.0 Ω)	t_d	—	20	50	ns
Rise Time			t_r	—	100	250	
Storage Time			t_s	—	900	2200	
Fall Time			t_f	—	70	250	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	400	—	
Fall Time			t_f	—	50	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 5.0 Adc, I_{B1} = 0.5 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	500	1400	ns
Fall Time			t_{fi}	—	70	150	
Crossover Time			t_c	—	100	200	
Storage Time		(T_J = 150°C)	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	100	—	
Crossover Time			t_c	—	150	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

3

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

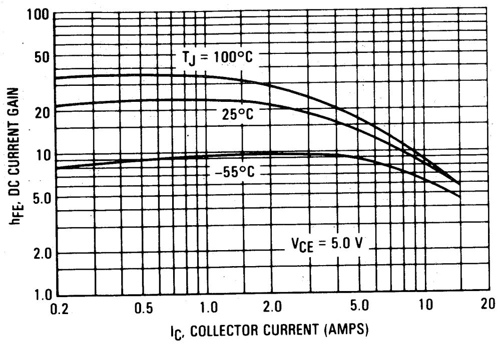


FIGURE 2 — COLLECTOR SATURATION REGION

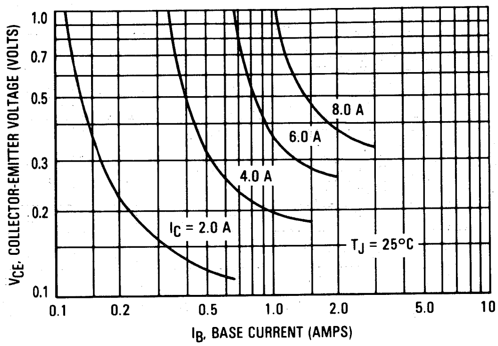


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

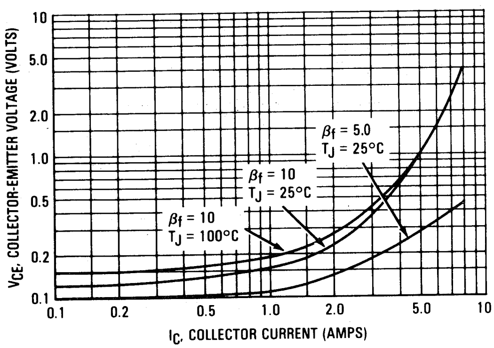


FIGURE 4 — BASE-EMITTER VOLTAGE

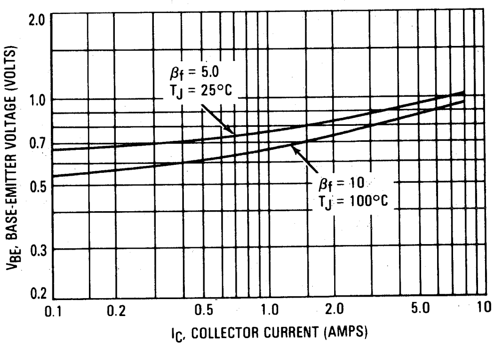


FIGURE 5 — COLLECTOR CUTOFF REGION

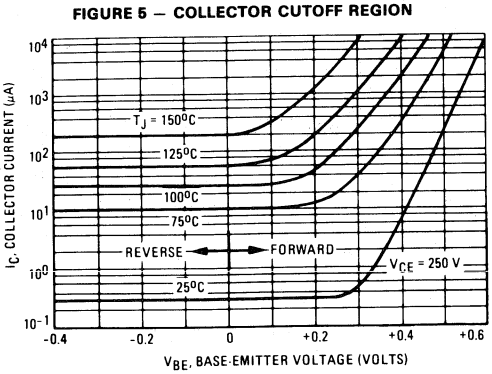
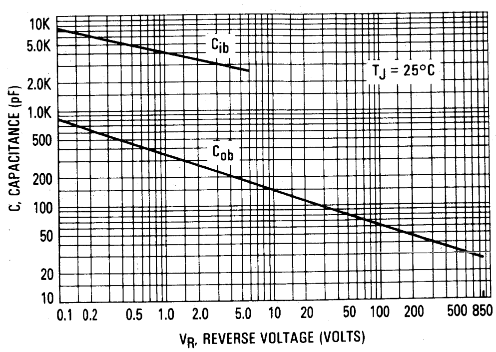


FIGURE 6 — CAPACITANCE



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TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

FIGURE 7 — STORAGE TIME

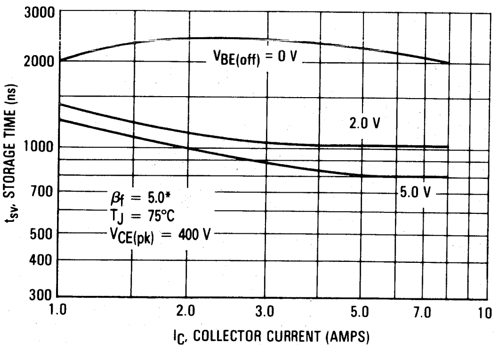


FIGURE 8 — STORAGE TIME

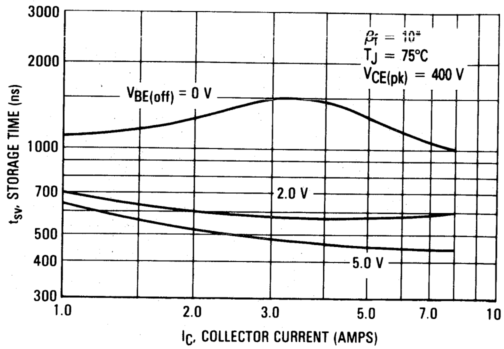


FIGURE 9 — COLLECTOR CURRENT FALL TIME

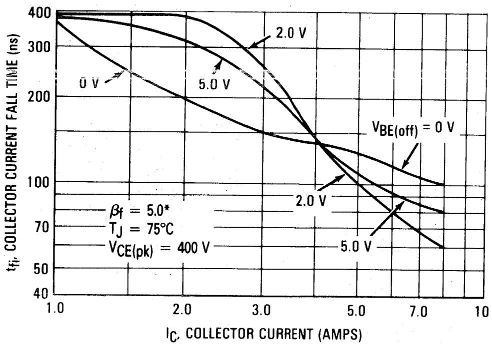


FIGURE 10 — COLLECTOR CURRENT FALL TIME

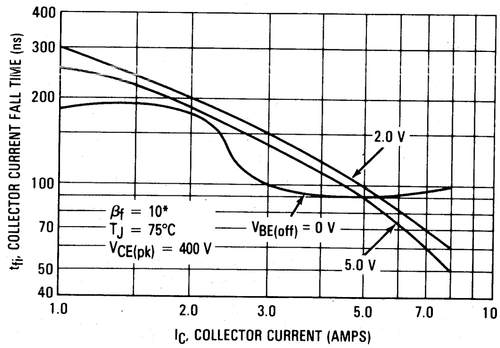


FIGURE 11 — CROSSOVER TIME

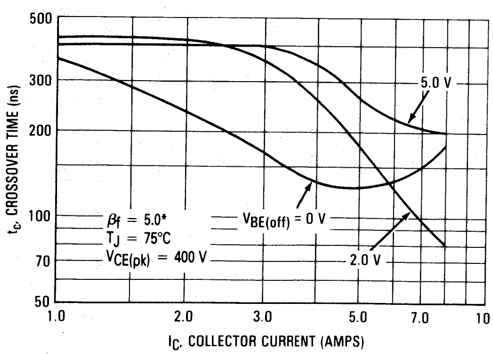
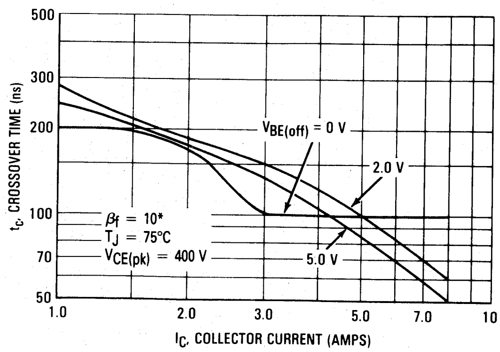


FIGURE 12 — CROSSOVER TIME



$*\beta_f = \frac{I_C}{I_{B1}}$

3

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

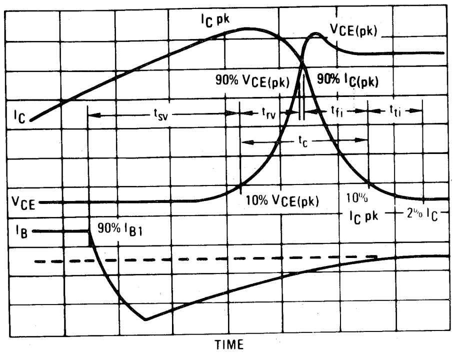


FIGURE 14 — PEAK REVERSE BASE CURRENT

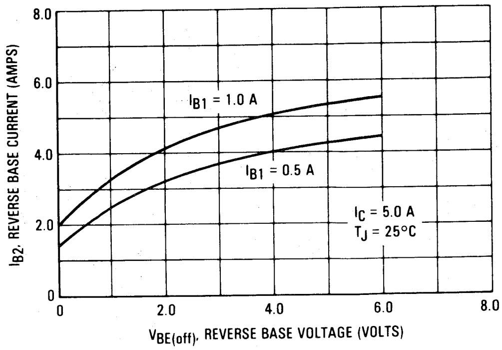
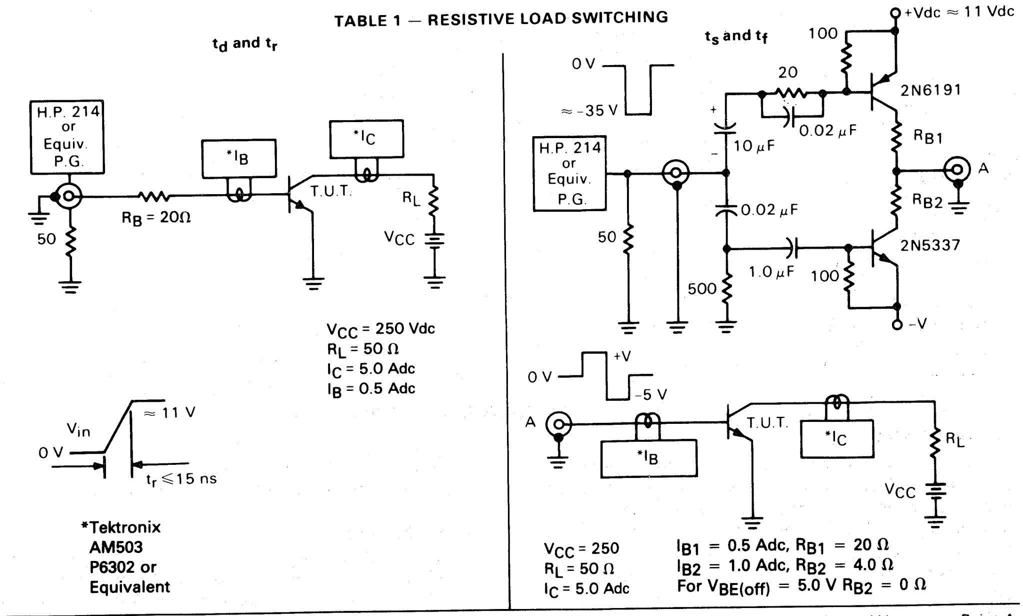


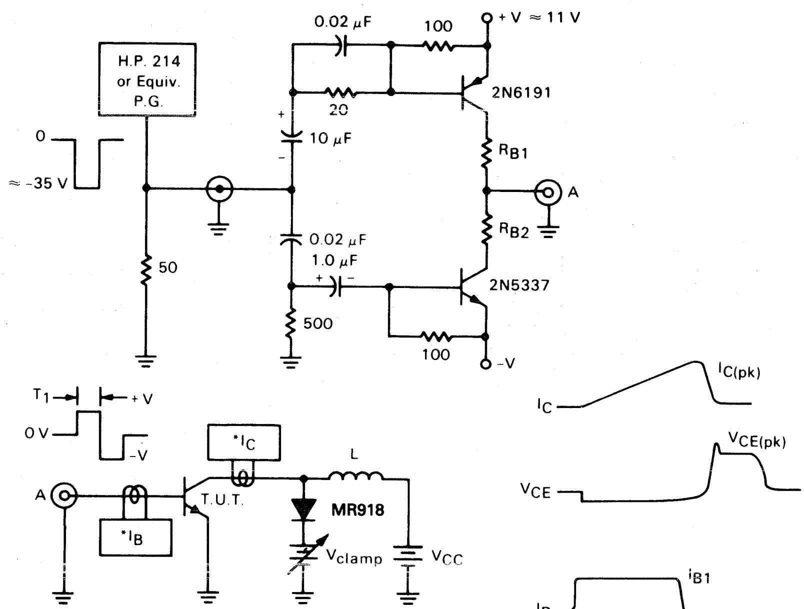
TABLE 1 — RESISTIVE LOAD SWITCHING



Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

3

TABLE 2 — INDUCTIVE LOAD SWITCHING



$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{CEO(sus)}$
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 Volts
$I_{C(pk)}$ = 100 mA
***Tektronix**
AM503
P6302 or
Equivalent

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Scope - Tektronix
7403 or
Equivalent

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 and 15A are based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 and 15A may be found at any case temperature by using the appropriate curve on Figure 17.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA, MJ16006 & MJ16008

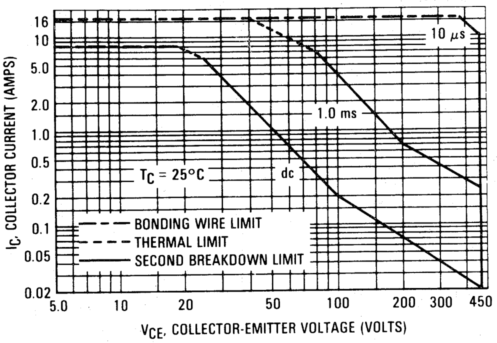


FIGURE 15A — SAFE OPERATING AREA, MJH16006 & MJH16008

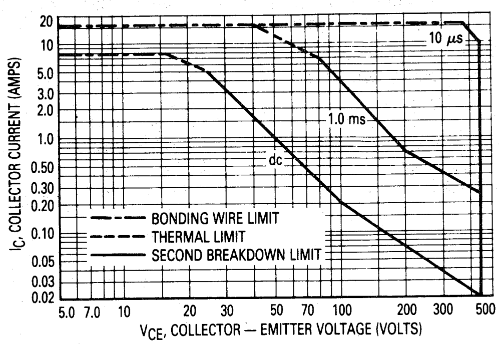


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA

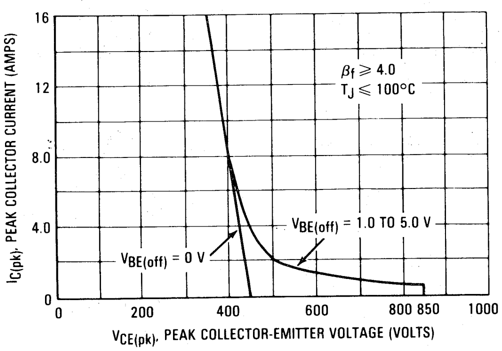


FIGURE 17 — POWER DERATING

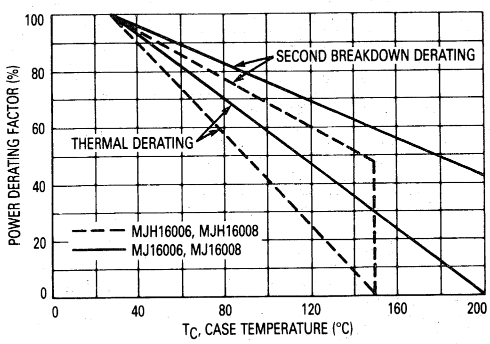
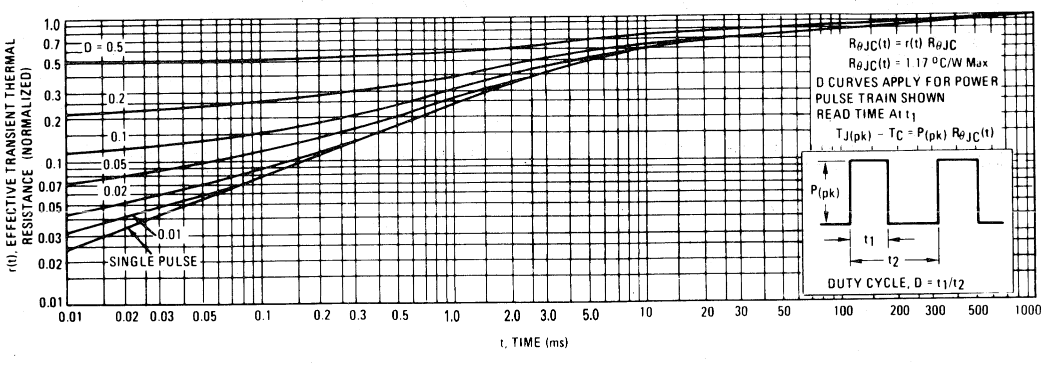


FIGURE 18 — THERMAL RESPONSE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

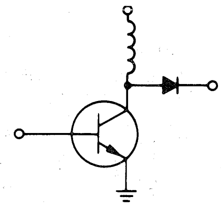
MJ16006A
MJH16006A

Designer's Data Sheet

NPN Silicon Power Transistors

1 kV Switchmode III Series

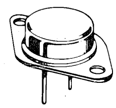
POWER TRANSISTORS
8 AMPERES
500 VOLTS
125 and 150 WATTS



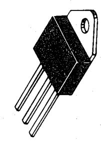
These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:
- Collector-Emitter Voltage — V_{CEV} = 1000 Vdc
- Fast Turn-Off Times
  80 ns Inductive Fall Time – 100°C (Typ)
  120 ns Inductive Crossover Time – 100°C (Typ)
  800 ns Inductive Storage Time – 100°C (Typ)
- 100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Load
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents
- Extended FBSOA Rating Using Ultra-fast Rectifiers
- Extremely High RBSOA Capability



CASE 1-05
TO-204AA
MJ16006A



CASE 340-01
TO-218AC
MJH16006A

MAXIMUM RATINGS

Rating	Symbol	MJ16006A	MJH16006A	Unit
Collector-Emitter Voltage	V_{CEO}	500		Vdc
Collector-Emitter Voltage	V_{CEV}	1000		Vdc
Emitter-Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	8 16		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	6 12		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	150 85 0.86	125 50 1	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	1	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	0.003	0.15	mAdc
(V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	0.020	1.0	
Collector Cutoff Current (V_{CE} = 1000 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	0.020	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	I_{EBO}	—	0.005	0.15	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14a or 14b			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 15			
ON CHARACTERISTICS(1)					
Collector-Emitter Saturation Voltage (I_C = 3 Adc, I_B = 0.6 Adc)	$V_{CE(sat)}$	—	0.35	0.7	Vdc
(I_C = 5 Adc, I_B = 1 Adc)		—	0.50	1	
(I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)		—	0.60	1.5	
Base-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc)	$V_{BE(sat)}$	—	1	1.5	Vdc
(I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)		—	1	1.5	
DC Current Gain (I_C = 8 Adc, V_{CE} = 5 Vdc)	h_{FE}	5	8	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)	C_{ob}	—	—	350	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Inductive Load (Table 1)							
Storage Time	(I_C = 5 Adc, I_{B1} = 0.66 Adc, $V_{BE(off)}$ = 5 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	800	2000	ns
Fall Time			t_{fi}	—	80	200	
Crossover Time			t_c	—	120	300	
Storage Time		(T_J = 150°C)	t_{sv}	—	1000	—	
Fall Time			t_{fi}	—	90	—	
Crossover Time			t_c	—	150	—	
Resistive Load (Table 2)							
Delay Time	(I_C = 5 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.66 Adc, PW = 30 μs, Duty Cycle ≤ 2%)	(I_{B2} = 1.3 Adc, R_{B2} = 4 Ω)	t_d	—	25	100	ns
Rise Time			t_r	—	400	700	
Storage Time			t_s	—	1400	3000	
Fall Time			t_f	—	175	400	
Storage Time		($V_{BE(off)}$ = 5 Vdc)	t_s	—	475	—	
Fall Time			t_f	—	100	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL STATIC CHARACTERISTICS

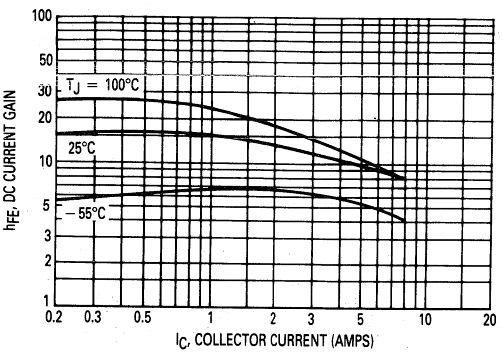


Figure 1. DC Current Gain

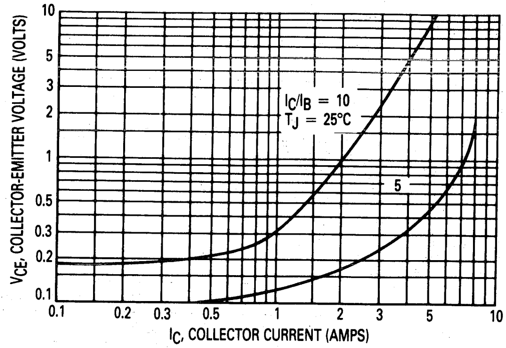


Figure 2. Collector-Emitter Saturation Region

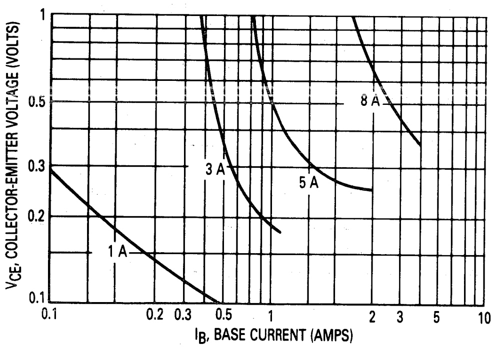


Figure 3. Collector-Emitter Saturation Region

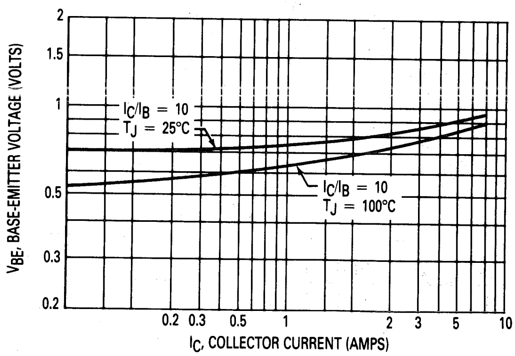


Figure 4. Base-Emitter Saturation Region

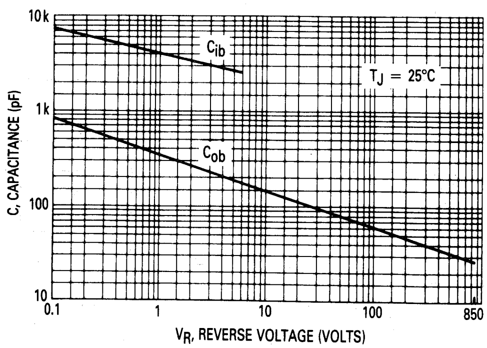


Figure 5. Capacitance

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

I_C/I_{B1} = 5, T_C = 75°C, $V_{CE(pk)}$ = 400 V | **I_C/I_{B1} = 10, T_C = 75°C, $V_{CE(pk)}$ = 400 V**

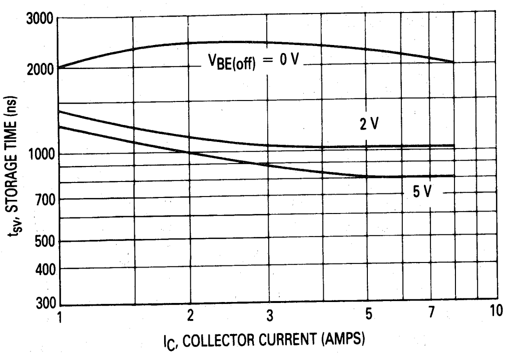


Figure 6. Storage Time

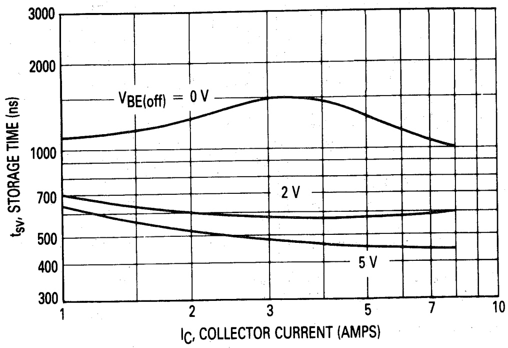
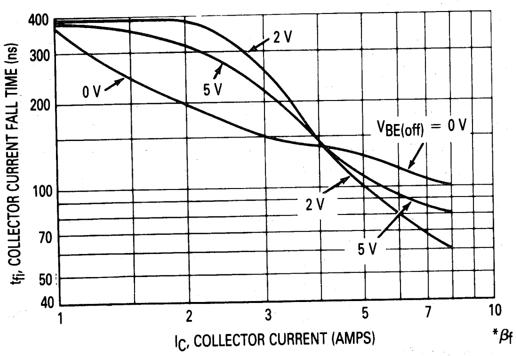


Figure 7. Storage Time



$*\beta_f = \frac{I_C}{I_{B1}}$

Figure 8. Collector Current Fall Time

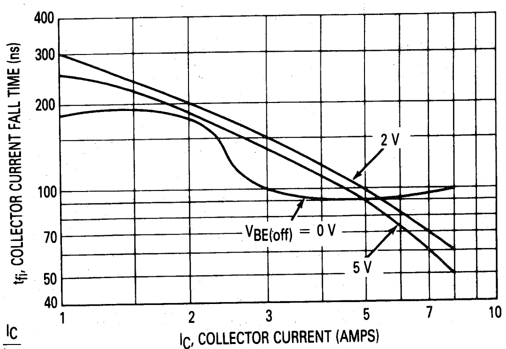


Figure 9. Collector Current Fall Time

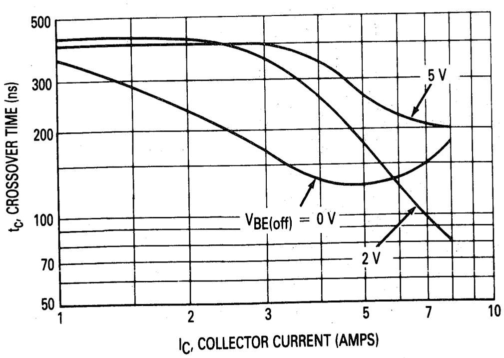


Figure 10. Crossover Time

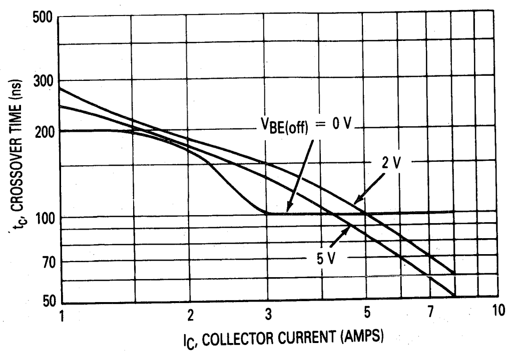
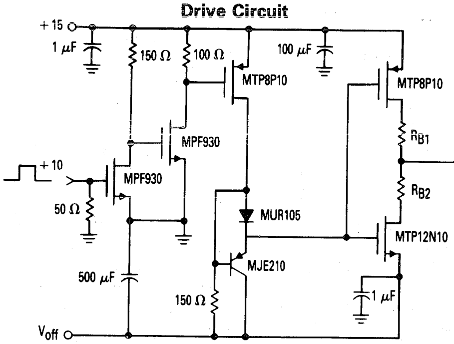


Figure 11. Crossover Time

3

Table 1. Inductive Load Switching

Drive Circuit



*Tektronix AM503
P6302 or Equivalent

Scope — Tektronix
7403 or Equivalent

$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

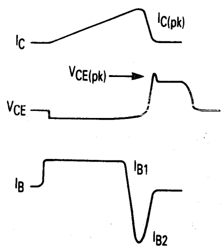
T_1 adjusted to obtain $I_{C(pk)}$

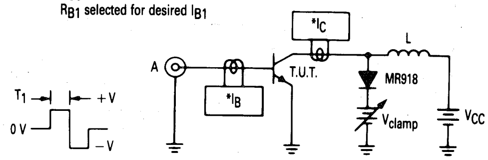
Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

$V_{CEO(sus)}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

Inductive Switching
L = 750 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 750 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}





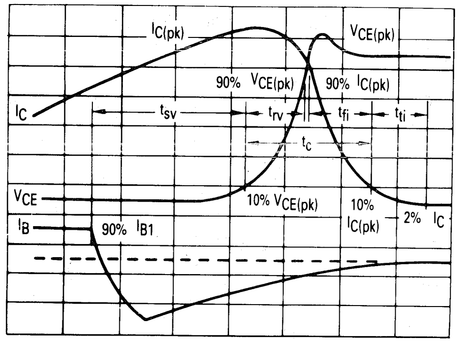


Figure 12. Inductive Switching Measurements

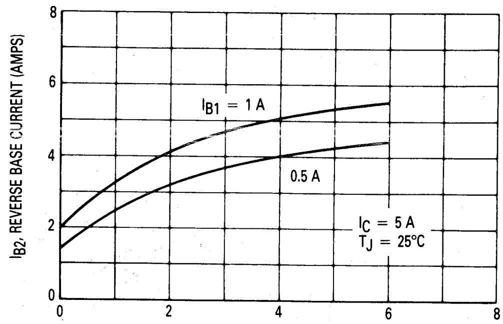
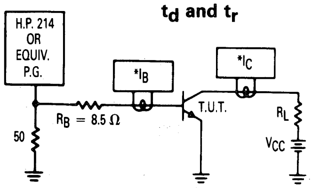
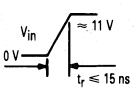


Figure 13. Peak Reverse Base Current

Table 2. Resistive Load Switching

t_d and t_r



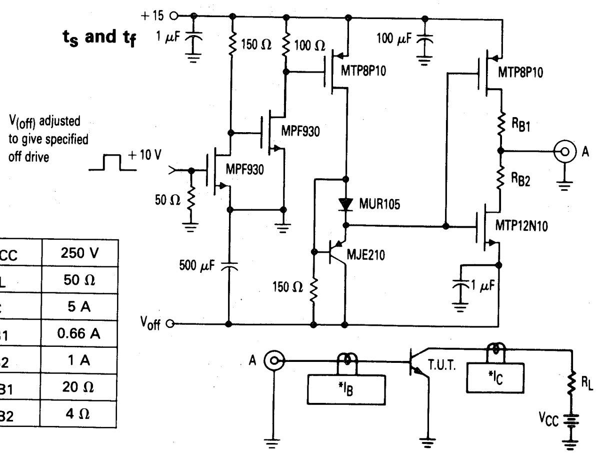


V_{CC}	250 V
R_L	50 Ω
I_C	5 A
I_B	0.66 A

*Tektronix AM503
P6302 or Equivalent

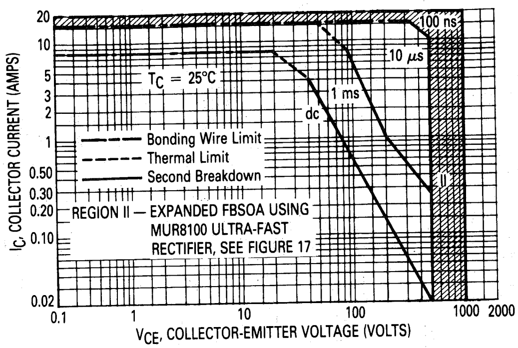
t_s and t_f

V_{CC}	250 V
R_L	50 Ω
I_C	5 A
I_{B1}	0.66 A
I_{B2}	1 A
R_{B1}	20 Ω
R_{B2}	4 Ω

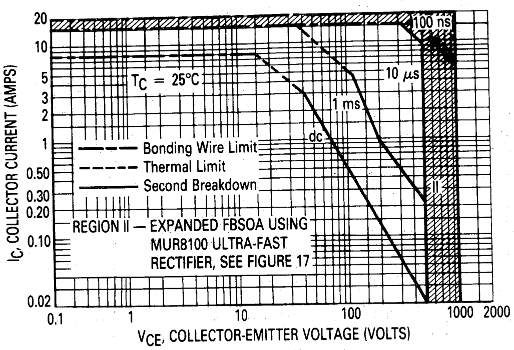


3

GUARANTEED SAFE OPERATING AREA LIMITS



a. MJ16006A



b. MJH16006A

Figure 14. Maximum Rated Forward Biased Safe Operating Area

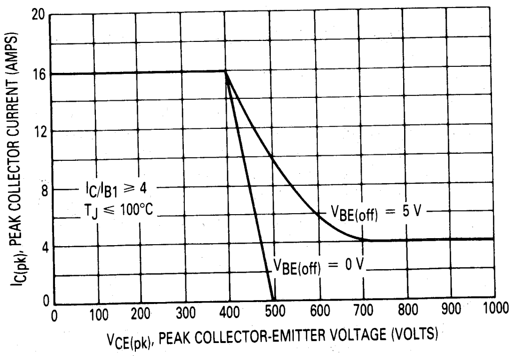


Figure 15. Maximum Reverse Biased Safe Operating Area

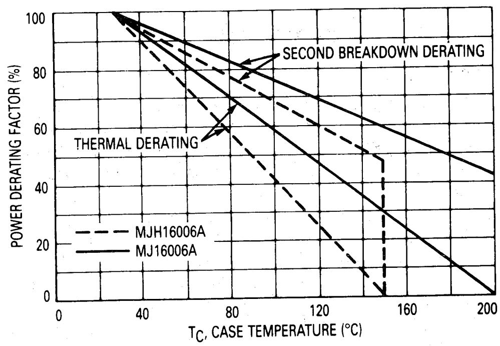
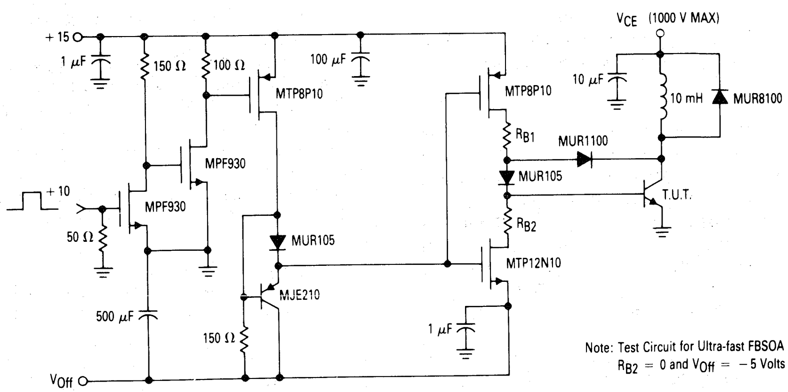


Figure 16. Power Derating



Note: Test Circuit for Ultra-fast FBSOA R_{B2} = 0 and V_{Off} = −5 Volts

Figure 17. Switching Safe Operating Area

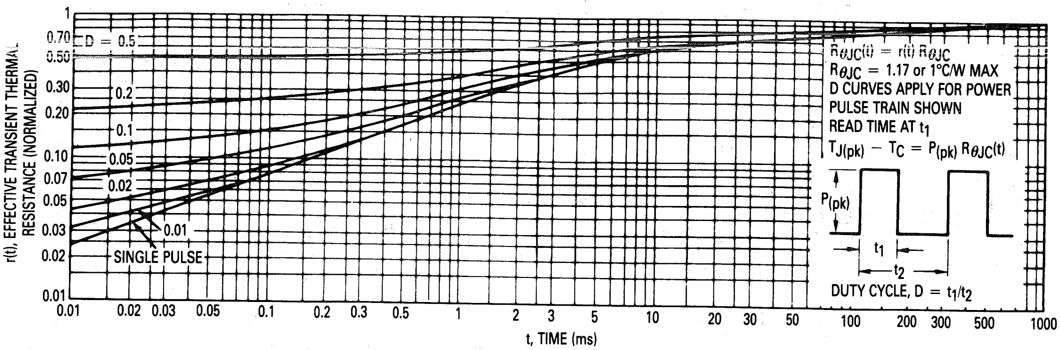


Figure 18. Thermal Response

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 14a and 14b is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 14a and 14b may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE III DESIGN CONSIDERATIONS

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector-emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{CEO(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN-ON —

Safe turn-on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra-fast recovery rectifiers, and are valid for turn-on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{CEO(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn-on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

3. TURN-OFF —

A bipolar transistor's ability to withstand turn-off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

SWITCHMODE III DESIGN CONSIDERATIONS (Cont.)

4. OPERATION ABOVE $V_{CEO(sus)}$ —

When bipolars are operated above collector-emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn-on, as is a stiff negative bias needed for safe turn-off. Any hiccup in the base-drive circuitry that even momemtarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

5. RBSOA —

Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

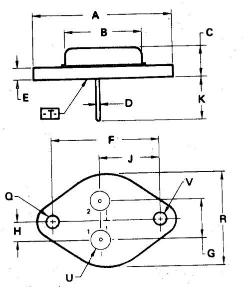
6. DESIGN SAMPLES —

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR4100 types are well-suited for higher drive requirements (see Article Reprint AR131).

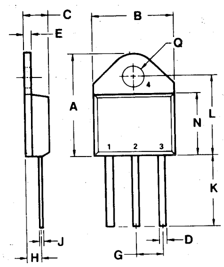
OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ | ϕ.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ | ϕ.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

CASE 1-05
TO-204AA
MJ16006A



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340-01
TO-218AC
MJH16006A

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

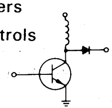
MJ16010 MJH16010
MJ16012 MJH16012

Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16012 and MJH16012 are selected high gain versions of the MJ16010 and MJH16010 for applications where drive current is limited.

Typical Applications:
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits



Features:
- Fast Turn-Off Times — $T_C = 100°C$
  50 ns Inductive Fall Time (Typ)
  90 ns Inductive Crossover Time (Typ)
  800 ns Inductive Storage Time (Typ)
- 100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents

15 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
135 AND 175 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJ16010 MJ16012	MJH16010 MJH16012	Unit
Collector-Emitter Voltage	V_{CEO}	450		Vdc
Collector-Emitter Voltage	V_{CEV}	850		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15		Adc
Total Device Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	 175 100 1.0	 135 53.8 1.11	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	-55 to 150	°C

THERMAL CHARACTERISTICS

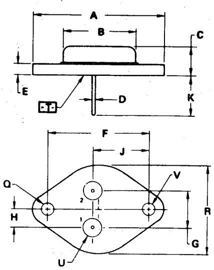
Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	0.93	°C/W
Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	275		°C

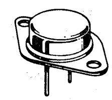
(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MJ16010
MJ16012





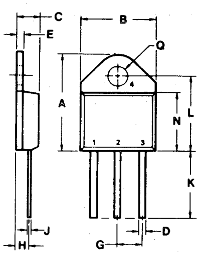
STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

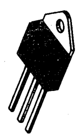
NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ ∅.13 (0.005) Ⓜ | T | V Ⓜ
   FOR LEADS:
   ⌖ ∅.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA

MJH16010
MJH16012





1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

3

MJ16010
MJH16010

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)			I_{CEV}	—	—	0.25	mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)				—	—	1.5	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 16			
ON CHARACTERISTICS (1)							
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.7 Adc)			$V_{CE(sat)}$	—	—	2.5	Vdc
(I_C = 10 Adc, I_B = 1.3 Adc)				—	—	3.0	
(I_C = 10 Adc, I_B = 1.3 Adc, T_C = 100°C)				—	—	3.0	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.3 Adc)			$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 10 Adc, I_B = 1.3 Adc, T_C = 100°C)				—	—	1.5	
DC Current Gain (I_C = 15 Adc, V_{CE} = 5.0 Vdc)			h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	—	—	400	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.3 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 2.6 Adc, R_B = 1.6 Ω)	t_d	—	20	—	ns
Rise Time			t_r	—	200	—	
Storage Time			t_s	—	1200	—	
Fall Time			t_f	—	200	—	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	650	—	
Fall Time			t_f	—	80	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.3 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	800	1800	ns
Fall Time			t_{fi}	—	50	200	
Crossover Time			t_c	—	90	250	
Storage Time		(T_C = 150°C)	t_{sv}	—	1050	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

3

MJ16012
MJH16012

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	— — —	2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 15 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	7.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	400	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.0 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 2.0 Adc, R_B = 1.6 Ω)	t_d	—	20	—	ns
Rise Time			t_r	—	200	—	
Storage Time			t_s	—	900	—	
Fall Time			t_f	—	150	—	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	500	—	
Fall Time			t_f	—	40	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	650	1500	ns
Fall Time			t_{fi}	—	30	150	
Crossover Time			t_c	—	50	200	
Storage Time		(T_C = 150°C)	t_{sv}	—	850	—	
Fall Time			t_{fi}	—	30	—	
Crossover Time			t_c	—	70	—	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

3

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

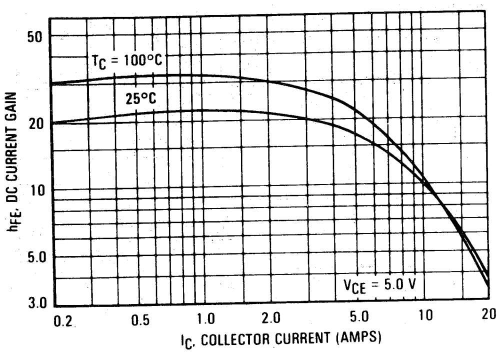


FIGURE 2 — COLLECTOR SATURATION REGION

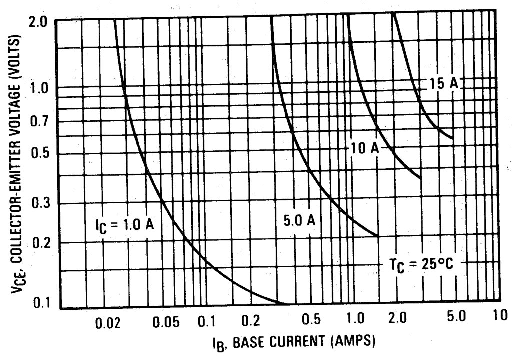


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

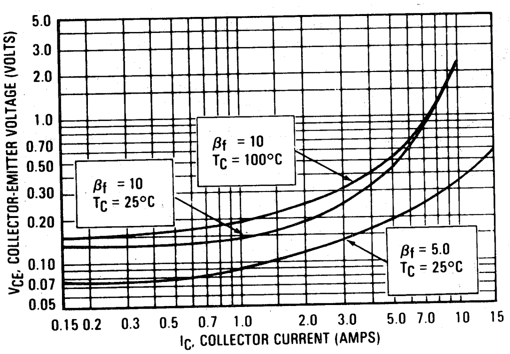


FIGURE 4 — BASE-EMITTER VOLTAGE

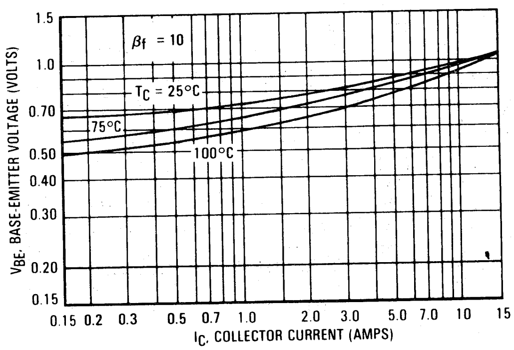


FIGURE 5 — COLLECTOR CUTOFF REGION

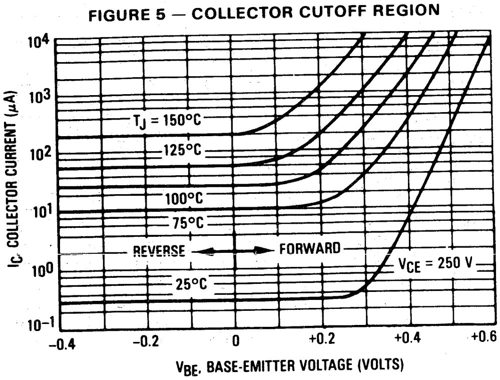
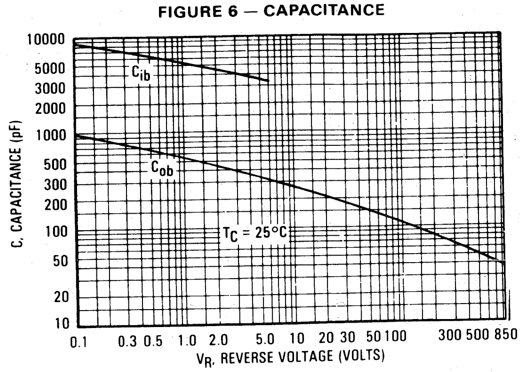


FIGURE 6 — CAPACITANCE



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TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

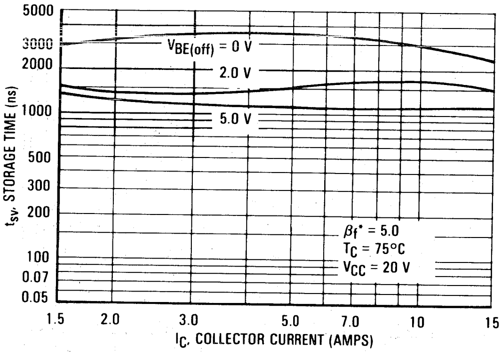


FIGURE 8 — STORAGE TIME

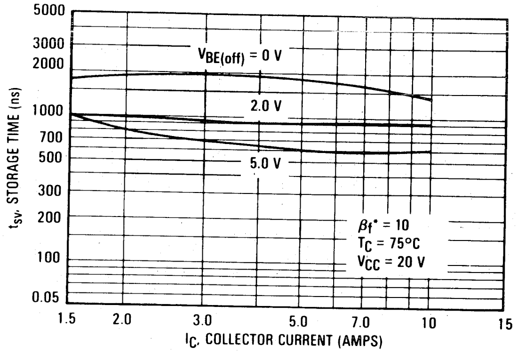


FIGURE 9 — COLLECTOR CURRENT FALL TIME

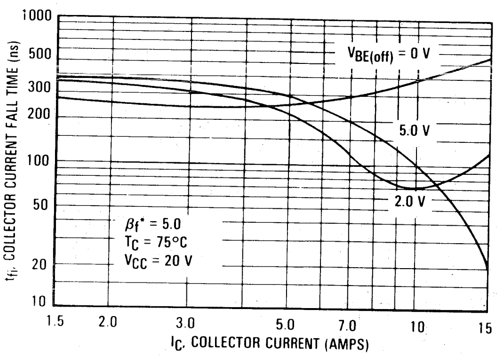


FIGURE 10 — COLLECTOR CURRENT FALL TIME

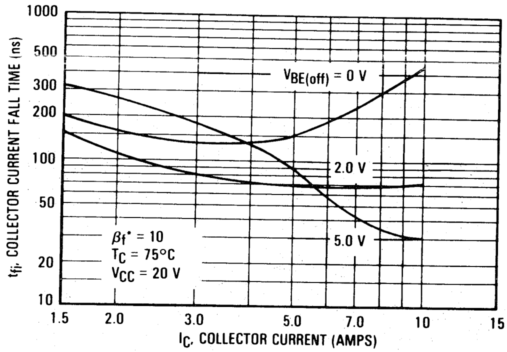


FIGURE 11 — CROSSOVER TIME

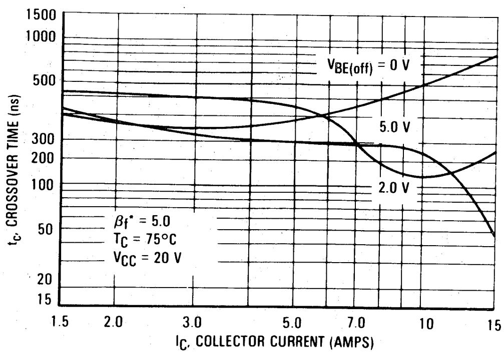
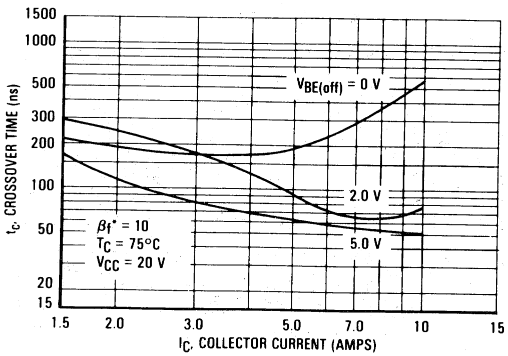


FIGURE 12 — CROSSOVER TIME



$*\beta_f = \frac{I_C}{I_{B1}}$

3

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

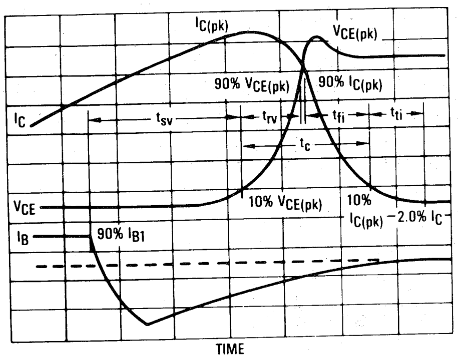
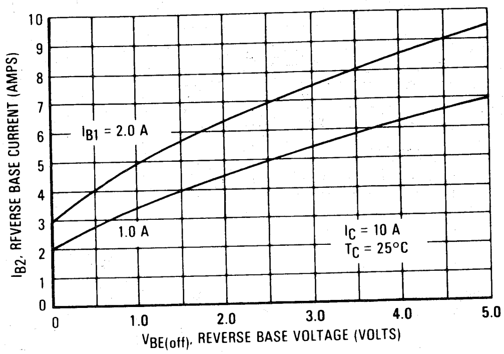


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

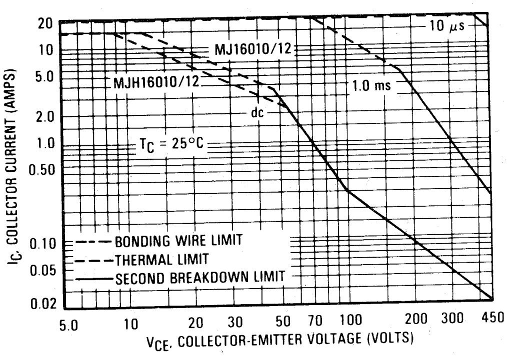
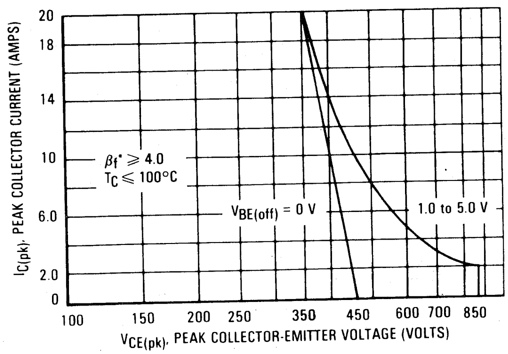


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



$*\beta_f = \frac{I_C}{I_{B1}}$

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

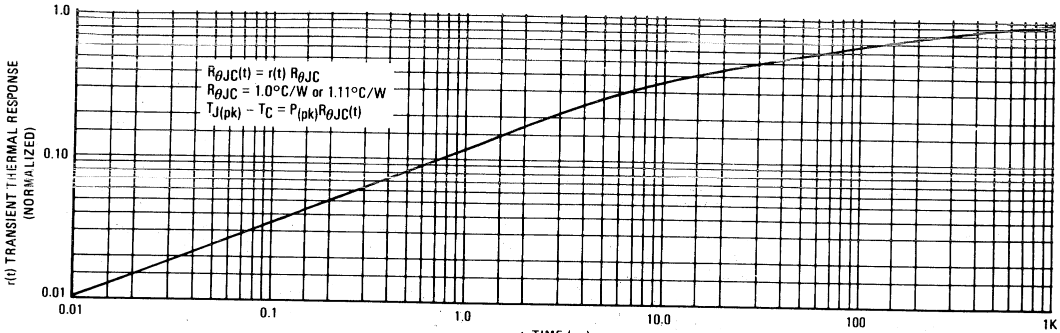


FIGURE 18 — POWER DERATING

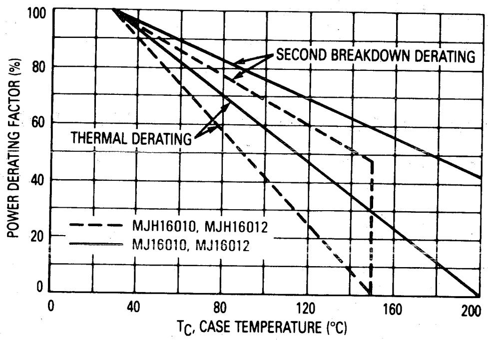
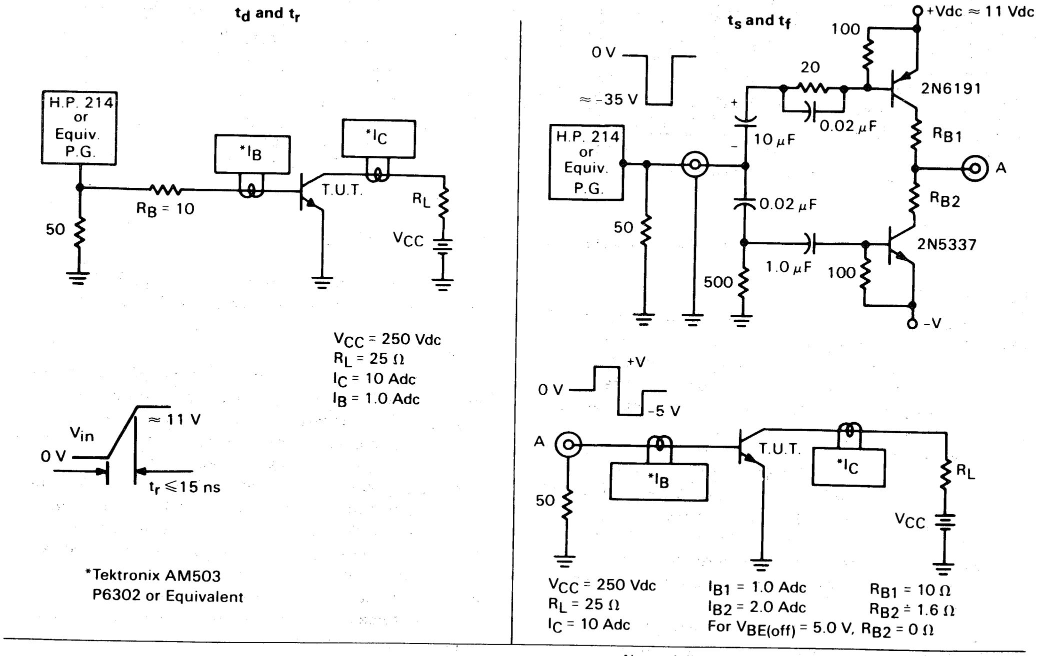
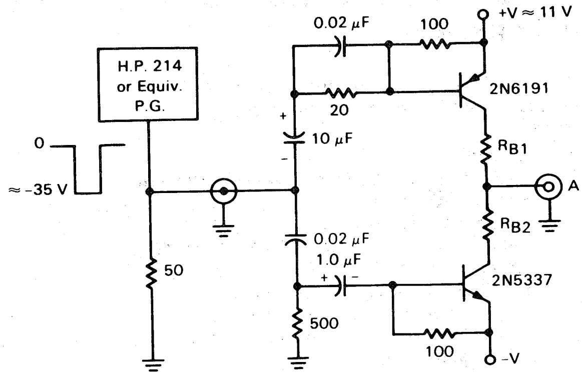


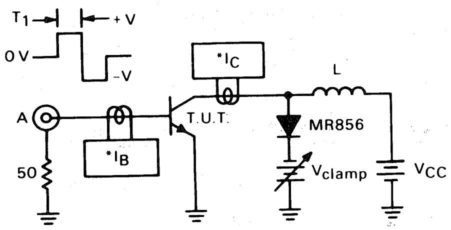
TABLE 1 — RESISTIVE LOAD SWITCHING

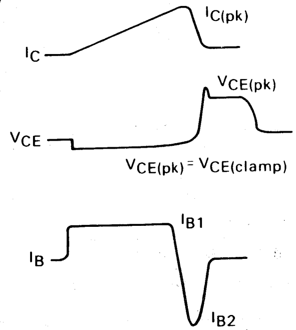


Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING







$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{CEO(sus)}$
$L = 10$ mH
$R_{B2} = \infty$
$V_{CC} = 20$ V Its

Inductive Switching
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ V
R_{B1} selected for desired I_{B1}

RBSOA
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ V
R_{B1} selected for desired I_{B1}

*Tektronix AM503
P6302 or Equivalent

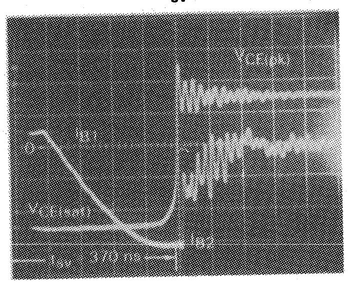
Scope — Tektronix
7403 or Equivalent

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

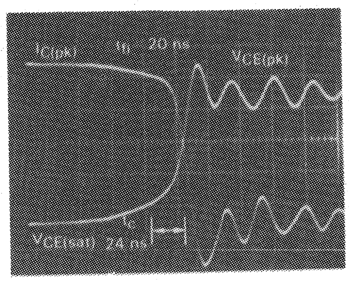
t_{sv}

$I_{C(pk)} = 10$ A
$I_{B1} = 1.0$ A
$V_{BE(off)} = 5.0$ V
$V_{CE(pk)} = 400$ V
$T_C = 25°C$
Time Base =
100 ns/cm



t_{fi}, t_c

$I_{C(pk)} = 10$ A
$I_{B1} = 1.0$ A
$V_{BE(off)} = 5.0$ V
$V_{CE(pk)} = 400$ V
$T_C = 25°C$
Time Base =
20 ns/cm



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ16010A
MJH16010A

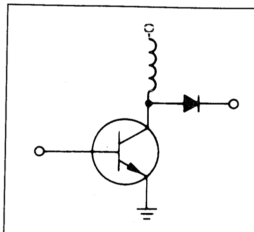
POWER TRANSISTORS
15 AMPERES
500 VOLTS
125 and 175 WATTS

Designer's Data Sheet

NPN Silicon Power Transistors

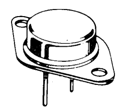
1 kV Switchmode III Series

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

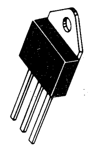


Typical Applications:
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:
- Collector-Emitter Voltage — V_{CEV} = 1000 Vdc
- Fast Turn-Off Times
  50 ns Inductive Fall Time — 100°C (Typ)
  90 ns Inductive Crossover Time — 100°C (Typ)
  900 ns Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Load
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents
- Extended FBSOA Rating Using Ultra-fast Rectifiers
- Extremely High RBSOA Capability



CASE 1-05
TO-204AA
MJ16010A



CASE 340-01
TO-218AC
MJH16010A

MAXIMUM RATINGS

Rating	Symbol	MJ16010A	MJH16010A	Unit
Collector-Emitter Voltage	V_{CEO}	500		Vdc
Collector-Emitter Voltage	V_{CEV}	1000		Vdc
Emitter-Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	15 20		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	175 100 1	135 54 1.09	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	0.92	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	0.003 0.020	0.15 1.0	mAdc
Collector Cutoff Current (V_{CE} = 1000 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	0.020	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	I_{EBO}	—	0.005	0.15	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14a or 14b			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 15			
ON CHARACTERISTICS(1)					
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc) (I_C = 10 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	0.25 0.45 0.60	0.7 1 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	1.2 1.2	1.5 1.5	Vdc
DC Current Gain (I_C = 15 Adc, V_{CE} = 5 Vdc)	h_{FE}	5	8	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)	C_{ob}	—	—	400	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Inductive Load (Table 1)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.3 Adc, $V_{BE(off)}$ = 5 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	900	2000	ns
Fall Time			t_{fi}	—	50	250	
Crossover Time			t_c	—	90	300	
Storage Time		(T_J = 150°C)	t_{sv}	—	1100	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	
Resistive Load (Table 2)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.3 Adc, PW = 30 μs, Duty Cycle ≤ 2%)	(I_{B2} = 2.6 Adc, R_{B2} = 1.6 Ω)	t_d	—	25	100	ns
Rise Time			t_r	—	325	600	
Storage Time			t_s	—	1300	3000	
Fall Time			t_f	—	175	400	
Storage Time		($V_{BE(off)}$ = 5 Vdc)	t_s	—	700	—	
Fall Time			t_f	—	80	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL STATIC CHARACTERISTICS

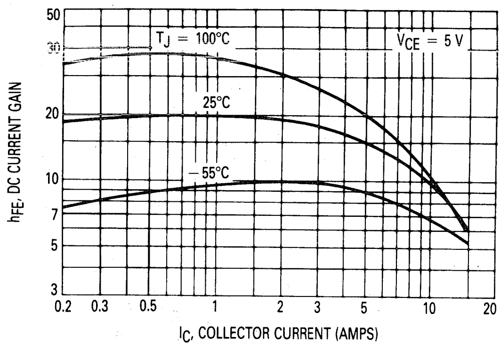


Figure 1. DC Current Gain

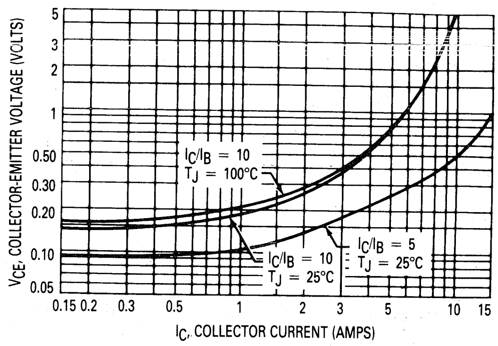


Figure 2. Collector-Emitter Saturation Region

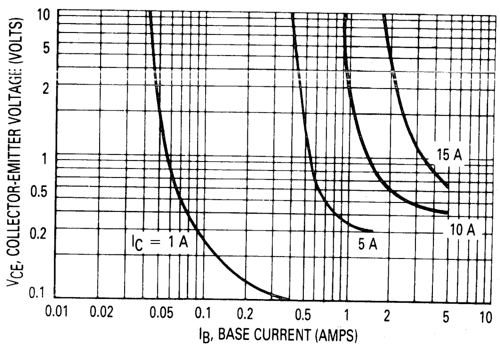


Figure 3. Collector-Emitter Saturation Region

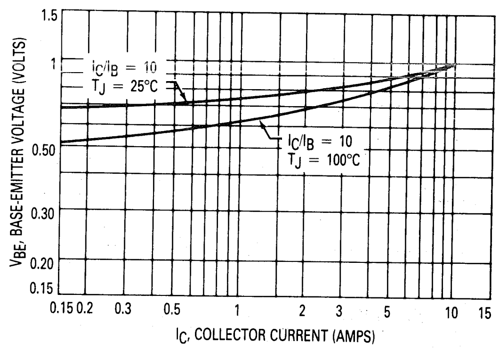


Figure 4. Base-Emitter Saturation Region

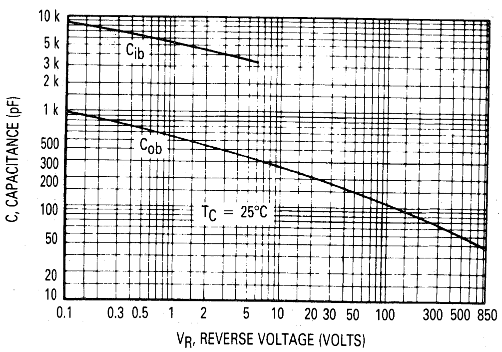


Figure 5. Capacitance

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

$I_C/I_{B1} = 5$, $T_C = 75°C$, $V_{CE(pk)} = 400$ V

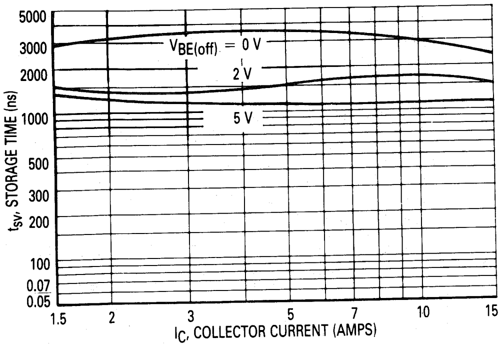


Figure 6. Storage Time

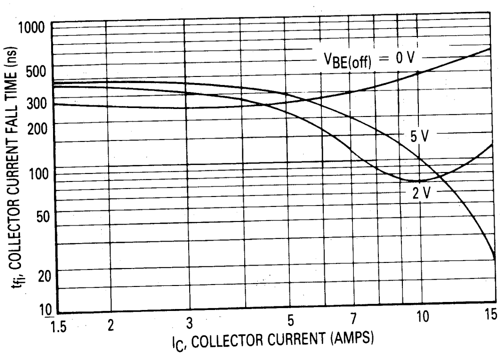


Figure 8. Collector Current Fall Time

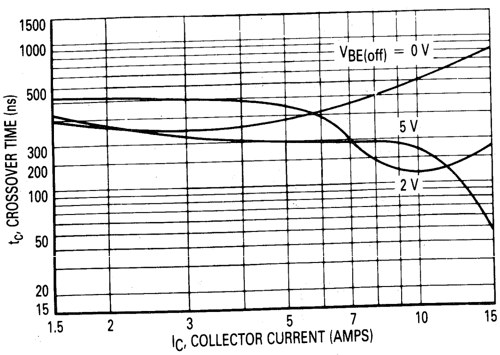


Figure 10. Crossover Time

$I_C/I_{B1} = 10$, $T_C = 75°C$, $V_{CE(pk)} = 400$ V

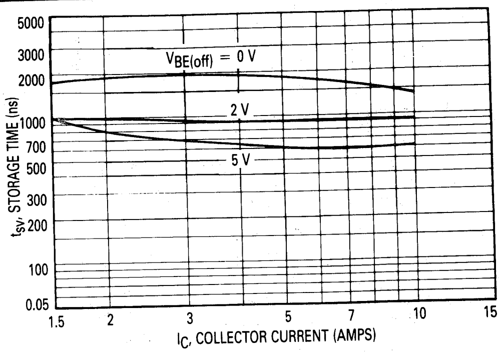


Figure 7. Storage Time

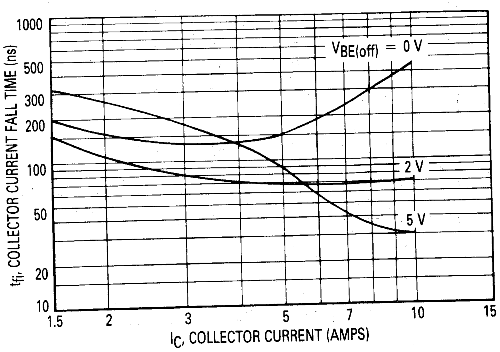


Figure 9. Collector Current Fall Time

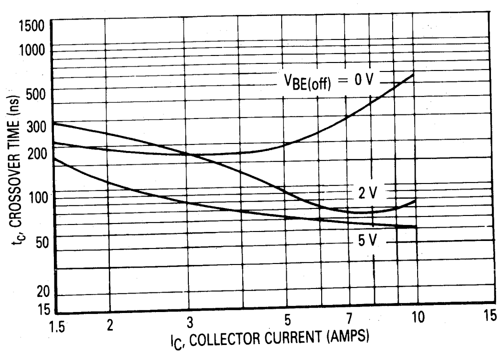
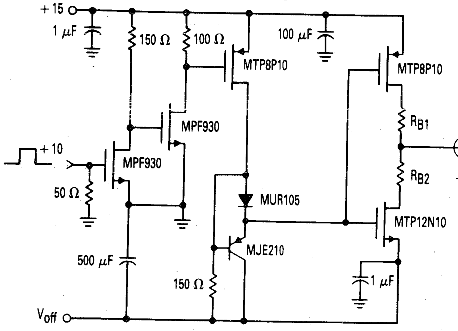


Figure 11. Crossover Time

Table 1. Inductive Load Switching

Drive Circuit



*Tektronix AM503 P6302 or Equivalent

Scope — Tektronix 7403 or Equivalent

$T_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$

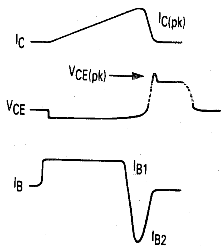
T_1 adjusted to obtain $I_{C(pk)}$

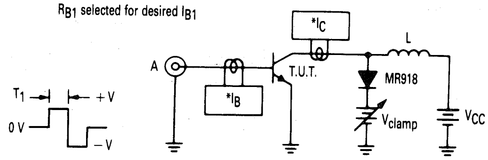
Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

$V_{CEO(sus)}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts
$I_{C(pk)}$ = 100 mA

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}





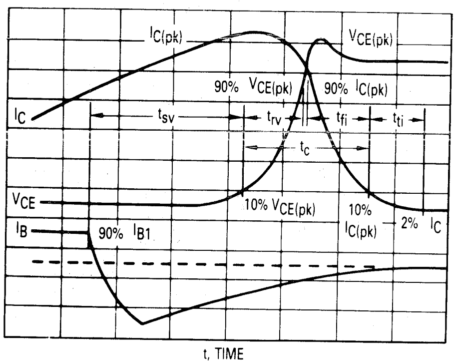


Figure 12. Inductive Switching Measurements

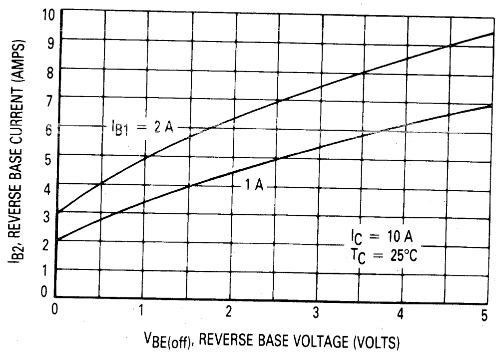
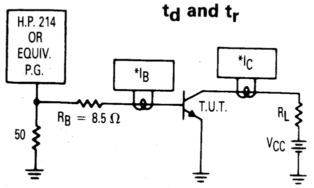
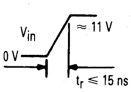


Figure 13. Peak Reverse Base Current

Table 2. Resistive Load Switching

t_d and t_r



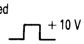


V_{CC}	250 V
R_L	25 Ω
I_C	10 A
I_B	1.3 A

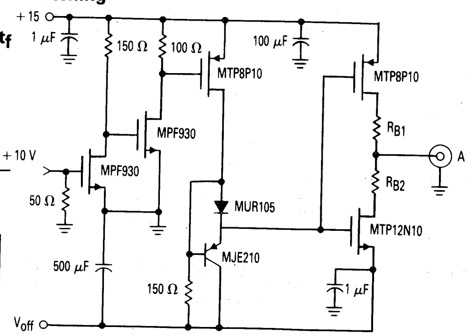
*Tektronix AM503 P6302 or Equivalent

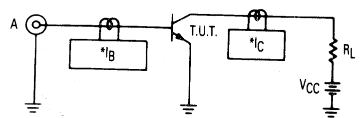
t_s and t_f

$V_{(off)}$ adjusted to give specified off drive

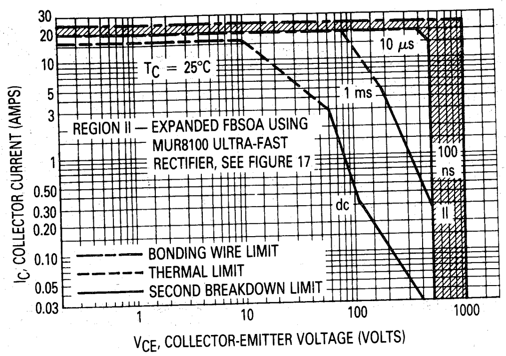


V_{CC}	250 V
I_C	10 A
I_{B1}	1.3 A
I_{B2}	Per Spec
R_{B1}	11.5 Ω
R_{B2}	Per Spec
R_L	25 Ω

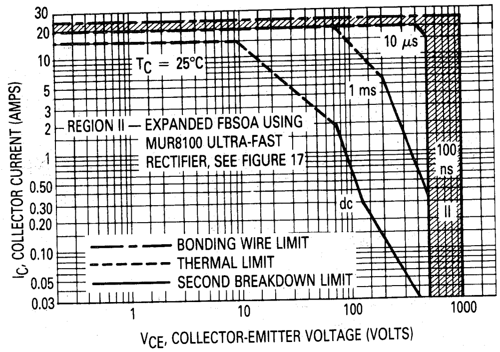




GUARANTEED OPERATING AREA INFORMATION



a. MJ16010A



b. MJH16010A

Figure 14. Maximum Rated Forward Biased Safe Operating Area

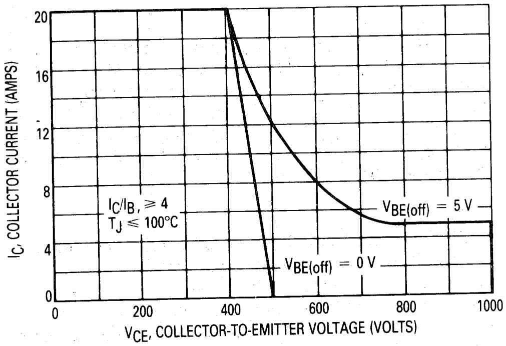


Figure 15. Maximum Reverse Biased Safe Operating Area

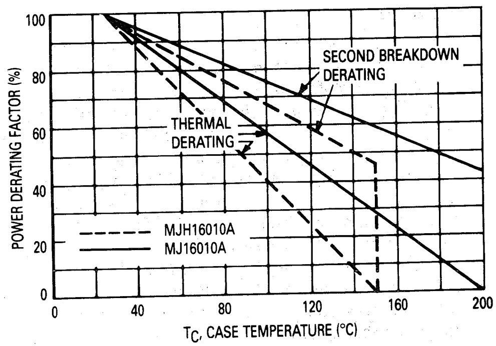


Figure 16. Power Derating

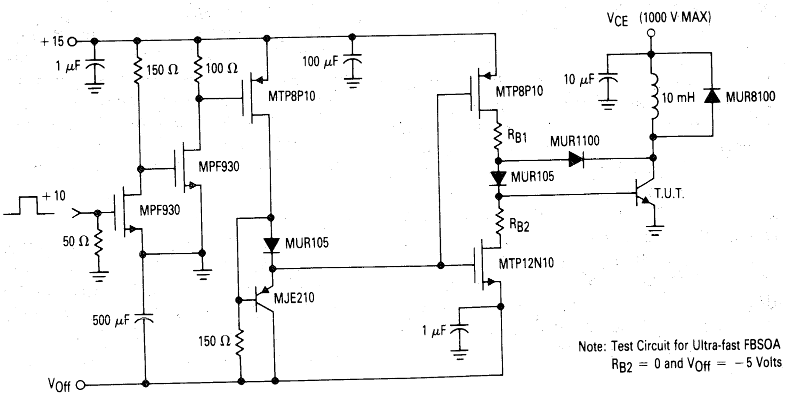


Figure 17. Switching Safe Operating Area

3

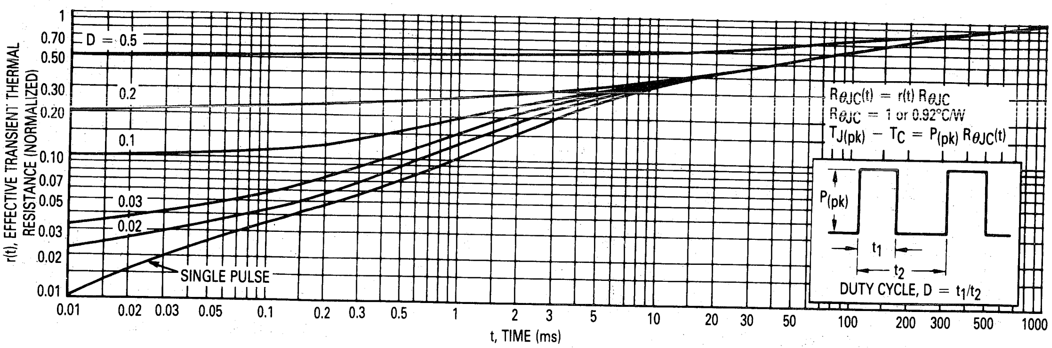


Figure 18. Thermal Response

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 14a and 14b is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 14a and 14b may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE III DESIGN CONSIDERATIONS

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector-emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{CEO(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN-ON —

Safe turn-on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra-fast recovery rectifiers, and are valid for turn-on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{CEO(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn-on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

3. TURN-OFF —

A bipolar transistor's ability to withstand turn-off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

SWITCHMODE III DESIGN CONSIDERATIONS (Cont.)

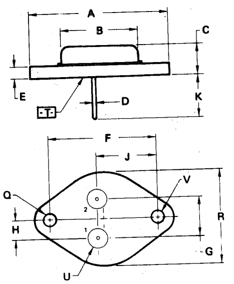
4. OPERATION ABOVE $V_{CEO(sus)}$ —
When bipolars are operated above collector-emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn-on, as is a stiff negative bias needed for safe turn-off. Any hiccup in the base-drive circuitry that even momemtarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

5. RBSOA —
Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

6. DESIGN SAMPLES —
Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —
Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR4100 types are well-suited for higher drive requirements (see Article Reprint AR131).

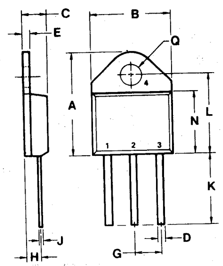
OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
   ⌖ 0.13 (0.005) Ⓜ T V Ⓜ
   FOR LEADS:
   ⌖ 0.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

CASE 1-05
TO-204AA
MJ16010A



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

CASE 340-01
TO-218AC
MJH16010A

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ16014
MJ16016

Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16016 is a selected high-gain version of the MJ16014 for applications where drive current is limited.

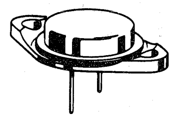
Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  40 ns Inductive Fall Time — 75°C (Typ)
  40 ns Inductive Crossover Time — 75°C (Typ)
  800 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents

20 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
250 WATTS



Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

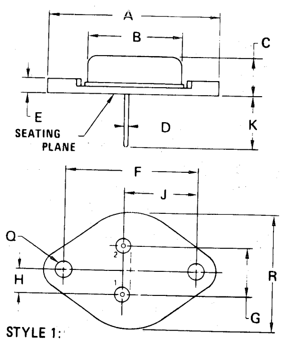
MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 20	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

MJ16014

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.25	
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 1.3 Adc)		—	—	2.5	
(I_C = 15 Adc, I_B = 2.0 Adc)		—	—	3.0	
(I_C = 15 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	—	3.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 15 Adc, I_B = 2.0 Adc)		—	—	1.5	
(I_C = 15 Adc, I_B = 2.0 Adc, T_C = 100°C)		—	—	1.5	
DC Current Gain (I_C = 20 Adc, V_{CE} = 5.0 Vdc	h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	500	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 15 Adc, V_{CC} = 250 Vdc, I_{B1} = 2.0 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 4.0 Adc, R_B = 1.6 Ω)	t_d	—	20	50	ns
Rise Time			t_r	—	200	500	
Storage Time			t_s	—	1200	2700	
Fall Time			t_f	—	200	350	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	650	—	
Fall Time			t_f	—	80	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 15 Adc, I_{B1} = 2.0 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	800	2700	ns
Fall Time			t_{fi}	—	50	200	
Crossover Time			t_c	—	90	250	
Storage Time		(T_C = 150°C)	t_{sv}	—	1050	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$^*\beta_f = \frac{I_C}{I_{B1}}$

3

MJ16016

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.25	mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	—	—	2.5	Vdc
(I_C = 15 Adc, I_B = 1.5 Adc)		—	—	3.0	
(I_C = 15 Adc, I_B = 1.5 Adc, T_C = 100°C)		—	—	3.0	
Base-Emitter Saturation Voltage (I_C = 15 Adc, I_B = 1.5 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 15 Adc, I_B = 1.5 Adc, T_C = 100°C)		—	—	1.5	
DC Current Gain (I_C = 20 Adc, V_{CE} = 5.0 Vdc	h_{FE}	7.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	500	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 15 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.5 Adc, PW = 30 μs, Duty Cycle ≤2.0%)	(I_{B2} = 3.0 Adc, R_B = 1.6 Ω)	t_d	—	20	50	ns
Rise Time			t_r	—	200	500	
Storage Time			t_s	—	900	2200	
Fall Time			t_f	—	100	250	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	500	—	
Fall Time			t_f	—	40	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 15 Adc, I_{B1} = 1.5 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	750	2500	ns
Fall Time			t_{fi}	—	30	150	
Crossover Time			t_c	—	50	200	
Storage Time		(T_C = 150°C)	t_{sv}	—	900	—	
Fall Time			t_{fi}	—	30	—	
Crossover Time			t_c	—	70	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

*$\beta_f = \frac{I_C}{I_{B1}}$

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

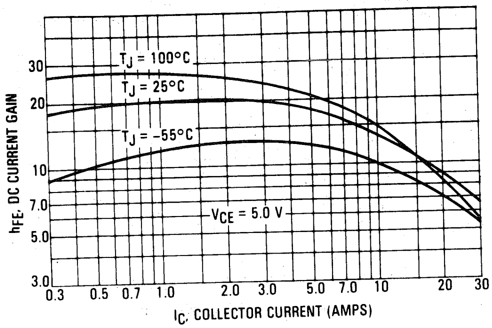


FIGURE 2 — COLLECTOR SATURATION REGION

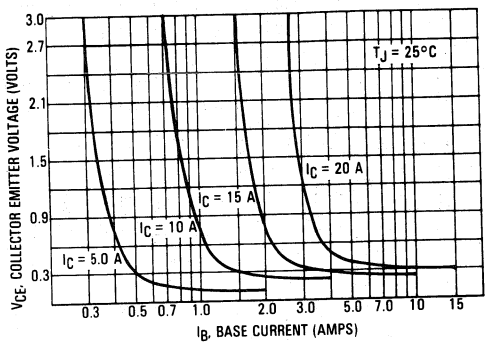


FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION

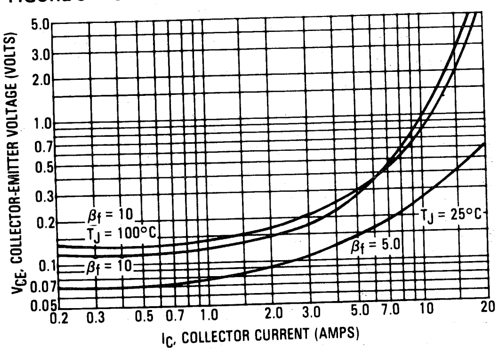


FIGURE 4 — BASE-EMITTER VOLTAGE

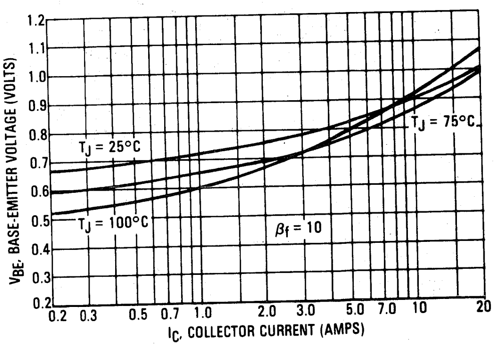


FIGURE 5 — COLLECTOR CUTOFF REGION

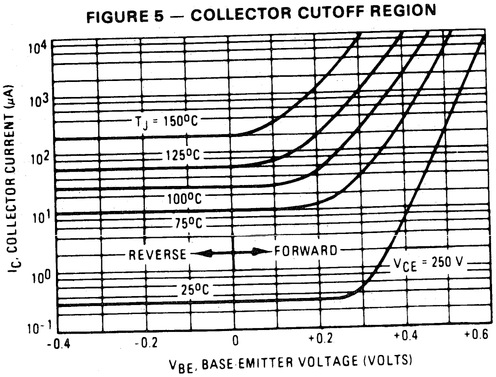
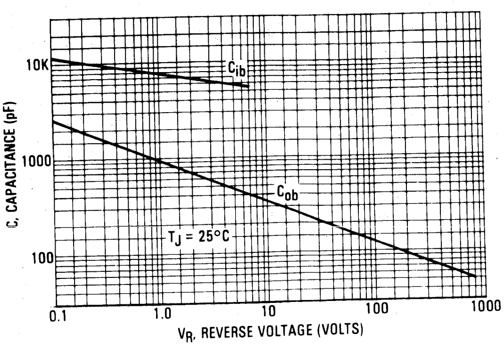


FIGURE 6 — CAPACITANCE



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TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

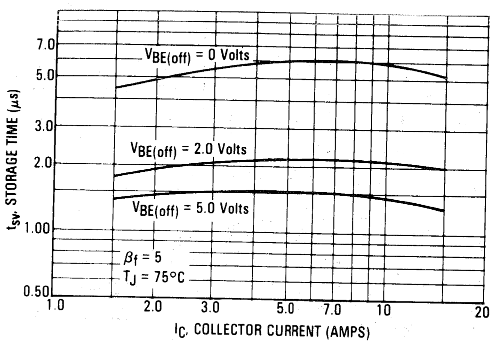

FIGURE 8 — STORAGE TIME

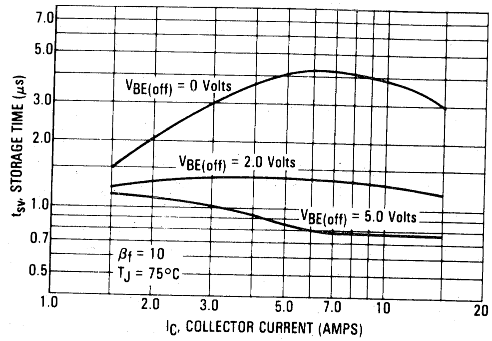

FIGURE 9 — COLLECTOR CURRENT FALL TIME

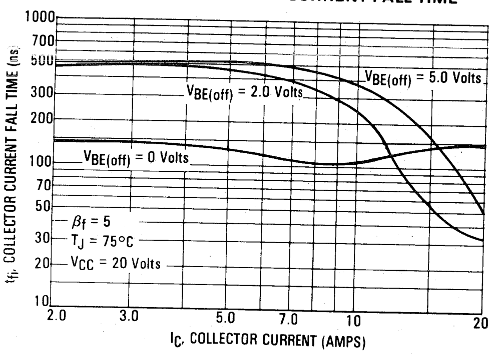

FIGURE 10 — COLLECTOR CURRENT FALL TIME

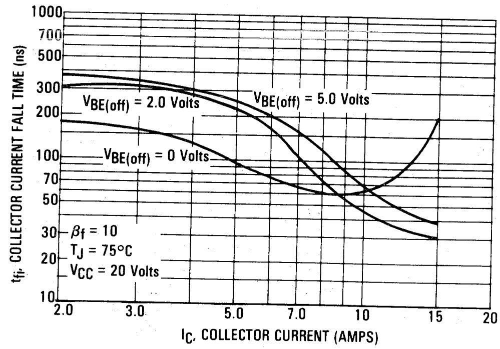

FIGURE 11 — CROSSOVER TIME

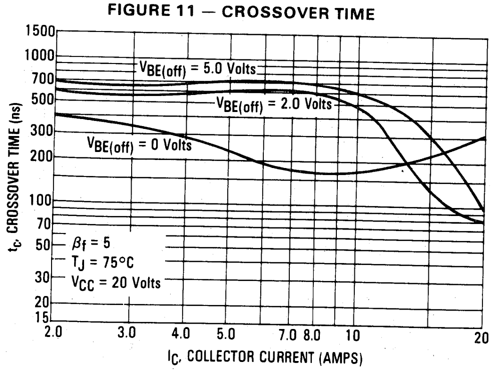

FIGURE 12 — CROSSOVER TIME

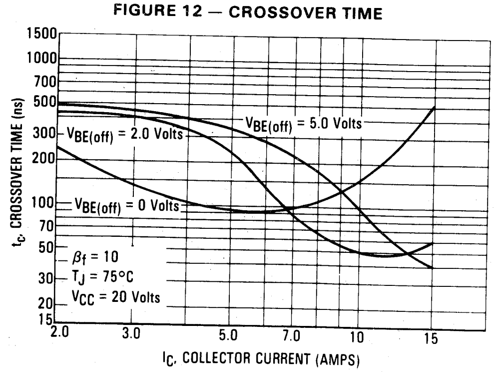

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FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

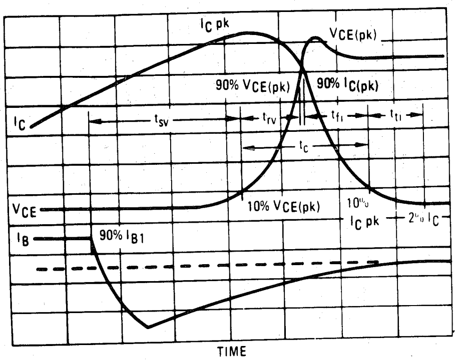
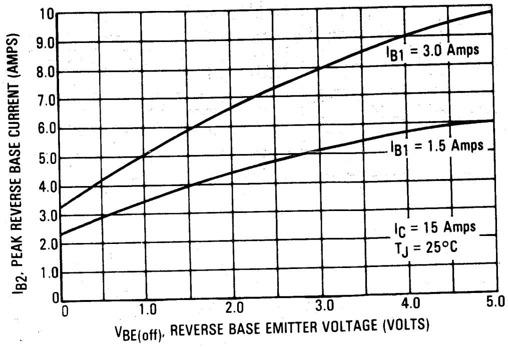


FIGURE 14 — REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

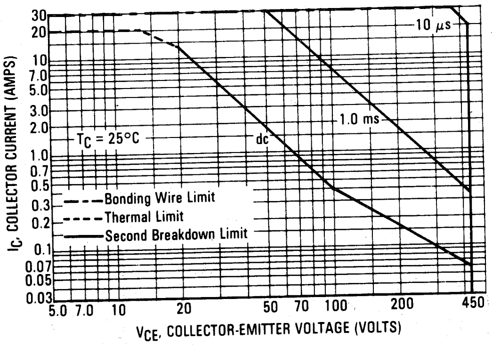
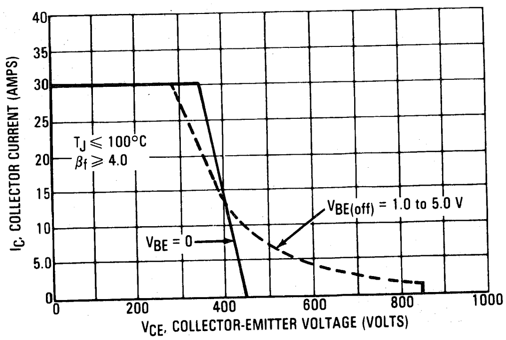


FIGURE 16 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

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FIGURE 17 — THERMAL RESPONSE

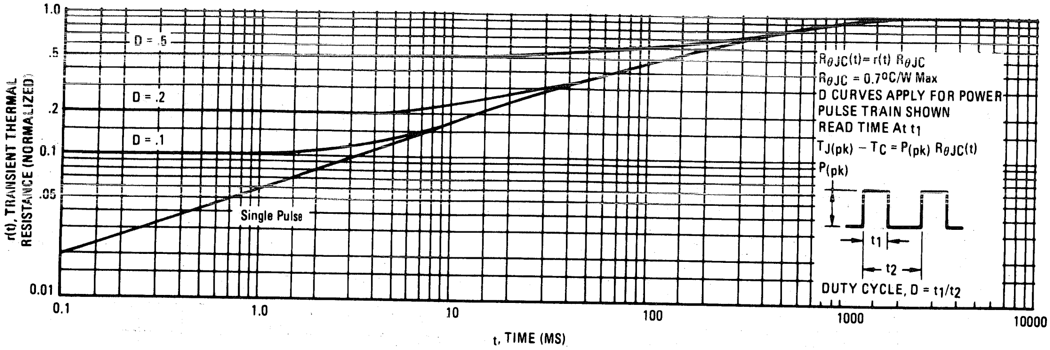


FIGURE 18 — POWER DERATING

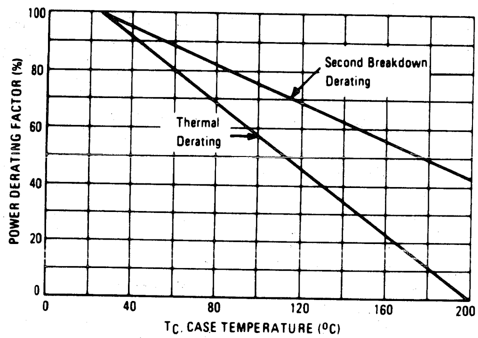
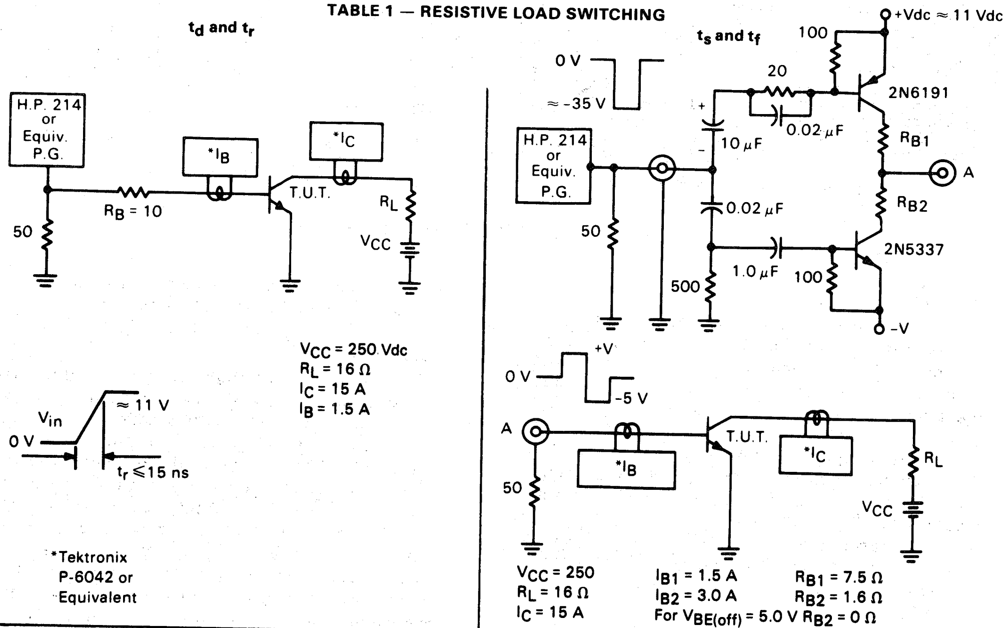
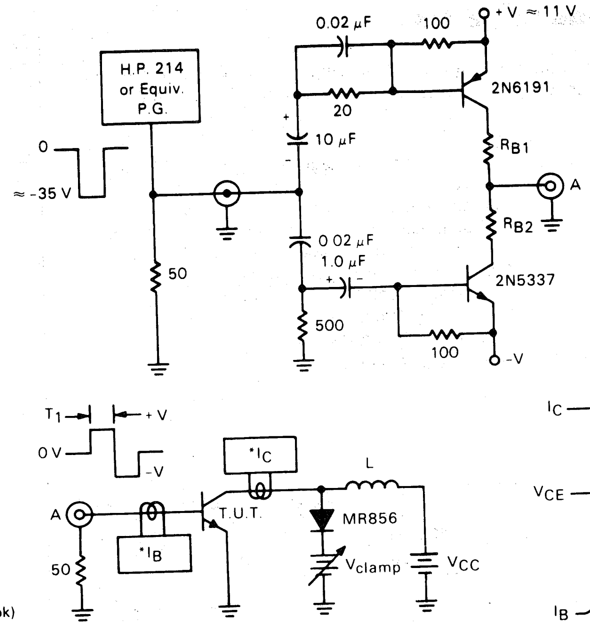


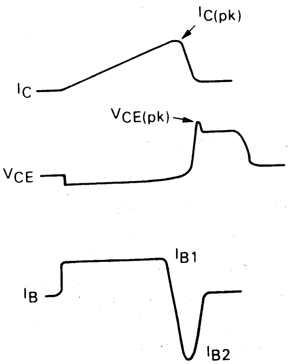
TABLE 1 — RESISTIVE LOAD SWITCHING



*Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING





$T_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{CEO(sus)}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

*Tektronix
P-6042 or
Equivalent

Inductive Switching
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Scope - Tektronix
7403 or
Equivalent

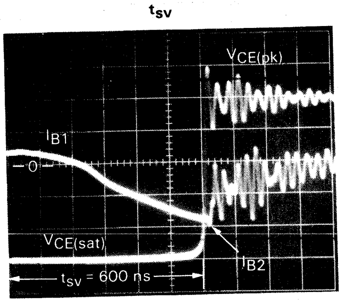
RBSOA
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

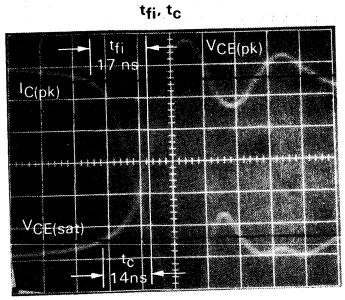
t_{sv}

$I_{C(pk)}$ = 15 A
I_{B1} = 1.5 A
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base = 100 ns/cm



t_{fi}, t_c

$I_{C(pk)}$ = 15 A
I_{B1} = 1.5 A
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base = 10 ns/cm



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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ16018
MJH16018

Designer's Data Sheet

NPN Silicon Power Transistors

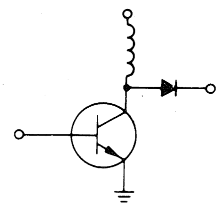
1.5 kV Switchmode III Series

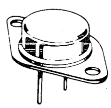
These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

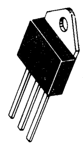
Features:
- Collector-Emitter Voltage — V_{CEV} = 1500 Vdc
- Fast Turn-Off Times
  - 80 ns Inductive Fall Time – 100°C (Typ)
  - 110 ns Inductive Crossover Time – 100°C (Typ)
  - 4.5 μs Inductive Storage Time – 100°C (Typ)
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Load
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

POWER TRANSISTORS
10 AMPERES
800 VOLTS
125 and 175 WATTS





CASE 1-05
TO-204AA
MJ16018



CASE 340-01
TO-218AC
MJH16018

MAXIMUM RATINGS

Rating	Symbol	MJ16018	MJH16018	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	800		Vdc
Collector-Emitter Voltage	V_{CEV}	1500		Vdc
Emitter-Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	10 15		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	8 12		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	175 100 1	125 50 1	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	1	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤ 10%.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 50 mA, I_B = 0)	$V_{CEO(sus)}$	800	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1500 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 1500 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	I_{EBO}	—	—	0.1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 13			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 14			
ON CHARACTERISTICS(1)					
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 5 Adc) (I_C = 5 Adc, I_B = 2 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	— — —	1 5 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 2 Adc) (I_C = 5 Adc, I_B = 2 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)	h_{FE}	4	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)	C_{ob}	—	—	450	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Inductive Load (Table 1)							
Storage Time	Baker Clamped (I_C = 5 Adc, I_{B1} = 2 Adc, $V_{BE(off)}$ = 2 Vdc, $V_{CE(pk)}$ = 400 Vdc) PW = 25 μs	(T_J = 25°C)	t_{sv}	—	4000	8000	ns
Fall Time			t_{fi}	—	60	200	
Crossover Time			t_c	—	90	300	
Storage Time		(T_J = 100°C)	t_{sv}	—	4500	9000	
Fall Time			t_{fi}	—	80	250	
Crossover Time			t_c	—	110	375	
Resistive Load (Table 1)							
Delay Time	(I_C = 5 Adc, V_{CC} = 250 Vdc, I_{B1} = 2 Adc, I_{B2} = 2 Adc, R_{B2} = 3 Ω, PW = 25 μs, Duty Cycle ≤ 2%)		t_d	—	85	200	ns
Rise Time			t_r	—	900	2000	
Storage Time			t_s	—	4500	9000.	
Fall Time			t_f	—	200	400	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

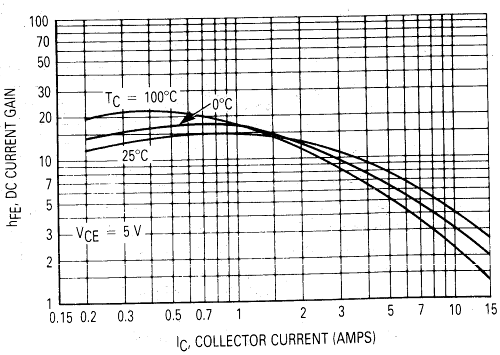


Figure 1. DC Current Gain

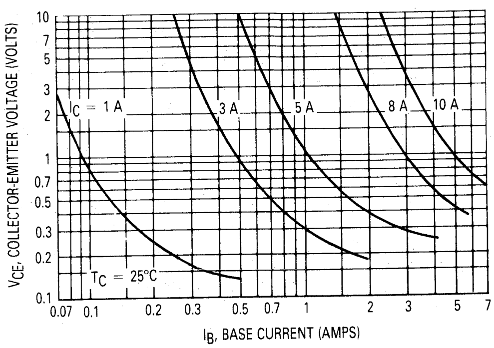


Figure 2. Collector Saturation Region

TYPICAL STATIC CHARACTERISTICS

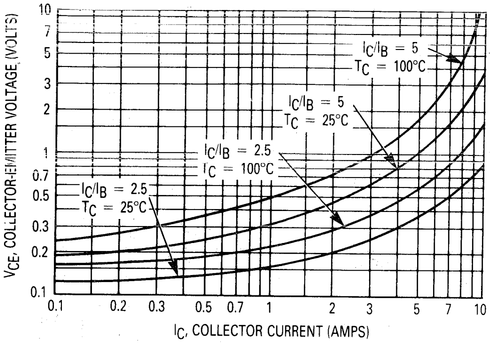


Figure 3. Collector-Emitter Saturation Region

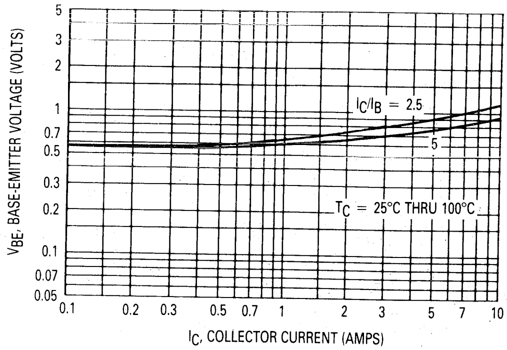


Figure 4. Base-Emitter Saturation Region

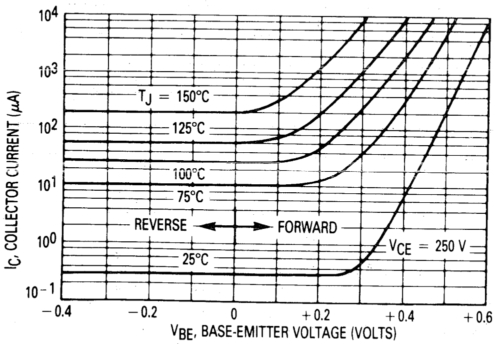


Figure 5. Collector Cutoff Region

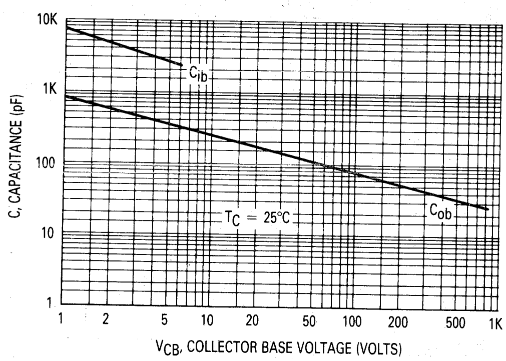


Figure 6. Typical Capacitance

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

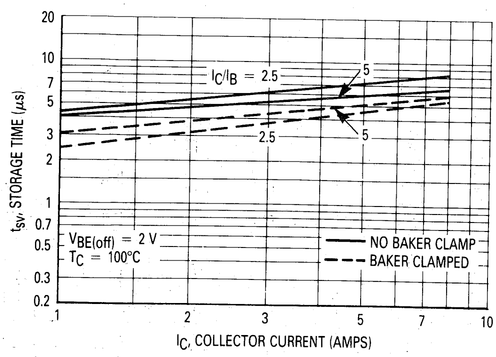


Figure 7. Storage Time

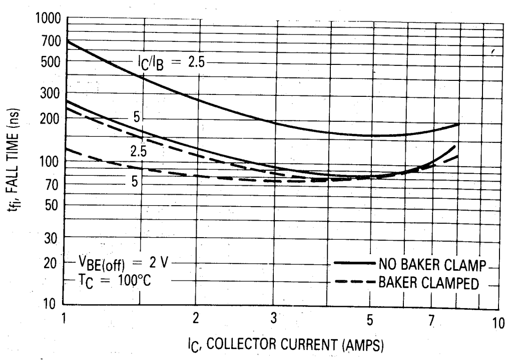


Figure 8. Inductive Switching Fall Time

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

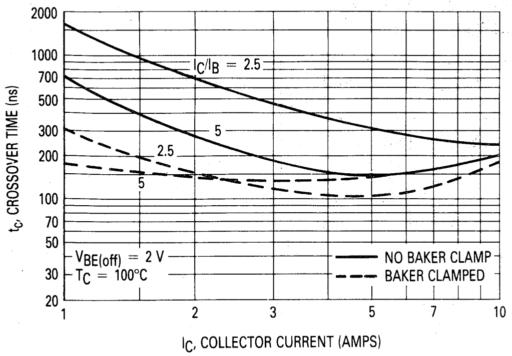


Figure 9. Inductive Switching Crossover Time

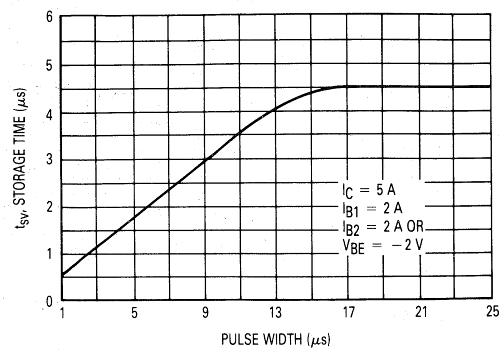


Figure 10. (t_{sv}) Storage Time versus I_{B1} Pulse Width

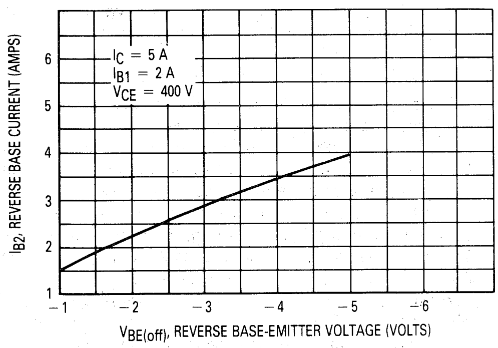


Figure 11. Reverse Base Current versus Off Voltage

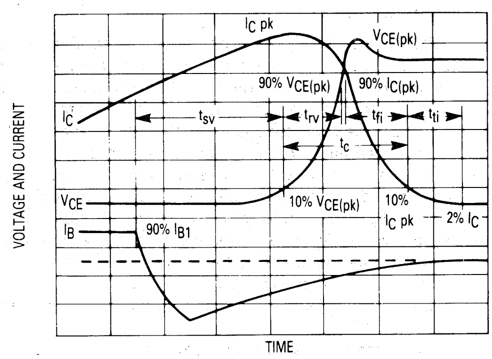


Figure 12. Inductive Switching Measurements

GUARANTEED SAFE OPERATING AREA LIMITS

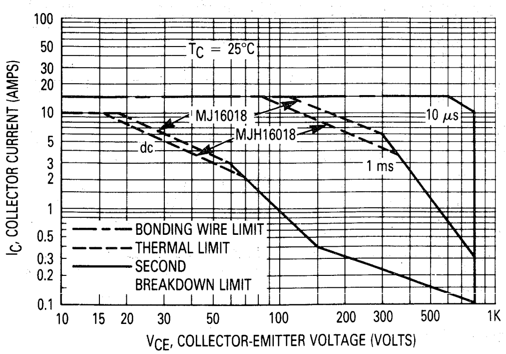


Figure 13. Maximum Forward Bias Safe Operating Area

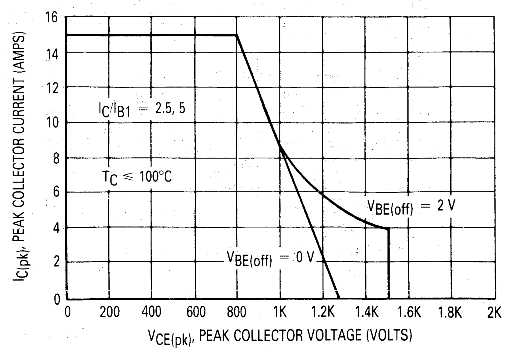


Figure 14. Maximum Reverse Bias Safe Operating Area

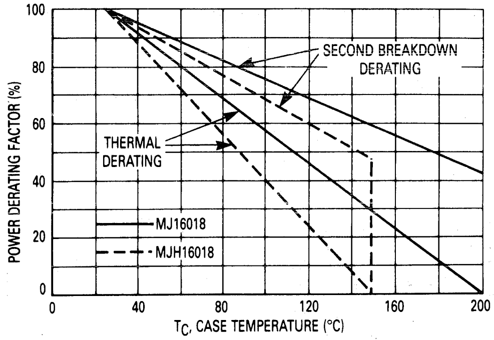


Figure 15. Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 16. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

3

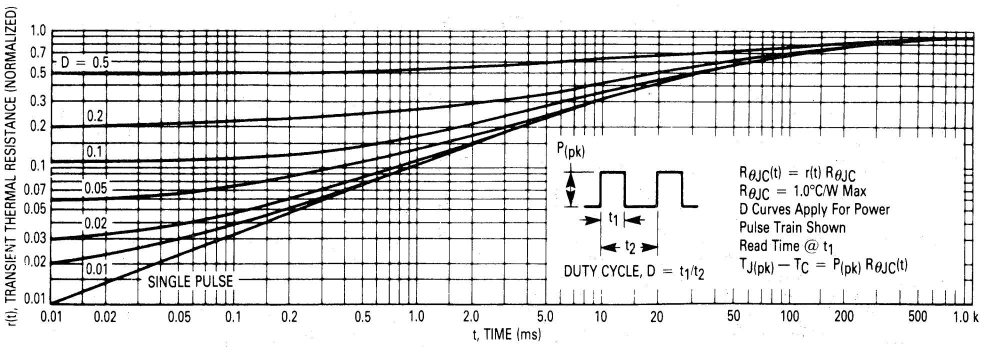
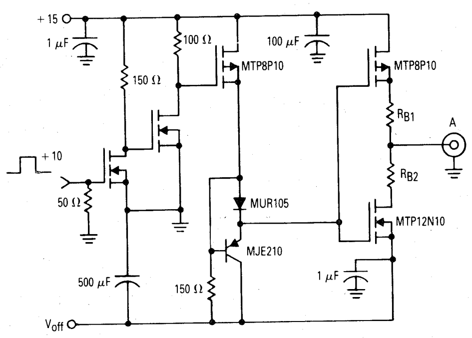
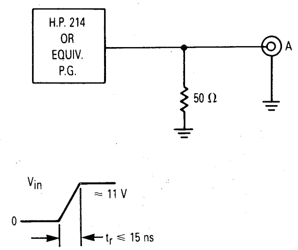
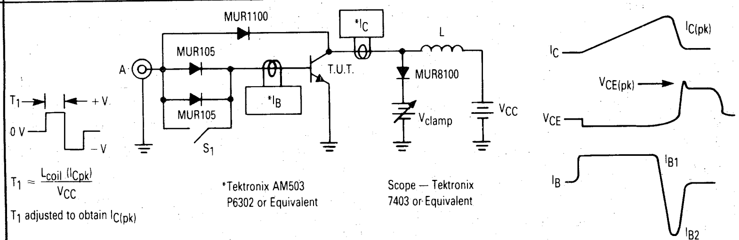
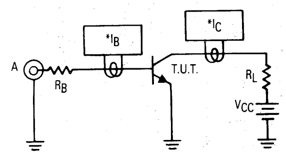


Figure 16. Thermal Response

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA	Inductive Switching	Resistive Switching
Input Conditions	**Drive Circuit**  Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.			**For t_d and t_r:**  **For t_s and t_f:** Use Inductive Switching Drive Circuit
Circuit Values	L = 10 mH $R_{B2} = \infty$ V_{CC} = 20 Volts $I_{(pk)}$ = 50 mA S_1 Closed	L = 200 μH $R_{B2} = 0$ V_{CC} = 20 Volts R_{B1} selected for desired I_{B1} S_1 Closed	L = 200 μH $R_{B2} = 0$ when $V_{BE(off)}$ is specified or selected for desired I_{B2} $V_{CC} \approx$ 20 Volts, Adjusted to obtain desired IC R_{B1} selected for desired I_{B1} S_1 = Open for baker clamp condition	**for t_d and t_r** V_{CC} = 250 Volts R_B selected for desired I_{B1} R_L selected for desired I_C **for t_s and t_f** V_{CC} = 250 Volts $R_B = 0$ R_{B1} & R_{B2} selected for I_{B1} & I_{B2} R_L selected for desired I_C
Test Circuit	 $T_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ T_1 adjusted to obtain $I_{C(pk)}$ *Tektronix AM503 P6302 or Equivalent Scope — Tektronix 7403 or Equivalent			 *Tektronix AM503 P6302 or Equivalent

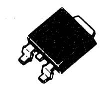
Complementary Power Transistors
DPAK For Surface Mount Applications

NPN MJD29,C
PNP MJD30,C

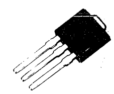
SILICON POWER TRANSISTORS
1 AMPERE
40 and 100 VOLTS
15 WATTS

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Electrically Similar to Popular TIP29 and TIP30 Series



CASE 369A-04



CASE 369-03

MAXIMUM RATINGS

Rating	Symbol	MJD29 MJD30	MJD29C MJD30C	Unit
Collector-Emitter Voltage	V_{CEO}	40	100	Vdc
Collector-Base Voltage	V_{CB}	40	100	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak	I_C	1 3		Adc
Base Current	I_B	0.4		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.56 0.012		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.3	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purposes	T_L	260	°C

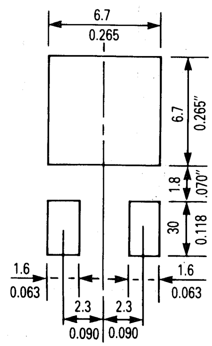
ELECTRICAL CHARACTERISTCS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	MJD29, MJD30 MJD29C, MJD30C	$V_{CEO(sus)}$	40 100	— —	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	 MJD29, MJD30 MJD29C, MJD30C	I_{CEO}	—	50	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)		I_{CES}	—	20	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	1	mAdc

* These ratings are applicable when surface mounted on the minimum pad size recommended.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



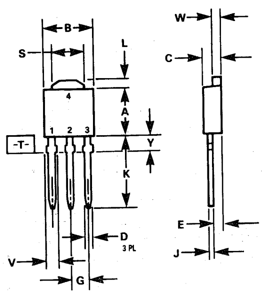
ELECTRICAL CHARACTERISTCS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.2 Adc, V_{CE} = 4 Vdc) (I_C = 1 Adc, V_{CE} = 4 Vdc)	h_{FE}	 40 15	 — 75	—
Collector-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 125 mAdc)	$V_{CE(sat)}$	—	0.7	Vdc
Base-Emitter On Voltage (I_C = 1 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	3	—	MHz
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1 kHz)	$\|h_{fe}\|$	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) $f_T = |h_{fe}| \cdot f_{test}$.

OUTLINE DIMENSIONS

CASE 369-03

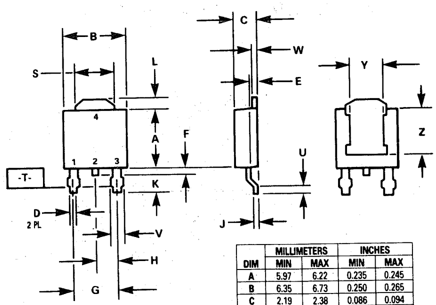


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER. | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

CASE 369A-04



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER. | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD29-1)

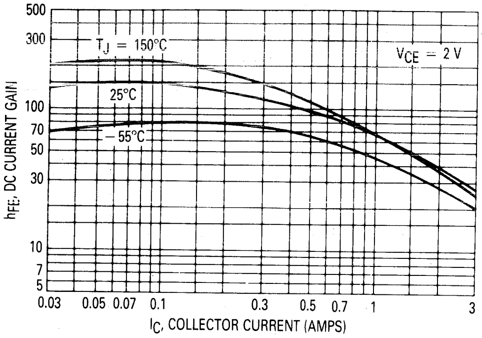


Figure 1. DC Current Gain

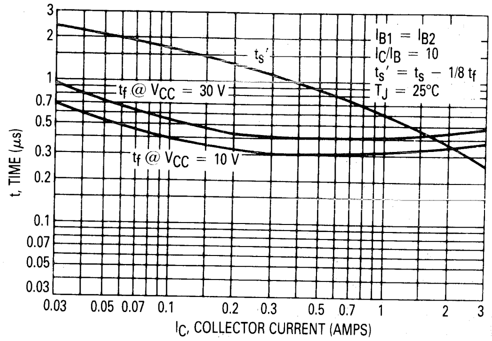


Figure 2. Turn-Off Time

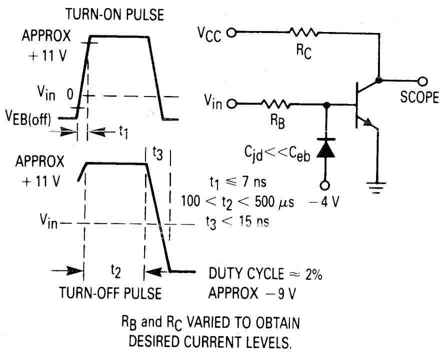


Figure 3. Switching Time Equivalent Circuit

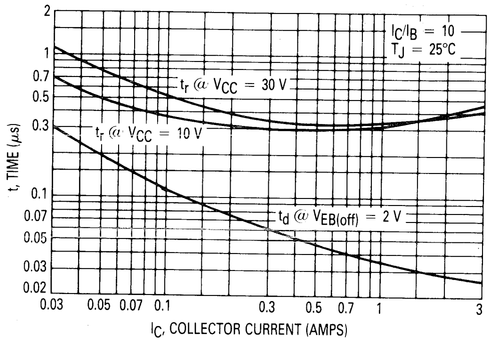


Figure 4. Turn-On Time

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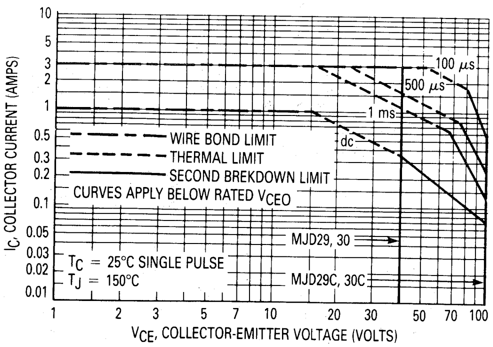


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

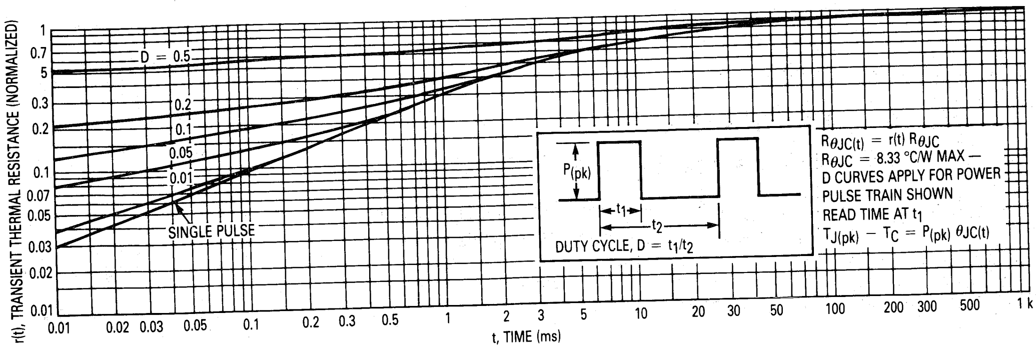


Figure 6. Thermal Response

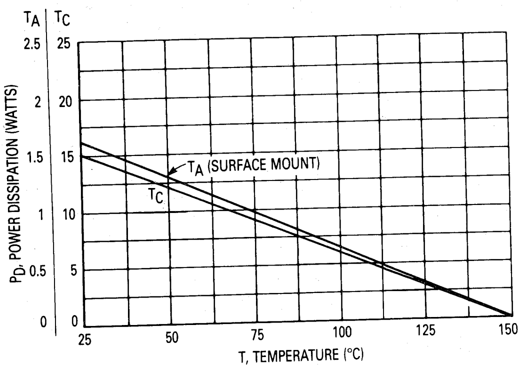


Figure 7. Power Derating

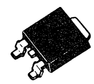
3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

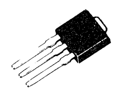
Complementary Power Transistors
DPAK For Surface Mount Applications

NPN
MJD31,C
PNP
MJD32,C

SILICON POWER TRANSISTORS
3 AMPERES
40 and 100 VOLTS
15 WATTS



CASE 369A-04



CASE 369-03

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Electrically Similar to Popular TIP31 and TIP32 Series

MAXIMUM RATINGS

Rating	Symbol	MJD31 MJD32	MJD31C MJD32C	Unit
Collector-Emitter Voltage	V_{CEO}	40	100	Vdc
Collector-Base Voltage	V_{CB}	40	100	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak	I_C	3 5		Adc
Base Current	I_B	1		Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	15 0.12		Watts W/°C
Total Power Dissipation* @ $T_A = 25°C$ Derate above 25°C	P_D	1.56 0.012		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.3	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purposes	T_L	260	°C

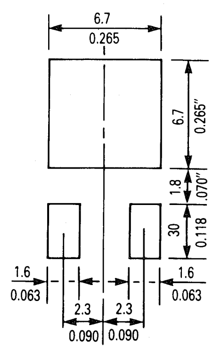
ELECTRICAL CHARACTERISTCS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	MJD31, MJD32 MJD31C, MJD32C	$V_{CEO(sus)}$	40 100	— —	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	 MJD31, MJD32 MJD31C, MJD32C	I_{CEO}	—	50	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)		I_{CES}	—	20	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	1	mAdc

* These ratings are applicable when surface mounted on the minimum pad size recommended.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



3

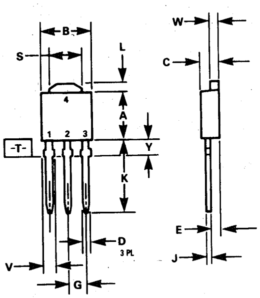
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 1 Adc, V_{CE} = 4 Vdc) (I_C = 3 Adc, V_{CE} = 4 Vdc)	h_{FE}	 25 10	 — 50	—
Collector-Emitter Saturation Voltage (I_C = 3 Adc, I_B = 375 mAdc)	$V_{CE(sat)}$	—	1.2	Vdc
Base-Emitter On Voltage (I_C = 3 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	3	—	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)	$\|h_{fe}\|$	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) $f_T = |h_{fe}| \cdot f_{test}$.

OUTLINE DIMENSIONS

CASE 369-03



STYLE 1:
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3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
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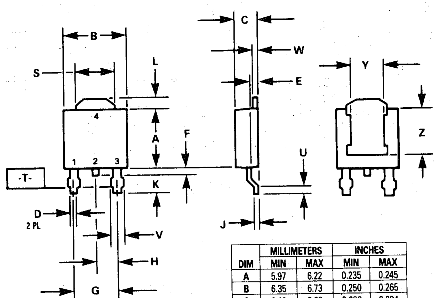
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
| ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

CASE 369A-04



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
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D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
| ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD31-1)

3

TYPICAL CHARACTERISTICS

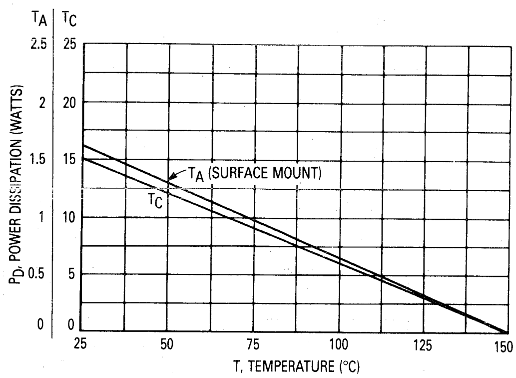


Figure 1. Power Derating

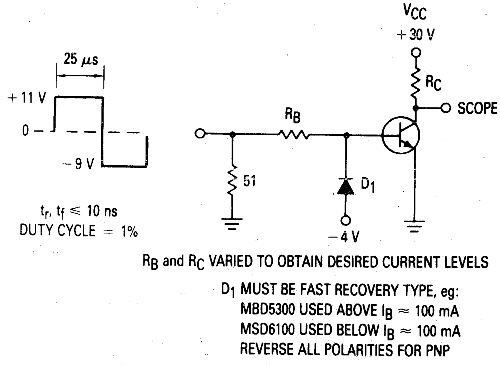


Figure 2. Switching Time Test Circuit

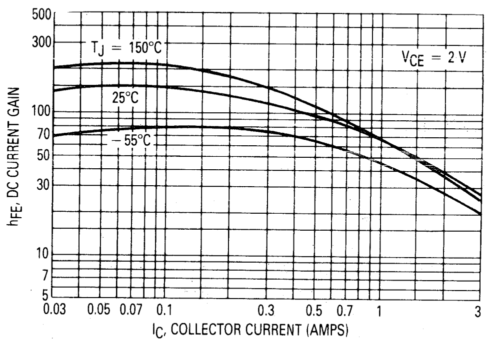


Figure 3. DC Current Gain

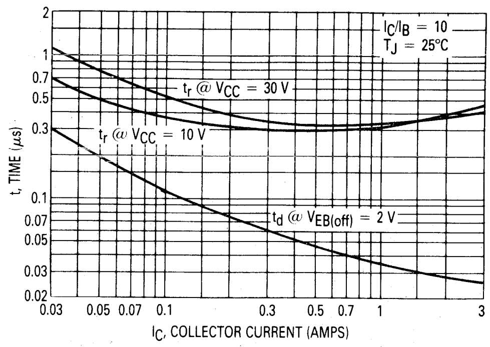


Figure 4. Turn-On Time

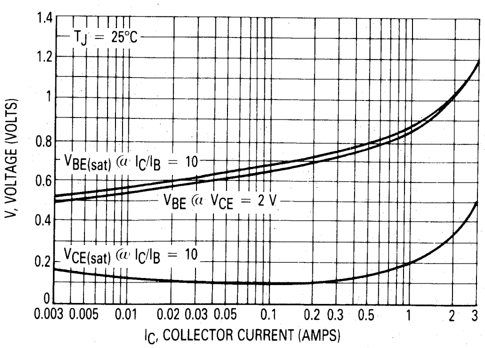


Figure 5. "On" Voltages

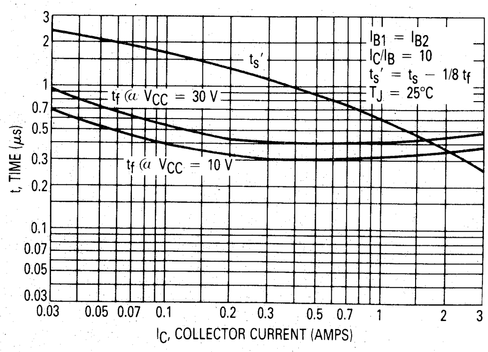


Figure 6. Turn-Off Time

3

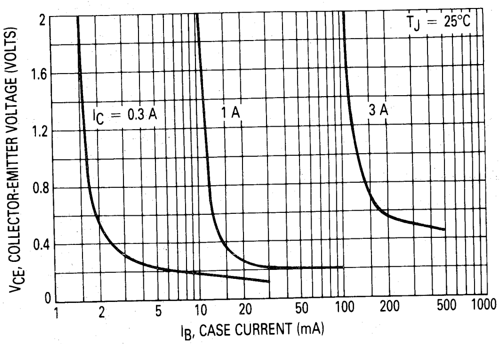


Figure 7. Collector Saturation Region

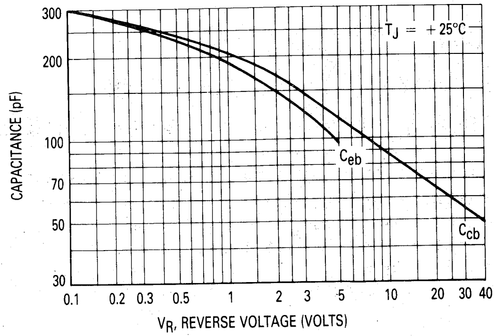


Figure 8. Capacitance

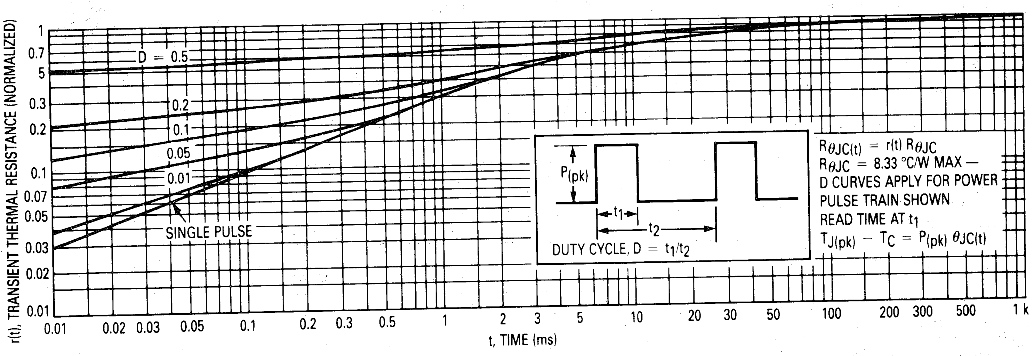


Figure 9. Thermal Response

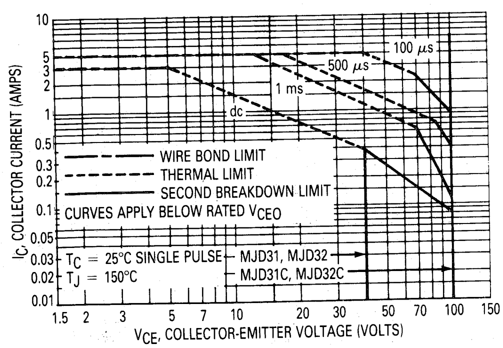


Figure 10. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

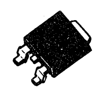
Complementary Power Transistors
DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

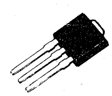
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Electrically Similar to Popular TIP41 and TIP42 Series
- Monolithic Construction With Built-in Base-Emitter Resistors

NPN MJD41C
PNP MJD42C

SILICON POWER TRANSISTORS
6 AMPERES
100 VOLTS
20 WATTS

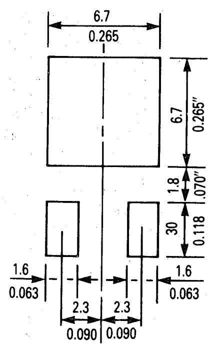


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	MJD41C MJD42C	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	6 10	Adc
Base Current	I_B	2	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	I_{CEO}	—	50	μAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, V_{EB} = 0)	I_{CES}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	0.5	mAdc

* These ratings are applicable when surface mounted on the minimum pad size recommended.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

3

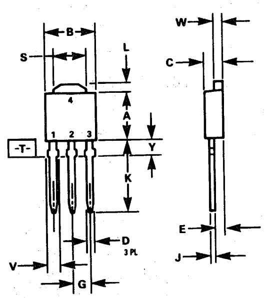
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4 Vdc) (I_C = 3 Adc, V_{CE} = 4 Vdc)	h_{FE}	30 15	— 75	—
Collector-Emitter Saturation Voltage (I_C = 6 Adc, I_B = 600 mAdc)	$V_{CE(sat)}$	—	1.5	Vdc
Base-Emitter On Voltage (I_C = 6 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	3	—	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)	$\|h_{fe}\|$	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

OUTLINE DIMENSIONS

CASE 369-03

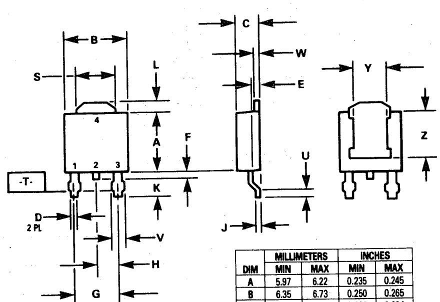


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER. ⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

CASE 369A-04



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
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3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD41C-1)

TYPICAL CHARACTERISTICS

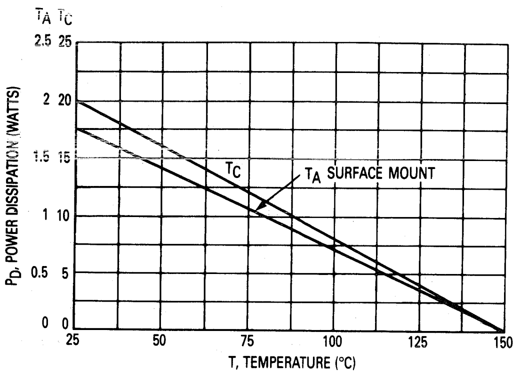


Figure 1. Power Derating

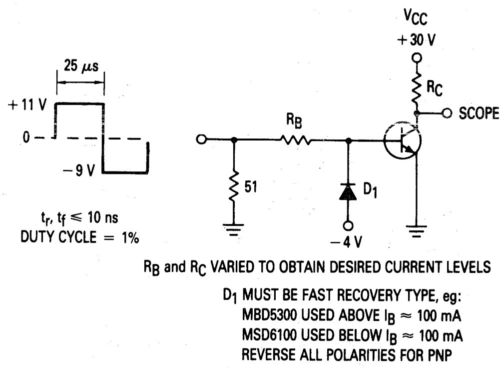


Figure 2. Switching Time Test Circuit

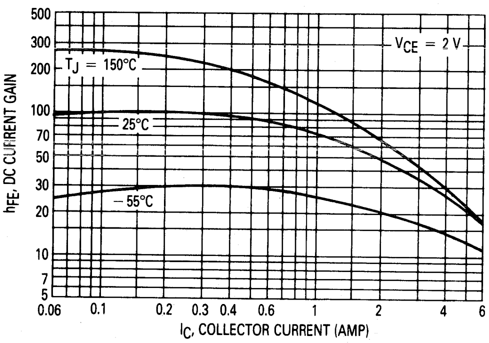


Figure 3. DC Current Gain

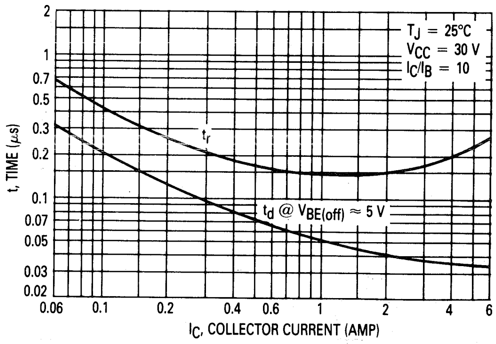


Figure 4. Turn-On Time

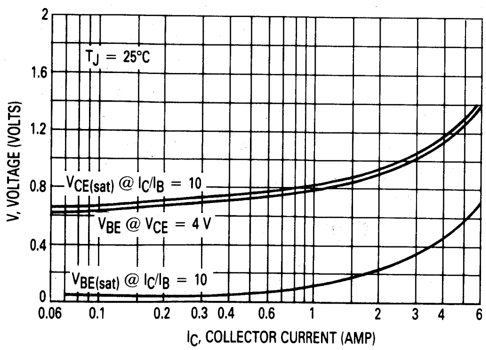


Figure 5. "On" Voltages

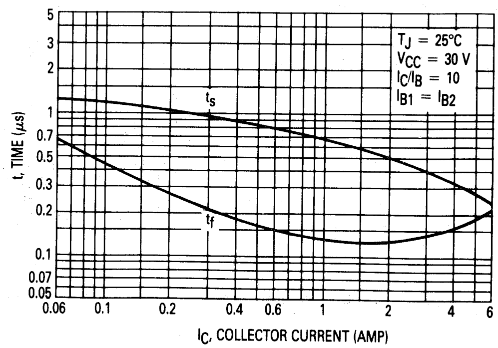


Figure 6. Turn-Off Time

3

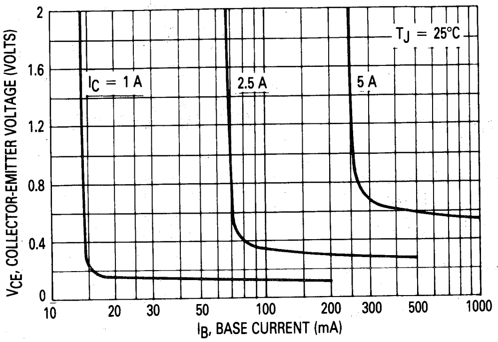


Figure 7. Collector Saturation Region

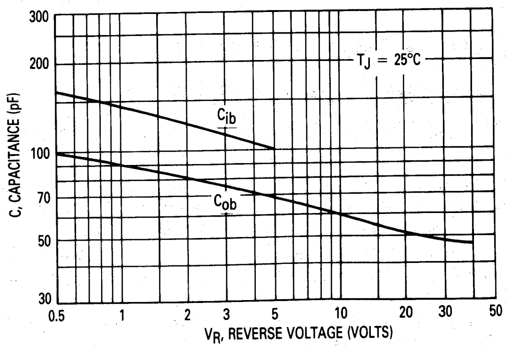


Figure 8. Capacitance

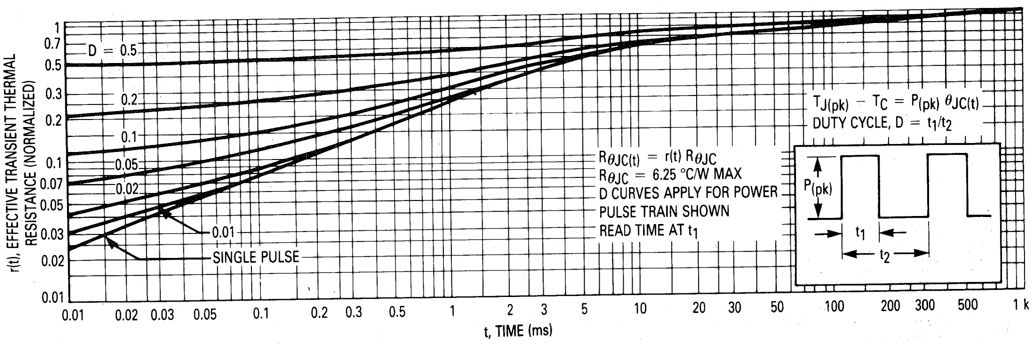


Figure 9. Thermal Response

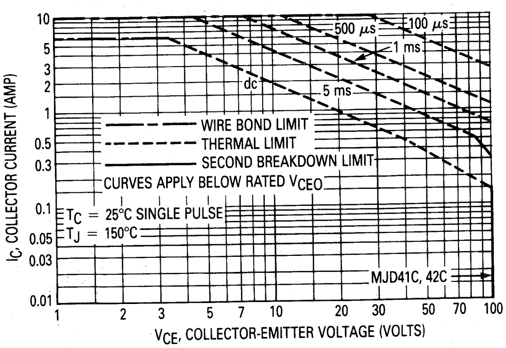


Figure 10. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

Complementary Power Transistors

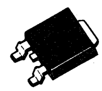
DPAK For Surface Mount Applications

NPN
MJD44H11
PNP
MJD45H11

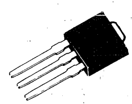
... for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel for Surface Mount ("RL" Suffix)
- Electrically Similar to Popular D44H/D45H Series
- Low Collector Emitter Saturation Voltage — $V_{CE(sat)}$ = 1 Volt Max @ 8 Amperes
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

SILICON POWER TRANSISTORS
8 AMPERES
80 VOLTS
20 WATTS



CASE 369A-04



CASE 369-03

MAXIMUM RATINGS

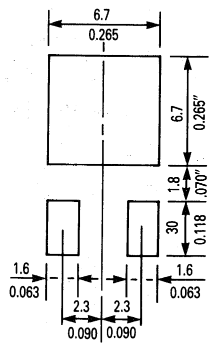
Rating	Symbol	D44H11 or D45H11	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	8 16	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation (1) @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	°C/W
Lead Temperature for Soldering	T_L	260	°C

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (I_C = 30 mA, I_B = 0)		$V_{CEO(sus)}$	80	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 5 Vdc)		I_{EBO}	—	—	50	μA
ON CHARACTERISTICS						
Collector-Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.4 Adc)		$V_{CE(sat)}$	—	—	1	Vdc
Base-Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	—	—	1.5	Vdc
DC Current Gain (V_{CE} = 1 Vdc, I_C = 2 Adc)		h_{FE}	60	—	—	—
DC Current Gain (V_{CE} = 1 Vdc, I_C = 4 Adc)			40	—	—	
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1 MHz)	MJD44H11	C_{cb}	—	130	—	pF
	MJD45H11		—	230	—	
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	MJD44H11	f_T	—	50	—	MHz
	MJD45H11		—	40	—	
SWITCHING TIMES						
Delay and Rise Times (I_C = 5 Adc, I_{B1} = 0.5 Adc)	MJD44H11	$t_d + t_r$	—	300	—	ns
	MJD45H11		—	135	—	
Storage Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJD44H11	t_s	—	500	—	ns
	MJD45H11		—	500	—	
Fall Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJD44H11	t_f	—	140	—	ns
	MJD45H11		—	100	—	

3

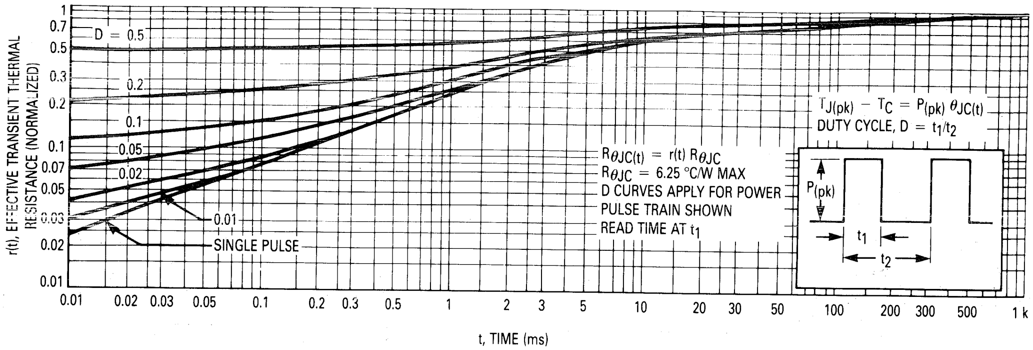


Figure 1. Thermal Response

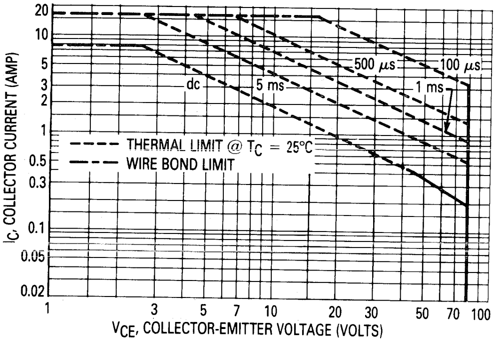


Figure 2. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

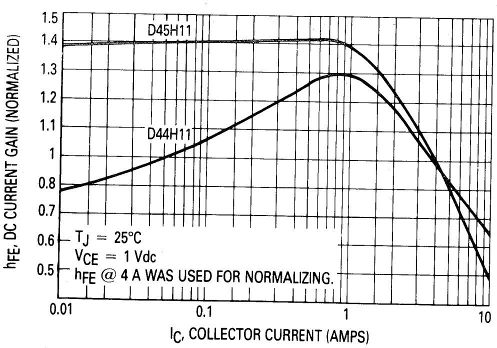


Figure 3. Normalized DC Current Gain

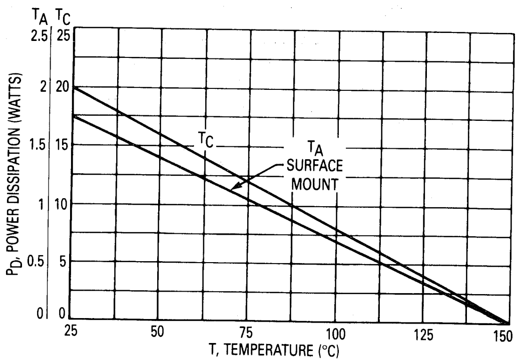
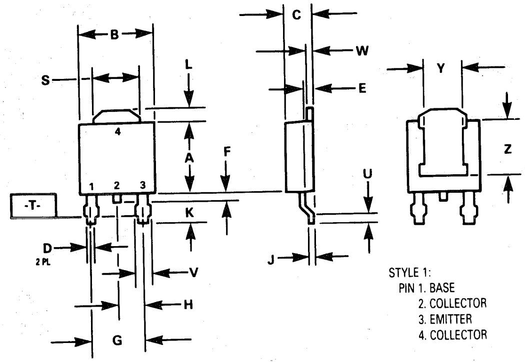


Figure 4. Power Derating

OUTLINE DIMENSIONS

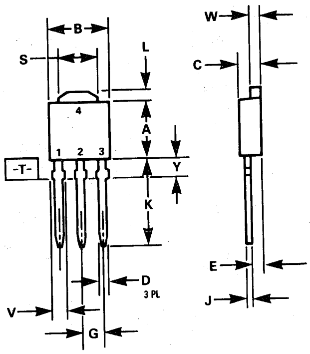


NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

CASE 369A-04



NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

CASE 369-03

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD44H11-1)

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

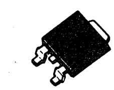
MJD47
MJD50

High Voltage Power Transistors
DPAK For Surface Mount Applications

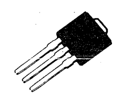
Designed for line operated audio output amplifier, switchmode power supply drivers and other switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Electrically Similar to Popular TIP47, and TIP50
- 250 and 400 V (Min) — $V_{CEO(sus)}$
- 1 A Rated Collector Current

NPN SILICON POWER TRANSISTORS
1 AMPERE
250, 400 VOLTS
15 WATTS

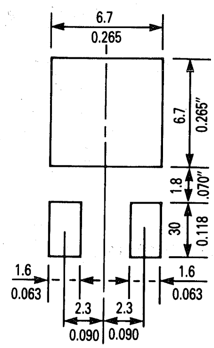


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	MJD47	MJD50	Unit
Collector-Emitter Voltage	V_{CEO}	250	400	Vdc
Collector-Base Voltage	V_{CB}	350	500	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak	I_C	1 2		Adc
Base Current	I_B	0.6		Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	15 0.12		Watts W/°C
Total Power Dissipation* @ $T_A = 25°C$ Derate above 25°C	P_D	1.56 0.0125		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 30$ mAdc, $I_B = 0$)	MJD47 MJD50	$V_{CEO(sus)}$	250 400	— —	Vdc
Collector Cutoff Current ($V_{CE} = 150$ Vdc, $I_B = 0$) ($V_{CE} = 300$ Vdc, $I_B = 0$)	 MJD47 MJD50	I_{CEO}	 — —	 0.2 0.2	mAdc

* When surface mounted on minimum pad sizes recommended.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

3

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued					
Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0)	MJD47	I_{CES}	—	0.1	mAdc
(V_{CE} = 500 Vdc, V_{BE} = 0)	MJD50		—	0.1	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	1	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc)		h_{FE}	30	150	—
(I_C = 1 Adc, V_{CE} = 10 Vdc)			10	—	
Collector-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	—	1	Vdc
Base-Emitter On Voltage (I_C = 1 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2 MHz)		f_T	10	—	MHz
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	25	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

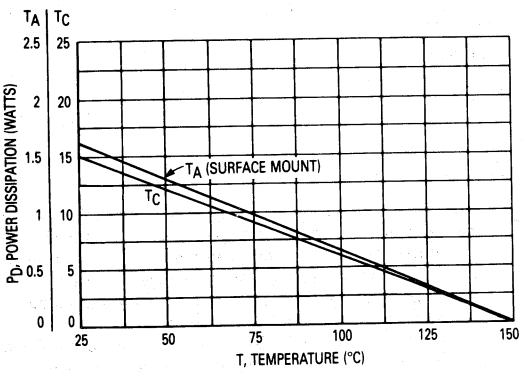


Figure 1. Power Derating

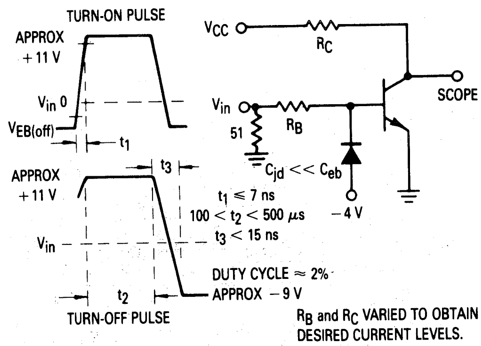


Figure 2. Switching Time Equivalent Circuit

3

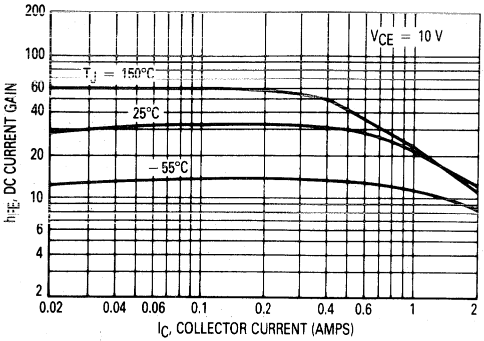


Figure 3. DC Current Gain

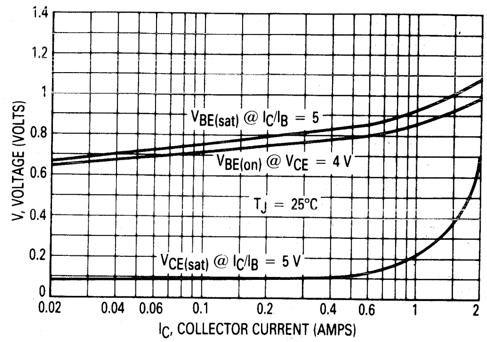


Figure 4. "On" Voltages

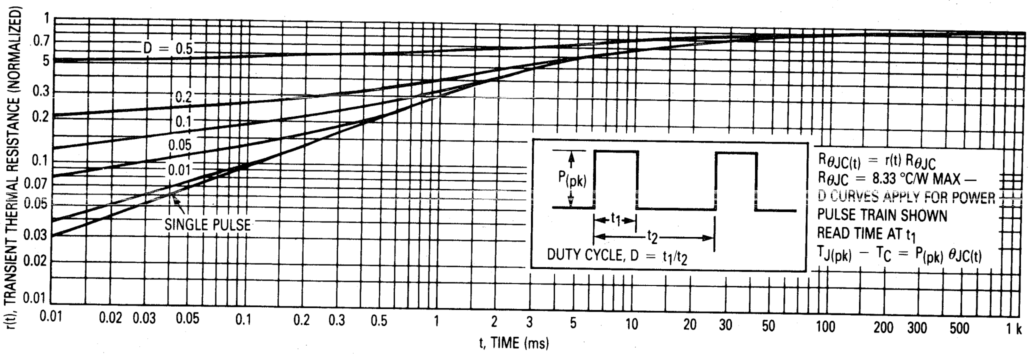


Figure 5. Thermal Response

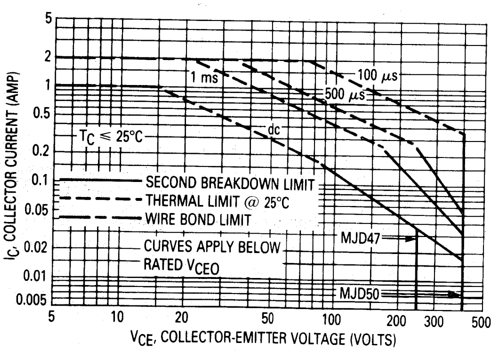


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

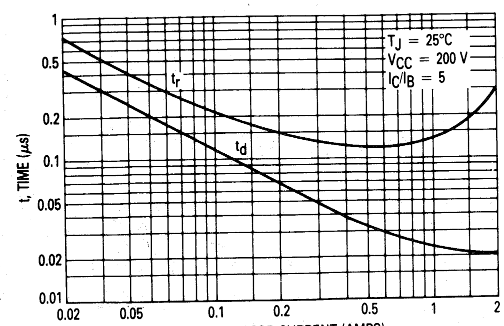


Figure 7. Turn-On Time

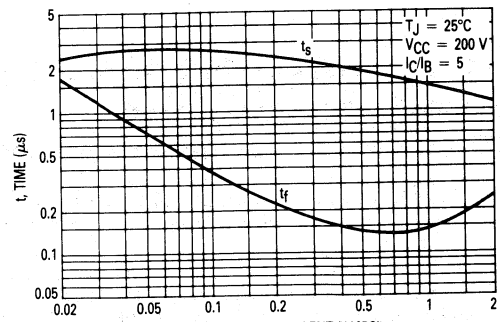
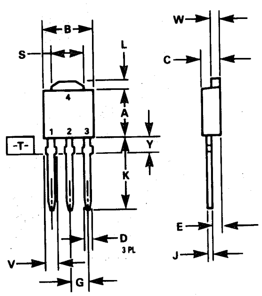


Figure 8. Turn-Off Time

OUTLINE DIMENSIONS

CASE 369-03

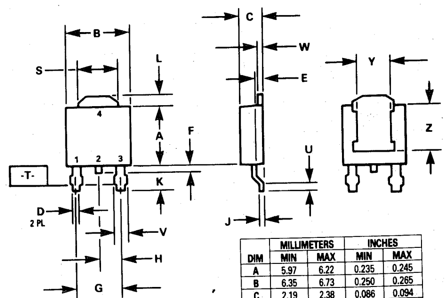


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER. | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

CASE 369A-04



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER. | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

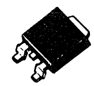
Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD47-1)

Complementary Darlington Power Transistors

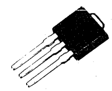
DPAK For Surface Mount Applications

NPN
MJD112
PNP
MJD117

SILICON
POWER TRANSISTORS
2 AMPERES
100 VOLTS
20 WATTS



CASE 369A-04



CASE 369-03

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, convertors, and power amplifiers.

- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Surface Mount Replacements for TIP110–TIP117 Series
- Monolithic Construction With Built-in Base-Emitter Shunt Resistors
- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 2 Adc
- Complementary Pairs Simplifies Designs

MAXIMUM RATINGS

Rating	Symbol	MJD112 MJD117	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	2 4	Adc
Base Current	I_B	50	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	°C/W

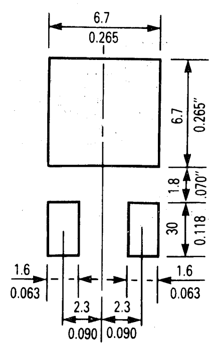
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	20	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	20	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc

* These ratings are applicable when surface mounted on the minimum pad sizes recommended.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



***ELECTRICAL CHARACTERISTICS — continued** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued				
Collector-Cutoff Current (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	— —	10 500	μAdc
Collector-Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter-Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3 Vdc) (I_C = 2 Adc, V_{CE} = 3 Vdc) (I_C = 4 Adc, V_{CE} = 3 Vdc)	h_{FE}	500 1000 200	— 12,000 —	—
Collector-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 8 mAdc) (I_C = 4 Adc, I_B = 40 mAdc)	$V_{CE(sat)}$	— —	2 3	Vdc
Base-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 40 mAdc)	$V_{BE(sat)}$	—	4	Vdc
Base-Emitter On Voltage (I_C = 2 Adc, V_{CE} = 3 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	25	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD117 MJD112	C_{ob}	— —	200 100	pF

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

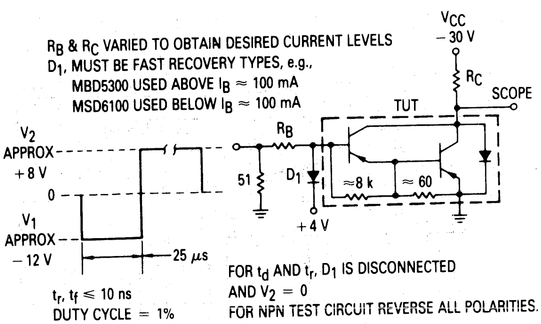


Figure 1. Switching Times Test Circuit

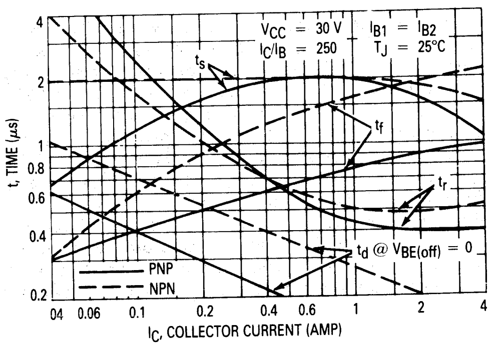


Figure 2. Switching Times

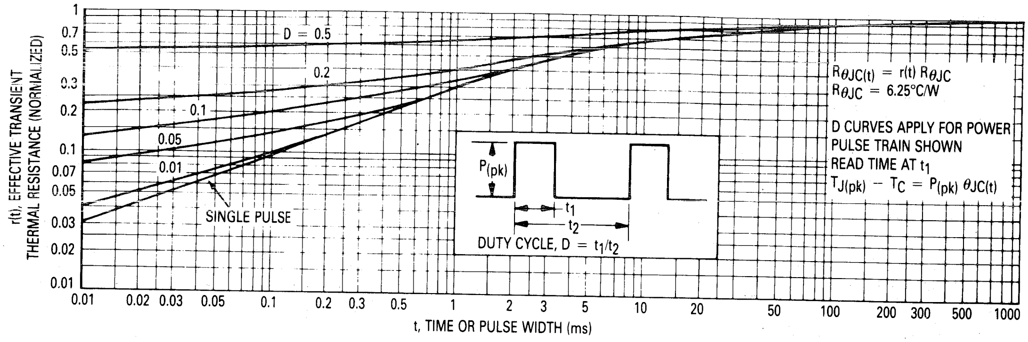


Figure 3. Thermal Response

ACTIVE-REGION SAFE-OPERATING AREA

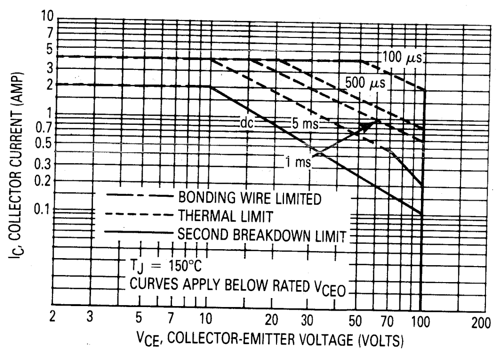


Figure 4. Maximum Rated Forward Biased Safe Operating Area

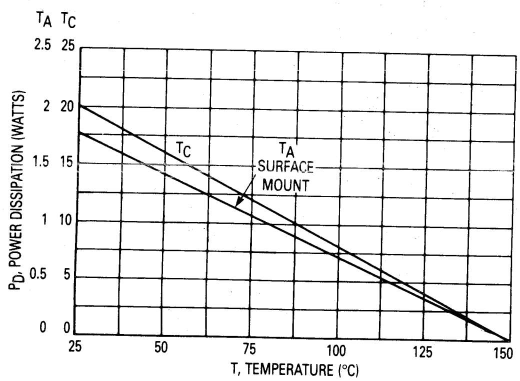


Figure 5. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

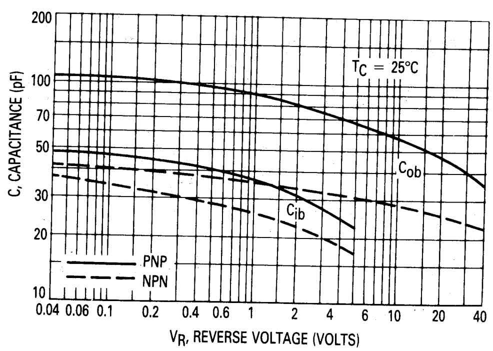


Figure 6. Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS

NPN MJD112 **PNP MJD117**

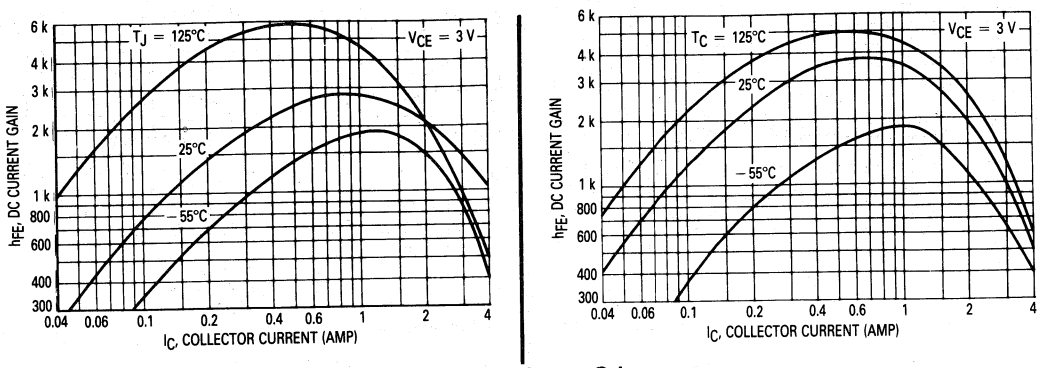


Figure 7. DC Current Gain

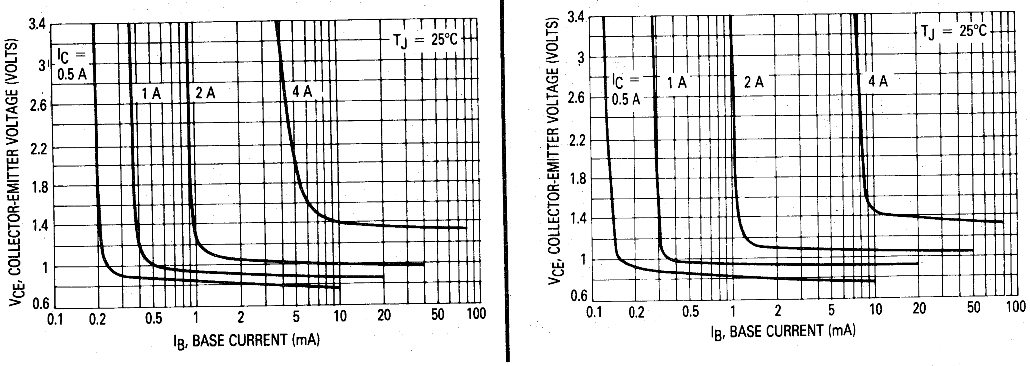


Figure 8. Collector Saturation Region

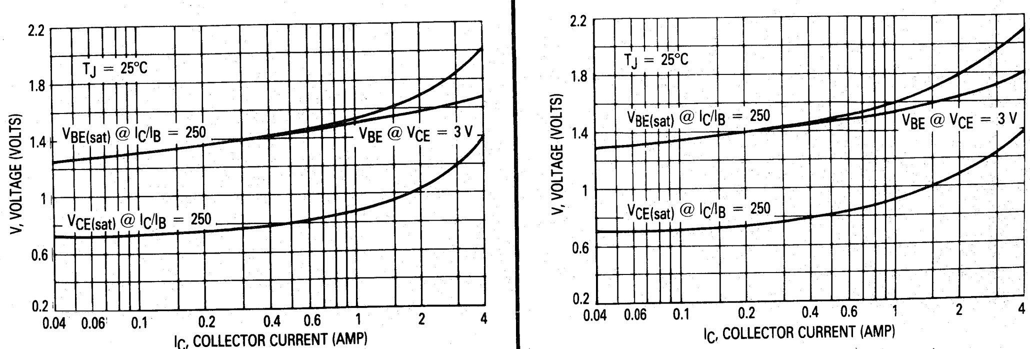
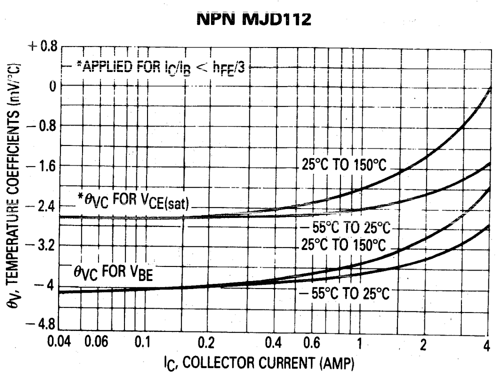


Figure 9. "On" Voltages

3



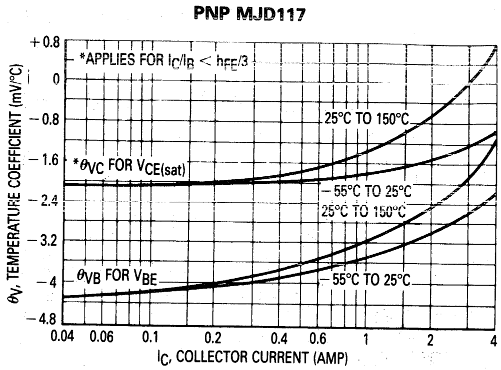
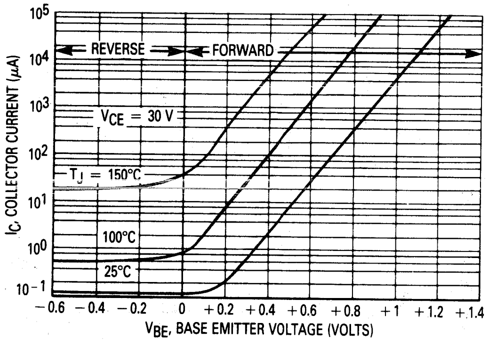


Figure 10. Temperature Coefficients



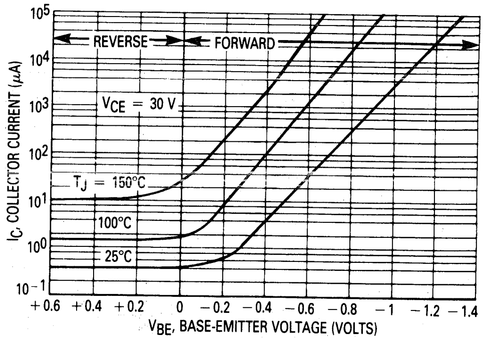
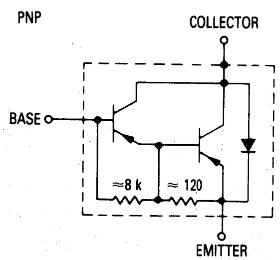


Figure 11. Collector Cut-Off Region



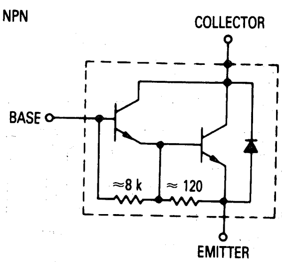
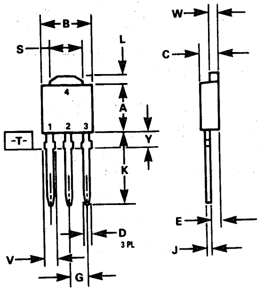


Figure 12. Darlington Schematic

OUTLINE DIMENSIONS

CASE 369-03

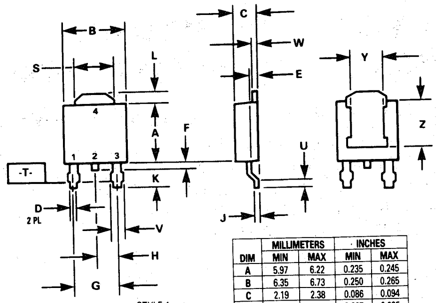


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   ⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

CASE 369A-04



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   ⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD112-1)

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

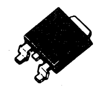
Complementary Darlington Power Transistors
DPAK For Surface Mount Applications

NPN
MJD122
PNP
MJD127

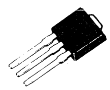
Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel ("RL" Suffix)
- Surface Mount Replacements for 2N6040–2N6045 Series, TIP120–TIP122 Series, and TIP125–TIP127 Series
- Monolithic Construction With Built-in Base-Emitter Shunt Resistors
- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 4 Adc
- Complementary Pairs Simplifies Designs

SILICON
POWER TRANSISTORS
8 AMPERES
100 VOLTS
20 WATTS



CASE 369A-04



CASE 369-03

MAXIMUM RATINGS

Rating	Symbol	MJD122 MJD127	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	8 16	Adc
Base Current	I_B	120	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	°C/W

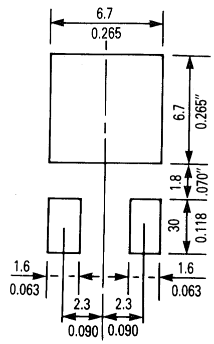
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	10	μAdc

* These ratings are applicable when surface mounted on the minimum pad sizes recommended.

(continued)

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued				
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	— —	10 500	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 4 Vdc) (I_C = 8 Adc, V_{CE} = 4 Vdc)	h_{FE}	1000 100	12,000 —	—
Collector-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 16 mAdc) (I_C = 8 Adc, I_B = 80 mAdc)	$V_{CE(sat)}$	— —	2 4	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 8 Adc, I_B = 80 mAdc)	$V_{BE(sat)}$	—	4.5	Vdc
Base-Emitter On Voltage (I_C = 4 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 MHz)	$\|h_{fe}\|$	4	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD127 MJD122	C_{ob}	— —	300 200	pF
Small-Signal Current Gain (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	300	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

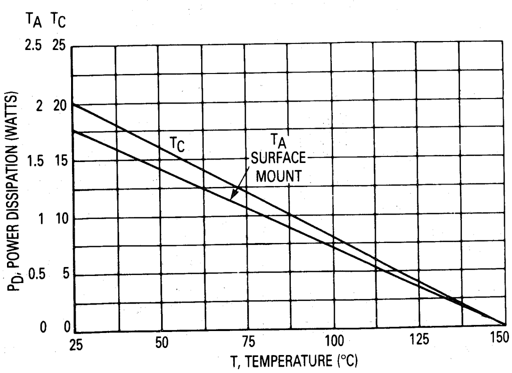


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

PNP MJD127 / **NPN MJD122**

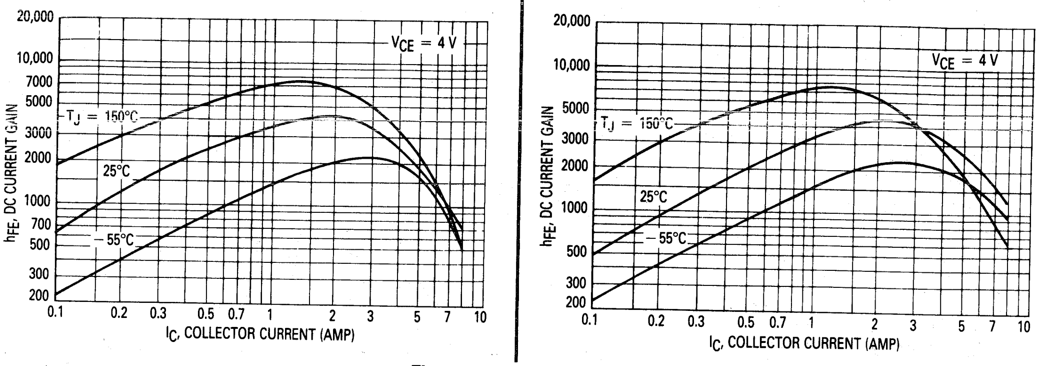


Figure 2. DC Current Gain

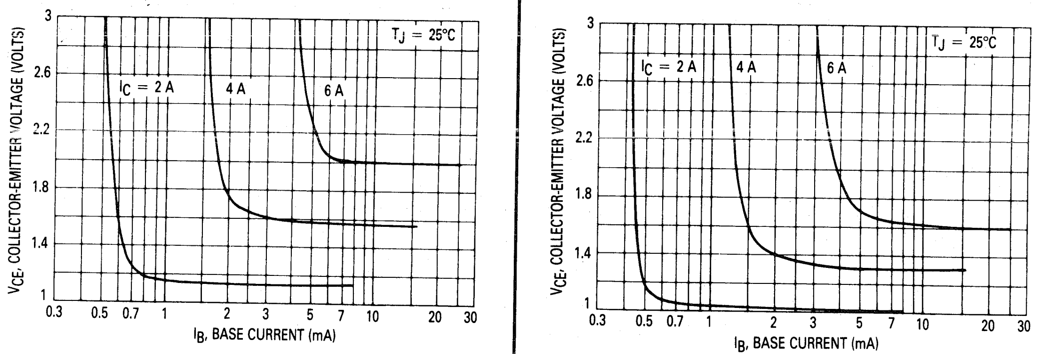


Figure 3. Collector Saturation Region

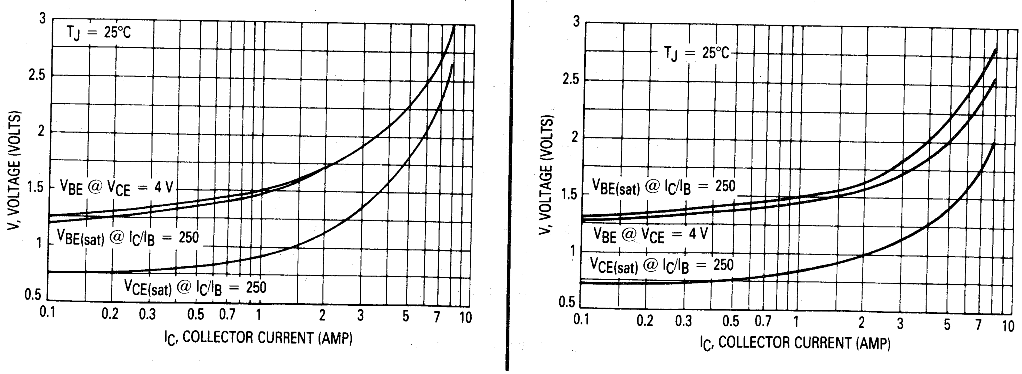


Figure 4. "On" Voltages

TYPICAL ELECTRICAL CHARACTERISTICS

PNP MJD127 **NPN MJD122**

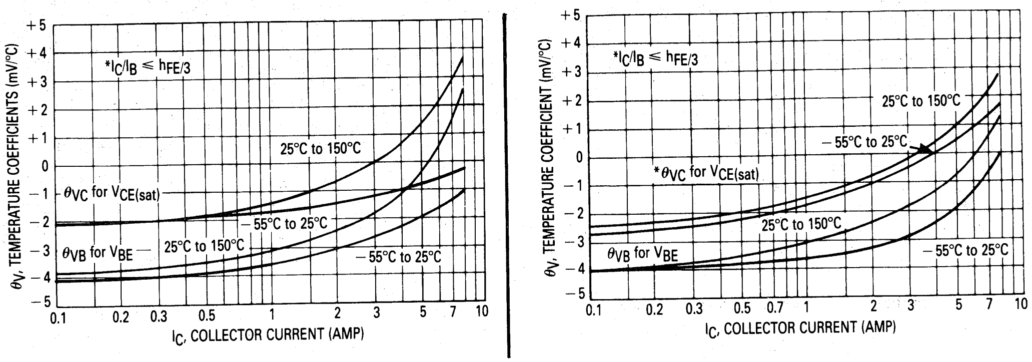


Figure 5. Temperature Coefficients

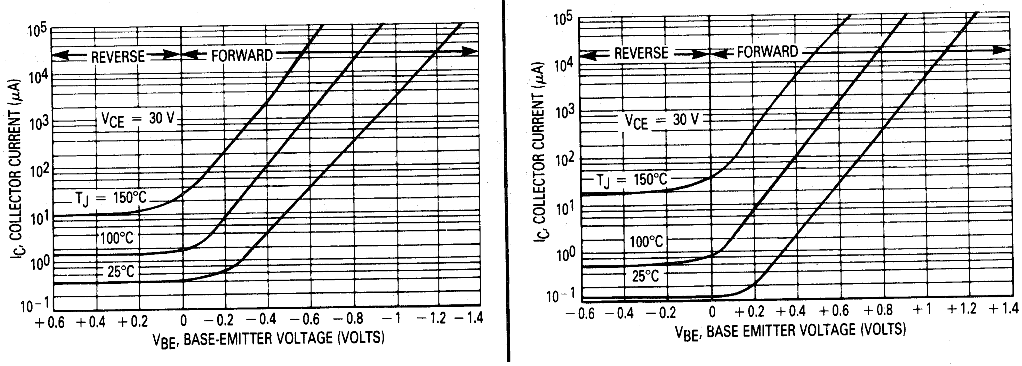


Figure 6. Collector Cut-Off Region

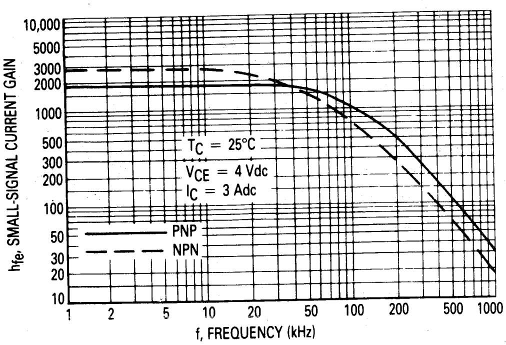


Figure 7. Small-Signal Current Gain

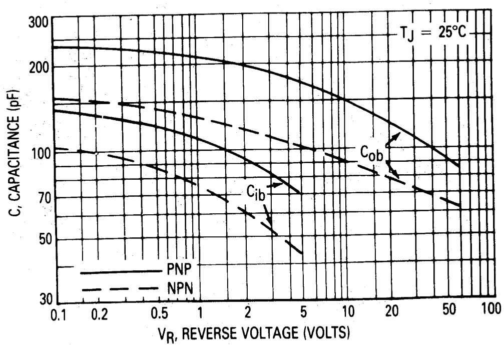


Figure 8. Capacitance

3

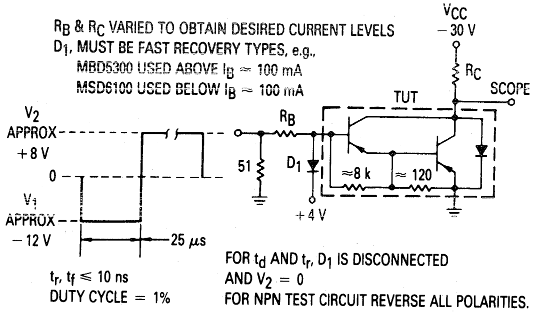


Figure 9. Switching Times Test Circuit

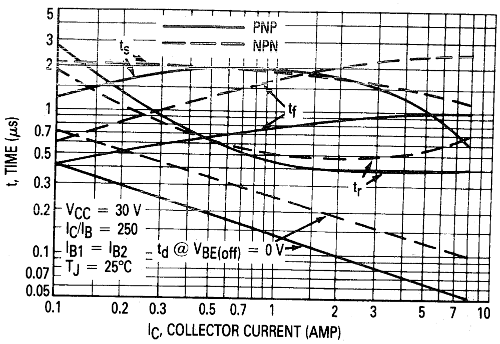


Figure 10. Switching Times

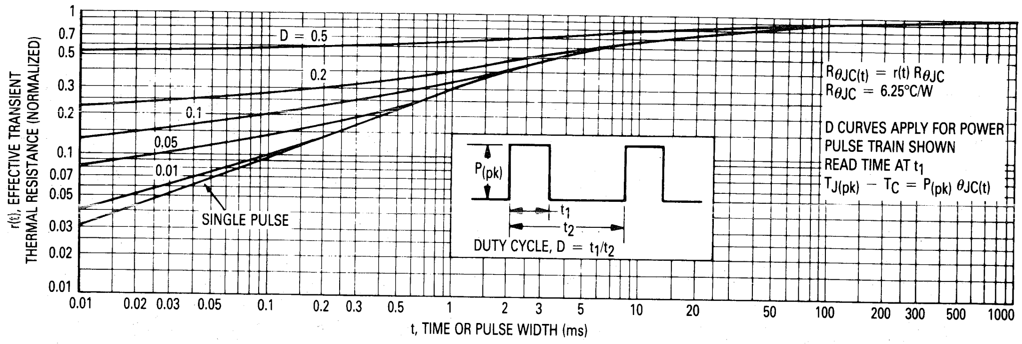


Figure 11. Thermal Response

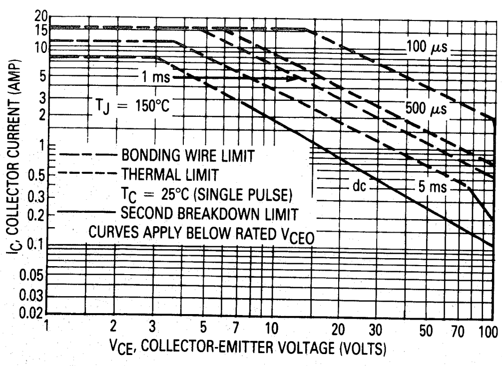


Figure 12. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

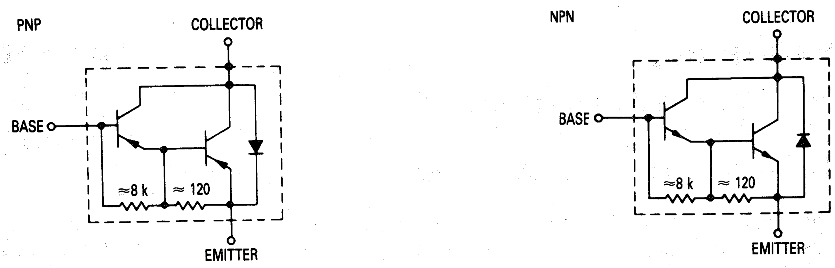
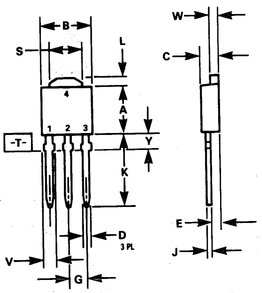


Figure 13. Darlington Schematic

OUTLINE DIMENSIONS

CASE 369-03

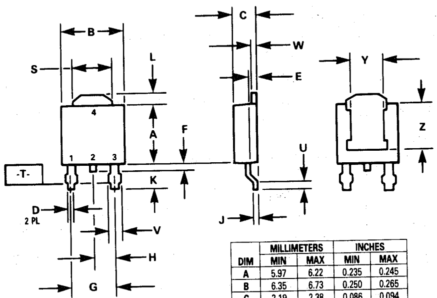


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   ⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

CASE 369A-04



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   ⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD122-1)

3

Complementary Plastic Power Transistors

NPN/PNP Silicon

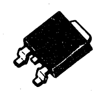
DPAK For Surface Mount Applications

NPN MJD200
PNP MJD210

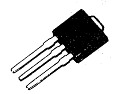
. . . designed for low voltage, low-power, high-gain audio amplifier applications.

- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain — h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2 Adc
  = 10 (Min) @ I_C = 5 Adc
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.75 Vdc (Max) @ I_C = 2 Adc
- High Current-Gain — Bandwidth Product — f_T = 65 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage — I_{CBO} = 100 nAdc @ Rated V_{CB}

SILICON POWER TRANSISTORS
5 AMPERES
25 VOLTS
12.5 WATTS



CASE 369A-04



CASE 369-03

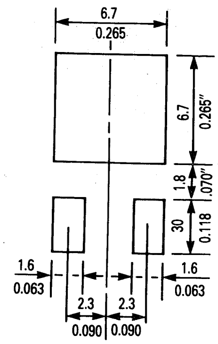
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	40	Vdc
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Emitter-Base Voltage	V_{EB}	8	Vdc
Collector Current — Continuous Peak	I_C	5 10	Adc
Base Current	I_B	1	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1	Watts W/°C
Total Device Dissipation @ T_A = 25°C* Derate above 25°C	P_D	1.4 0.011	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Junction to Ambient*	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	°C/W

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	—	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	— —	100 100	nAdc μAdc
Emitter Cutoff Current (V_{BE} = 8 Vdc, I_C = 0)	I_{EBO}	—	100	nAdc

* When surface mounted on minimum pad sizes recommended.
(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.

(continued)

3

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS				
DC Current Gain (1)	h_{FE}			—
(I_C = 500 mAdc, V_{CE} = 1 Vdc)		70	—	
(I_C = 2 Adc, V_{CE} = 1 Vdc)		45	180	
(I_C = 5 Adc, V_{CE} = 2 Vdc)		10	—	
Collector-Emitter Saturation Voltage (1)	$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)		—	0.3	
(I_C = 2 Adc, I_B = 200 mAdc)		—	0.75	
(I_C = 5 Adc, I_B = 1 Adc)		—	1.8	
Base-Emitter Saturation Voltage (1) (I_C = 5 Adc, I_B = 1 Adc)	$V_{BE(sat)}$	—	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 2 Adc, V_{CE} = 1 Vdc)	$V_{BE(on)}$	—	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}			pF
MJD200		—	80	
MJD210		—	120	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
(2) $f_T = |h_{FE}| \cdot f_{test}$

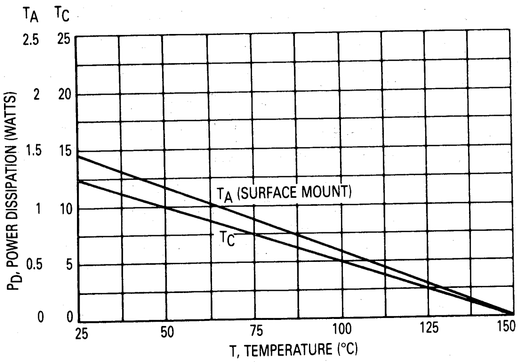


Figure 1. Power Derating

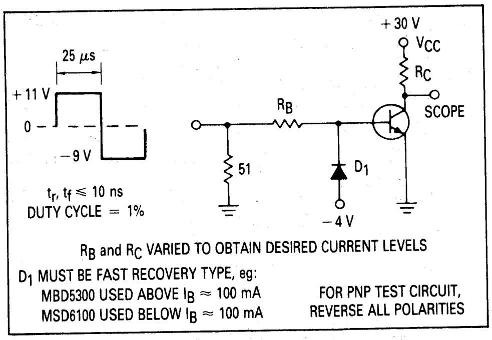


Figure 2. Switching Time Test Circuit

3

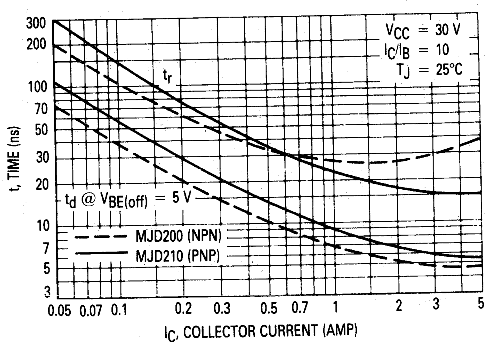


Figure 3. Turn-On Time

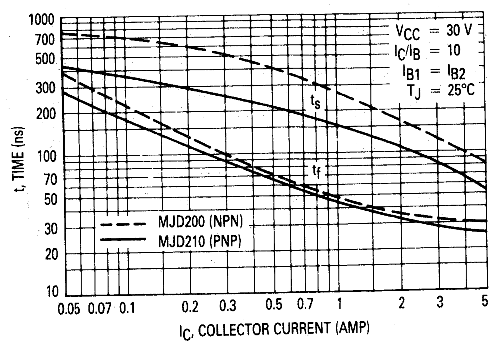


Figure 4. Turn-Off Time

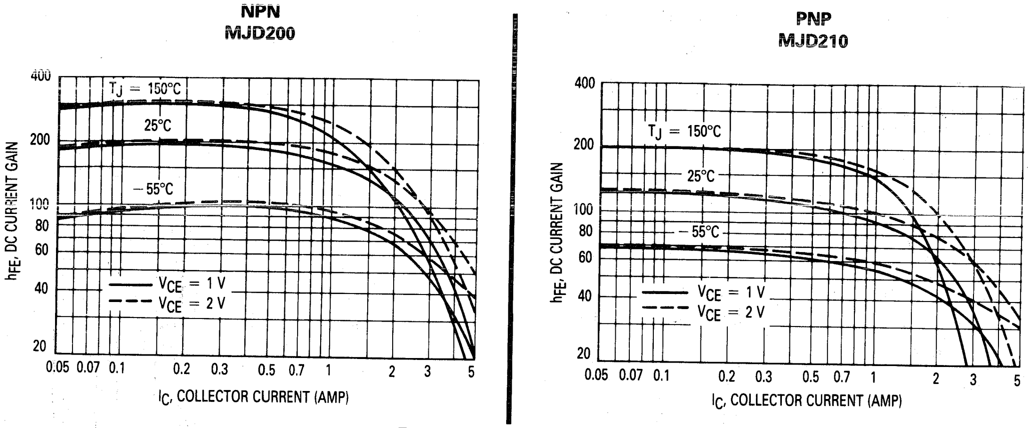


Figure 5. DC Current Gain

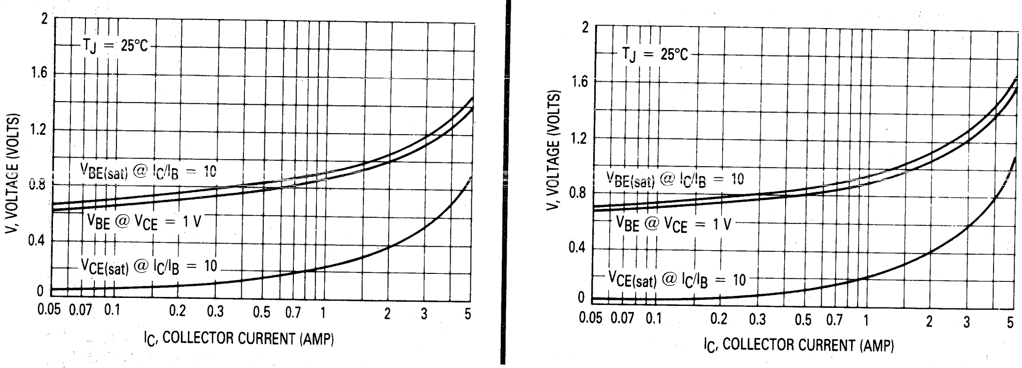


Figure 6. "On" Voltage

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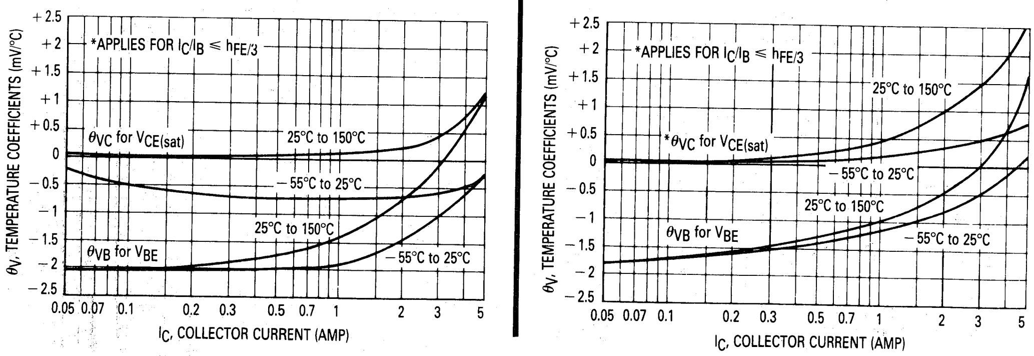


Figure 7. Temperature Coefficients

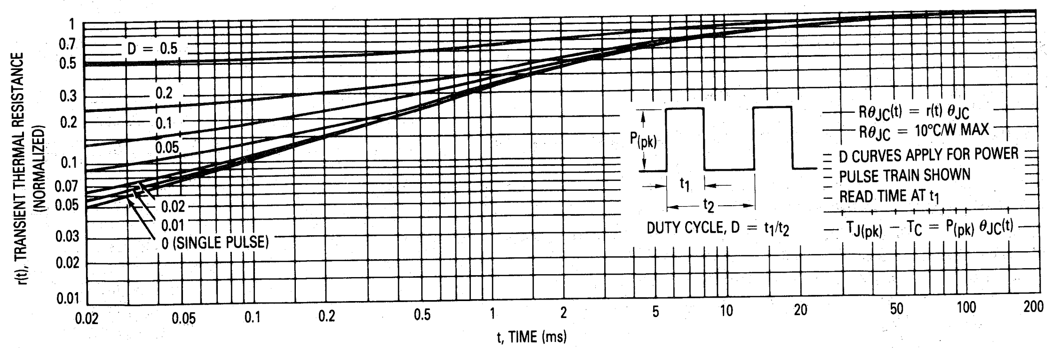


Figure 8. Thermal Response

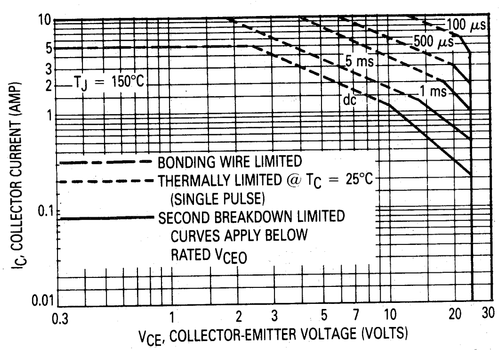


Figure 9. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

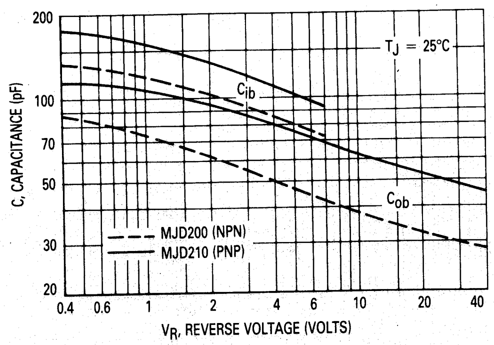
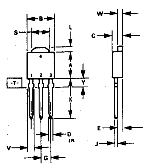


Figure 10. Capacitance

OUTLINE DIMENSIONS

CASE 369-03

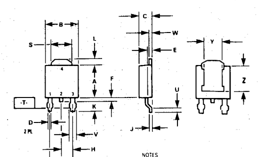


NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE
2. POSITIONAL TOLERANCE FOR "D" DIAMETER
   | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982
4. CONTROLLING DIMENSION: INCH

STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

CASE 369A-04



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE
2. POSITIONAL TOLERANCE FOR "D" DIAMETER
   | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982
4. CONTROLLING DIMENSION: INCH

STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD200-1)

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

High Voltage Power Transistors

DPAK For Surface Mount Applications

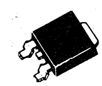
NPN MJD340

PNP MJD350

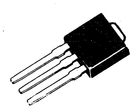
Designed for line operated audio output amplifier, switchmode power supply drivers and other switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Electrically Similar to Popular MJE340 and MJE350
- 300 V (Min) — $V_{CEO(sus)}$
- 0.5 A Rated Collector Current

SILICON POWER TRANSISTORS
0.5 AMPERE
300 VOLTS
15 WATTS

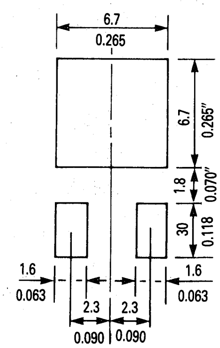


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	3	Vdc
Collector Current — Continuous — Peak	I_C	0.5 0.75	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.56 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 1 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 3 Vdc, I_C = 0)	I_{EBO}	—	0.1	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—

* When surface mounted on minimum pad sizes recommended.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

3

TYPICAL CHARACTERISTICS

MJD340

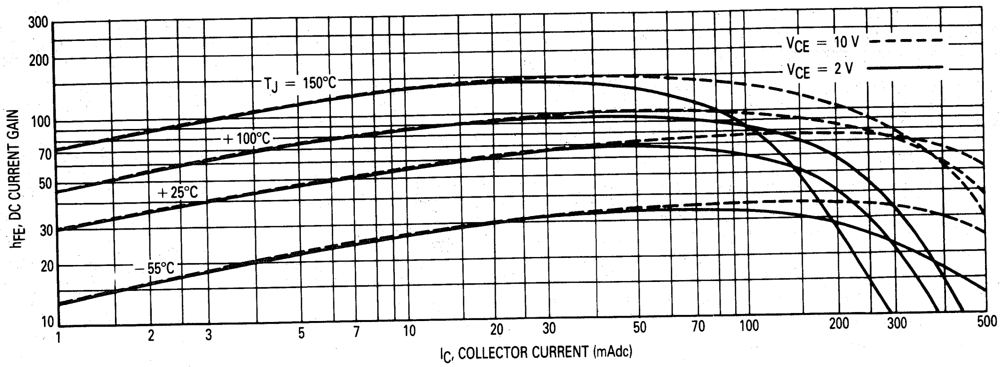


Figure 1. DC Current Gain

MJD340

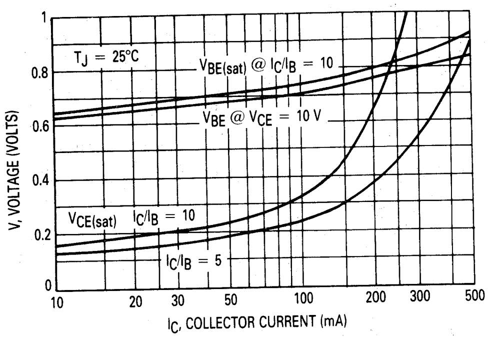


Figure 2. "On" Voltages

MJD350

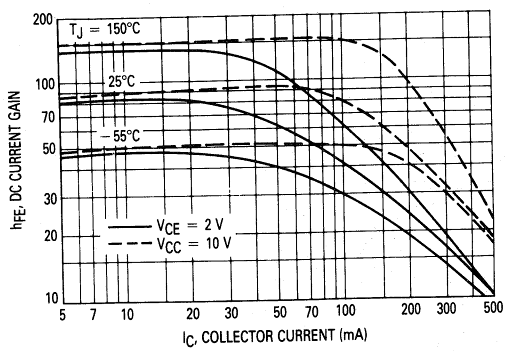


Figure 3. DC Current Gain

MJD350

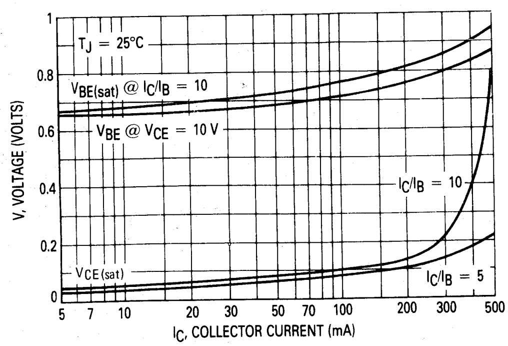


Figure 4. "On" Voltages

3

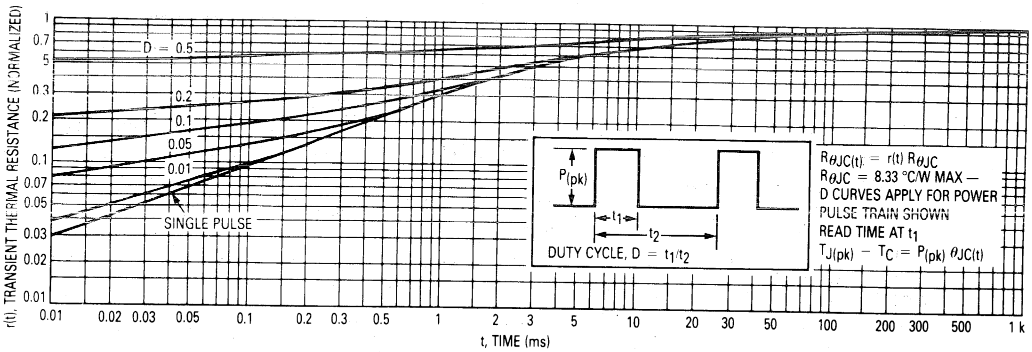


Figure 5. Thermal Response

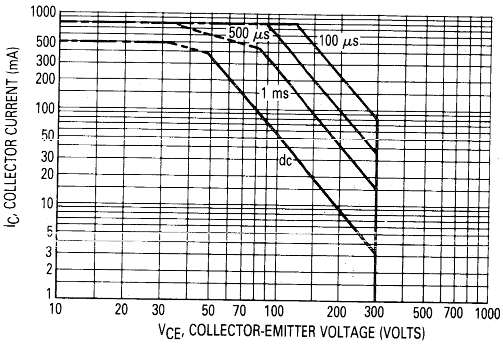


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

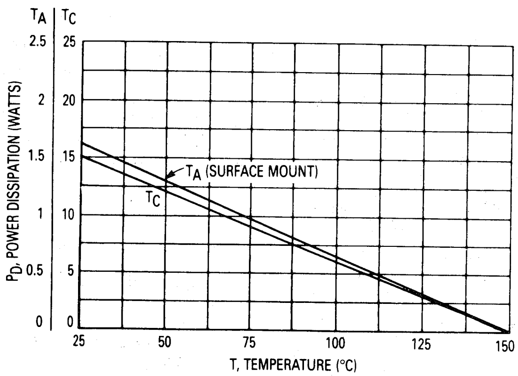
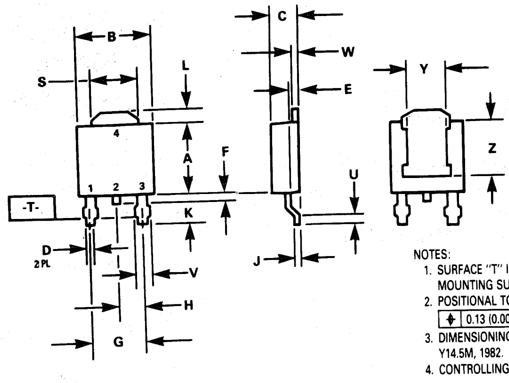


Figure 7. Power Derating

OUTLINE DIMENSIONS

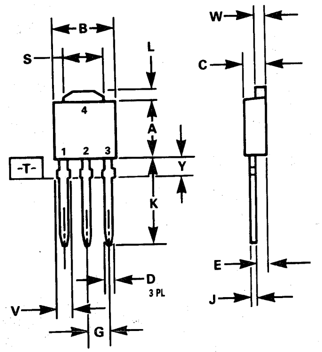


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   ⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

CASE 369A-04



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

NOTES
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2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   ⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

CASE 369-03

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD340-1)

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Complementary Power Transistors

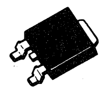
DPAK For Surface Mount Applications

PNP
MJD2955
NPN
MJD3055

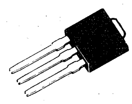
Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel ("RL" Suffix)
- Electrically Similar to MJE2955 and MJE3055
- DC Current Gain Specified to 10 Amperes
- High Current Gain-Bandwidth Product — f_T = 2 MHz (Min) @ I_C = 500 mAdc

SILICON
POWER TRANSISTORS
10 AMPERES
60 VOLTS
20 WATTS



CASE 369A-04



CASE 369-03

MAXIMUM RATINGS

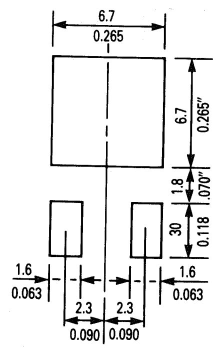
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	70	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D†	20 0.16	Watts W/°C
Total Power Dissipation (1) @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	°C/W

(1) These ratings are applicable when surface mounted on the minimum pad sizes recommended.
† Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS

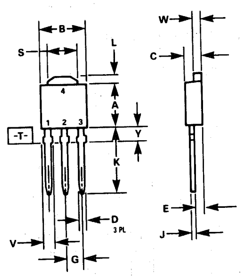


ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	50	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	0.02 2	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	— —	0.02 2	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4 Adc, V_{CE} = 4 Vdc) (I_C = 10 Adc, V_{CE} = 4 Vdc)	h_{FE}	20 5	100 —	—
Collector-Emitter Saturation Voltage (1) (I_C = 4 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	— —	1.1 8	Vdc
Base-Emitter On Voltage (1) (I_C = 4 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS

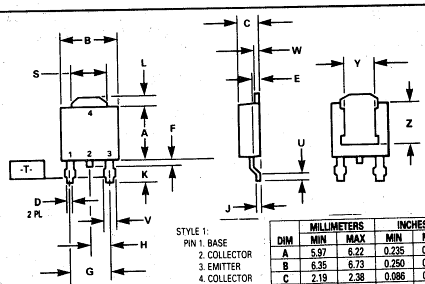


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
| ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

CASE 369-03



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
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2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
| ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

CASE 369A-04

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD3055-1)

3

TYPICAL CHARACTERISTICS

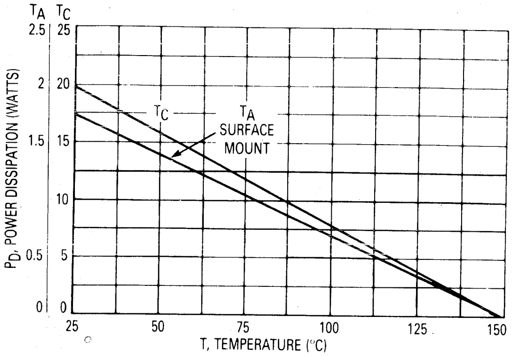


Figure 1. Power Derating

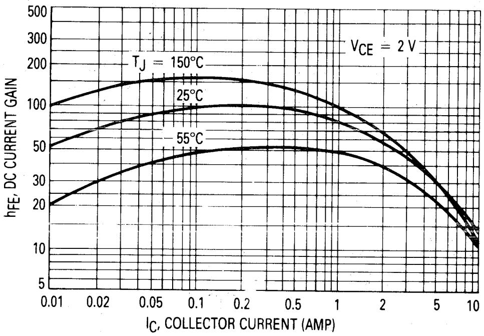


Figure 2. DC Current Gain

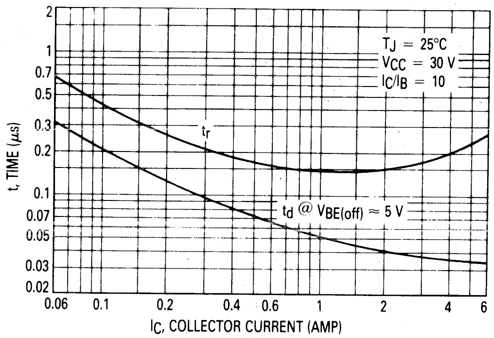


Figure 3. Turn-On Time

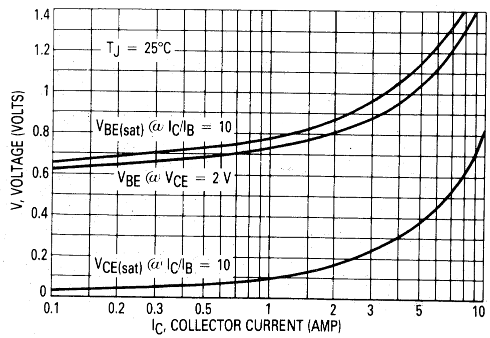


Figure 4. "On" Voltages, MJD3055

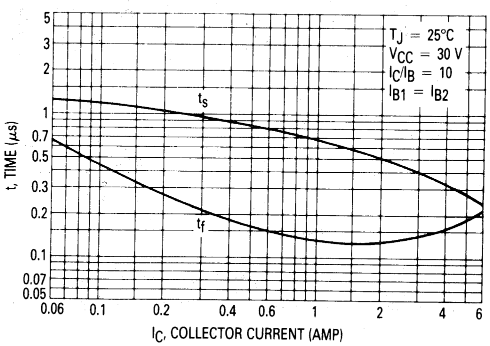


Figure 5. Turn-Off Time

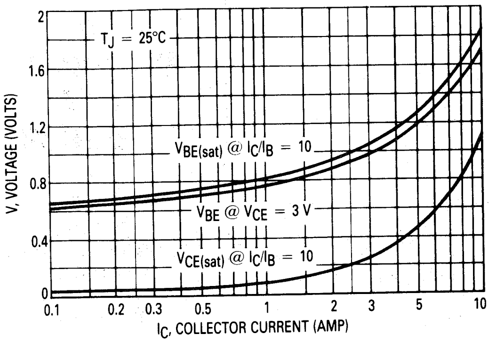


Figure 6. "On" Voltages, MJD2955

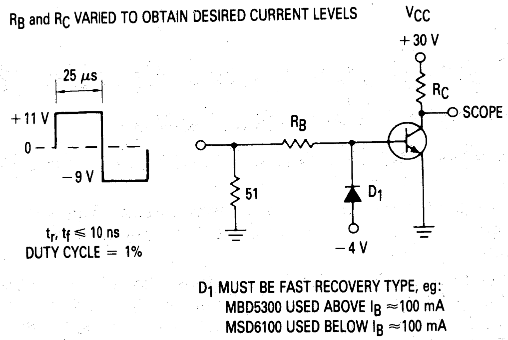


Figure 7. Switching Time Test Circuit

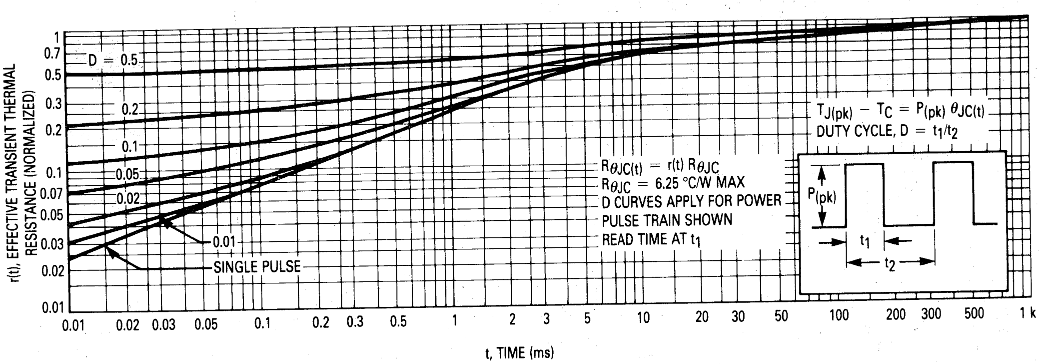


Figure 8. Thermal Response

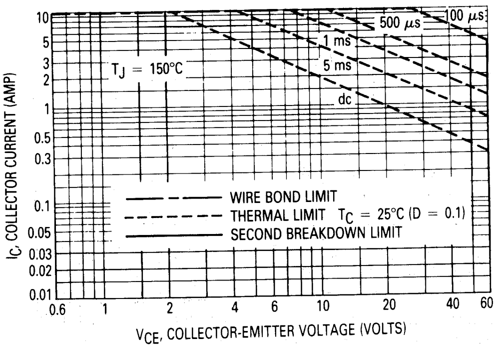


Figure 9. Maximum Forward Bias Safe Operating Area

FORWARD BIAS SAFE OPERATING AREA INFORMATION

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

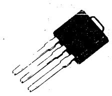
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Complementary Darlington Power Transistors
DPAK For Surface Mount Applications

PNP
MJD6036
NPN
MJD6039

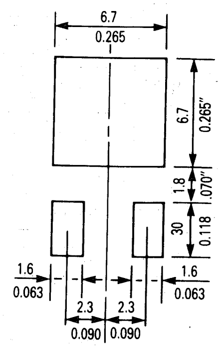
SILICON
POWER TRANSISTORS
4 AMPERES
80 VOLTS
20 WATTS

CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, convertors, and power amplifiers.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Available on 16 mm Tape and Reel for Automatic Handling ("RL" Suffix)
- Surface Mount Replacements for 2N6034–2N6039 Series
- Monolithic Construction With Built-in Base-Emitter Shunt Resistors
- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 4 Adc
- Complementary Pairs Simplifies Designs

MAXIMUM RATINGS

Rating	Symbol	MJD6036 MJD6039	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	4 8	Adc
Base Current	I_B	100	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation (1) @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	°C/W

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	80	—	Vdc
Collector-Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	—	10	μAdc

(1) These ratings are applicable when surface mounted on the minimum pad sizes recommended.
* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			—
(I_C = 1 Adc, V_{CE} = 4 Vdc)		1000	—	
(I_C = 2 Adc, V_{CE} = 4 Vdc)		500	—	
Collector-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 8 mAdc)	$V_{CE(sat)}$	—	2.5	Vdc
Base-Emitter On Voltage (I_C = 2 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1 kHz)	$\|h_{fe}\|$	25	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}			pF
MJD6036		—	200	
MJD6039		—	100	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

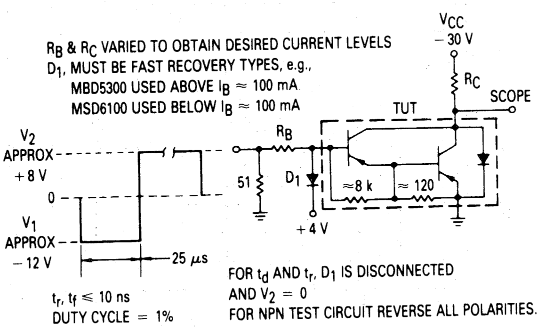


Figure 1. Switching Times Test Circuit

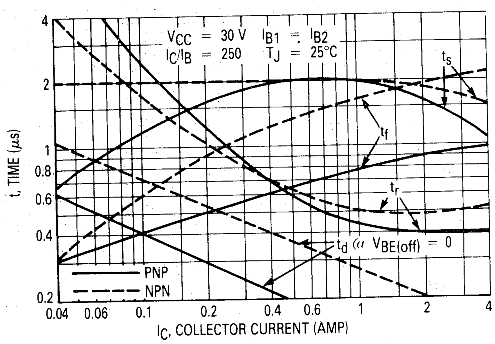


Figure 2. Switching Times

3

TYPICAL ELECTRICAL CHARACTERISTICS

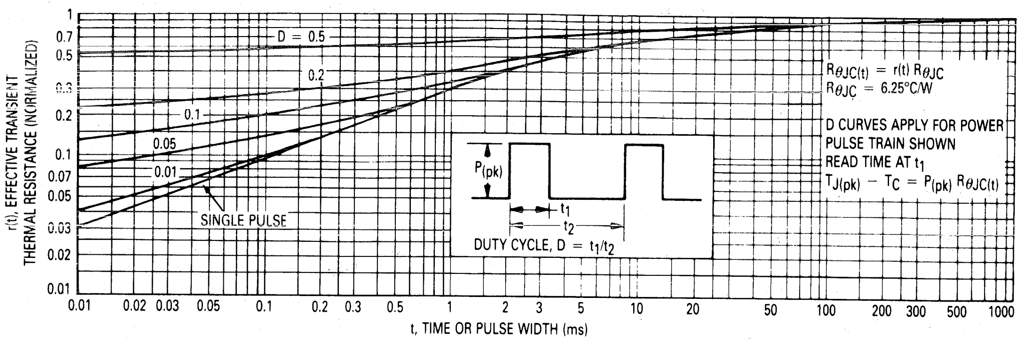


Figure 3. Thermal Response

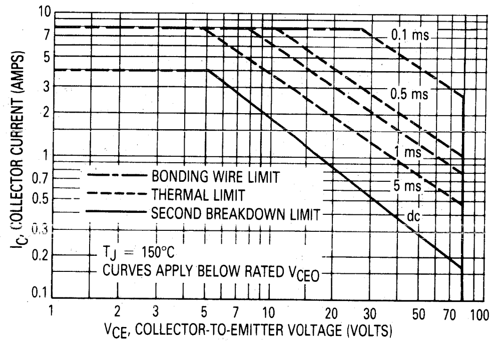


Figure 4. Maximum Rated Forward Biased Safe Operating Area

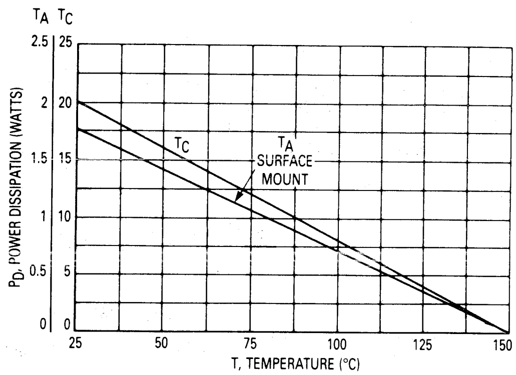


Figure 5. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 6 and 7 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

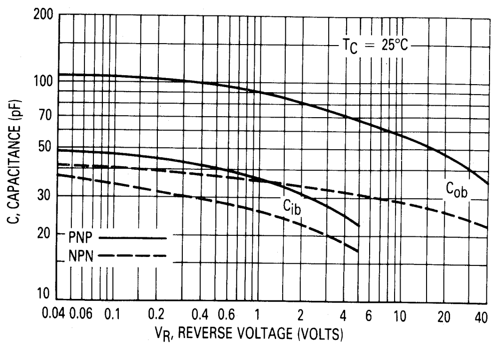


Figure 6. Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS

PNP MJD6036 | **NPN MJD6039**

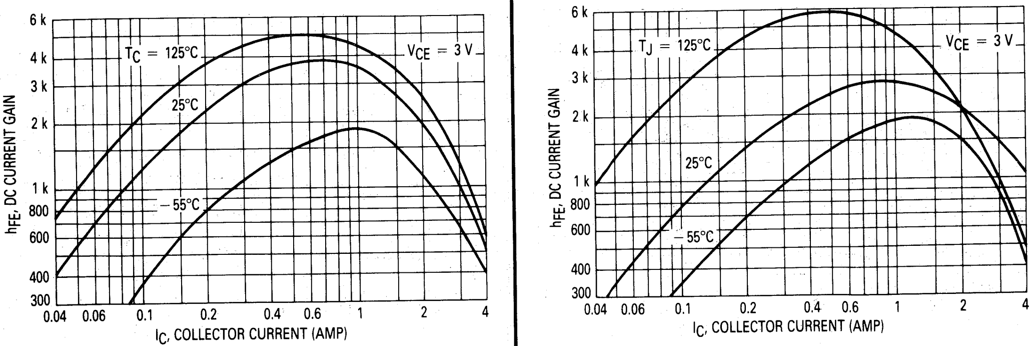


Figure 7. DC Current Gain

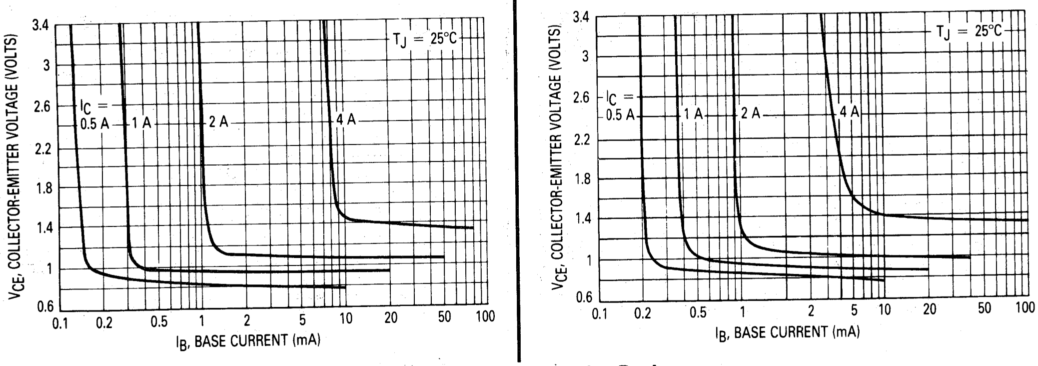


Figure 8. Collector Saturation Region

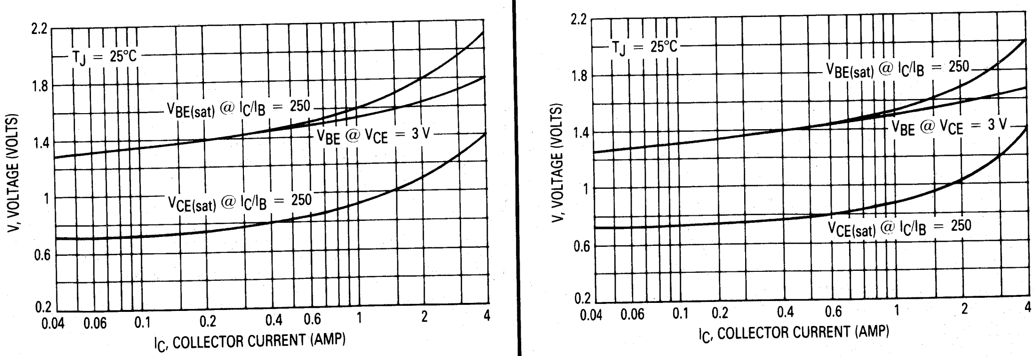


Figure 9. "On" Voltages

3

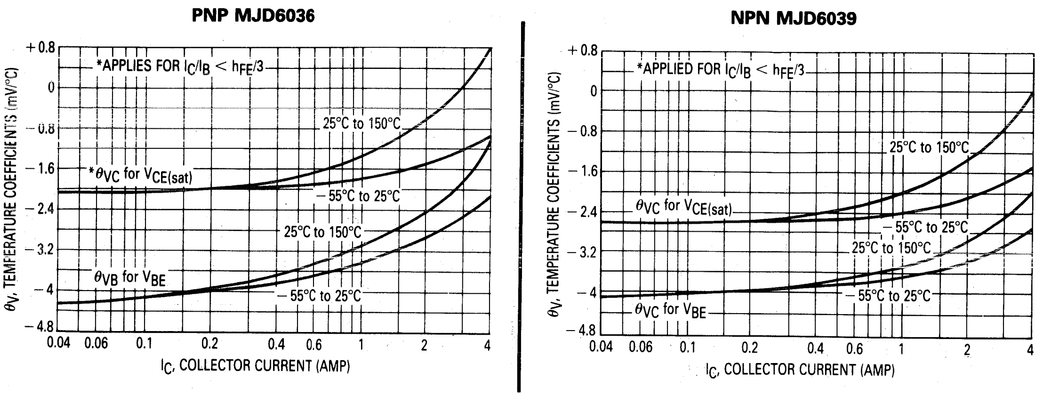


Figure 10. Temperature Coefficients

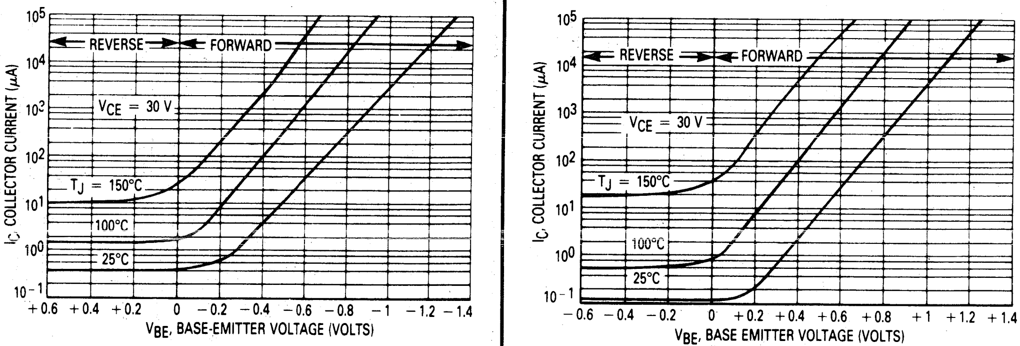


Figure 11. Collector Cut-Off Region

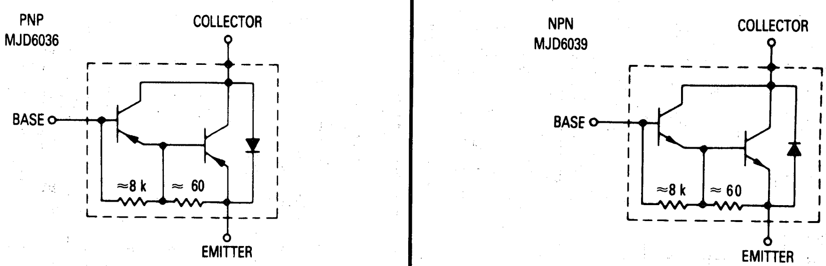
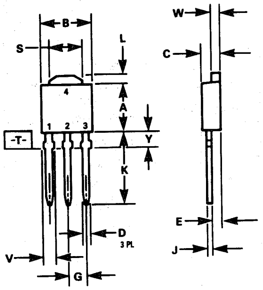


Figure 12. Darlington Schematic

3

OUTLINE DIMENSIONS

CASE 369-03

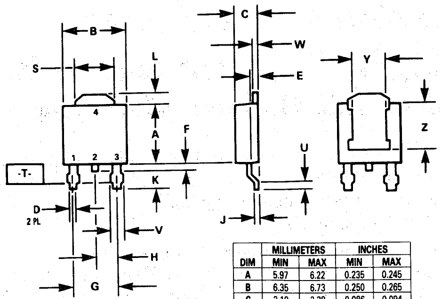


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   ⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

CASE 369A-04



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   ⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD6036-1)

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJD13003

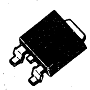
Designer's Data Sheet

High Voltage Switchmode Series
DPAK For Surface Mount Applications

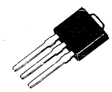
NPN SILICON POWER TRANSISTOR
1.5 AMPERES
400 VOLTS
15 WATTS

This device is designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 220 V SWITCHMODE applications such as switching regulators, inverters, motor controls, solenoid/relay drivers and deflection circuits.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Reverse Biased SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and 100°C . . . t_c @ 1 A, 100°C is 290 ns (Typ)
- 700 V Blocking Capability
- Switching and SOA Applications Information
- Electrically Similar to the Popular MJE13003

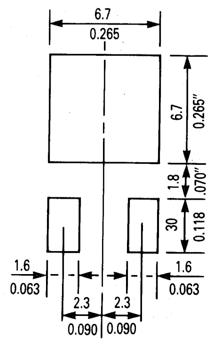


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	1.5 3	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	0.75 1.5	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	2.25 4.5	Adc
Total Power Dissipation @ T_A = 25°C (2) Derate above 25°C	P_D	1.56 0.0125	Watts W/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient (2)	$R_{\theta JA}$	80	°C/W
Maximum Lead Temperature for Soldering Purposes	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.
(2) When surface mounted on minimum pad sizes recommended.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

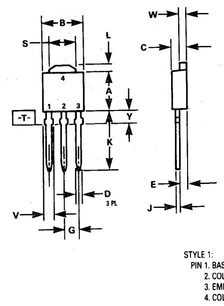
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)		$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	— —	— —	0.1 2	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	—	—	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 11			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 12			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 2 Vdc) (I_C = 1 Adc, V_{CE} = 2 Vdc)		h_{FE}	8 5	— —	40 25	—
Collector-Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc) (I_C = 1 Adc, I_B = 0.25 Adc) (I_C = 1.5 Adc, I_B = 0.5 Adc) (I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)		$V_{CE(sat)}$	— — — —	— — — —	0.5 1 3 1	Vdc
Base-Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc) (I_C = 1 Adc, I_B = 0.25 Adc) (I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)		$V_{BE(sat)}$	— — —	— — —	1 1.2 1.1	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	10	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	21	—	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	V_{CC} = 125 Vdc, I_C = 1 A, I_{B1} = I_{B2} = 0.2 A, t_p = 25 μs, Duty Cycle ≤ 1%	t_d	—	0.05	0.1	μs
Rise Time		t_r	—	0.5	1	μs
Storage Time		t_s	—	2	4	μs
Fall Time		t_f	—	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Storage Time	I_C = 1 A, V_{clamp} = 300 Vdc, I_{B1} = 0.2 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C	t_{sv}	—	1.7	4	μs
Crossover Time		t_c	—	0.29	0.75	μs
Fall Time		t_{fi}	—	0.15	—	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

3

OUTLINE DIMENSIONS

CASE 369-03



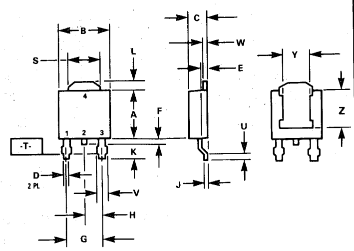
NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 369A-04

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—



NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

STYLE 1.
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD13003-1)

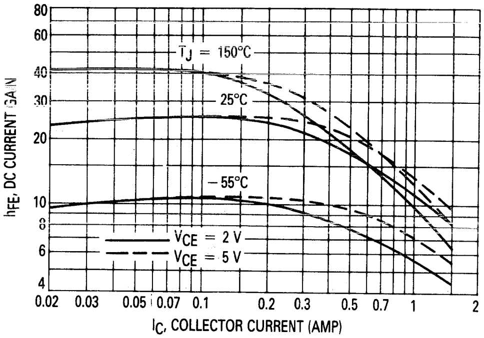


Figure 1. DC Current Gain

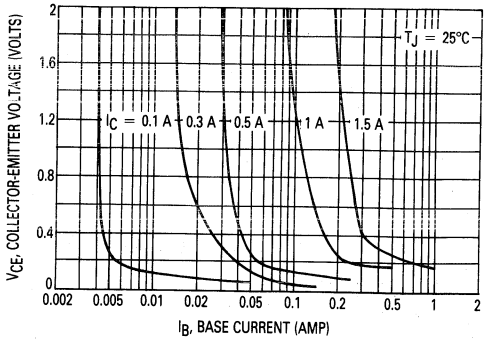


Figure 2. Collector Saturation Region

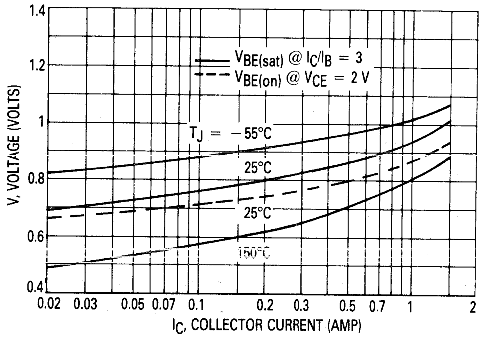


Figure 3. Base-Emitter Voltage

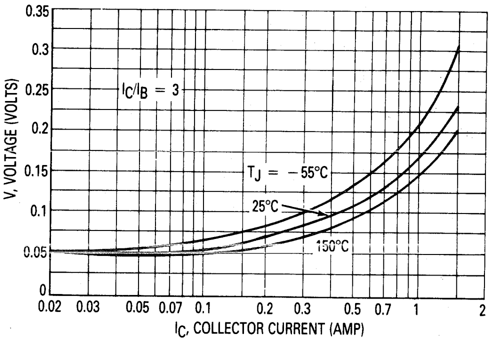


Figure 4. Collector-Emitter Saturation Region

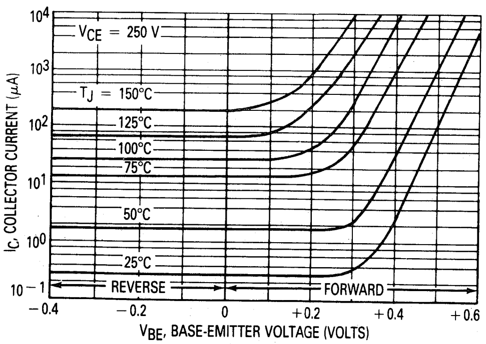


Figure 5. Collector Cutoff Region

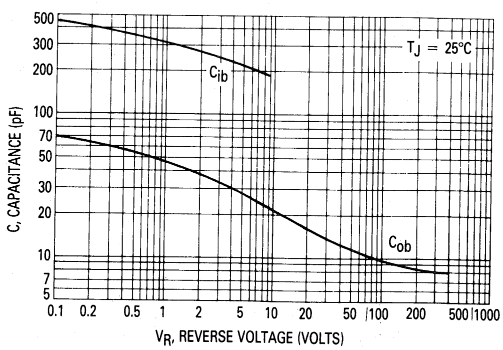


Figure 6. Capacitance

3

Table 1. Test Conditions For Dynamic Performance

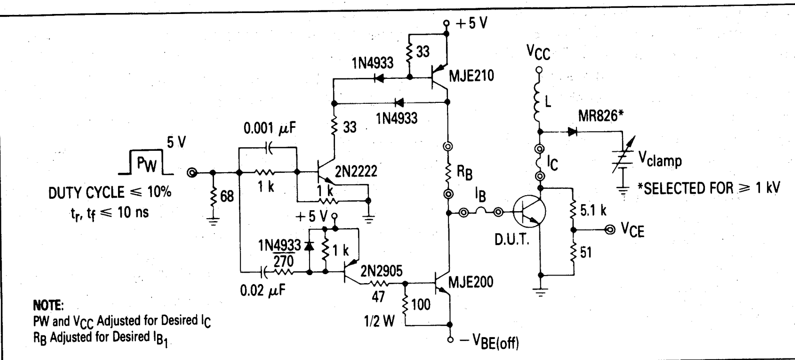
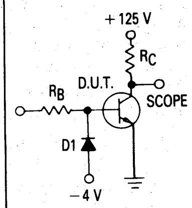
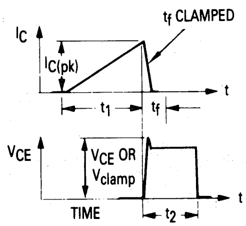
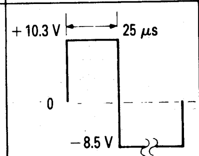
	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	COIL DATA: FERROXCUBE CORE #6656 FULL BOBBIN (~200 TURNS) #20; GAP FOR 30 mH/2 A; L_{coil} = 50 mH; V_{CC} = 20 V; V_{clamp} = 300 Vdc	V_{CC} = 125 V; R_C = 125 Ω; D1 = 1N5820 OR EQUIV.; R_B = 47 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 ADJUSTED TO OBTAIN I_C; $t_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$; $t_2 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{clamp}}$; TEST EQUIPMENT SCOPE-TEKTRONICS 475 OR EQUIVALENT	 t_r, t_f < 10 ns; DUTY CYCLE = 1.0%; R_B AND R_C ADJUSTED FOR DESIRED I_B AND I_C

Table 2. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

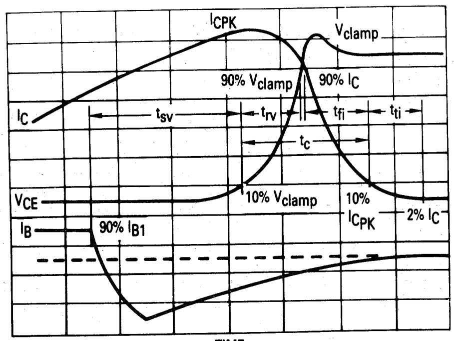


Figure 7. Inductive Switching Measurements

3

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the equation:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

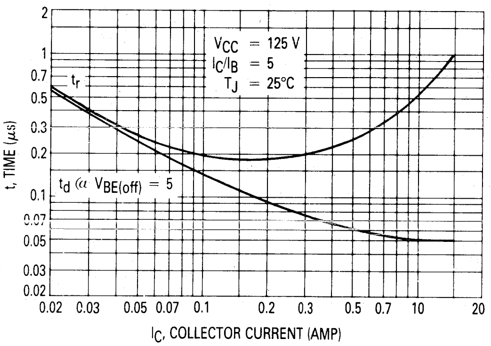


Figure 8. Turn-On Time

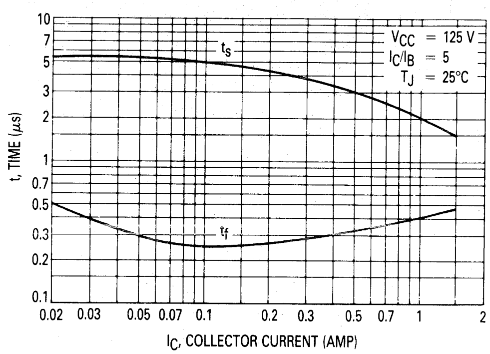


Figure 9. Turn-Off Time

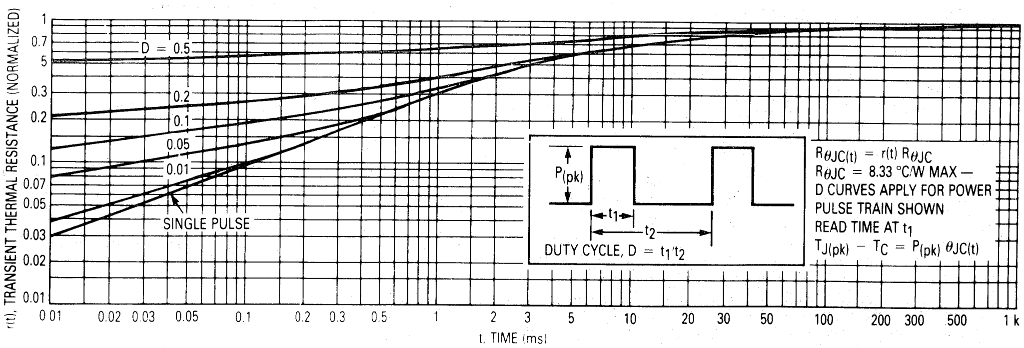


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

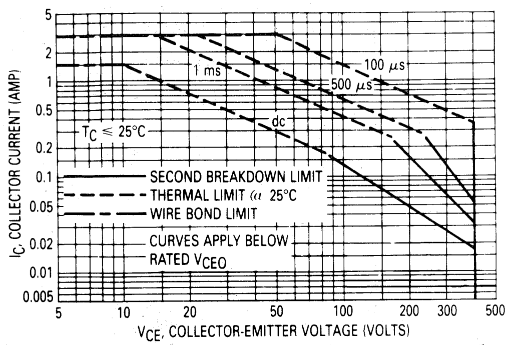


Figure 11. Active Region Safe Operating Area

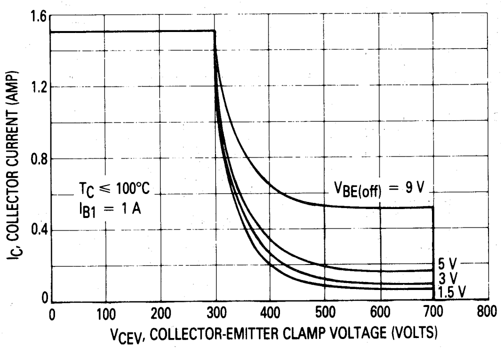


Figure 12. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by applying curves on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

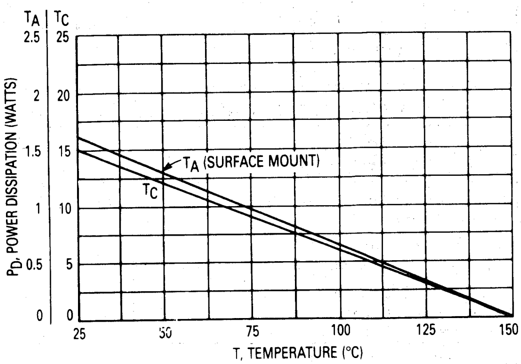


Figure 13. Power Derating

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE105

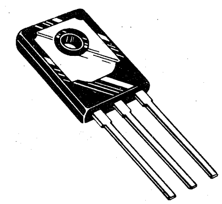
MEDIUM-POWER PNP SILICON TRANSISTOR

. . . for use as an output device in complementary audio amplifiers up to 20-Watts music power per channel.

- High DC Current Gain – h_{FE} = 25-100 @ I_C = 2.0 A
- Thermopad High-Efficiency Compact Package
- Complementary to NPN MJE205

5 AMPERE
POWER TRANSISTOR
PNP SILICON

50 VOLTS
65 WATTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	5.0	Adc
Base Current	I_B	2.5	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D(1)	65 0.522	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

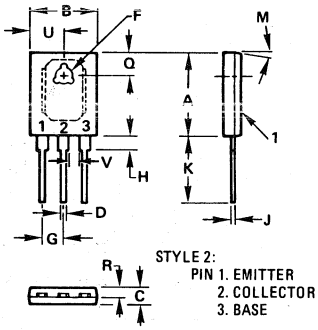
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.92	°C/W

(1) Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (2) (I_C = 100 mAdc, I_B = 0)	BV_{CEO}	50	–	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 50 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 – –	 0.1 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter Voltage (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	V_{BE}	–	1.2	Vdc

(2) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.



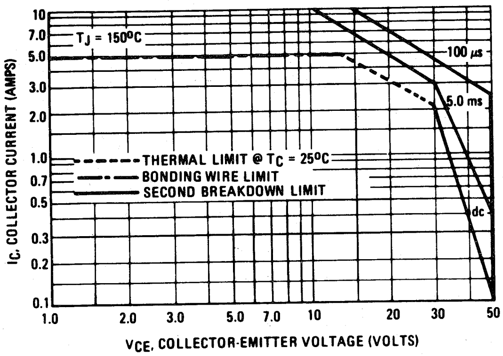
STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-225AB

3

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – "ON" VOLTAGES

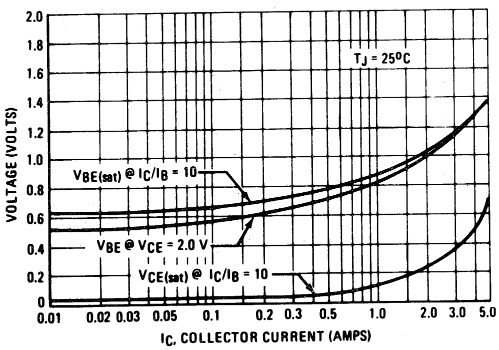


FIGURE 3 – DC CURRENT GAIN

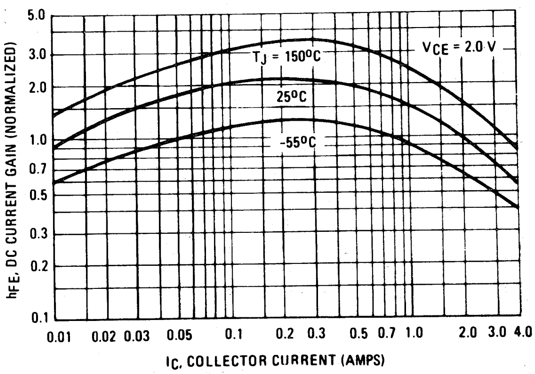
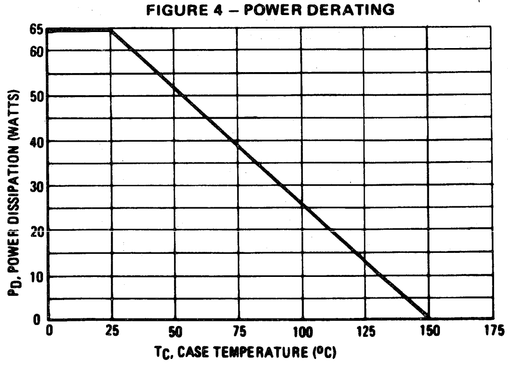


FIGURE 4 – POWER DERATING



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

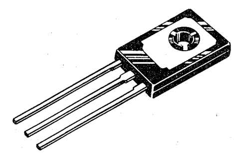
PNP
MJE170 thru MJE172
NPN
MJE180 thru MJE182

COMPLEMENTARY PLASTIC SILICON POWER TRANSISTORS

. . . designed for low power audio amplifier and low current, high speed switching applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc — MJE170, MJE180
  = 60 Vdc — MJE171, MJE181
  = 80 Vdc — MJE172, MJE182
- DC Current Gain —
  h_{FE} = 30 (Min) @ I_C = 0.5 Adc
  = 12 (Min) @ I_C = 1.5 Adc
- Current-Gain — Bandwidth Product —
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages —
  I_{CBO} = 100 nA (Max) @ Rated V_{CB}

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
40-60-80 VOLTS
12.5 WATTS



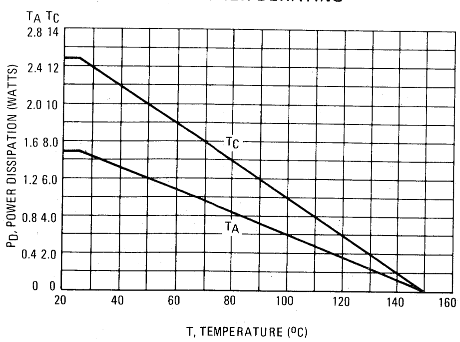
MAXIMUM RATINGS

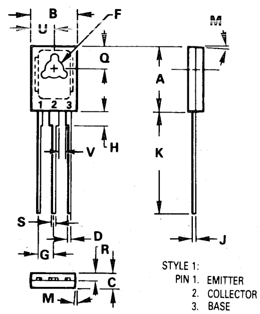
Rating	Symbol	MJE170 MJE180	MJE171 MJE181	MJE172 MJE182	Unit
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 3.0 → ← 6.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 1.5 → ← 0.012 →			Watts W/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 12.5 → ← 0.1 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

3

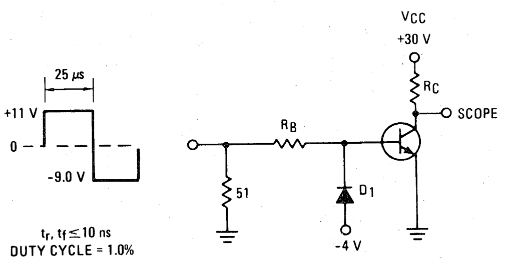
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	MJE170, MJE180		40	–	
	MJE171, MJE181		60	–	
	MJE172, MJE182		80	–	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 60 Vdc, I_E = 0)	MJE170, MJE180		–	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	MJE171, MJE181		–	0.1	
(V_{CB} = 100 Vdc, I_E = 0)	MJE172, MJE182		–	0.1	
(V_{CB} = 60 Vdc, I_E = 0, T_C = 150°C)	MJE170, MJE180		–	0.1	mAdc
(V_{CB} = 80 Vdc, I_E = 0, T_C = 150°C)	MJE171, MJE181		–	0.1	
(V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	MJE172, MJE182		–	0.1	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			50	250	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			30	–	
(I_C = 1.5 Adc, V_{CE} = 1.0 Vdc)			12	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			–	0.3	
(I_C = 1.5 Adc, I_B = 150 mAdc)			–	0.9	
(I_C = 3.0 Adc, I_B = 600 mAdc)			–	1.7	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 150 mAdc)			–	1.5	
(I_C = 3.0 Adc, I_B = 600 mAdc)			–	2.0	
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	50	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJE170/MJE172		–	60	
	MJE180/MJE182		–	40	

(1) $f_T = |h_{fe}| \bullet f_{test}$

3

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE IB ≈100 mA
MSD6100 USED BELOW IB ≈100 mA

For PNP test circuit, reverse all polarities.

FIGURE 3 — TURN-ON TIME

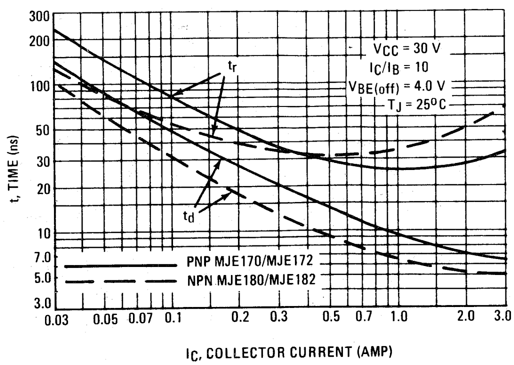
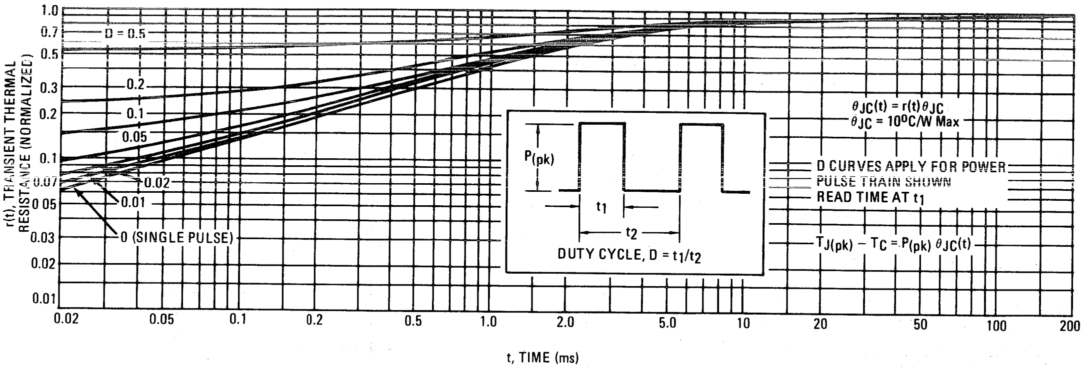


FIGURE 4 — THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 — MJE170, MJE171, MJE172

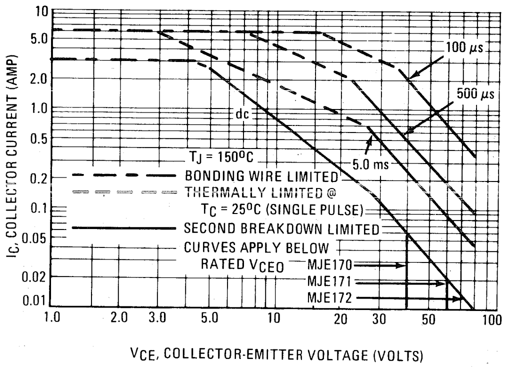
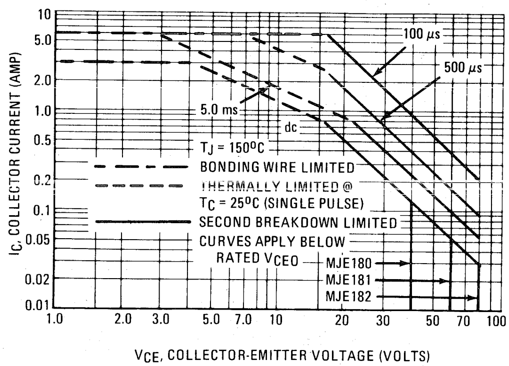


FIGURE 6 — MJE180, MJE181, MJE182



There are two limitations on the power handling ability of a transistor — average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperature, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 — TURN-OFF TIME

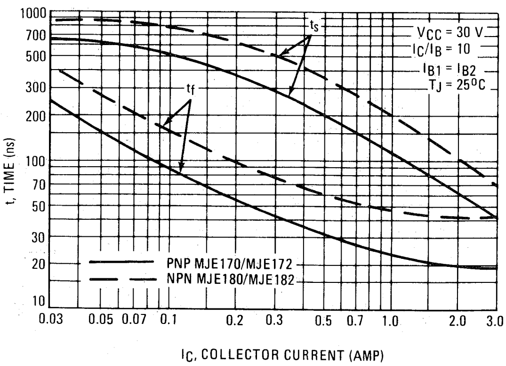
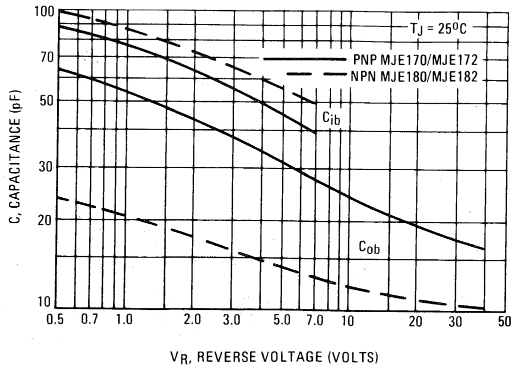


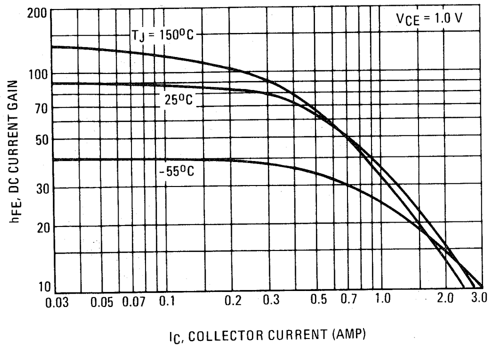
FIGURE 8 — CAPACITANCE



PNP
MJE170, MJE171, MJE172

NPN
MJE180, MJE181, MJE182

FIGURE 9 – DC CURRENT GAIN



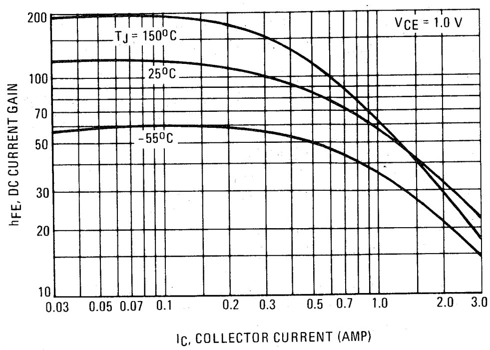
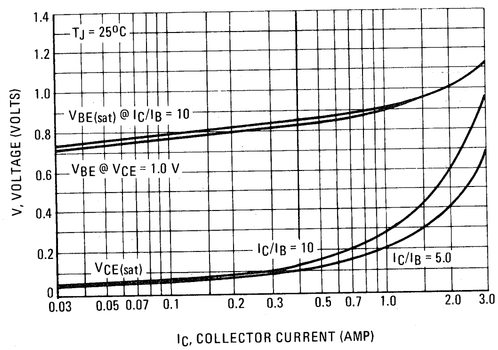


FIGURE 10 – "ON" VOLTAGES



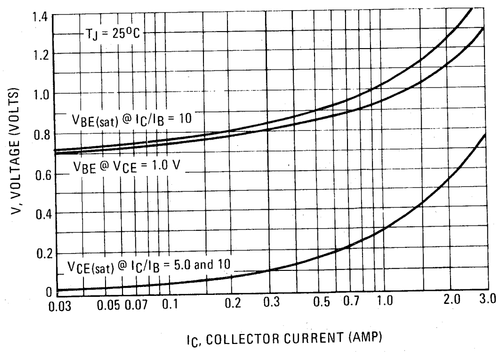
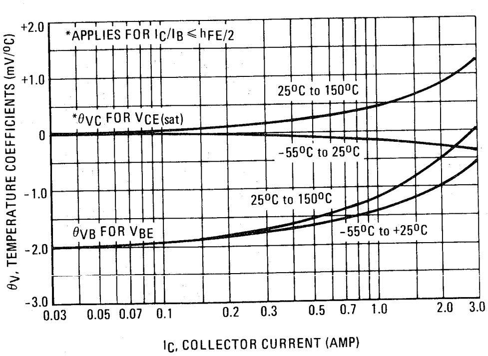
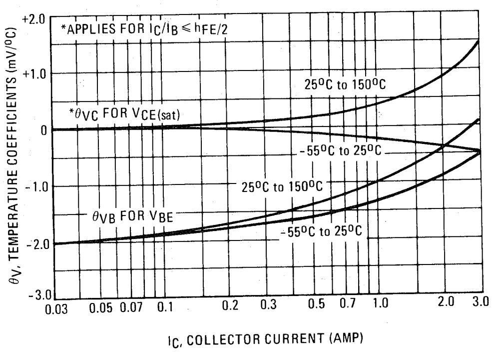


FIGURE 11 – TEMPERATURE COEFFICIENTS





3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

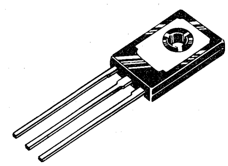
NPN
MJE200
PNP
MJE210

COMPLEMENTARY SILICON POWER PLASTIC TRANSISTORS

. . . designed for low voltage, low-power, high-gain audio amplifier applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain — h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2.0 Adc
  = 10 (Min) @ I_C = 5.0 Adc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.75 Vdc (Max) @ I_C = 2.0 Adc
- High Current-Gain — Bandwidth Product —
  f_T = 65 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage — I_{CBO} =100 nAdc @ Rated V_{CB}

5 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
25 VOLTS
15 WATTS



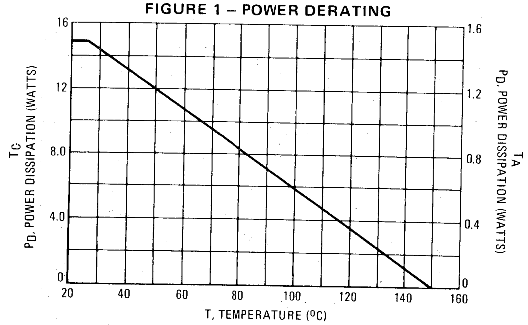
MAXIMUM RATINGS

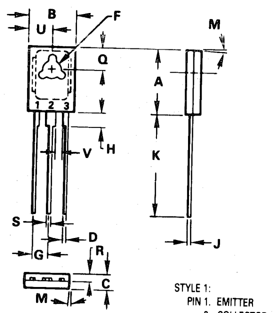
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	40	Vdc
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Emitter-Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous Peak	I_C	5.0 10	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	–	100	nAdc
(V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)		–	100	μAdc
Emitter Cutoff Current (V_{BE} = 8.0 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (1)	h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		70	–	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)		45	180	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)		10	–	
Collector-Emitter Saturation Voltage (1)	$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)		–	0.3	
(I_C = 2.0 Adc, I_B = 200 mAdc)		–	0.75	
(I_C = 5.0 Adc, I_B = 1.0 Adc)		–	1.8	
Base-Emitter Saturation Voltage (1) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	–	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJE200	C_{ob}	–	80	pF
MJE210		–	120	

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle ≈ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

3

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

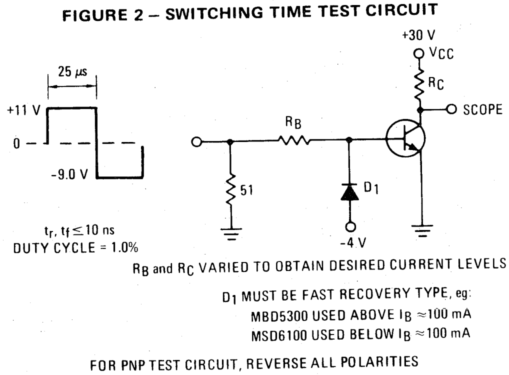


FIGURE 3 – TURN-ON TIME

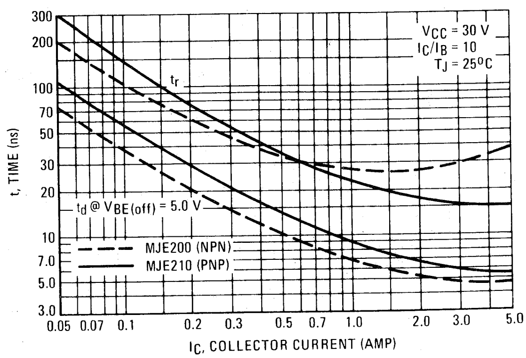


FIGURE 4 – THERMAL RESPONSE

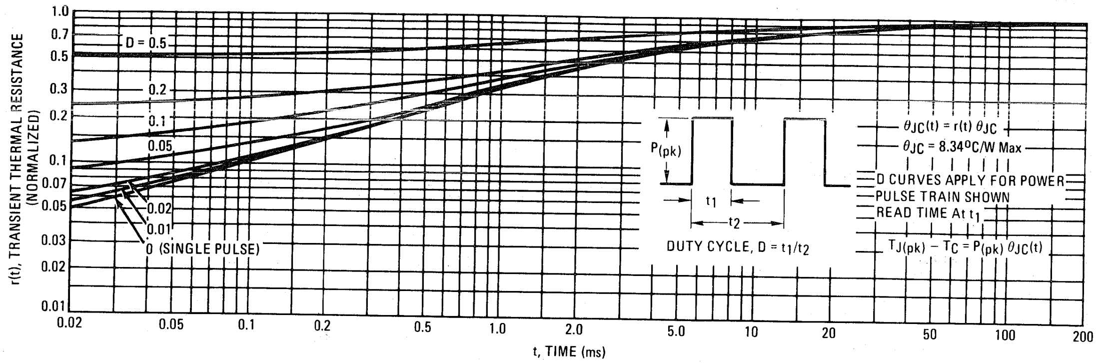
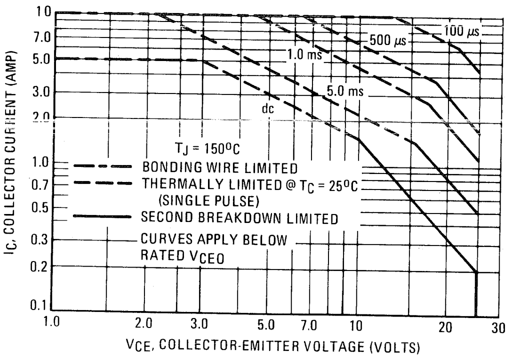


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

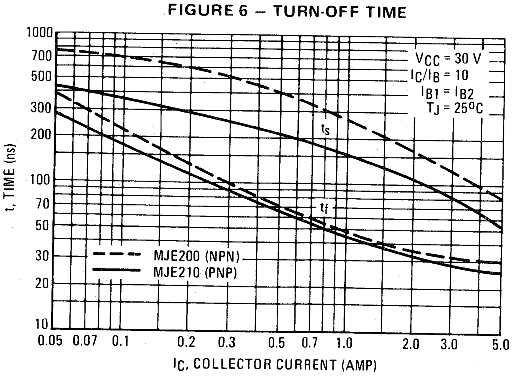
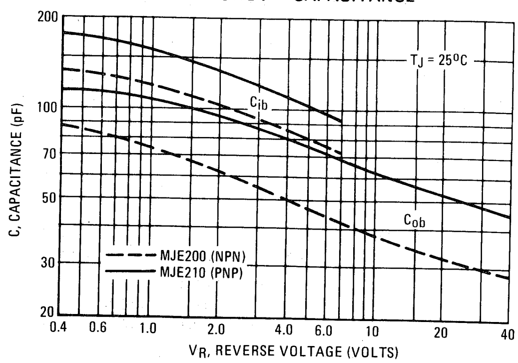


FIGURE 7 – CAPACITANCE



NPN
MJE200

PNP
MJE210

FIGURE 8 – DC CURRENT GAIN

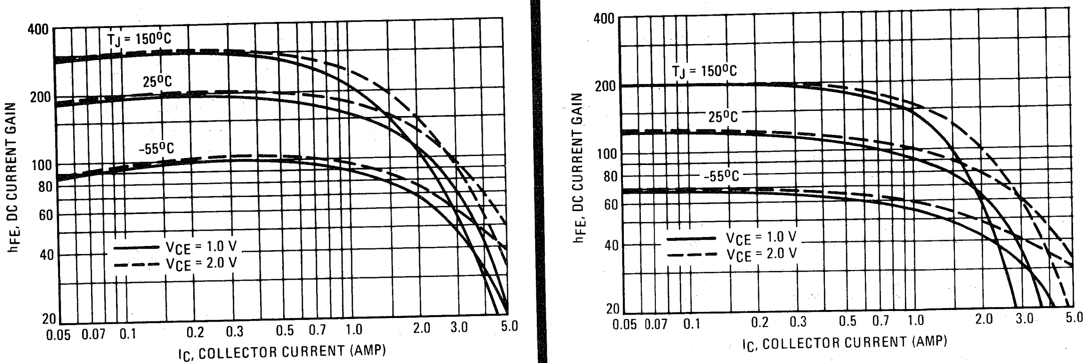


FIGURE 9 – "ON" VOLTAGE

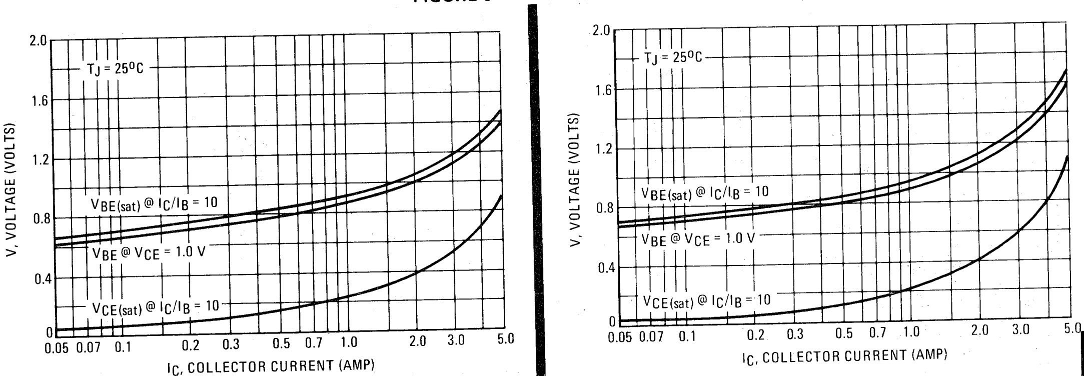
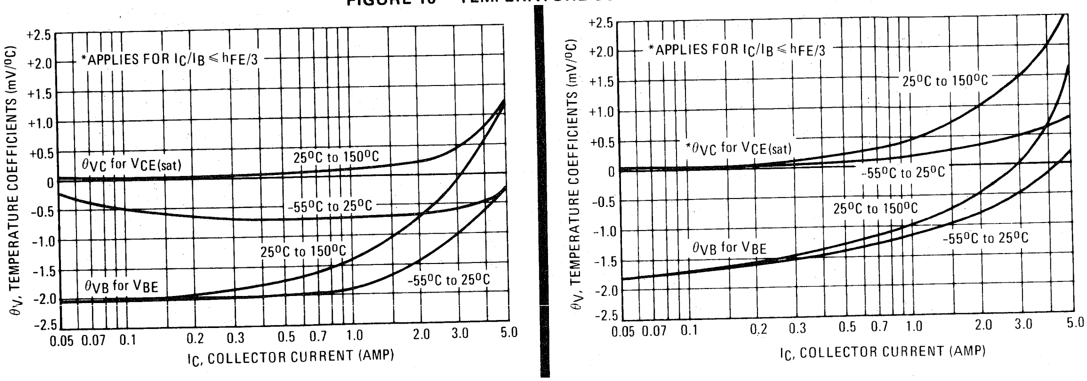


FIGURE 10 – TEMPERATURE COEFFICIENTS



3

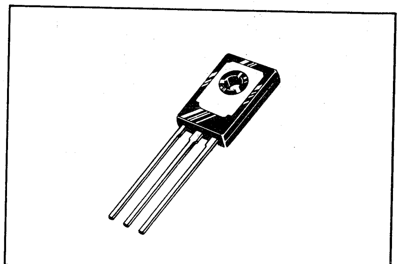
NPN
MJE240, MJE241
MJE243, MJE244
PNP
MJE250 thru MJE254

COMPLEMENTARY SILICON POWER PLASTIC TRANSISTORS

. . . designed for low power audio amplifier and low-current, high-speed switching applications.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — MJE240, MJE250/2
  = 100 Vdc (Min) — MJE243/4, MJE253/4
- High DC Current Gain @ I_C = 200 mAdc
  h_{FE} = 40–200 — MJE240, MJE250
  = 40–120 — MJE241,243, MJE251,253
  = 25 (Min) — MJE244, MJE252,54
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
- High Current Gain Bandwidth Product —
  f_T = 40 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages
  I_{CBO} = 100 nAdc (Max) @ Rated V_{CB}

4 AMPERE
POWER TRANSISTORS COMPLEMENTARY SILICON
80, 100 VOLTS
15 WATTS

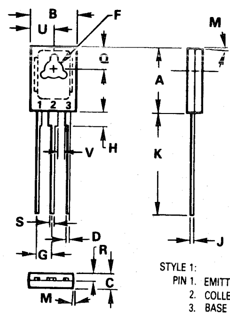


MAXIMUM RATINGS

Rating	Symbol	MJE240 MJE241 MJE250 MJE251 MJE252	MJE243 MJE244 MJE253 MJE254	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current – Continuous Peak	I_C	4.0 8.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W



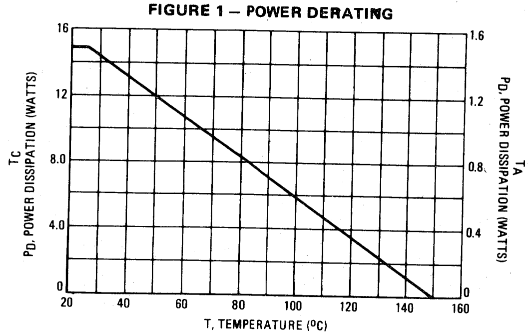
STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

FIGURE 1 — POWER DERATING



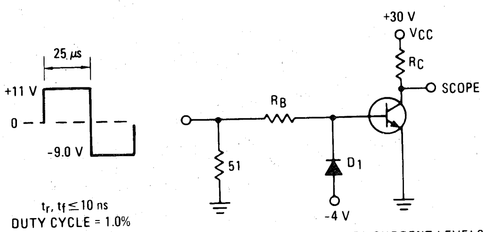
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	MJE240,MJE241, MJE250,MJE251,MJE252	$V_{CEO(sus)}$	80	–	Vdc
	MJE243,MJE244 MJE253,MJE254		100	–	
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	MJE240,MJE241, MJE250,MJE251,MJE252	I_{CBO}	–	0.1	μAdc
(V_{CB} = 100 Vdc, I_E = 0)	MJE243,MJE244, MJE253,MJE254,		–	0.1	
(V_{CE} = 80 Vdc, I_E = 0, T_C = 125°C)	MJE240,MJE241, MJE250,MJE251,MJE252,		–	0.1	mAdc
(V_{CE} = 100 Vdc, I_E = 0, T_C = 125°C)	MJE243,MJE244 MJE253,MJE254		–	0.1	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 1.0 Vdc)	MJE240,MJE250	h_{FE}	40	200	–
	MJE241,MJE251,		40	120	
	MJE243,MJE253		40	180	
	MJE252, MJE244,MJE254		25	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	MJE241,MJE251,		20	–	
	MJE243,MJE253		15	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	MJE252 MJE244,MJE254		10	–	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)	MJE240,MJE250		15	–	
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	All Types	$V_{CE(sat)}$	–	0.3	Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc)	MJE241,MJE251, MJE243,MJE253		–	0.6	
(I_C = 2.0 Adc, I_B = 200 mAdc)	MJE240, MJE250		–	0.8	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	1.8	Vdc
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJE240/MJE244	C_{ob}	–	50	pF
	MJE250/MJE254		–	70	

3

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

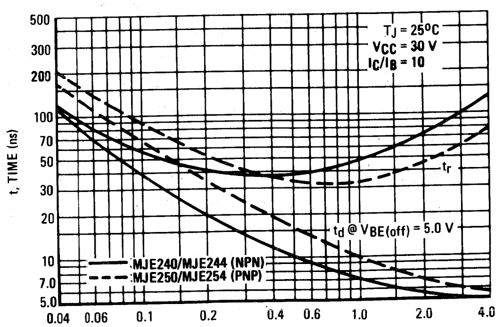


FIGURE 4 – THERMAL RESPONSE

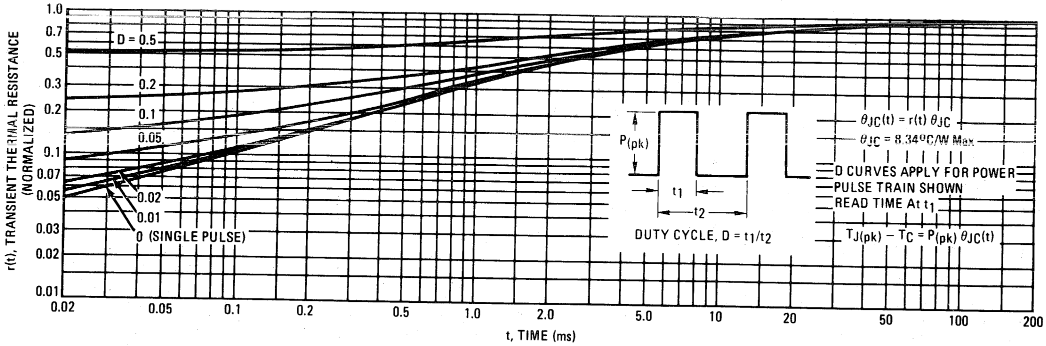
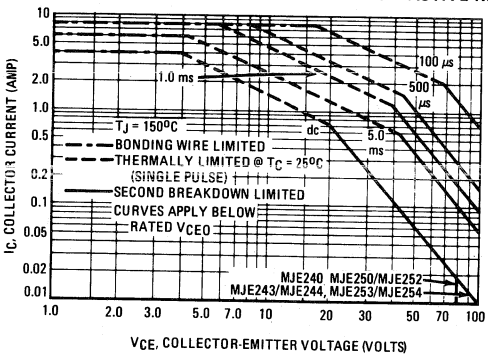


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

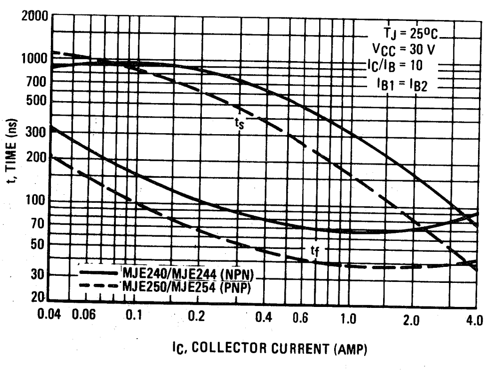
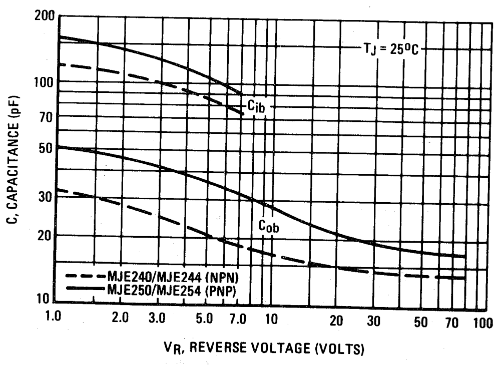
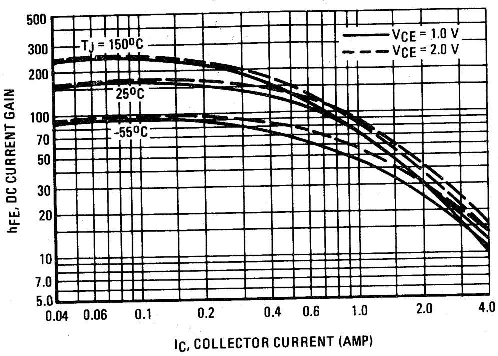


FIGURE 7 – CAPACITANCE



NPN MJE240 thru MJE244	PNP MJE250 thru MJE254

FIGURE 8 – DC CURRENT GAIN



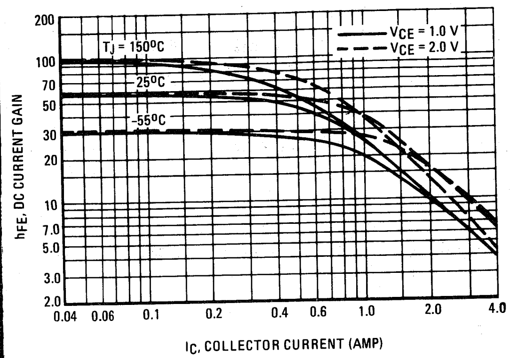
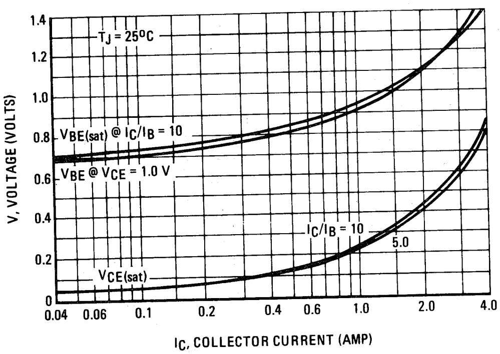


FIGURE 9 – "ON" VOLTAGES



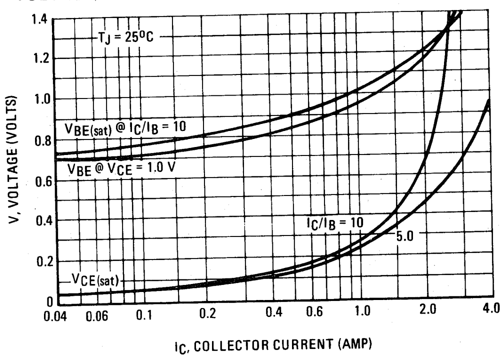
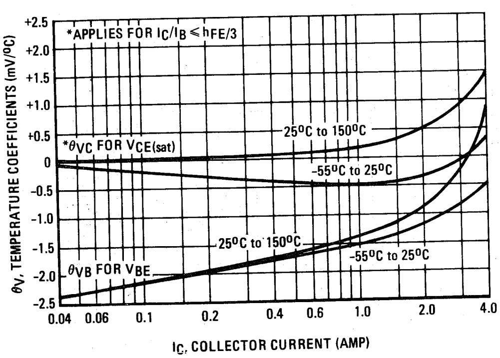
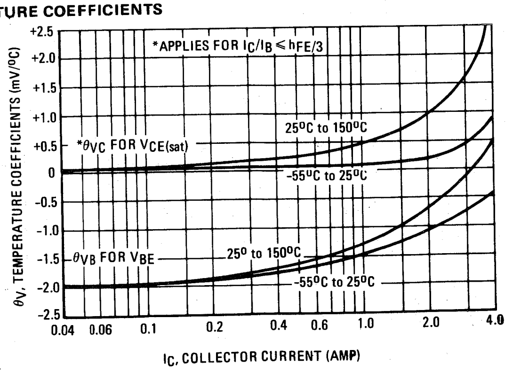


FIGURE 10 – TEMPERATURE COEFFICIENTS





3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE340

PLASTIC MEDIUM POWER NPN SILICON TRANSISTOR

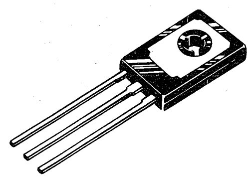
. . . useful for high-voltage general purpose applications.

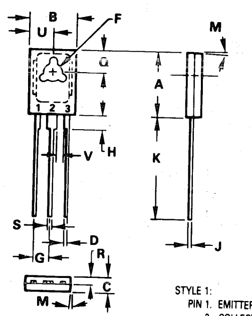
- Suitable for Transformerless, Line-Operated Equipment
- Thermopad Construction Provides High Power Dissipation Rating for High Reliability

0.5 AMPERE

POWER TRANSISTOR NPN SILICON

300 VOLTS
20 WATTS





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ($I_C = 1.0$ mAdc, $I_B = 0$)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current ($V_{CB} = 300$ Vdc, $I_E = 0$)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current ($V_{EB} = 3.0$ Vdc, $I_C = 0$)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 50$ mAdc, $V_{CE} = 10$ Vdc)	h_{FE}	30	240	—

3

FIGURE 1 – POWER TEMPERATURE DERATING

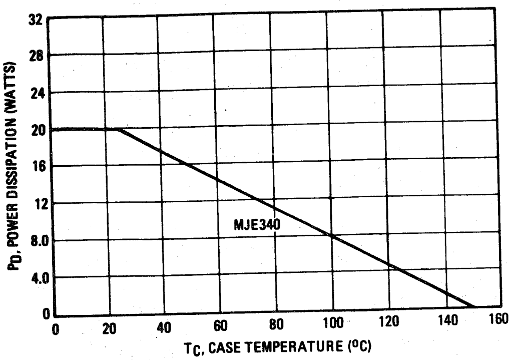
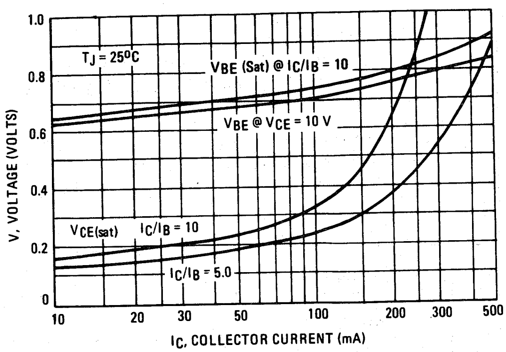
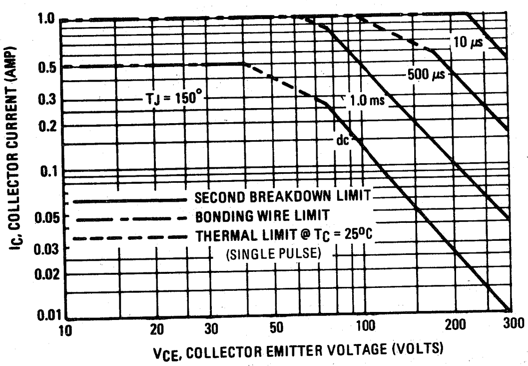


FIGURE 2 – "ON" VOLTAGES



ACTIVE-REGION SAFE OPERATING AREA

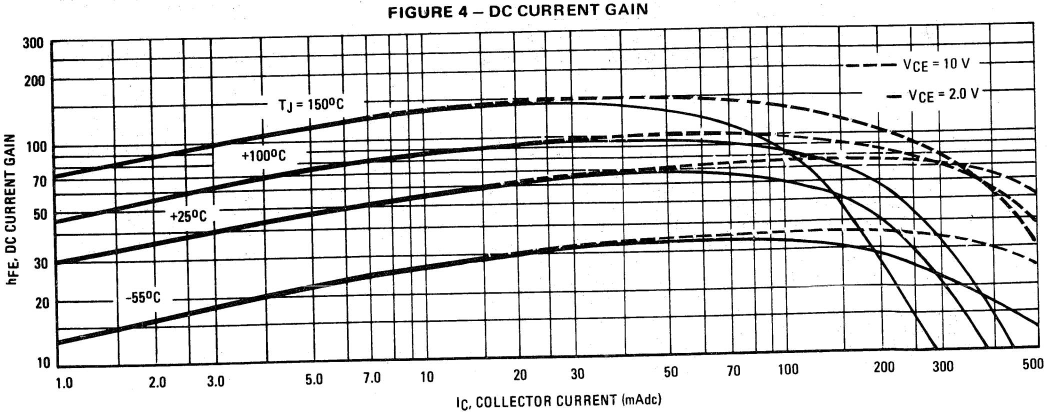
FIGURE 3 – MJE340



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 – DC CURRENT GAIN



3

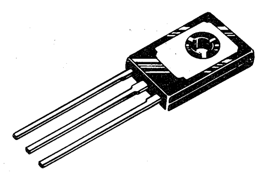
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE341
MJE344

PLASTIC NPN SILICON MEDIUM-POWER TRANSISTORS

. . .useful for medium voltage applications requiring high f_T such as converters and extended range amplifiers.

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON
150-200 VOLTS
20 WATTS

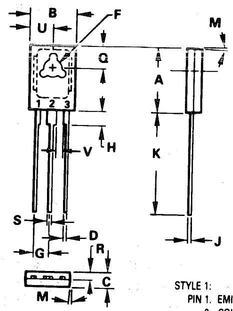


MAXIMUM RATINGS

Rating	Symbol	MJE341	MJE344	Unit
Collector-Emitter Voltage	V_{CEO}	150	200	Vdc
Collector-Base Voltage	V_{CB}	175	200	Vdc
Emitter-Base Voltage	V_{EB}	3.0	5.0	Vdc
Collector Current — Continuous	I_C	← 500 →		mAdc
Base Current	I_B	← 250 →		mAdc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above 25°C	P_D	20 0.16		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W



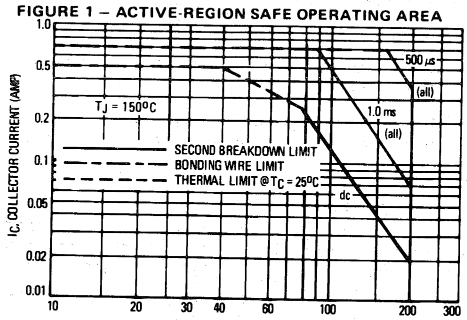
STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	MJE341 MJE344	$V_{CEO(sus)}$	150 200	– –	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0)	MJE341 MJE344	I_{CEO}	– –	1.0 1.0	mAdc
Collector Cutoff Current (V_{CB} = 175 Vdc, I_E = 0) (V_{CB} = 200 Vdc, I_E = 0)	MJE341 MJE344	I_{CBO}	– –	0.3 0.1	mAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0) (V_{EB} = 5.0 Vdc, I_C = 0)	MJE341 MJE344	I_{EBO}	– –	0.1 0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 50 mAdc, V_{CE} = 10 Vdc) (I_C = 150 mAdc, V_{CE} = 10 Vdc)	MJE341 MJE341 MJE344 MJE341	h_{FE}	20 25 30 20	– 200 300 –	–
Collector-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc) (I_C = 150 mAdc, I_B = 15 mAdc)	MJE344 MJE341	$V_{CE(sat)}$	– –	1.0 2.3	Vdc
Base-Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 25 Vdc, f = 10 MHz)		f_T	15	–	MHz
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	15	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

3

FIGURE 2 – DC CURRENT GAIN

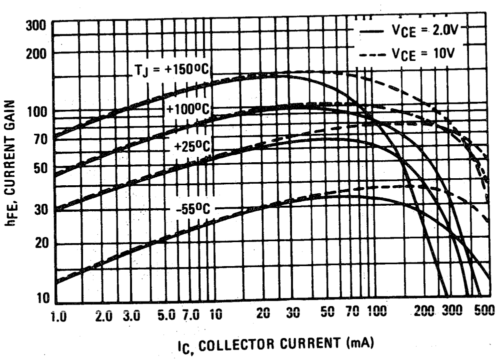
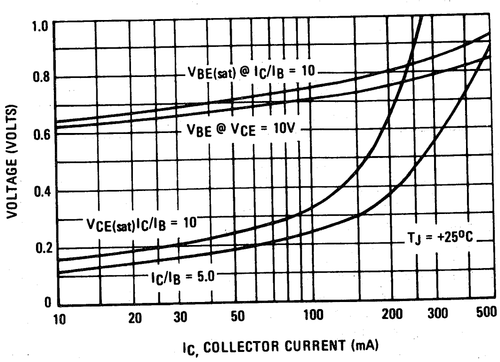


FIGURE 3 – "ON" VOLTAGES



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE350

PLASTIC MEDIUM POWER PNP SILICON TRANSISTOR

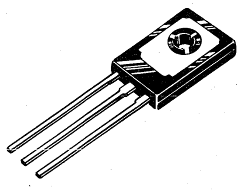
. . . designed for use in line-operated applications such as low power, line-operated series pass and switching regulators requiring PNP capability.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 300 Vdc @ I_C = 1.0 mAdc
- Excellent DC Current Gain —
  h_{FE} = 30-240 @ I_C = 50 mAdc
- Plastic Thermopad Package

0.5 AMPERE

POWER TRANSISTOR PNP SILICON

300 VOLTS
20 WATTS



MAXIMUM RATINGS

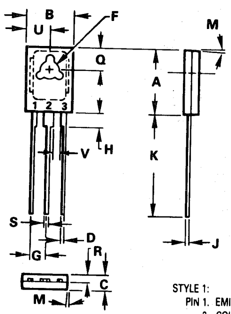
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

FIGURE 1 – DC CURRENT GAIN

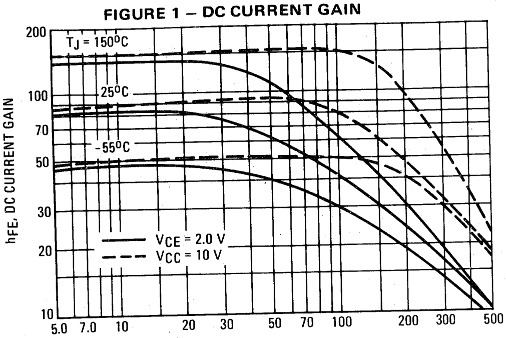


FIGURE 2 – "ON" VOLTAGES

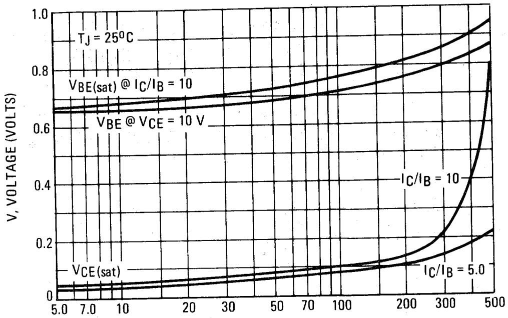


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA

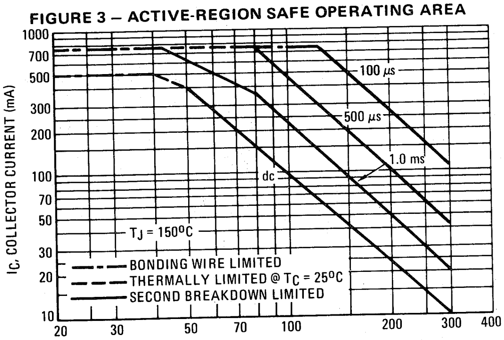


FIGURE 4 – TEMPERATURE COEFFICIENTS

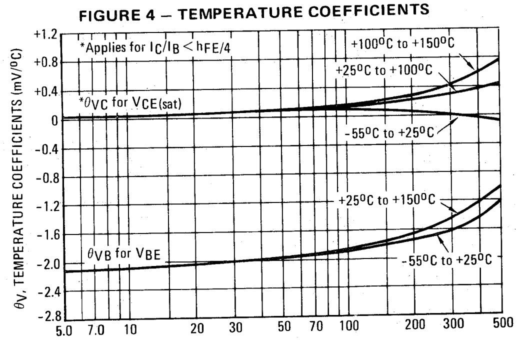
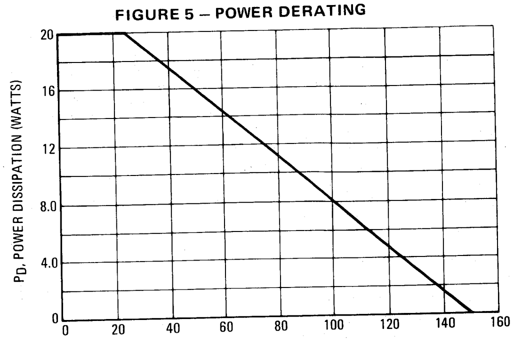


FIGURE 5 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE370

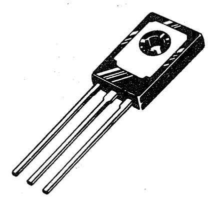
PLASTIC MEDIUM-POWER PNP SILICON TRANSISTOR

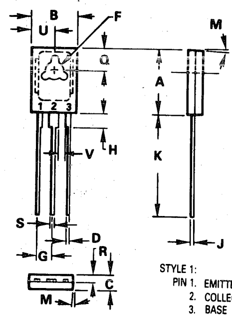
. . . designed for use in general-purpose amplifiers and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain — h_{FE} = 25 (Min) @ I_C = 1.0 Adc
- Complementary to NPN MJE520

3 AMPERE POWER TRANSISTOR PNP SILICON

30 VOLTS
25 WATTS





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	3.0	Adc
— Peak		7.0	
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.2	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W

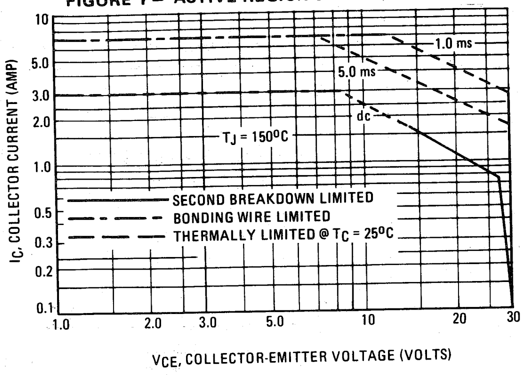
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	—	Vdc
Collector-Base Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter-Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	25	—	—

(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 — DC CURRENT GAIN

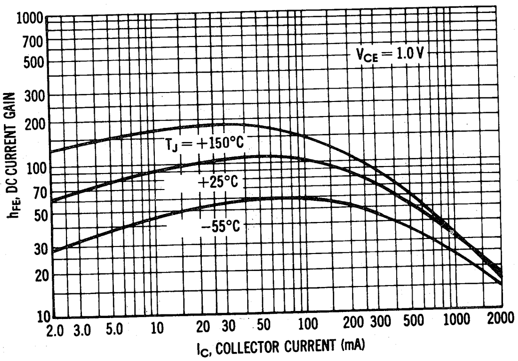


FIGURE 3 — "ON" VOLTAGE

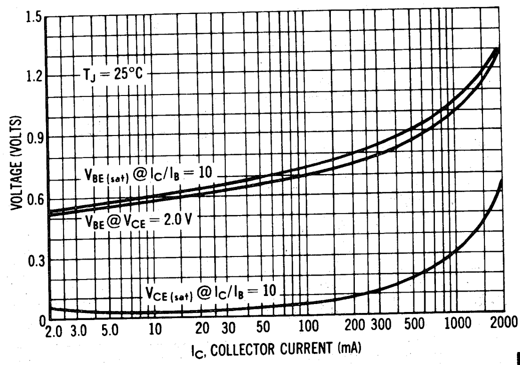
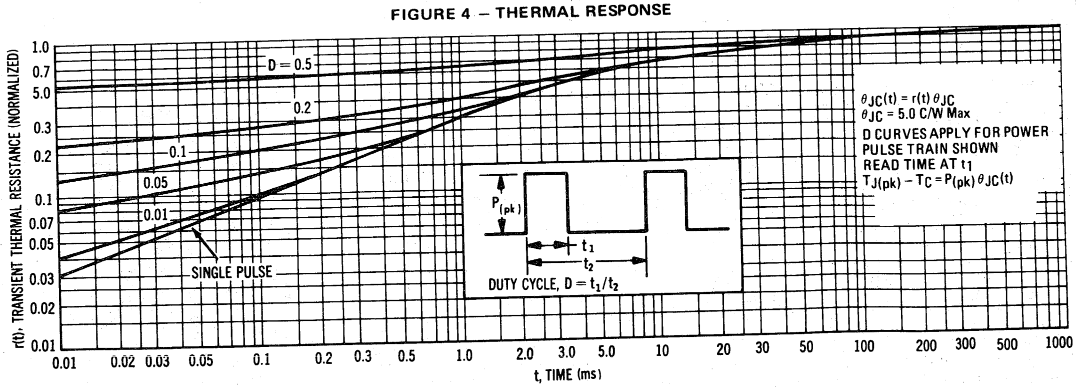


FIGURE 4 — THERMAL RESPONSE



3

MJE371

PLASTIC MEDIUM-POWER PNP SILICON TRANSISTORS

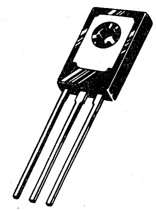
. . . designed for use in general-purpose amplifier and switching circuits. Recommended for use in 5 to 20 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- MJE371 is Complementary to NPN MJE521

4 AMPERE

POWER TRANSISTORS PNP SILICON

40 VOLTS
40 WATTS



3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	4.0	Adc
— Peak		8.0	
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

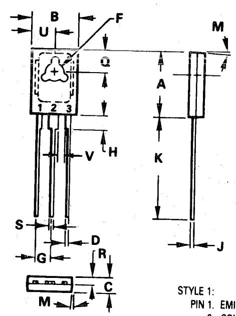
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	—	Vdc
Collector-Base Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter-Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs Duty Cycle ≤ 2.0%.



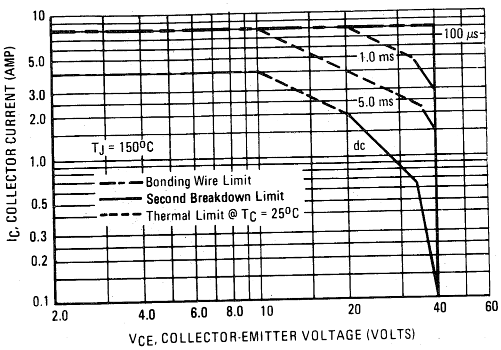
STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – DC CURRENT GAIN

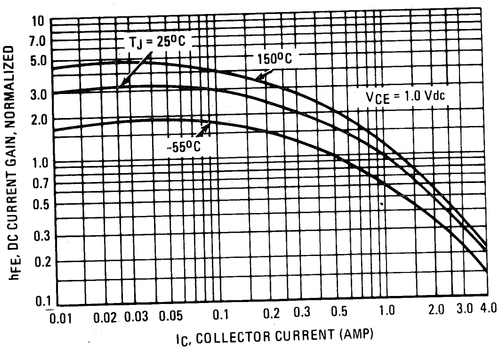


FIGURE 3 – "ON" VOLTAGE

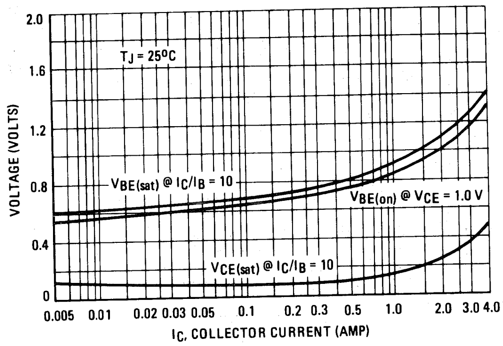
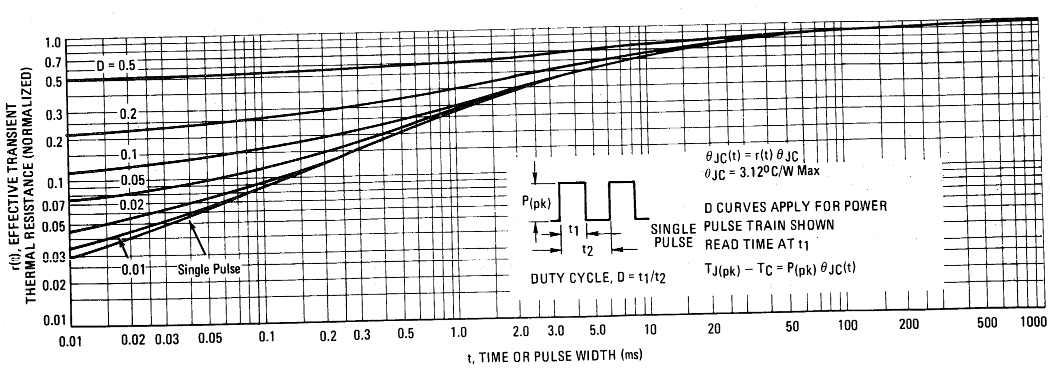


FIGURE 4 – THERMAL RESPONSE



3

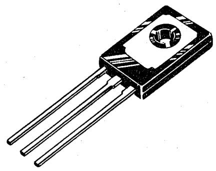
MJE520

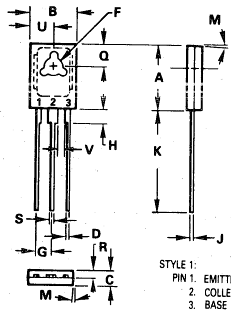
PLASTIC MEDIUM-POWER NPN SILICON TRANSISTOR

. . . designed for use in general-purpose amplifier and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain — h_{FE} = 25 (Min) @ I_C = 1.0 Adc
- Complementary to PNP MJE370

3 AMPERE
POWER TRANSISTOR
NPN SILICON
30 VOLTS
25 WATTS





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	3.0 7.0	Adc
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.2	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W

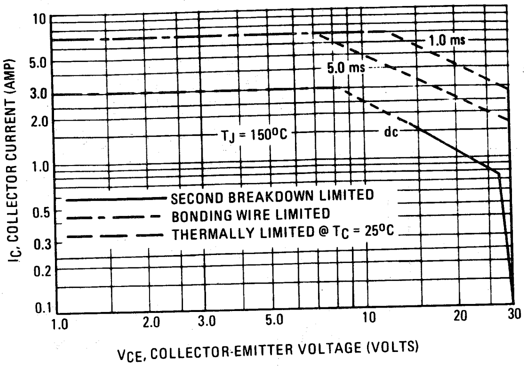
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	—	Vdc
Collector-Base Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter-Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	25	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 ACTIVE-REGION SAFE OPERATING AREA



The data of Figure 1 based on $T_{J(pk)} = 150^{o}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $(T_{Jpk}) \leqslant 150^{o}C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

FIGURE 2 – DC CURRENT GAIN

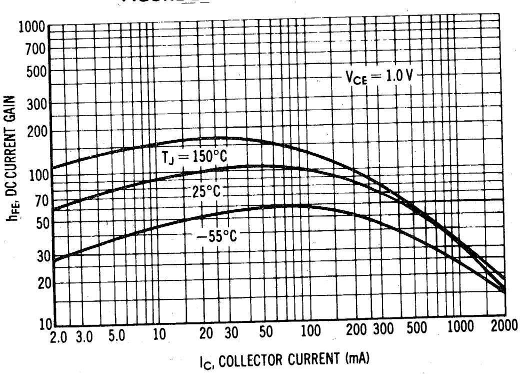
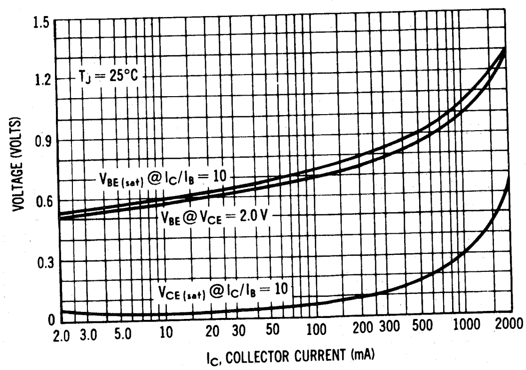
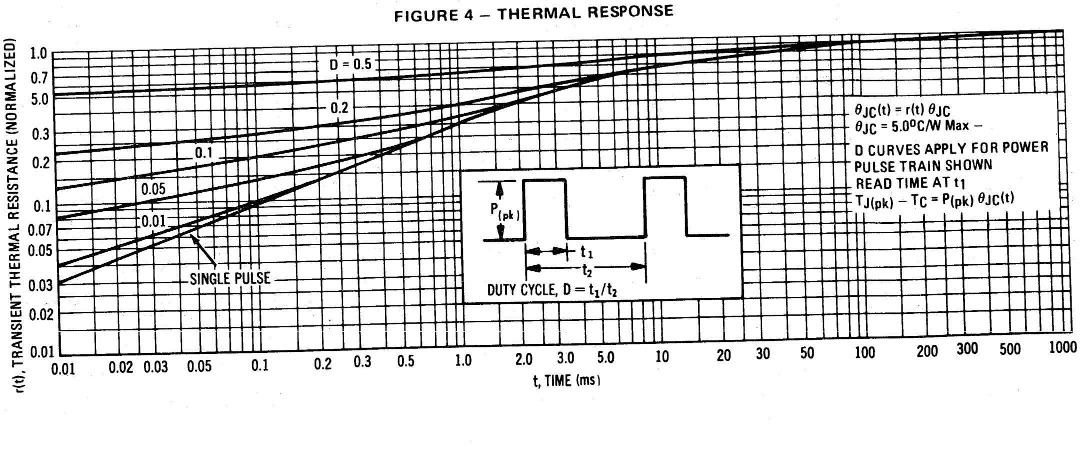


FIGURE 3 – "ON" VOLTAGE



3

FIGURE 4 – THERMAL RESPONSE



PNP MJE700,T thru MJE703 — NPN MJE800,T thru MJE803

PLASTIC DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
  h_{FE} = 2000 (Typ) @ I_C = 2.0 Adc
- Monolithic Construction with Built-in Base-Emitter Resistors to Limit Leakage Muliplication
- Choice of Packages —
  MJE700 and MJE800 series
  TO220AB, MJE700T and MJE800T

4.0 AMPERE

DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

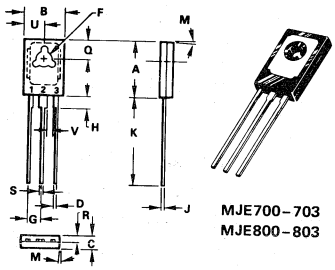
40 WATT
50 WATT

MAXIMUM RATINGS

Rating	Symbol	MJE700,T MJE701 MJE800,T MJE801	MJE702 MJE703 MJE802 MJE803	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	0.1		Adc
		CASE 77	TO-220	
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	50 0.40	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case CASE 77 TO-220	$R_{\theta JC}$	 3.13 2.50	°C/W



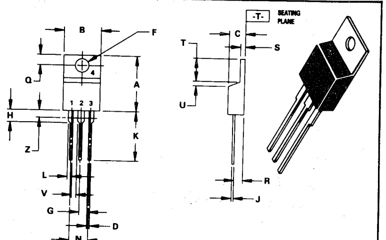
MJE700–703
MJE800–803

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05



MJE700T
MJE800T

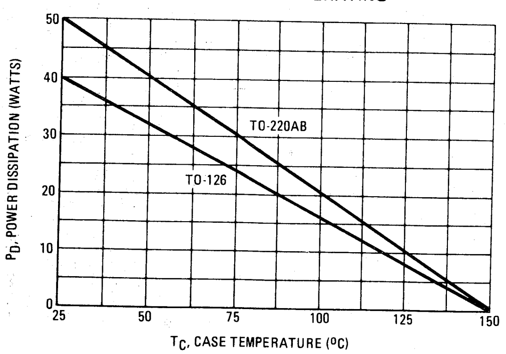
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

FIGURE 1 — POWER DERATING



ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 50 mAdc, I_B = 0)	MJE700,T MJE701, MJE800,T MJE801 MJE702, MJE703, MJE802, MJE803	$V_{(BR)CEO}$	60 80	– –	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	MJE700,T MJE701, MJE800,T, MJE801 MJE702, MJE703, MJE802, MJE803	I_{CEO}	– –	100 100	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	– –	100 500	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	MJE700,T MJE702, MJE800,T MJE802 MJE701, MJE703, MJE801, MJE803 All devices	h_{FE}	750 750 100	– – –	–
Collector-Emitter Saturation Voltage (1) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc) (I_C = 4.0 Adc, I_B = 40 mAdc)	MJE700,T MJE702, MJE800,T MJE802 MJE701, MJE703, MJE801, MJE803 All devices	$V_{CE(sat)}$	– – –	2.5 2.8 3.0	Vdc
Base-Emitter On Voltage (1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	MJE700,T MJE702, MJE800,T MJE802 MJE701, MJE703, MJE801, MJE803 All devices	$V_{BE(on)}$	– – –	2.5 2.5 3.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	1.0	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

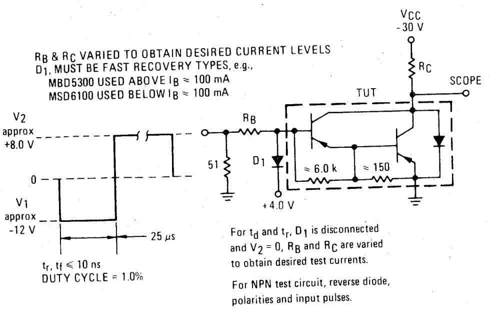


FIGURE 3 – SWITCHING TIMES

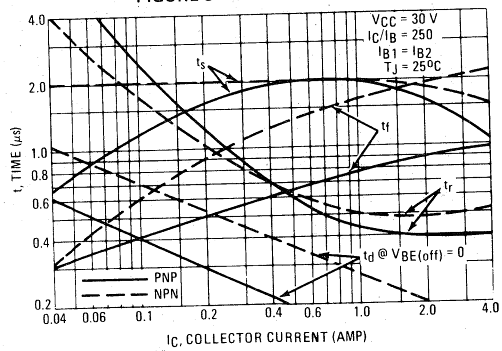


FIGURE 4 – THERMAL RESPONSE (MJE700T, 800T series)

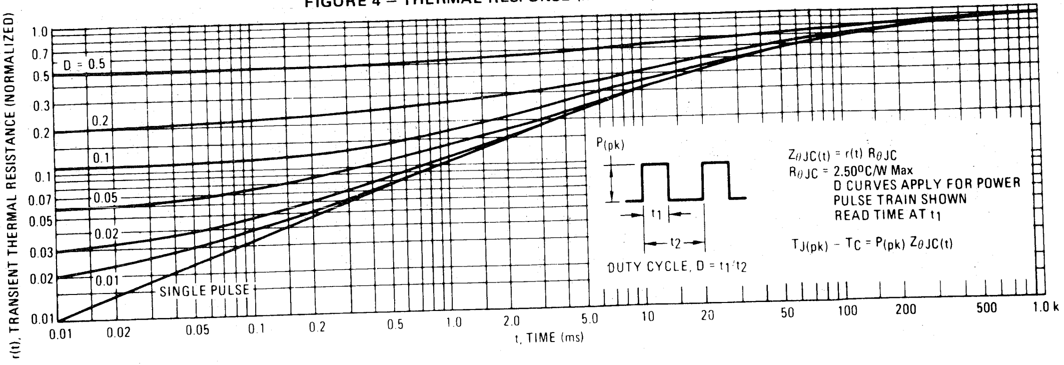
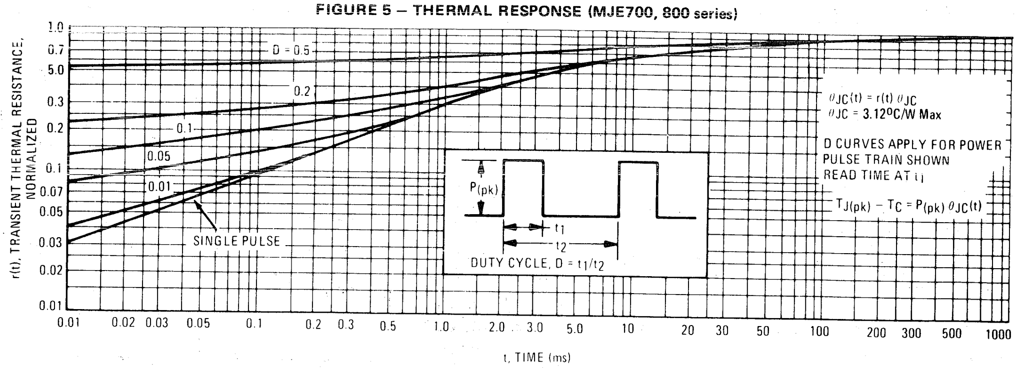


FIGURE 5 — THERMAL RESPONSE (MJE700, 800 series)



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 6 — MJE700 series

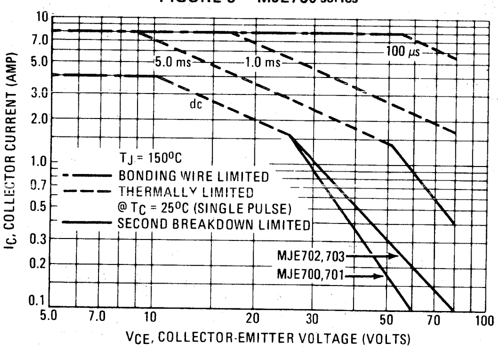
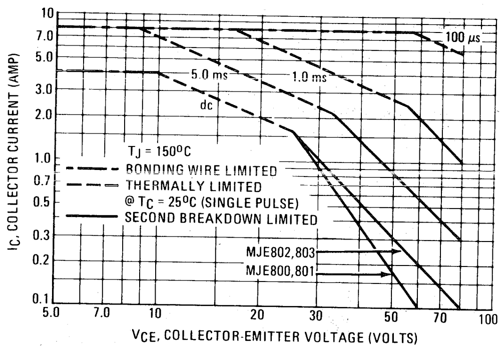


FIGURE 7 — MJE800 series



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 6 and 7 are based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4 or 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 — MJE700T

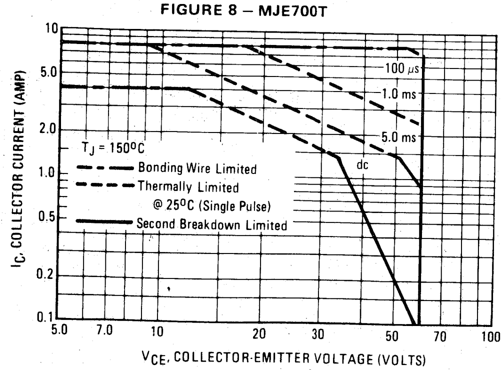
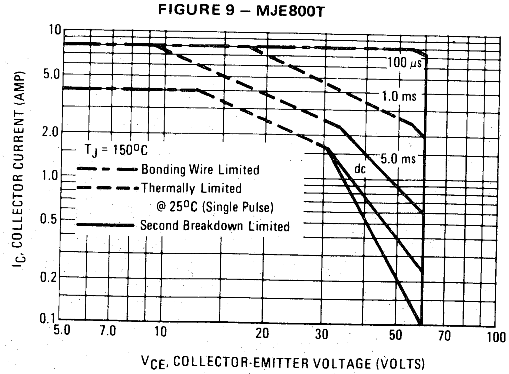


FIGURE 9 — MJE800T



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PNP MJE700,T series — **NPN** MJE800,T series

FIGURE 10 — DC CURRENT GAIN

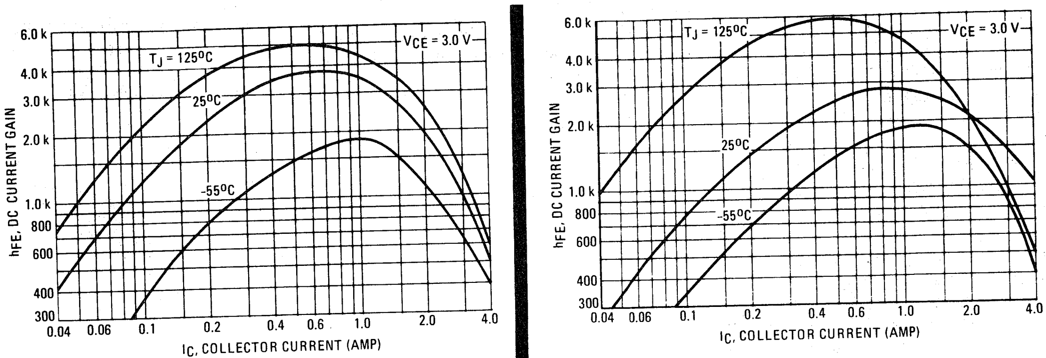


FIGURE 11 — COLLECTOR SATURATION REGION

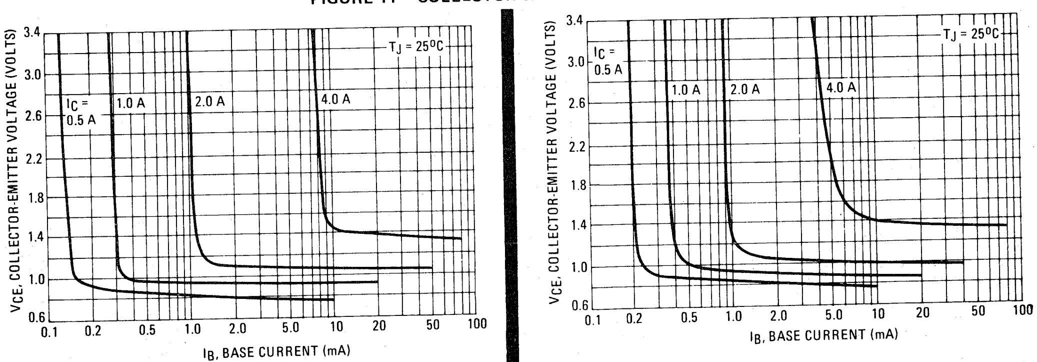
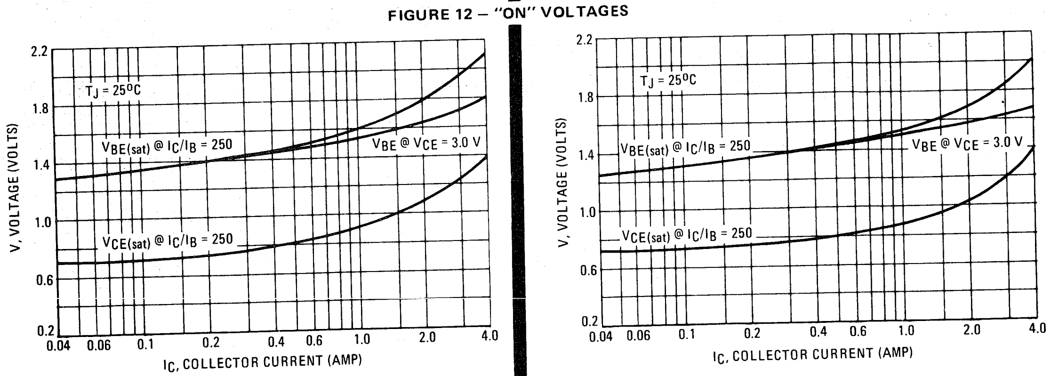


FIGURE 12 — "ON" VOLTAGES



3

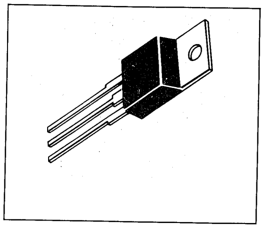
MJE1320

Designer's Data Sheet

NPN Silicon Power Transistor

Switchmode III Series

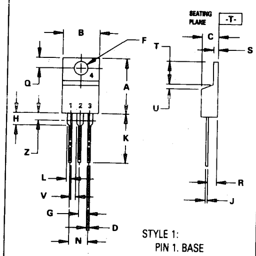
POWER TRANSISTOR
2 AMPERES
900 VOLTS
80 WATTS



This transistor is designed for high-voltage, power switching in inductive circuits where RBSOA and breakdown voltage are critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:
- Fluorescent Lamp Ballasts
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Features:
- High V_{CEV} Capability (1800 Volts)
- Low Saturation Voltage
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
(TO-220AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	900	Vdc
Collector-Emitter Voltage	V_{CEV}	1800	Vdc
Emitter Base Voltage	V_{EB}	9	Vdc
Collector Current — Continuous Peak(1)	I_C I_{CM}	2 5	Adc
Base Current — Continuous Peak(1)	I_B I_{BM}	1.5 2.5	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	80 32 0.64	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 50 mA, I_B = 0)	$V_{CEO(sus)}$	900	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	— —	0.25 2.5	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	—	—	0.25	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 13			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 14			
ON CHARACTERISTICS(1)					
DC Current Gain (V_{CE} = 5 Vdc) I_C = 2 Adc I_C = 1 Adc	h_{FE}	2.5 3	4.5 7	— —	— —
Collector-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.5 Adc) (I_C = 2 Adc, I_B = 1 Adc) (I_C = 1 Adc, I_B = 0.5 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 0.18 0.3 0.3	 1 2.5 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.5 Adc) (I_C = 2 Adc, I_B = 1 Adc) (I_C = 1 Adc, I_B = 0.5 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — — —	 0.2 0.9 0.15	 1.5 2.8 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	80	—	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1) (V_{CC} = 250 Vdc, I_C = 1 A, I_{B1} = I_{B2} = 0.5 Adc, t_p = 25 μs, Duty Cycle ≤ 2%)					
Delay Time	t_d	—	0.1	—	μs
Rise Time	t_r	—	0.8	—	μs
Storage Time	t_s	—	4	—	μs
Fall Time	t_f	—	0.8	—	μs
Inductive Load, Clamped (Table 2) (I_C = 1 A, V_{clamp} = 400 Vdc, $V_{BE(off)}$ = 2 Vdc, I_{B1} = 0.5 Adc)					
Storage Time (T_C = 25°C)	t_{sv}	—	2.8	—	μs
Crossover Time (T_C = 25°C)	t_c	—	2.2	—	μs
Storage Time (T_C = 100°C)	t_{sv}	—	3.7	10.5	μs
Crossover Time (T_C = 100°C)	t_c	—	3.5	10	μs
Fall Time					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

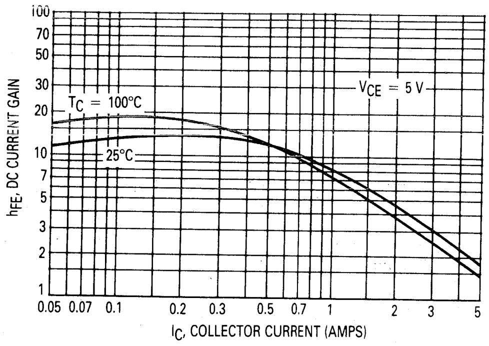


Figure 1. DC Current Gain

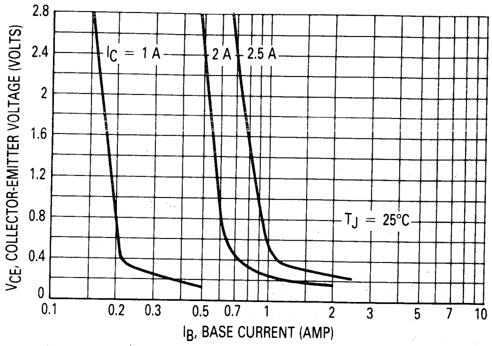


Figure 2. Collector Saturation Region

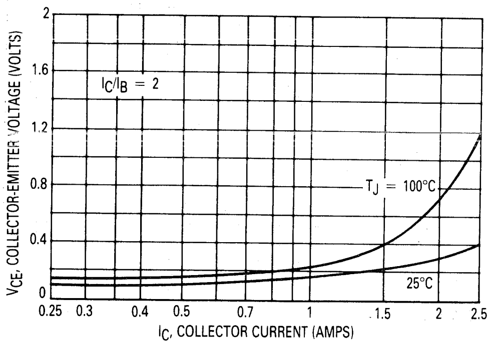


Figure 3. Collector Emitter Saturation Voltage

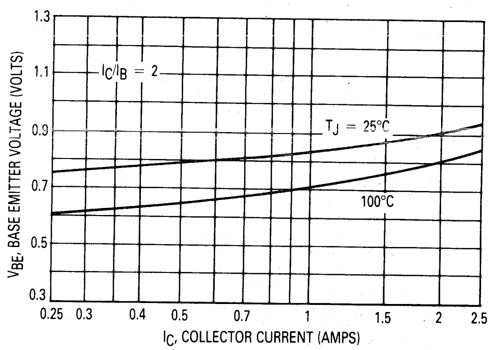


Figure 4. Base Emitter Saturation Voltage

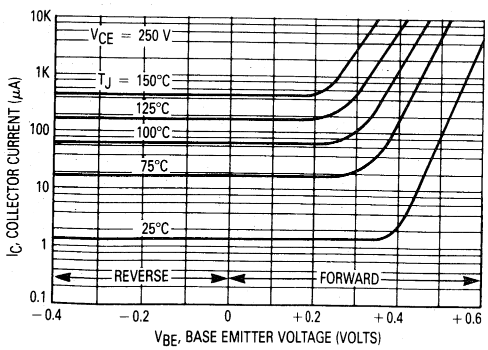


Figure 5. Collector Cutoff Region

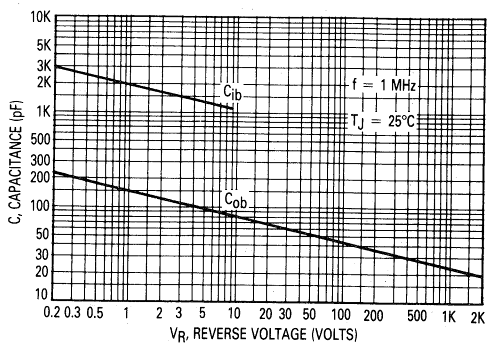


Figure 6. Capacitance Variation

3

TYPICAL DYNAMIC CHARACTERISTICS

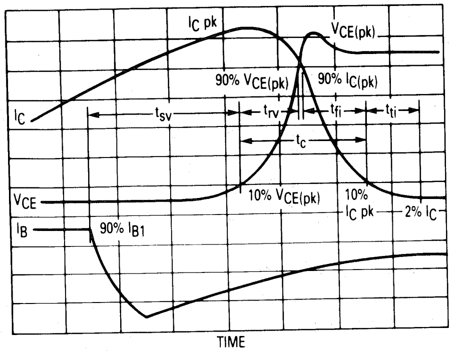


Figure 7. Inductive Switching Measurements

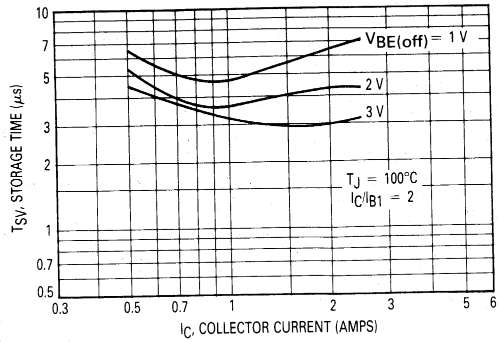


Figure 8. Inductive Storage Time

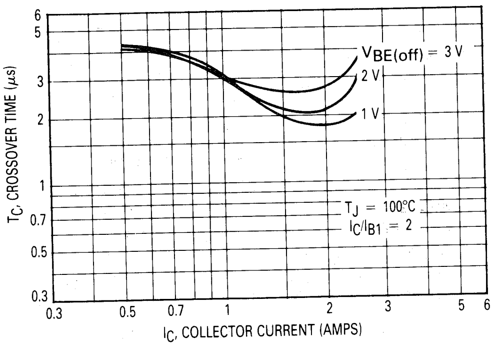


Figure 9. Inductive Crossover Time

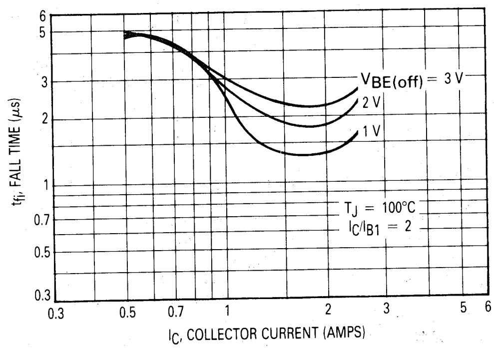
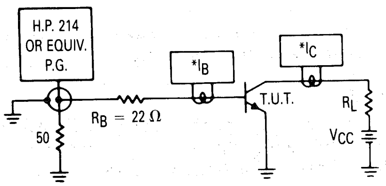


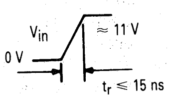
Figure 10. Inductive Fall Time

Table 1. Resistive Load Switching

t_d and t_r

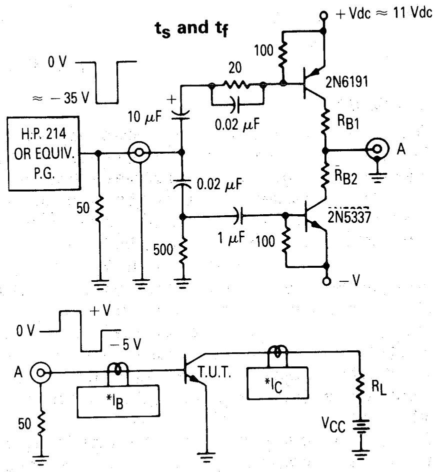


V_{CC} = 250 Vdc
R_L = 250 Ω
I_C = 1 Adc
I_B = 0.5 Adc



*Tektronix AM503
P6302 or Equivalent

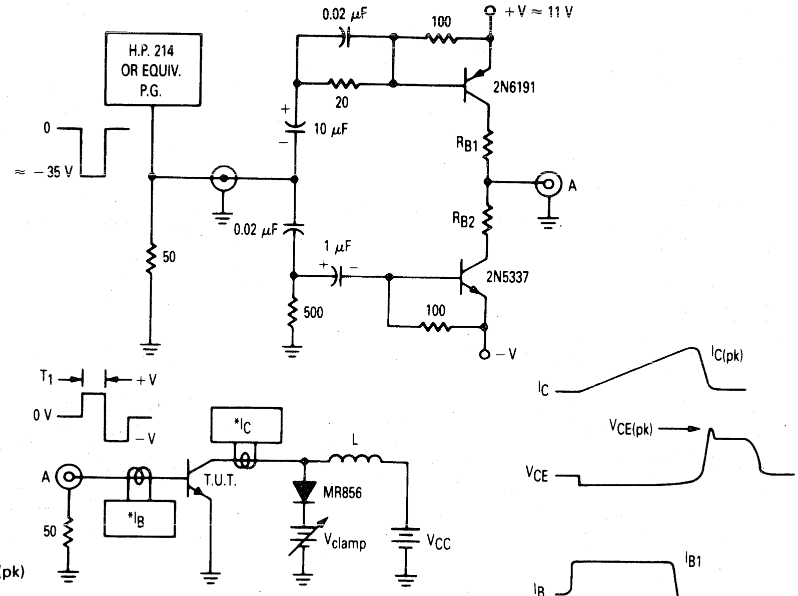
t_s and t_f

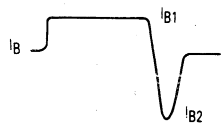


V_{CC} = 250 Vdc I_{B1} = 0.5 Adc, R_{B1} = 22 Ω
R_L = 250 Ω I_{B2} = 0.5 Adc, R_{B2} = 10 Ω
I_C = 1 Adc   For $V_{BE(off)}$ = 5 V R_{B2} = 0 Ω
Note: Adjust −V to obtain desired $V_{BE(off)}$ at point A.

3

Table 2. Inductive Load Switching





$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$	Inductive Switching	RBSOA
L = 10 mH	L = 1.1 mH	L = 1.1 mH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 20 Volts	V_{CC} = 20 Volts
	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}
*Tektronix P-6042 or Equivalent	Scope — Tektronix 7403 or Equivalent	Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 14. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

GUARANTEED SAFE OPERATING AREA

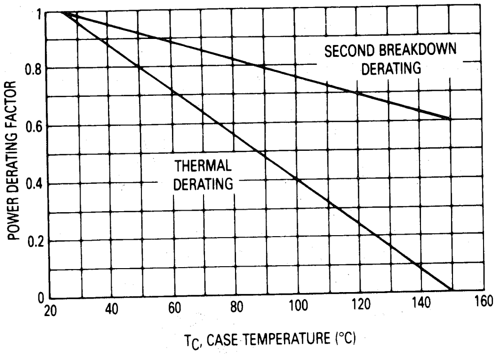


Figure 11. Power Derating

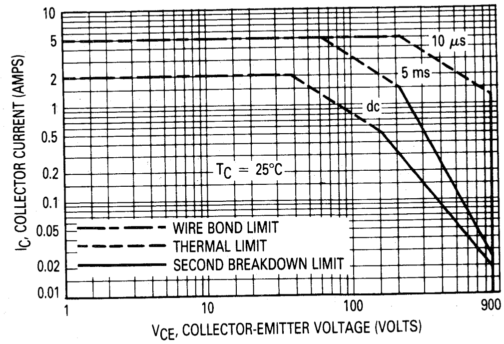


Figure 12. Maximum Rated Forward Bias Safe Operating Area

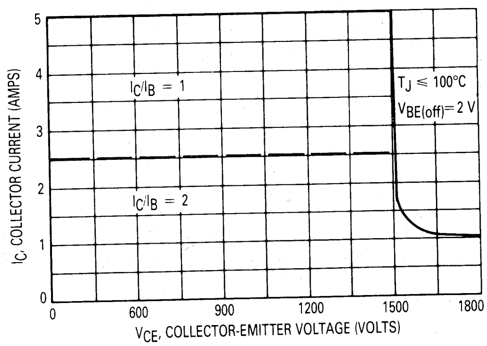


Figure 13. Maximum Rated Reverse Bias Safe Operating Area

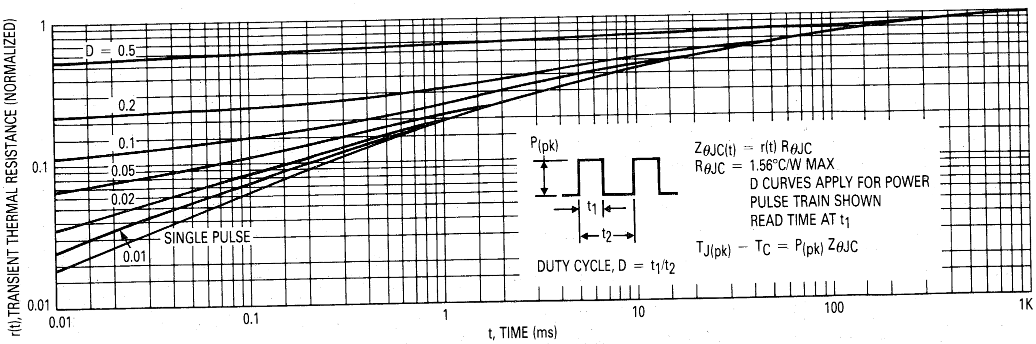


Figure 14. Thermal Response

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN

MJE1660, MJE1661

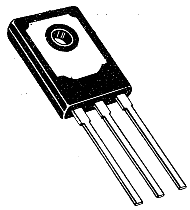
SILICON MEDIUM-POWER TRANSISTORS

. . . designed for use in power amplifier and switching applications.

- High Collector Current — I_C = 15 Adc
- High DC Current Gain — h_{FE} = 10 (Min) @ I_C = 15 Adc

15 AMPERE
POWER TRANSISTORS
SILICON

40–60 VOLTS
90 WATTS



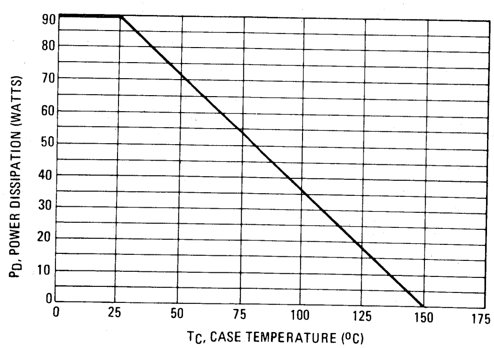
MAXIMUM RATINGS

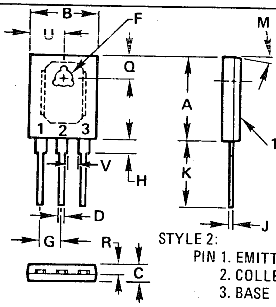
Rating	Symbol	MJE1660	MJE1661	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Base Voltage	V_{CB}	40	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current-Continuous	I_C	15		Adc
Base Current	I_B	5.0		Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	90 0.72		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W

FIGURE 1 — POWER TEMPERATURE DERATING CURVE





STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-225AB

When mounting the device, torque not to exceed 8.0 in.-lb.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

3

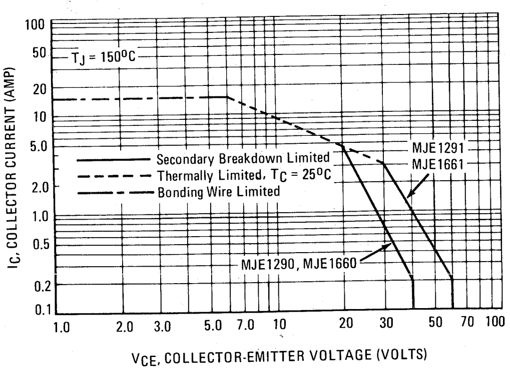
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	MJE1660 MJE1661	$V_{CEO(sus)}$	40 60	– –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)		I_{CEO}	–	1.0	mAdc
Collector Cutoff Current (V_{CE} = 40 Vdc, V_{BE} = 0) (V_{CE} = 60 Vdc, V_{BE} = 0)	MJE1660 MJE1661	I_{CES}	– –	0.7 0.7	mAdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0)	MJE1660 MJE1661	I_{CBO}	– –	0.7 0.7	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_E = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	20 10	100 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 15 Adc, I_B = 1.5 Adc)		$V_{CE(sat)}$	–	1.8	Vdc
Base-Emitter on Voltage (1) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs. Duty Cycle ≤ 2.0%.

3

FIGURE 2 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE2360T
MJE2361T

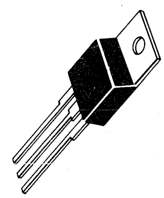
NPN SILICON HIGH-VOLTAGE TRANSISTOR

. . . useful for general-purpose, high voltage applications requiring high f_T.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 350 Vdc (Min) @ I_C = 2.5 mAdc
- DC Current Gain —
  h_{FE} = 40 (Min) @ I_C = 100 mAdc — MJE2361T
- Current-Gain—Bandwidth Product —
  f_T = 10 MHz (Typ) @ I_C = 50 mAdc

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON

350 VOLTS
30 WATTS



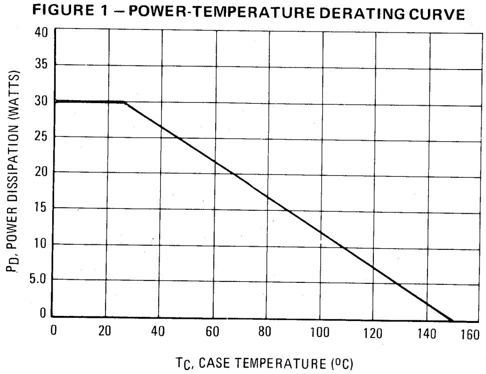
MAXIMUM RATINGS

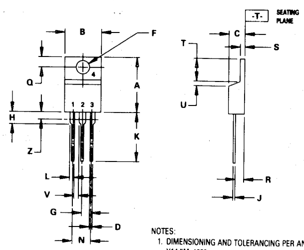
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	350	Vdc
Collector-Base Voltage	V_{CB}	375	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	0.5	Adc
Base Current	I_B	0.25	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.167	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

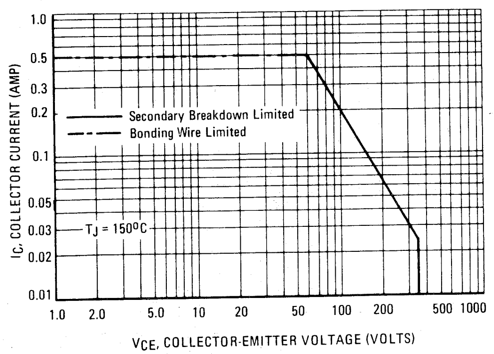
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage(1) (I_C = 2.5 mAdc, I_B = 0)		$V_{CEO(sus)}$	350	–	–	Vdc
Collector Cutoff Current (V_{CE} = 250 Vdc, I_B = 0)		I_{CEO}	–	–	0.25	mAdc
Collector Cutoff Current (V_{CE} = 375 Vdc, $V_{EB(off)}$ = 1.5 Vdc)		I_{CEX}	–	–	0.5	mAdc
Collector Cutoff Current (V_{CB} = 375 Vdc, I_E = 0)		I_{CBO}	–	–	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				–
(I_C = 50 mAdc, V_{CE} = 10 Vdc)	MJE2360T		25	–	200	
	MJE2361T		50	–	250	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)	MJE2360T		15	–	–	
	MJE2361T		40	–	–	
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)		$V_{CE(sat)}$	–	–	1.5	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	–	1.0	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	–	10	–	MHz
Output Capacitance (V_{CB} = 100 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	20	–	pF

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

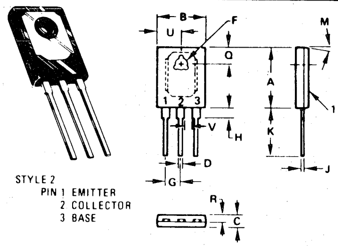
NPN
MJE2801, MJE2801T
PNP
MJE2901

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . for use as an output device in complementary audio amplifiers up to 35-Watts music power per channel.

- High DC Current Gain — h_{FE} = 25-100 @ I_C = 3.0 A
- Choice of Packages — MJE2801, 2901 — TO-225AB
  MJE2801T — TO-220AB

10 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60 VOLTS
75, 90 WATTS



STYLE 2
PIN 1 EMITTER
2 COLLECTOR
3 BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	—	0.080	—

MJE2801
MJE2901

CASE 90-05
TO-225AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C	P_D†		Watts
MJE2801, 2901		90	
MJE2801T		75	
Derate above 25°C			W/°C
MJE2801, 2901		0.72	
MJE2801T		0.6	
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

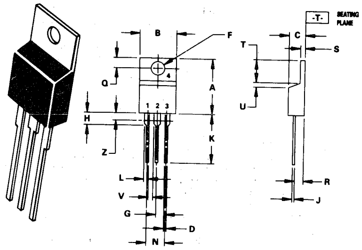
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		°C/W
MJE2801, 2901		1.39	
MJE2801T		1.67	

†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	60	—	Vdc
Collector-Cutoff Current	I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)		—	0.1	
(V_{CB} = 60 Vdc, I_E = 0, T_C = 150°C)		—	2.0	
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	—
Base-Emitter Voltage (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	V_{BE}	—	1.4	Vdc

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

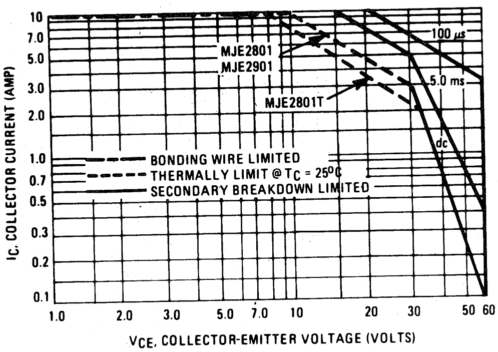
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

3

FIGURE 1 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 — DC CURRENT GAIN

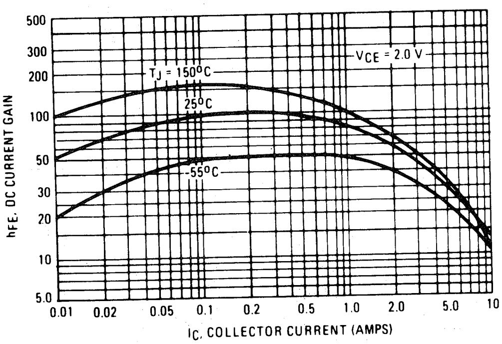


FIGURE 3 — POWER DERATING

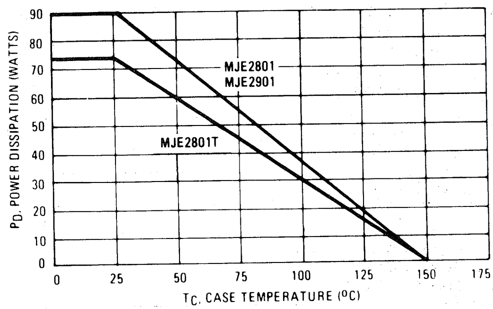
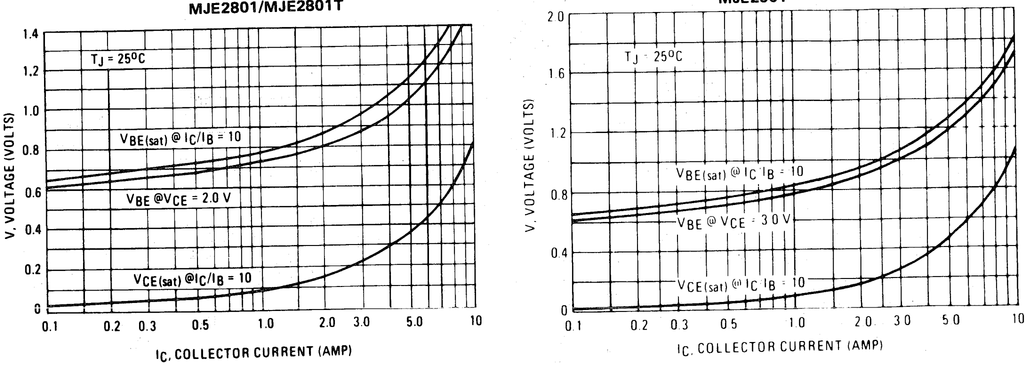


FIGURE 4 — "ON" VOLTAGES

MJE2801/MJE2801T **MJE2901**



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
MJE2955, MJE2955T
NPN
MJE3055, MJE3055T

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 10 Amperes
- High Current Gain — Bandwidth Product — f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Choice of Packages — MJE3055, MJE2955 — TO-225AB (TO-127)
  MJE3055T, MJE2955T — TO-220AB

10 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60 VOLTS
75, 90 WATTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	70	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6.0	Adc
Total Power Dissipation @ T_C = 25°C	P_D†		Watts
MJE3055, MJE2955		90	
MJE3055T, MJE2955T		75	
Derate above 25°C			W/°C
MJE3055, MJE2955		0.72	W/°C
MJE3055T, MJE2955T		0.6	
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

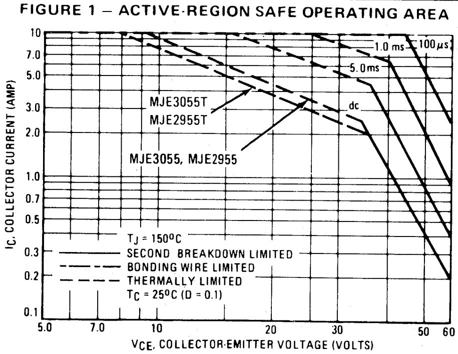
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		°C/W
MJE3055, MJE2955		1.39	
MJE3055T, MJE2955T		1.67	

†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

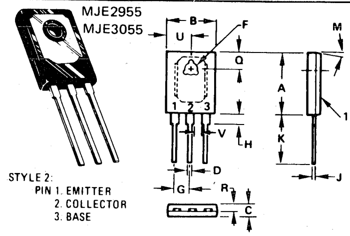
3

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

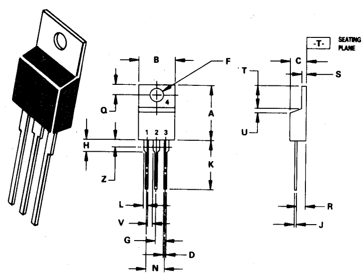
The data of Figure 1 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN 415A)



STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-225AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	700	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	– –	1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	100 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	– –	1.1 8.0	Vdc
Base-Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2.0	–	MHz

(1) **Pulse Test:** Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

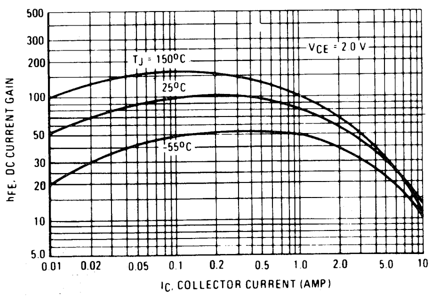


FIGURE 3 – POWER DERATING

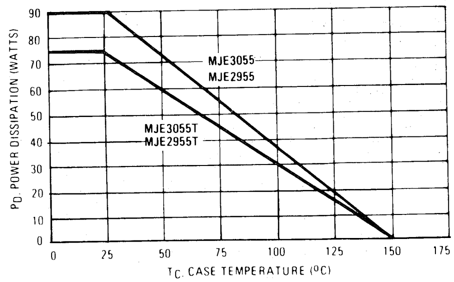
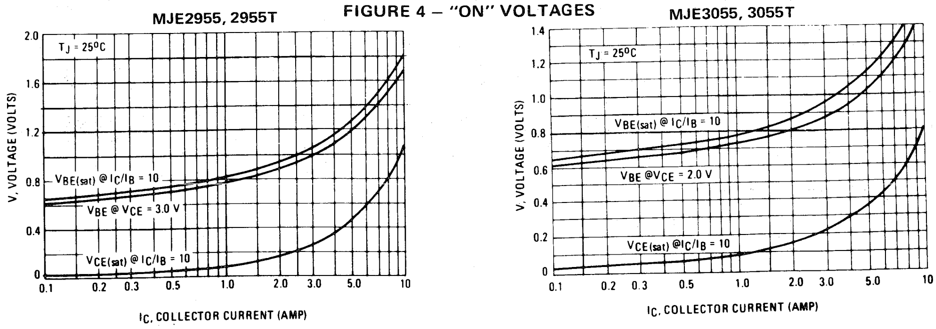


FIGURE 4 – "ON" VOLTAGES



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

NPN MJE3300, MJE3301
PNP MJE3310

PLASTIC DARLINGTON COMPLEMENTARY SILICON ANNULAR POWER TRANSISTORS

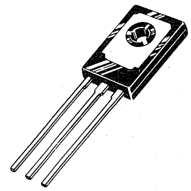
. . . designed for general-purpose amplifier and high-speed switching applications.

- High DC Current Gain — h_{FE} = 2000 (Typ) @ I_C = 1.0 Adc
- Collector-Emitter Sustaining Voltage — @ 10 mAdc
  $V_{CEO(sus)}$ = 40 Vdc (Min) — MJE3310/MJE3300
  = 60 Vdc (Min) — MJE3301
- Reverse Voltage Protection Diode
- Pinout Compatible with TO-220 Package
- Monolithic Construction with Built-In Base-Emitter Output Resistor
- Thermopad II Construction With Hard Solder for High Reliability

DARLINGTON 4-AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40, 60 VOLTS
15 WATTS



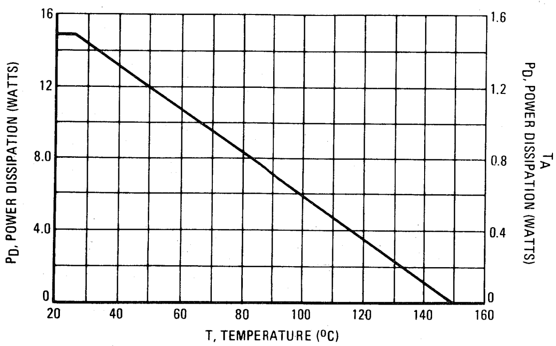
MAXIMUM RATINGS

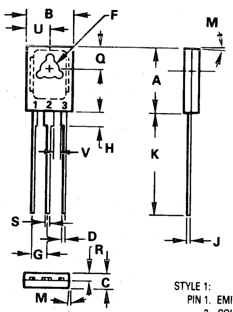
Rating	Symbol	MJE3310 MJE3300	MJE3301	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Base Voltage	V_{CB}	40	60	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →		Vdc
Collector Current — Continuous	I_C	← 4.0 →		Adc
Peak		← 6.0 →		
Base Current	I_B	← 100 →		mAdc
Total Power Dissipation @ T_C = 25°C	P_D	← 15 →		Watts
Derate above 25°C		← 0.12 →		W/°C
Total Power Dissipation @ T_A = 25°C	P_D	← 1.5 →		Watts
Derate above 25°C		← 0.012 →		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83.3	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0) MJE3310, MJE3300 / MJE3301	$V_{CEO(sus)}$	40 / 60 / —	— / —	Vdc
Collector-Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) MJE3310, MJE3300 / (V_{CE} = 30 Vdc, I_B = 0) MJE3301 / (V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	— / —	100 / 100 / —	μAdc
Collector Cutoff Current (V_{CB} = Rated $V_{CEO(sus)}$, I_E = 0) / (V_{CB} = Rated $V_{CEO(sus)}$, I_E = 0, T_C = 100°C)	I_{CBO}	— / —	1.0 / 100	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc) / (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	1000 / 750	— / —	—
Collector-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 6.0 mAdc)	$V_{CE(sat)}$	—	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 6.0 mAdc)	$V_{BE(sat)}$	—	2.5	Vdc
Base-Emitter On Voltage (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	2.5	Vdc
Output Diode Voltage Drop (I_{EC} = 2.0 Adc)	V_{EC}	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	f_T	20	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — ACTIVE-REGION SAFE OPERATING AREA

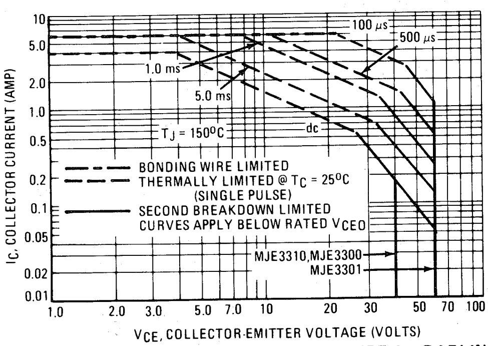


FIGURE 3 — TYPICAL DC CURRENT GAIN

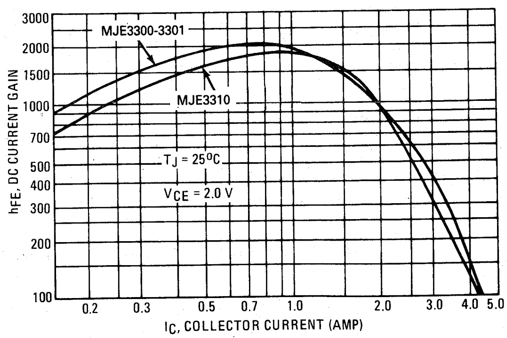
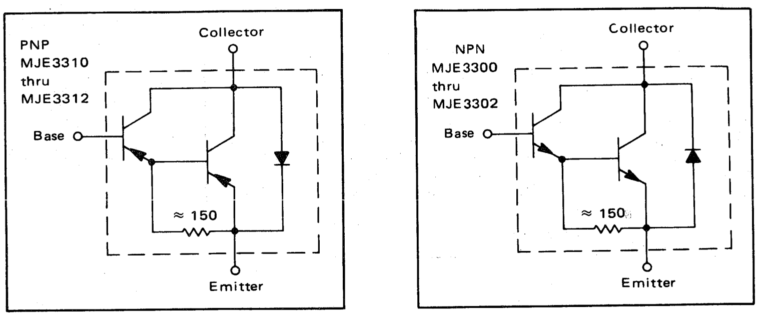


FIGURE 4 — DARLINGTON CIRCUIT SCHEMATIC



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE3439
MJE3440

NPN SILICON HIGH-VOLTAGE POWER TRANSISTORS

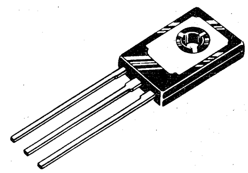
. . . designed for use in line-operated equipment requiring high f_T.

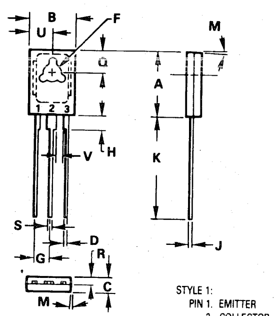
- High DC Current Gain — h_{FE} = 40–160 @ I_C = 20 mAdc
- Current-Gain—Bandwidth Product — f_T = 15 MHz (Min) @ I_C = 10 mAdc
- Low Output Capacitance — C_{ob} = 10 pF (Max) @ f = 1.0 MHz

0.3 AMPERE

POWER TRANSISTORS NPN SILICON

250–350 VOLTS
15 WATTS





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

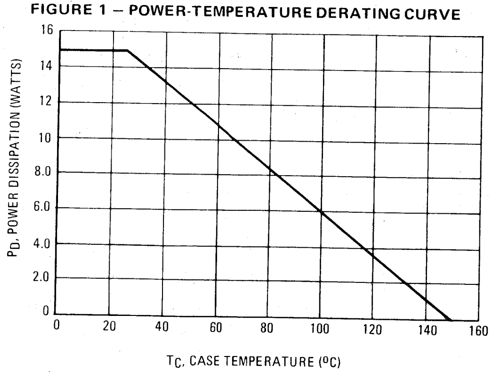
MAXIMUM RATINGS

Rating	Symbol	MJE3439	MJE3440	Unit
Collector-Emitter Voltage	V_{CEO}	350	250	Vdc
Collector-Base Voltage	V_{CB}	450	350	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	0.3		Adc
Base Current	I_B	150		mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.33	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE

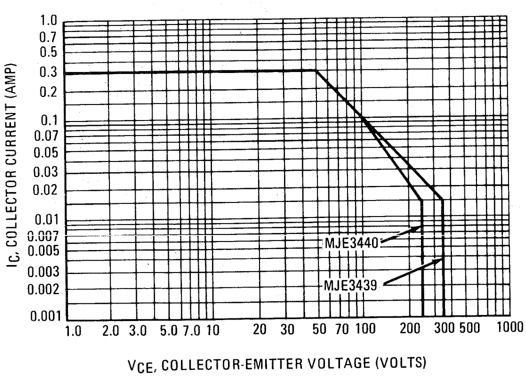


3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	MJE3439	$V_{CEO(sus)}$	350	–	Vdc
(I_C = 50 mAdc, I_B = 0)	MJE3440		250	–	
Collector Cutoff Current (V_{CE} = 300 Vdc, I_B = 0)	MJE3439	I_{CEO}	–	20	μAdc
(V_{CE} = 200 Vdc, I_B = 0)	MJE3440		–	50	
Collector Cutoff Current (V_{CE} = 450 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	MJE3439	I_{CEX}	–	500	μAdc
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	MJE3440		–	500	
Collector Cutoff Current (V_{CB} = 350 Vdc, I_E = 0)	MJE3439	I_{CBO}	–	20	μAdc
(V_{CB} = 250 Vdc, I_E = 0)	MJE3440		–	20	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	20	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)		h_{FE}	30	–	–
(I_C = 20 mAdc, V_{CE} = 10 Vdc)			50	200	
Collector-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)		$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)		$V_{BE(sat)}$	–	1.3	Vdc
Base-Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	0.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 5.0 MHz)		f_T	15	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	10	pF
Small-Signal Current Gain (I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
MJE4340	MJE4350
MJE4341	MJE4351
MJE4342	MJE4352
MJE4343	MJE4353

HIGH-VOLTAGE — HIGH POWER TRANSISTORS

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

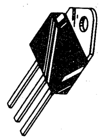
- High Collector-Emitter Sustaining Voltage —

	NPN	PNP
$V_{CEO(sus)}$ = 100 Vdc —	MJE4340	MJE4350
= 120 Vdc —	MJE4341	MJE4351
= 140 Vdc —	MJE4342	MJE4352
= 160 Vdc —	MJE4343	MJE4353

- High DC Current Gain — @ I_C = 8.0 Adc
  h_{FE} = 35 (Typ)
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 8.0 Adc

16 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

100-160 VOLTS



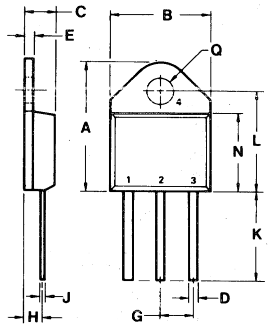
MAXIMUM RATINGS

Rating	Symbol	MJE4340 MJE4350	MJE4341 MJE4351	MJE4342 MJE4352	MJE4343 MJE4353	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	160	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	160	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →				Vdc
Collector Current — Continuous Peak (1)	I_C	← 16 → ← 20 →				Adc
Base Current — Continous	I_B	← 5.0 →				Adc
Total Device Dissipation @ T_C = 25°C	P_D	← 125 →				Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.



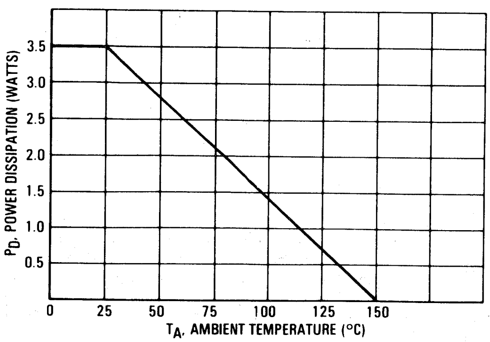
STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

3

FIGURE 1 — POWER DERATING
REFERENCE: AMBIENT TEMPERATURE



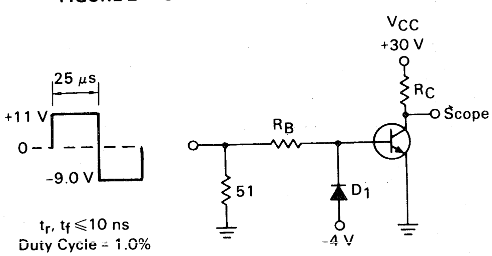
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	MJE4340, MJE4350		100	—	
	MJE4341, MJE4351		120	—	
	MJE4342, MJE4352		140	—	
	MJE4343, MJE4353		160	—	
Collector-Emitter Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	MJE4340, MJE4350		—	750	
(V_{CE} = 60 Vdc, I_B = 0)	MJE4341, MJE4351		—	750	
(V_{CE} = 70 Vdc, I_B = 0)	MJE4342, MJE4352		—	750	
(V_{CE} = 80 Vdc, I_B = 0)	MJE4343, MJE4353		—	750	
Collector-Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)			—	1.0	
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			—	5.0	
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	750	μAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)			15	35 (Typ)	
(I_C = 16 Adc, V_{CE} = 4.0 Vdc)			8.0	15 (Typ)	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 8.0 Adc, I_B = 800 mA)			—	2.0	
(I_C = 16 Adc, I_B = 2.0 Adc)			—	3.5	
Base-Emitter Saturation Voltage (I_C = 16 Adc, I_B = 2.0 Adc)		$V_{BE(sat)}$	—	3.9	Vdc
Base-Emitter On Voltage (I_C = 16 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	3.9	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	800	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

3

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT

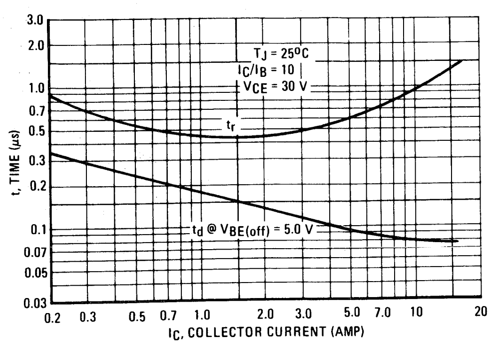


R_B and R_C varied to obtain desired current levels

D_1 must be fast recovery type, eg:
MBD5300 used above $I_B \approx$ 100 mA
MSD6100 used below $I_B \approx$ 100 mA

Note: Reverse polarities to test PNP devices.

FIGURE 3 — TYPICAL TURN-ON TIME



TYPICAL CHARACTERISTICS

FIGURE 4 — TURN-OFF TIME

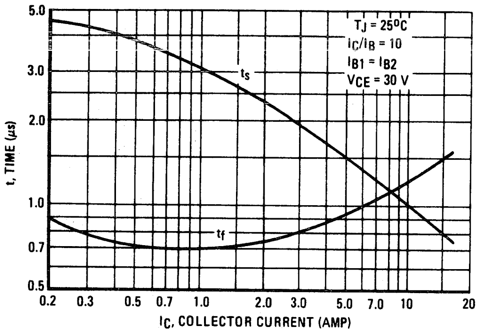
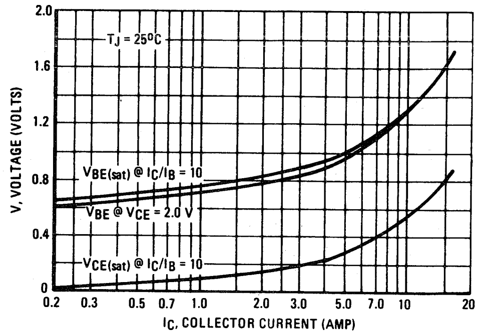


FIGURE 5 — ON VOLTAGES



DC CURRENT GAIN

FIGURE 6 — MJE4340 SERIES (NPN)

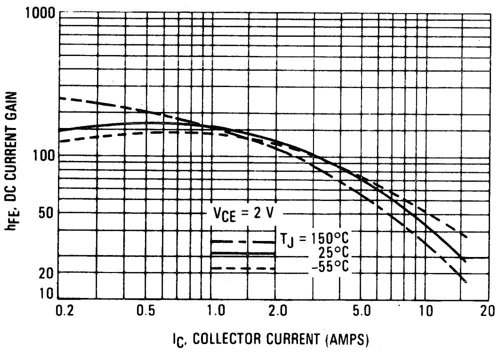


FIGURE 7 — MJE4350 SERIES (PNP)

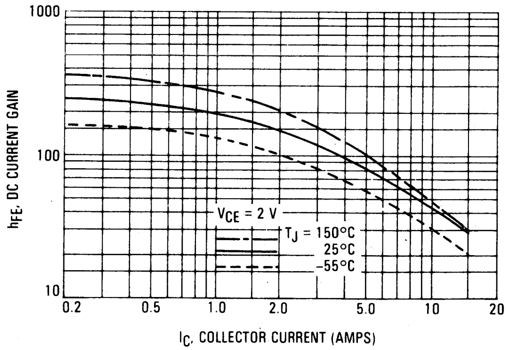


FIGURE 8 — COLLECTOR SATURATION REGION

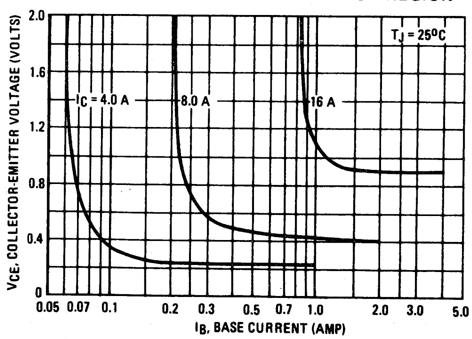


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FIGURE 9 — THERMAL RESPONSE

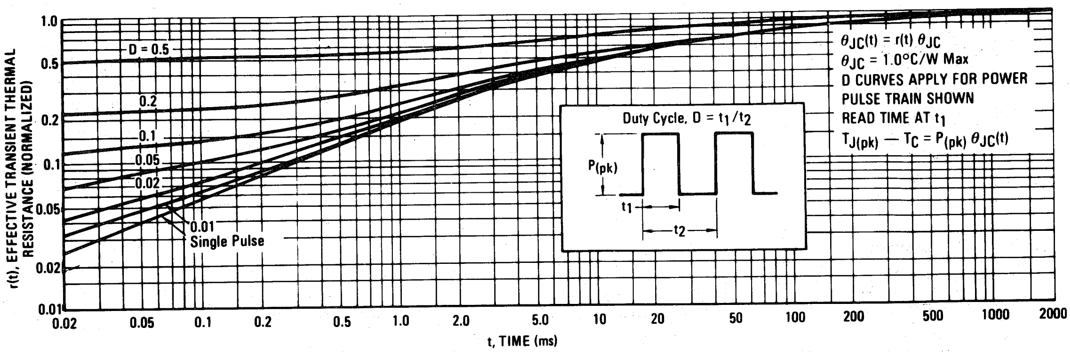
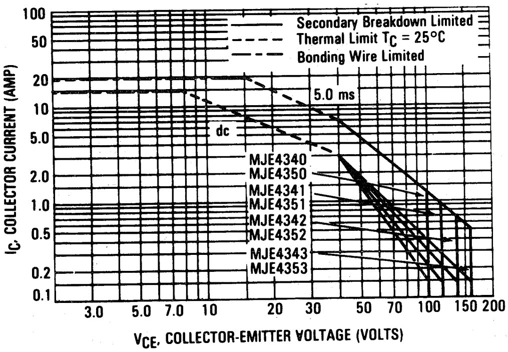


FIGURE 10 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



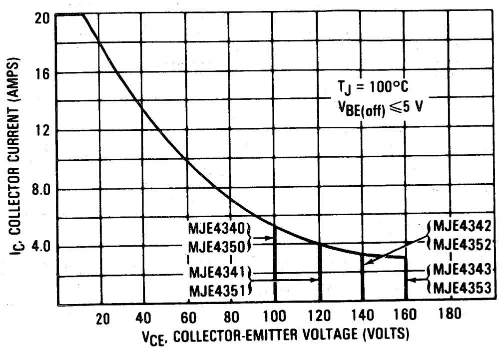
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 11 gives RBSOA characteristics.

FIGURE 11 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

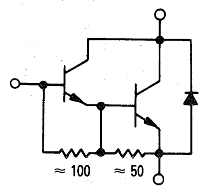
MJE5740
MJE5741
MJE5742

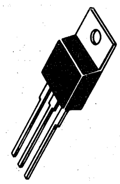
NPN Silicon Power Darlington Transistors

The MJE5740, 41, 42 Darlington transistors are designed for high-voltage power switching in inductive circuits. They are particularly suited for operation in applications such as:

- Small Engine Ignition
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

POWER DARLINGTON TRANSISTORS
8 AMPERES
300, 350, 400 VOLTS
80 WATTS





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MJE5740	MJE5741	MJE5742	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	800	Vdc
Emitter Base Voltage	V_{EB}		8		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}		8 16		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}		2.5 5		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D		2 16		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		80 640		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle = 10%.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)						
Collector-Emitter Sustaining Voltage (I_C = 50 mA, I_B = 0)	MJE5740 MJE5741 MJE5742	$V_{CEO(sus)}$	300 350 400	— — —	— — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	— —	— —	1 5	mAdc
Emitter Cutoff Current (V_{EB} = 8 Vdc, I_C = 0)		I_{EBO}	—	—	75	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 6			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 7			

(2) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5 Vdc) (I_C = 4 Adc, V_{CE} = 5 Vdc)		h_{FE}	50 200	100 400	— —	—
Collector-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.2 Adc) (I_C = 8 Adc, I_B = 0.4 Adc) (I_C = 4 Adc, I_B = 0.2 Adc, T_C = 100°C)		$V_{CE(sat)}$	 — — —	 — — —	 2 3 2.2	Vdc
Base-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.2 Adc) (I_C = 8 Adc, I_B = 0.4 Adc) (I_C = 4 Adc, I_B = 0.2 Adc, T_C = 100°C)		$V_{BE(sat)}$	 — — —	 — — —	 2.5 3.5 2.4	Vdc
Diode Forward Voltage (2) (I_F = 5 Adc)		V_f	—	—	2.5	Vdc
SWITCHING CHARACTERISTICS						
Typical Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, $I_{C(pk)}$ = 6 A I_{B1} = I_{B2} = 0.25 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	—	0.04	—	μs
Rise Time		t_r	—	0.5	—	μs
Storage Time		t_s	—	8	—	μs
Fall Time		t_f	—	2	—	μs
Inductive Load, Clamped (Table 1)						
Voltage Storage Time	($I_{C(pk)}$ = 6 A, $V_{CE(pk)}$ = 250 Vdc I_{B1} = 0.06 A, $V_{BE(off)}$ = 5 Vdc	t_{sv}	—	4	—	μs
Crossover Time		t_c	—	2	—	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
(2) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

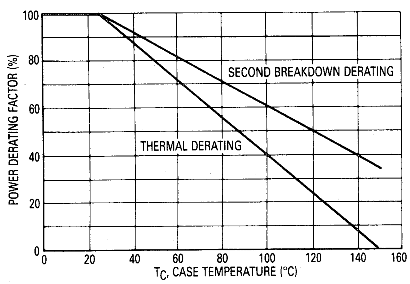


Figure 1. Power Derating

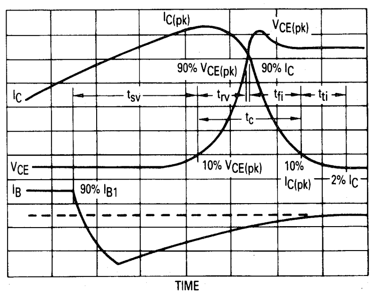


Figure 2. Inductive Switching Measurements

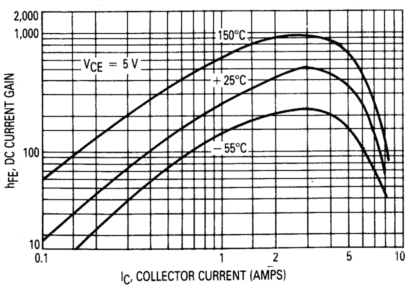


Figure 3. DC Current Gain

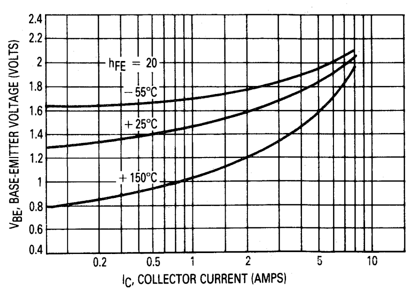
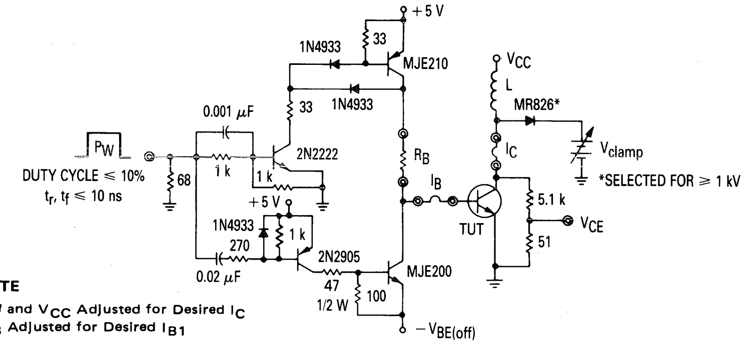


Figure 4. Base-Emitter Voltage

Table 1. Test Conditions for Dynamic Performance

Reverse Bias Safe Operating Area and Inductive Switching

Test Circuits



NOTE
PW and V_{CC} Adjusted for Desired I_C
R_B Adjusted for Desired I_{B1}

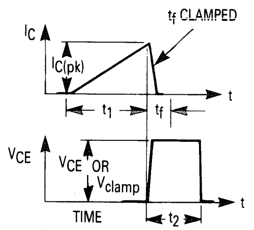
Circuit Values

COIL DATA:
FERROXCUBE CORE #6656
FULL BOBBIN (~16 TURNS) #16

GAP FOR 200 μH/20 A
L_{coil} = 200 μH

V_{CC} = 30 V
$V_{CE(pk)}$ = 250 Vdc
$I_{C(pk)}$ = 6 A

Test Waveforms



Output Waveforms

t_1 ADJUSTED TO OBTAIN I_C

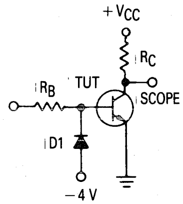
$$t_1 \approx \frac{L_{coil}\,(I_{C_{pk}})}{V_{CC}}$$

$$t_2 \approx \frac{L_{coil}\,(I_{C_{pk}})}{V_{clamp}}$$

TEST EQUIPMENT
SCOPE — TEKTRONIX
475 OR EQUIVALENT

Resistive Switching

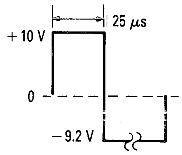
Test Circuits



Circuit Values

V_{CC} = 250 V
D1 = 1N5820 OR EQUIV.

Test Waveforms



t_r, t_f < 10 ns
DUTY CYCLE = 1%
R_B AND R_C ADJUSTED FOR DESIRED I_B AND I_C

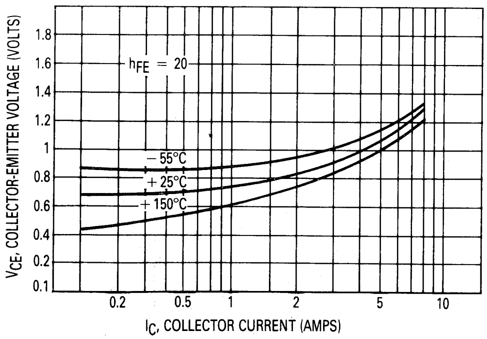
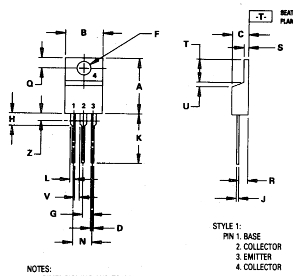


Figure 5. Collector Saturation Voltage

OUTLINE DIMENSIONS



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 1.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives the complete RBSOA characteristics.

The Safe Operating Area figures shown in Figures 6 and 7 are specified ratings for these devices under the test conditions shown.

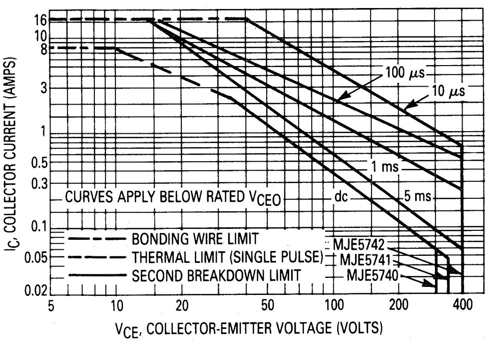


Figure 6. Forward Bias Safe Operating Area

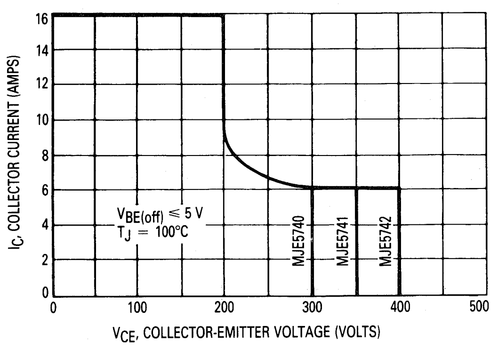


Figure 7. Reverse Bias Safe Operating Area

RESISTIVE SWITCHING PERFORMANCE

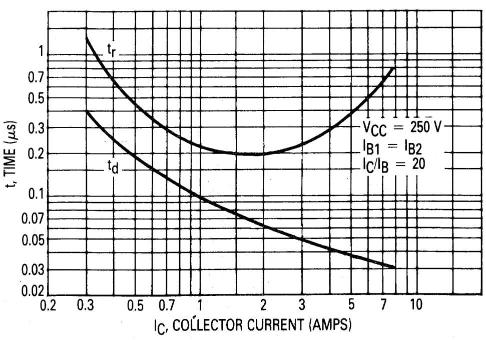


Figure 8. Turn-On Time

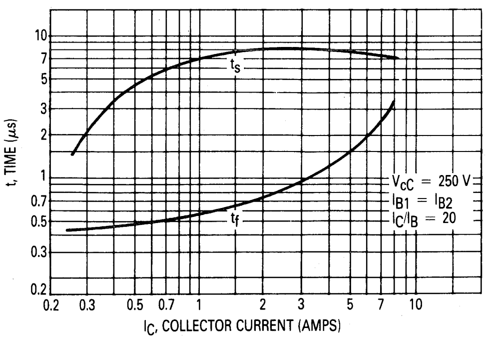


Figure 9. Turn-Off Time

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE5850
MJE5851
MJE5852

Designer's Data Sheet

SWITCHMODE SERIES
PNP SILICON POWER TRANSISTORS

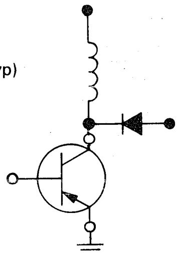
The MJE5850, MJE5851 and the MJE5852 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Delfection Circuits

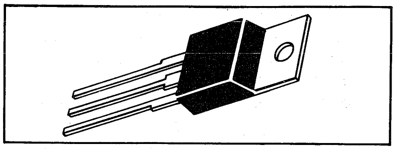
Fast Turn-Off Times
100 ns Inductive Fall Time @ 25°C (Typ)
125 ns Inductive Crossover Time @ 25°C (Typ)

Operating Temperature Range -65 to +150°C

100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



8 AMPERE
PNP SILICON POWER TRANSISTORS
300, 350, 400 VOLTS
80 WATTS



Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

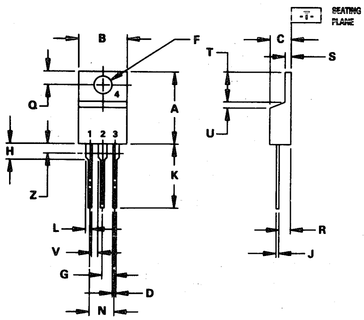
MAXIMUM RATINGS

Rating	Symbol	MJE 5850	MJE 5851	MJE 5852	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	350	400	450	Vdc
Emitter Base Voltage	V_{EB}		6.0		Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}		8.0 16		Adc
Base Current — Continuous Peak (1)	I_B I_{BM}		4.0 8.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		80 0.640		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES:
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DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
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B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE5850 / MJE5851 / MJE5852	$V_{CEO(sus)}$	300 350 400	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	— —	0.5 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 13			
***ON CHARACTERISTICS**					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5 Vdc) (I_C = 5.0 Adc, V_{CE} = 5 Vdc)	h_{FE}	15 5	— —	— —	—
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 1.0 Adc) (I_C = 8.0 Adc, I_B = 3.0 Adc) (I_C = 4.0 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	— — —	2.0 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 1.0 Adc) (I_C = 4.0 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	270	—	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, t_p = 50 μs, Duty Cycle ≤ 2%)	t_d	—	0.025	0.1	μs
Rise Time		t_r	—	0.100	0.5	μs
Storage Time	(V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%)	t_s	—	0.60	2.0	μs
Fall Time		t_f	—	0.11	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_{CM} = 4 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	0.8	3.0	μs
Crossover Time		t_c	—	0.4	1.5	μs
Fall Time		t_{fi}	—	0.1	—	μs
Storage Time	(I_{CM} = 4 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	—	0.5	—	μs
Crossover Time		t_c	—	0.125	—	μs
Fall Time		t_{fi}	—	0.1	—	μs

* Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%

3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

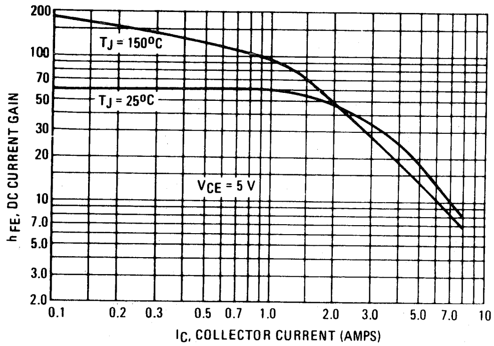


FIGURE 2 – COLLECTOR SATURATION REGION

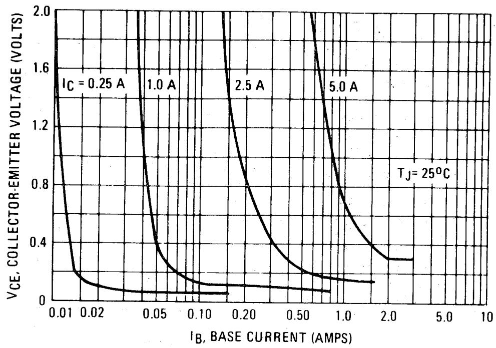


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

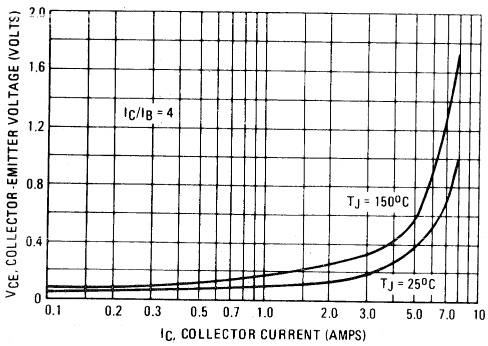


FIGURE 4 – BASE-EMITTER VOLTAGE

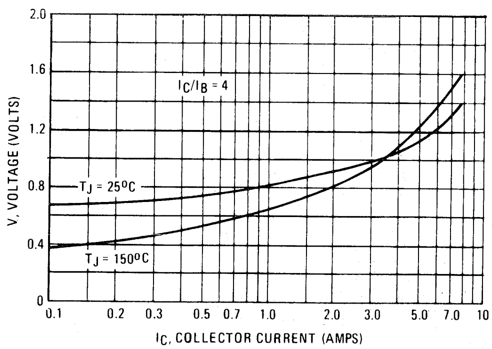


FIGURE 5 – COLLECTOR CUTOFF REGION

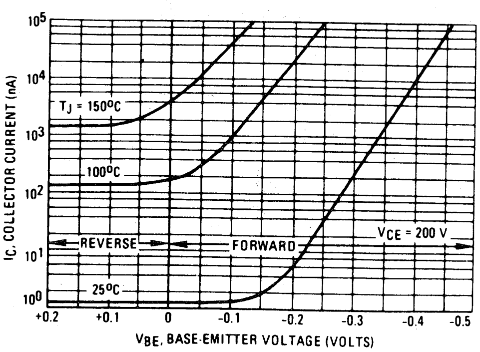
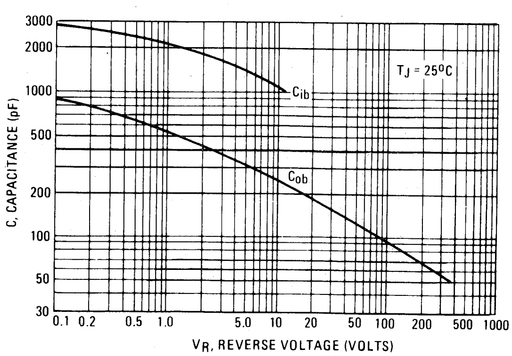


FIGURE 6 – CAPACITANCE



3

TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

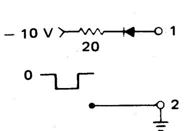
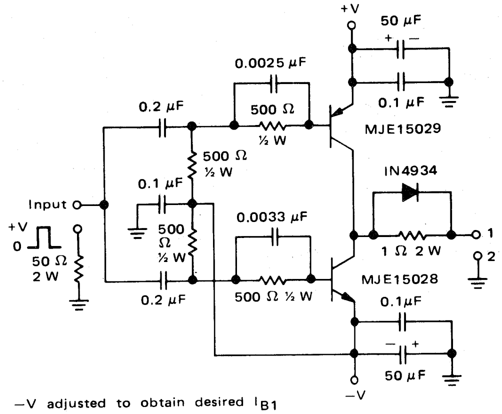
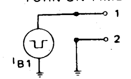
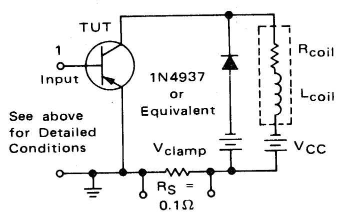
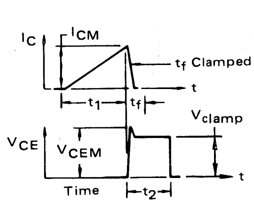
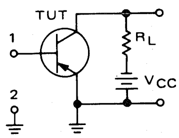
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 −V adjusted to obtain desired I_{B1} +V adjusted to obtain desired $V_{BE(off)}$	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain I_{B1}	V_{CC} = 250 V R_L = 62 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

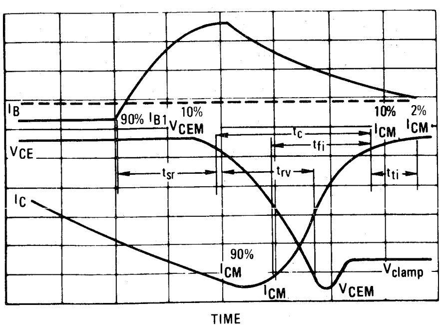
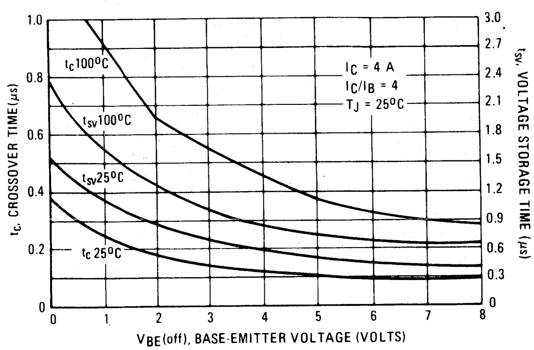


FIGURE 8 — INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user orinented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 9 – TURN-ON SWITCHING TIMES

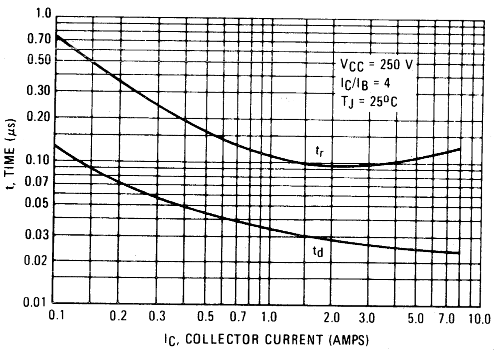


FIGURE 10 – TURN-OFF SWITCHING TIMES

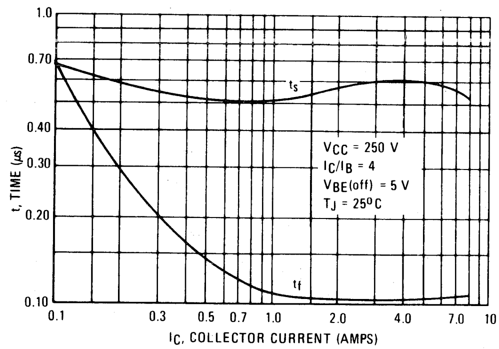
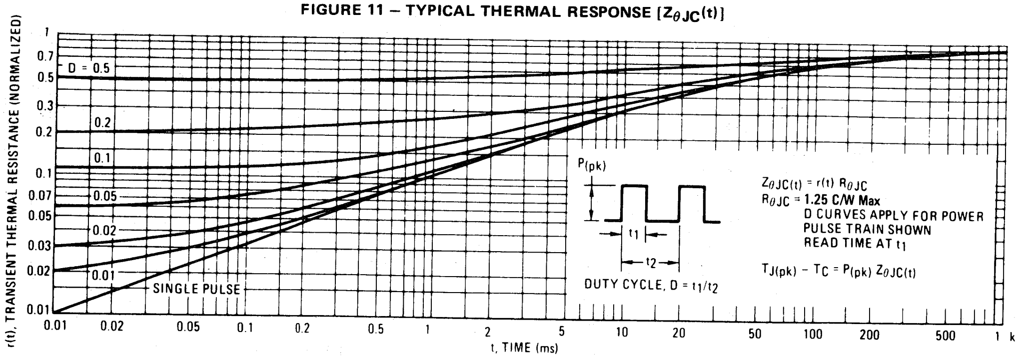


FIGURE 11 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA

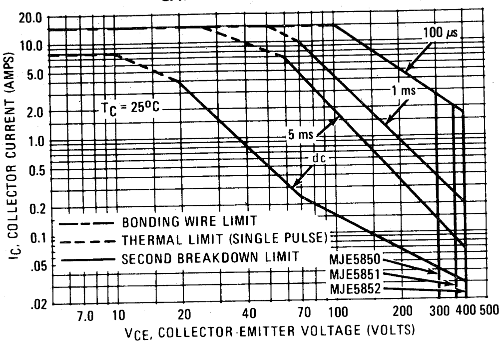
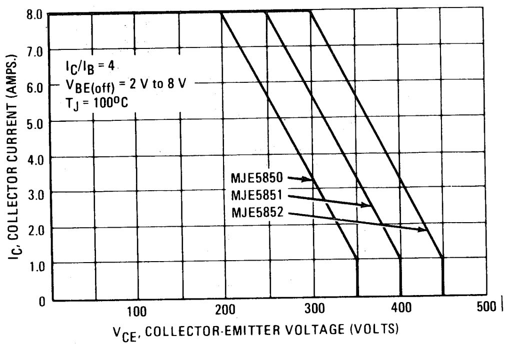


FIGURE 13 – RBSOA, MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

3

FIGURE 14 PEAK REVERSE BASE CURRENT

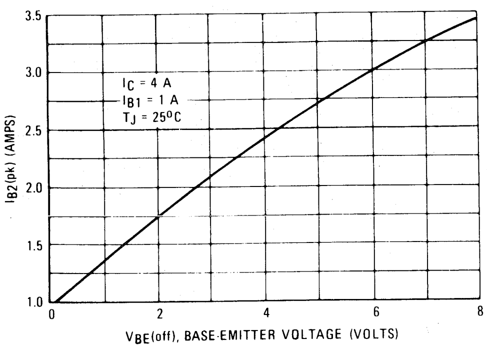
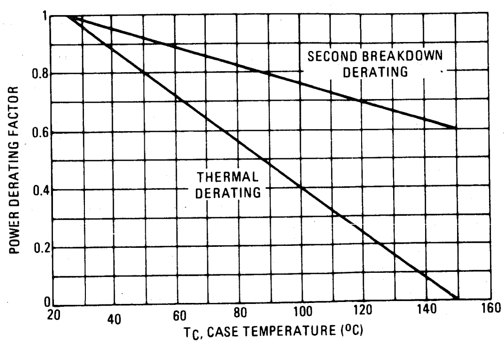


FIGURE 15 – FORWARD BIAS POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE6040 thru MJE6045
See Page 3-146

MJE8500
MJE8501

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE8500 and MJE8501 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 300 ns Inductive Fall Time – 25°C (Typ)
- 500 ns Inductive Crossover Time – 25°C (Typ)
- 900 ns Inductive Storage Time – 25°C (Typ)

Operating Temperature Range –65 to +125°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

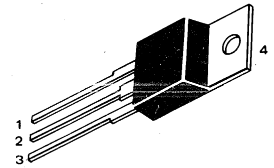
2.5 AMPERE

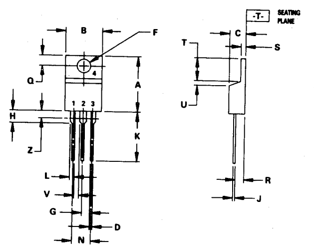
NPN SILICON POWER TRANSISTORS

700 and 800 VOLTS
65 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	MJE8500	MJE8501	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current – Continuous Peak (1)	I_C I_{CM}	2.5 5.0	2.5 5.0	Adc
Base Current – Continuous Peak (1)	I_B I_{BM}	2.0 4.0	2.0 4.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	65 17 0.65	65 17 0.65	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +125		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.54	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJE8500	$V_{CEO(sus)}$	700	–	–	Vdc
	MJE8501		800	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	–	0.25	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	–	5.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	7.5	–	–	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.33 Adc)		$V_{CE(sat)}$	–	–	2.0	Vdc
(I_C = 2.5 Adc, I_B = 1.0 Adc)			–	–	5.0	
(I_C = 1.0 Adc, I_B = 0.33 Adc, T_C = 100°C)			–	–	3.0	
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.33 Adc)		$V_{BE(sat)}$	–	–	1.5	Vdc
(I_C = 1.0 Adc, I_B = 0.33 Adc, TC = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	50	–	250	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 500 Vdc, I_C = 1.0 A, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.045	0.20	μs
Rise Time		t_r	–	0.2	2.0	μs
Storage Time		t_s	–	1.0	4.0	μs
Fall Time		t_f	–	0.5	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 1.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	1.3	4.0	μs
Crossover Time		t_c	–	0.6	2.0	μs
Storage Time	(I_C = 1.0 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 0.33 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	0.9	–	μs
Crossover Time		t_c	–	0.5	–	μs
Fall Time		t_{fi}	–	0.3	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

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FIGURE 1 — DC CURRENT GAIN

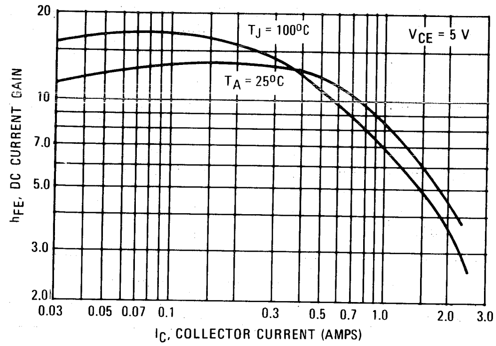

FIGURE 2 — COLLECTOR SATURATION REGION

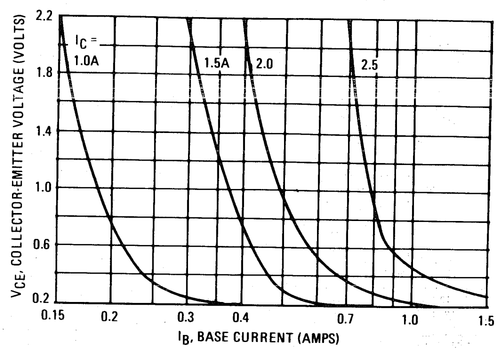

FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

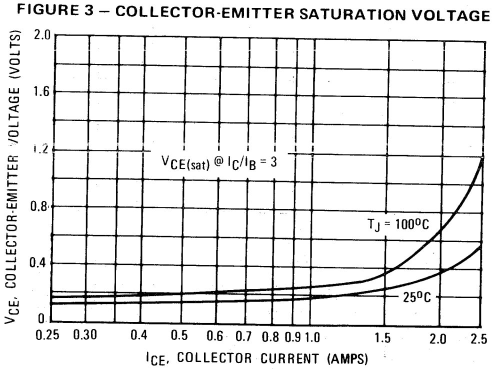

FIGURE 4 — BASE-EMITTER VOLTAGE

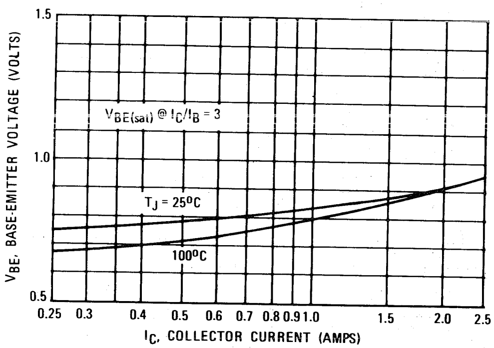

FIGURE 5 — COLLECTOR CUTOFF REGION

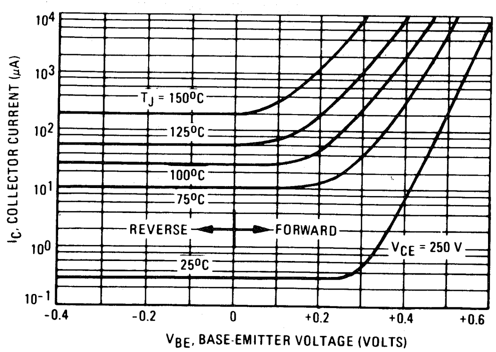

FIGURE 6 — CAPACITANCE

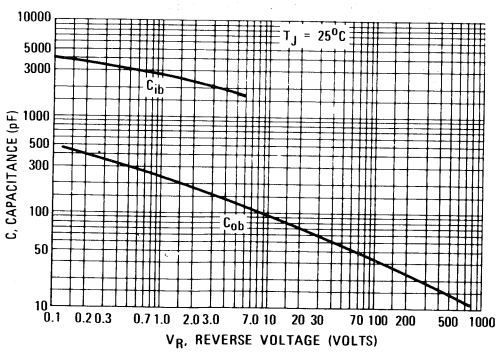

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FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

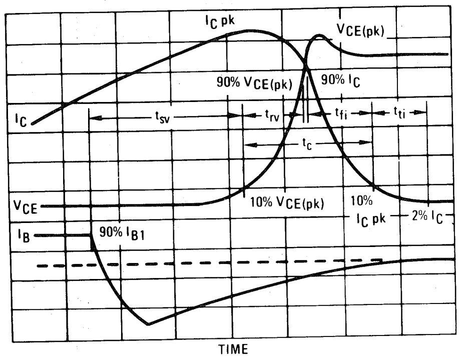
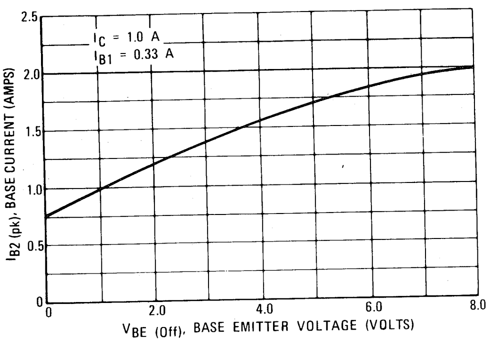


FIGURE 8 — PEAK REVERSE BASE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CE} (pk)
t_{rv} = Voltage Rise Time, 10–90% V_{CE} (pk)
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{CE} (pk) to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

3

TYPICAL RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 — TURN - ON SWITCHING TIMES

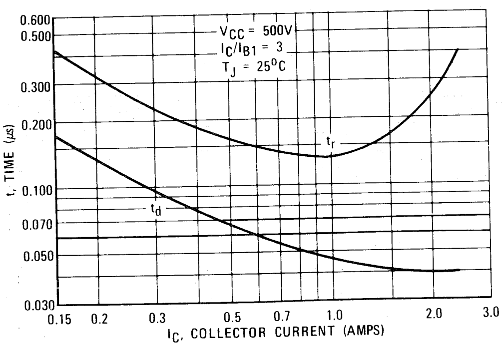


FIGURE 10 — TURN - OFF SWITCHING TIMES

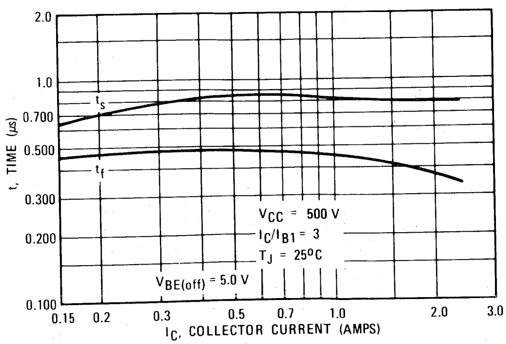


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

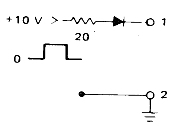
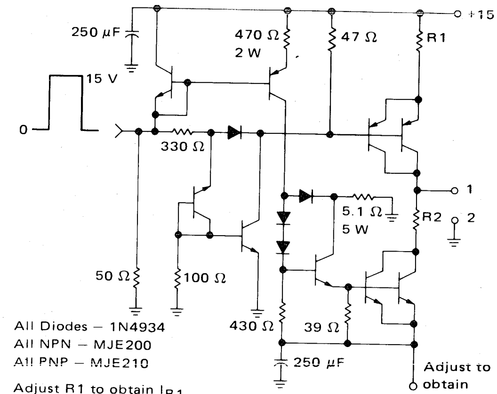
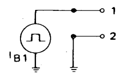
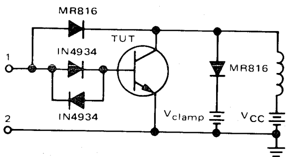
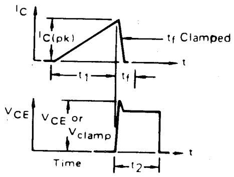
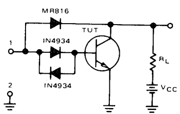
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞ Adjust to obtain $V_{BE(off)}$ = 5.0 V	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 500 V	V_{CC} = 500 V R_L = 500 Ω Pulse Width = 10 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 11 – THERMAL RESPONSE

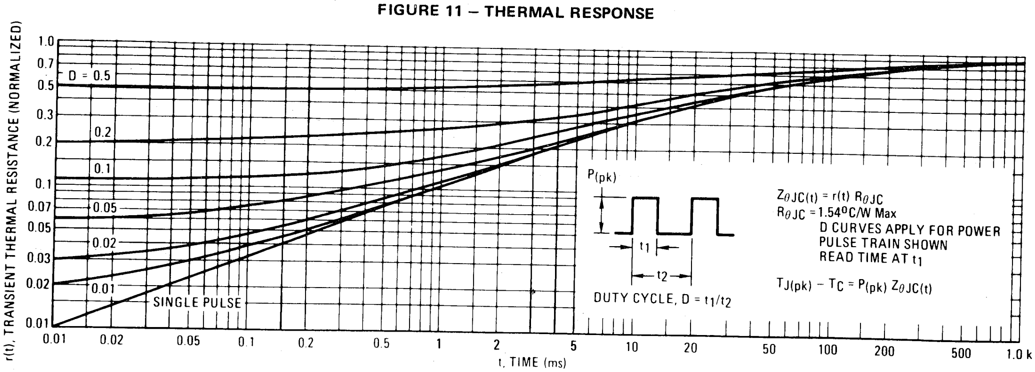


FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

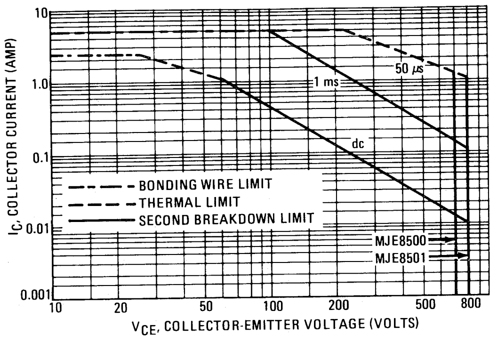
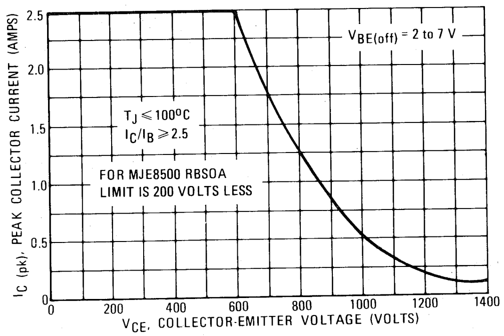


FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

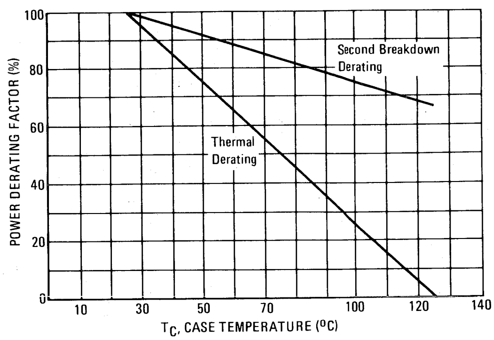
$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

3

FIGURE 14 — POWER DERATING



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

MJE8502
MJE8503

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

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- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 150 ns Inductive Fall Time—25°C (Typ)
- 400 ns Inductive Crossover Time—25°C (Typ)
- 1200 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range −65 to +125°C

100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
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5.0 AMPERE

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700 and 800 VOLTS
80 WATTS

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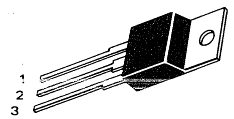

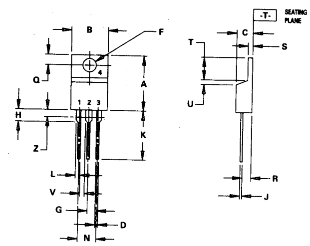

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
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G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
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L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

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Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	5.0 10	5.0 10	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	4.0 8.0	4.0 8.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	80 21 0.80	80 21 0.80	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +125		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) MJE8502 (I_C = 100 mA, I_B = 0) MJE8503		$V_{CEO(sus)}$	700 800	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	– –	– –	0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	7.5	–	–	–
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 2.0 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	– – –	– – –	2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 1.0 Adc) (I_C = 2.5 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{BE(sat)}$	– –	– –	1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	60	–	300	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 500 Vdc, I_C = 2.5 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.040	0.20	μs
Rise Time		t_r	–	0.125	2.0	μs
Storage Time		t_s	–	1.2	4.0	μs
Fall Time		t_f	–	0.65	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 2.5 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, TC = 100°C)	t_{sv}	–	1.6	5.0	μs
Crossover Time		t_c	–	0.60	2.0	μs
Storage Time	(I_C = 2.5 A(pk), V_{clamp} = 500 Vdc, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	1.2	–	μs
Crossover Time		t_c	–	0.4	–	μs
Fall Time		t_{fi}	–	0.15	–	μs

(1) Pulse Test: PW · 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

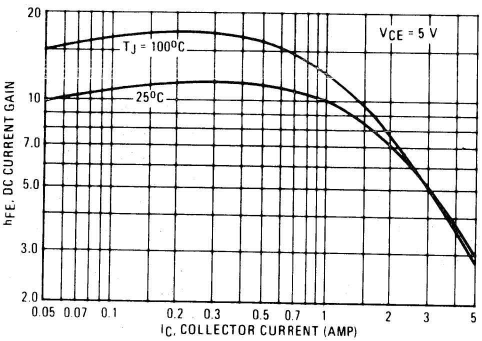


FIGURE 2 — COLLECTOR SATURATION REGION

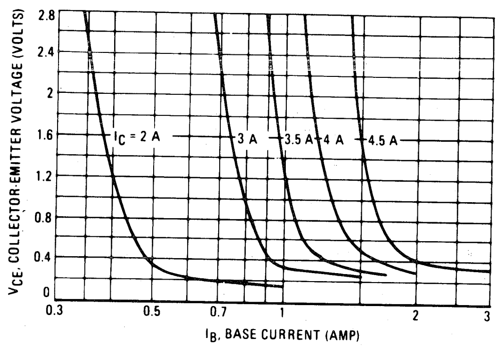


FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION

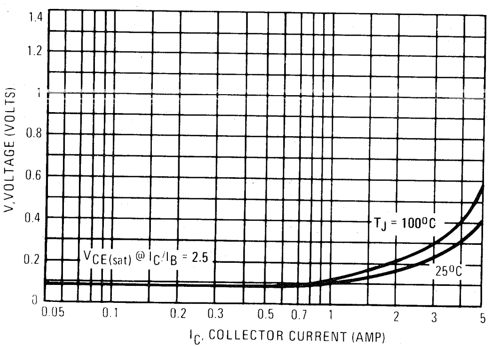


FIGURE 4 — BASE-EMITTER VOLTAGE

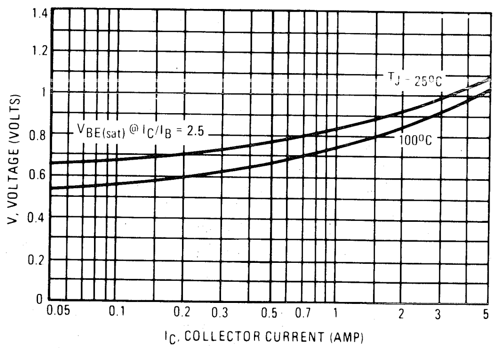


FIGURE 5 — COLLECTOR CUTOFF REGION

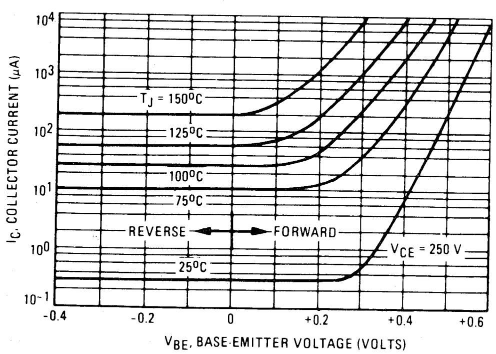


FIGURE 6 — CAPACITANCE

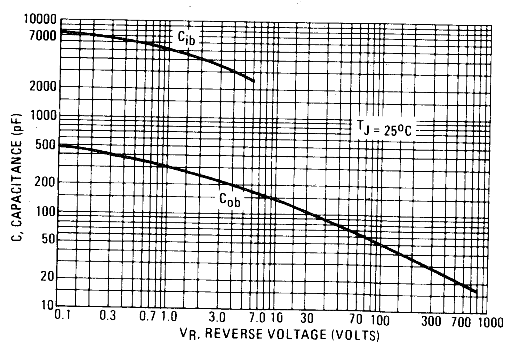


FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

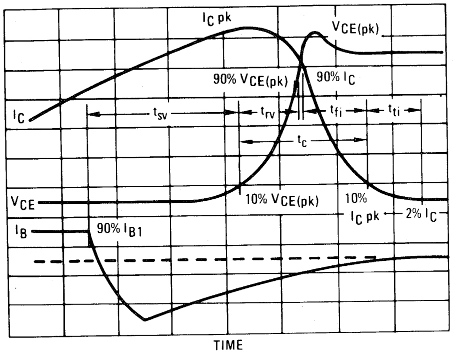
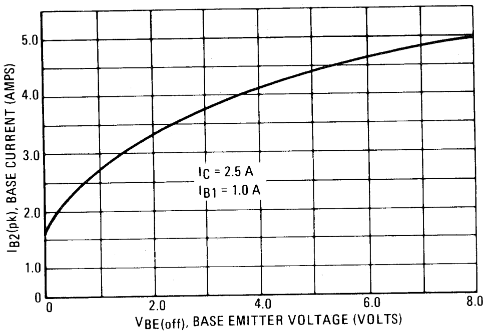


FIGURE 8 – PEAK REVERSE BASE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$
t_{rv} = Voltage Rise Time, 10–90% $V_{CE(pk)}$
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

3

TYPICAL RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON SWITCHING TIMES

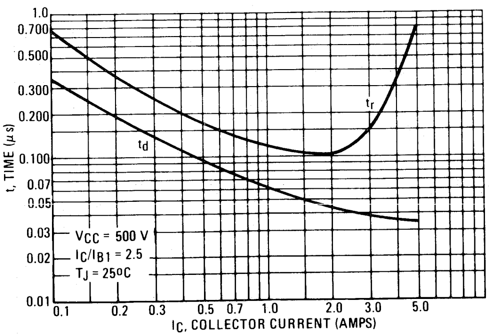


FIGURE 10 – TURN-OFF SWITCHING TIMES

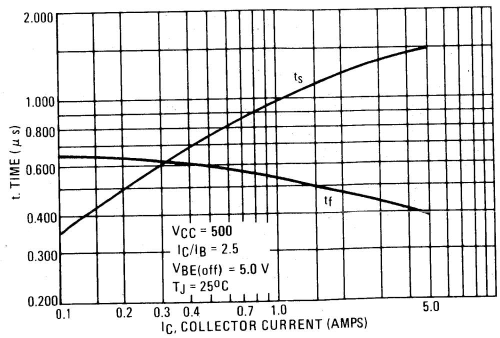


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

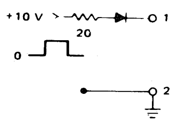
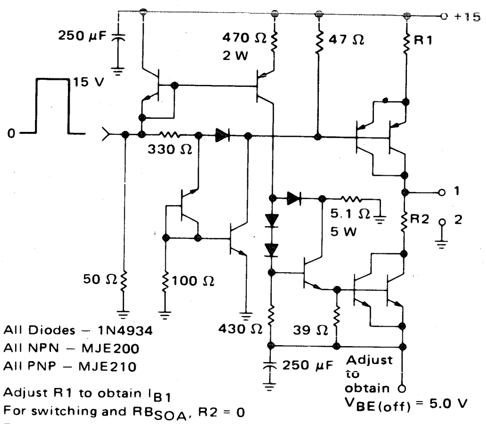
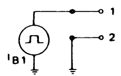
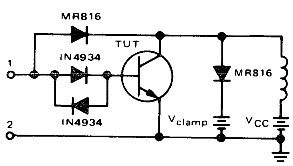
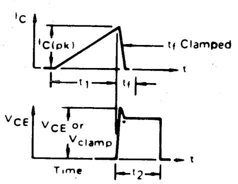
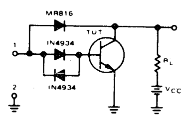
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 All Diodes — 1N4934 All NPN — MJE200 All PNP — MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 500 V	V_{CC} = 500 V R_L = 200 Ω Pulse Width = 10 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 11 — THERMAL RESPONSE

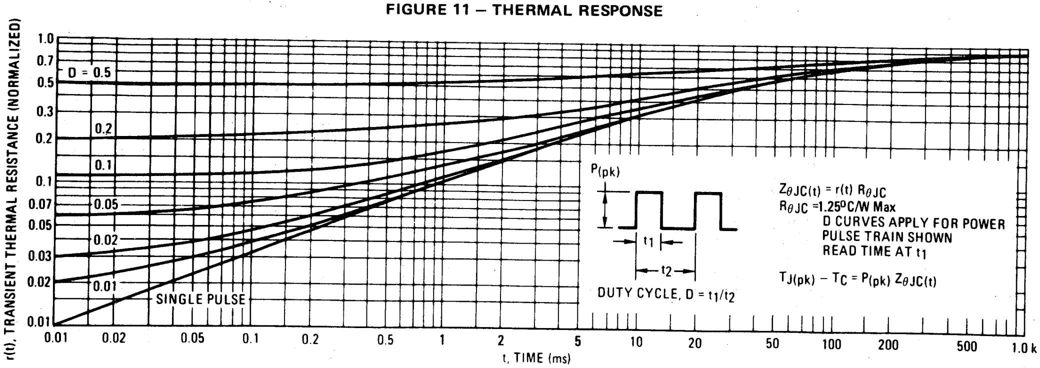


FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

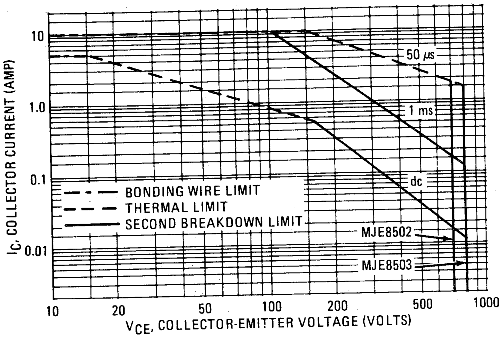
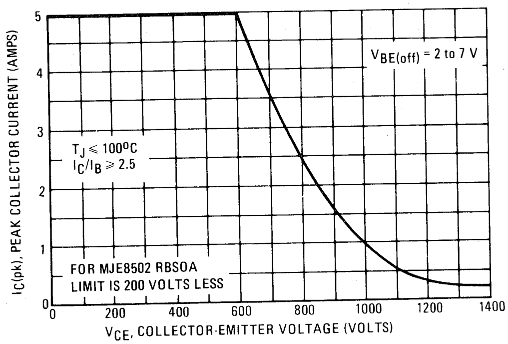


FIGURE 13 — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

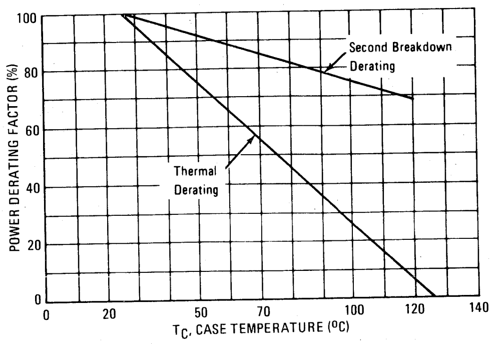
$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

3

FIGURE 14 — POWER DERATING



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

MJE12007

HORIZONTAL DEFLECTION TRANSISTOR

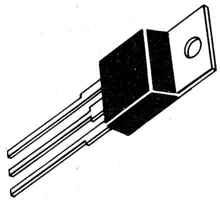
. . . specifically designed for use in small screen black and white deflection circuits.

- Collector-Emitter Voltage — V_{CEX} = 1500 Volts
- Glassivated Base-Collector Junction
- Switching Times with Inductive Loads — t_f = 0.65 μs (Typ) @ I_C = 2.0 A

2.5 AMPERE

NPN SILICON POWER TRANSISTOR

1500 VOLTS
65 WATTS

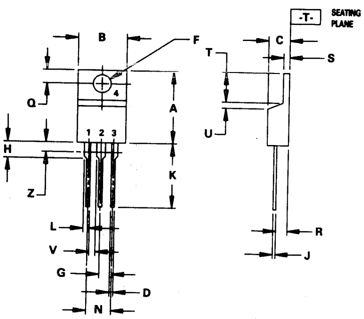


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous	I_C	2.5	Adc
Base Current — Continuous	I_B	2.0	Adc
Emitter Current — Continuous	I_E	4.5	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above 25°C	P_D	65 0.65	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.54	°C/W



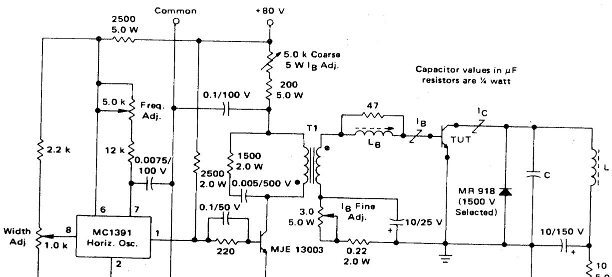
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

FIGURE 1 — TEST CIRCUIT



I_C	L	C
0.75 A	4.25 mH	.003 μF
1.5	2.18 mH	.006 μF
2.0	1.6 mH	.008 μF

DRIVER TRANSFORMER (T1)
Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance — 39 mH. Secondary Inductance — 22 mH, Leakage Inductance with primary shorted — 2.0 μH, Primary 260 turns #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.8 Adc)	$V_{CE(sat)}$	–	–	5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.8 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	50	–	pF
Current Gain — Bandwidth Product (1) (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	–	4.0	–	MHz
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 2.0 Adc, I_{B1} = 1.0 Adc, L_B = 12 μH)	t_f	–	0.65	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 2 — DC CURRENT GAIN

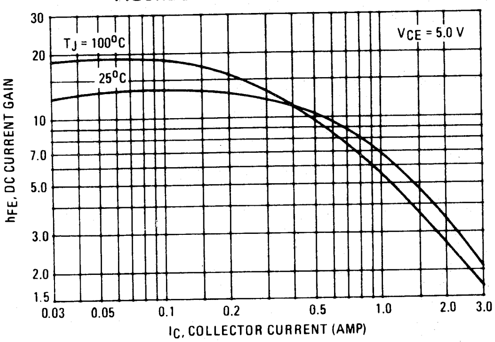


FIGURE 3 — "ON" VOLTAGE

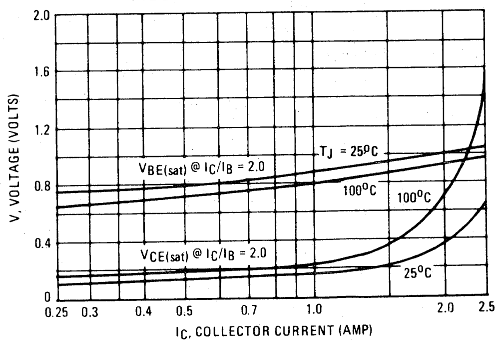
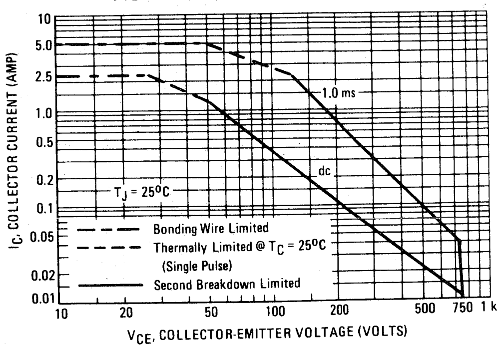


FIGURE 4 — SAFE OPERATING AREA



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE13002
MJE13003

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

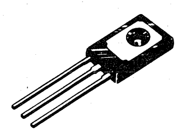
SPECIFICATION FEATURES:

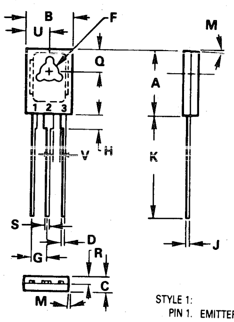
- Reverse Biased SOA with Inductive Loads @ $T_C = 100^oC$
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and 100^oC . . . t_c @ 1 A, 100^oC is 290 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

1.5 AMPERE

NPN SILICON POWER TRANSISTORS

300 and 400 VOLTS
40 WATTS





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

MAXIMUM RATINGS

Rating	Symbol	MJE13002	MJE13003	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	1.5 3		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	0.75 1.5		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	2.25 4.5		Adc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	1.4 11.2		Watts $mW/^oC$
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	40 320		Watts $mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	89	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13002	$V_{CEO(sus)}$	300	–	–	Vdc
MJE13003		400	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 100^oC$)		–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 12			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 2 Vdc)	h_{FE}	8	–	40	–
(I_C = 1 Adc, V_{CE} = 2 Vdc)		5	–	25	
Collector-Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	–	–	0.5	Vdc
(I_C = 1 Adc, I_B = 0.25 Adc)		–	–	1	
(I_C = 1.5 Adc, I_B = 0.5 Adc)		–	–	3	
(I_C = 1 Adc, I_B = 0.25 Adc, $T_C = 100^oC$)		–	–	1	
Base-Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	–	–	1	Vdc
(I_C = 1 Adc, I_B = 0.25 Adc)		–	–	1.2	
(I_C = 1 Adc, I_B = 0.25 Adc, $T_C = 100^oC$)		–	–	1.1	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	10	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	21	–	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 125 Vdc, I_C = 1 A, $I_{B1} = I_{B2}$ = 0.2 A, t_p - 25 μs, Duty Cycle ≤ 1%)	t_d	–	0.05	0.1	μs
Rise Time	t_r	–	0.5	1	μs
Storage Time	t_s	–	2	4	μs
Fall Time	t_f	–	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)					
Storage Time (I_C = 1 A, V_{clamp} = 300 Vdc, I_{B1} = 0.2 A, $V_{BE(off)}$ = 5 Vdc, $T_C = 100^oC$)	t_{sv}	–	1.7	4	μs
Crossover Time	t_c	–	0.29	0.75	μs
Fall Time	t_{fi}	–	0.15	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 1 — DC CURRENT GAIN

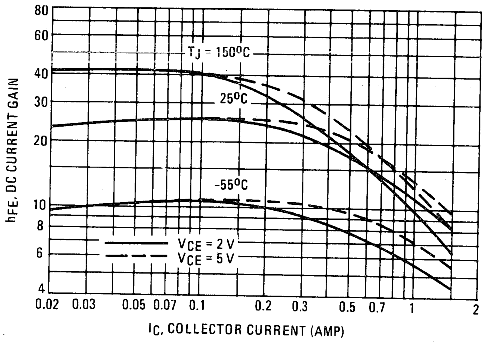


FIGURE 2 — COLLECTOR SATURATION REGION

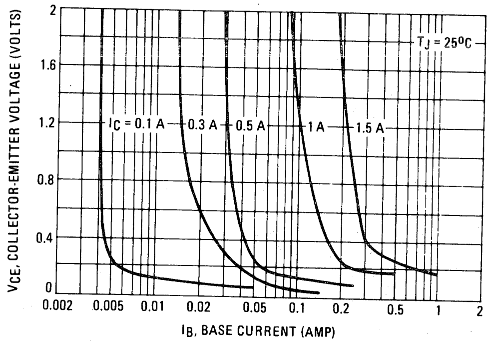


FIGURE 3 — BASE-EMITTER VOLTAGE

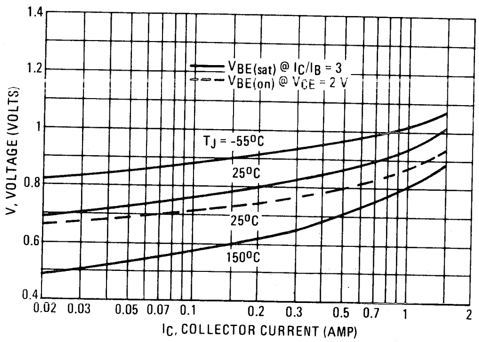


FIGURE 4 — COLLECTOR-EMITTER SATURATION REGION

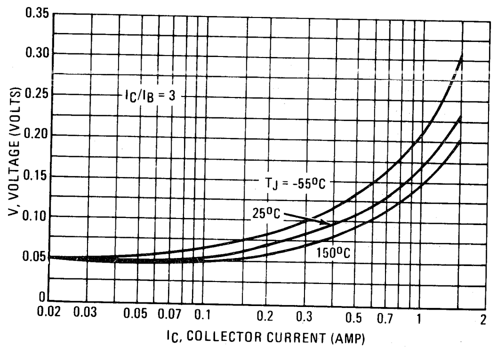


FIGURE 5 — COLLECTOR CUTOFF REGION

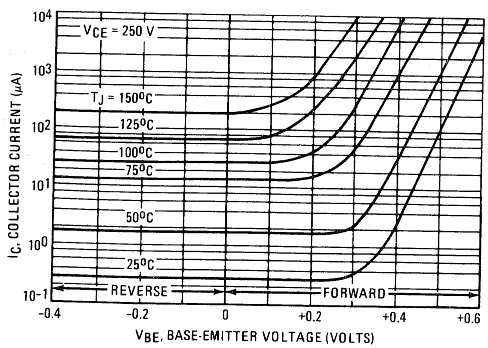


FIGURE 6 — CAPACITANCE

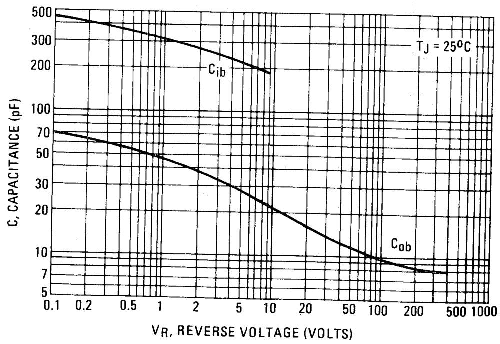


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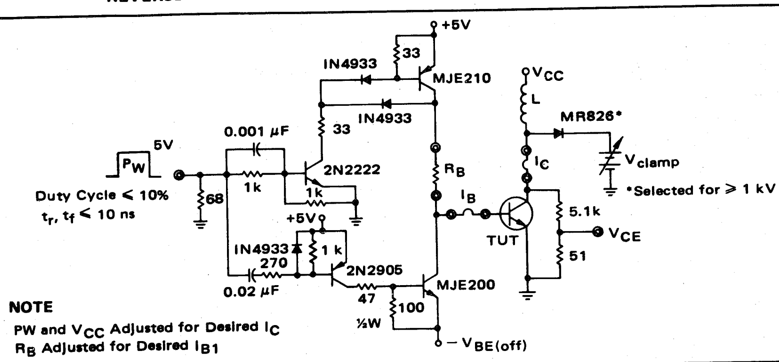
TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

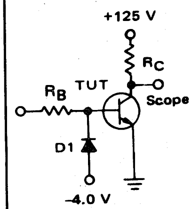
REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING

TEST CIRCUITS



NOTE
PW and V_{CC} Adjusted for Desired I_C
R_B Adjusted for Desired I_{B1}

RESISTIVE SWITCHING



CIRCUIT VALUES

Coil Data:
Ferroxcube Core #6656
Full Bobbin (~200 Turns) #20

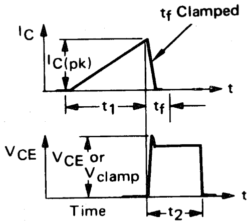
GAP for 30 mH/2A
L_{coil} = 50 mH

V_{CC} = 20 V
V_{clamp} = 300 Vdc

Resistive switching:
V_{CC} = 125 V
R_C = 125 Ω
D1 = 1N5820 or Equiv.
R_B = 47 Ω

TEST WAVEFORMS

OUTPUT WAVEFORMS

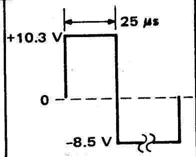


t_1 Adjusted to Obtain I_C

$$t_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$$

$$t_2 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{clamp}}$$

Test Equipment
Scope-Tektronics
475 or Equivalent



t_r, t_f < 10 ns
Duty Cycle = 1.0%
R_B and R_C adjusted for desired I_B and I_C

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

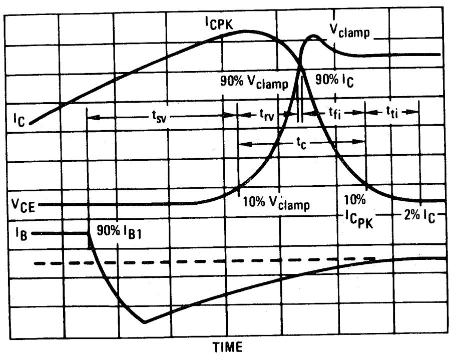


TABLE 2 — TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

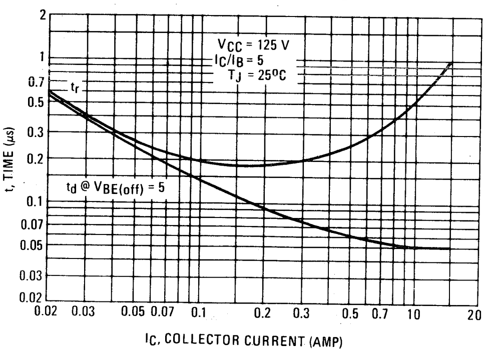


FIGURE 9 — TURN-OFF TIME

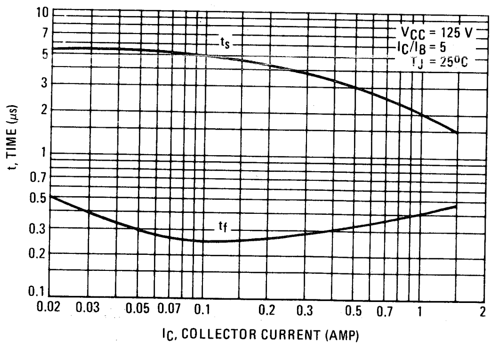
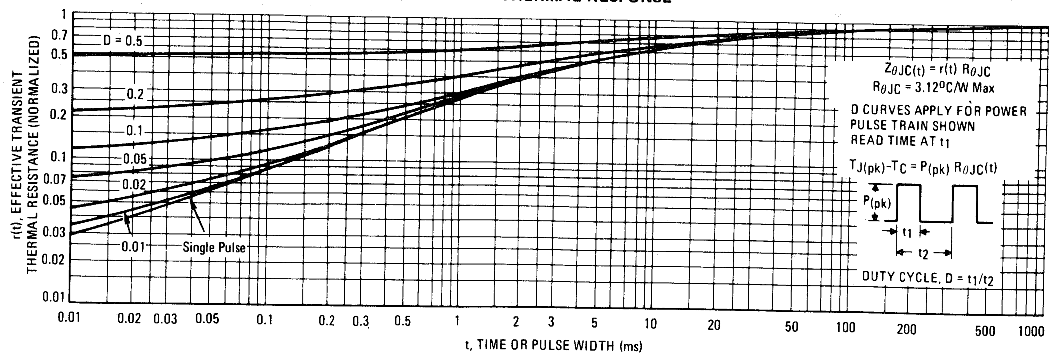


FIGURE 10 — THERMAL RESPONSE



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The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATION AREA

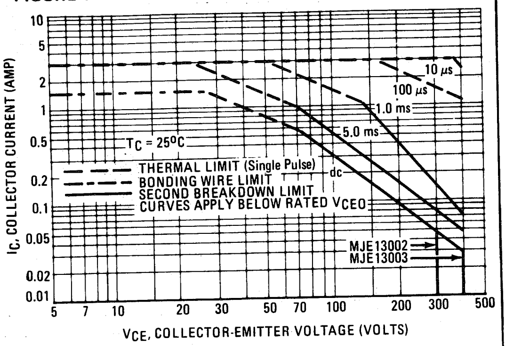
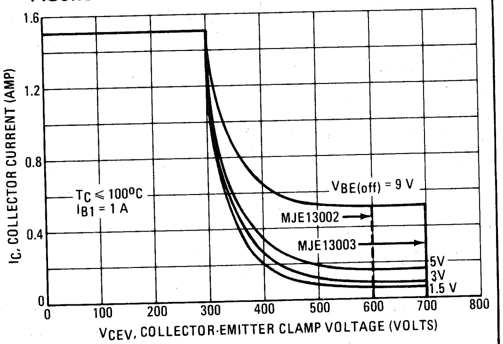


FIGURE 12 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

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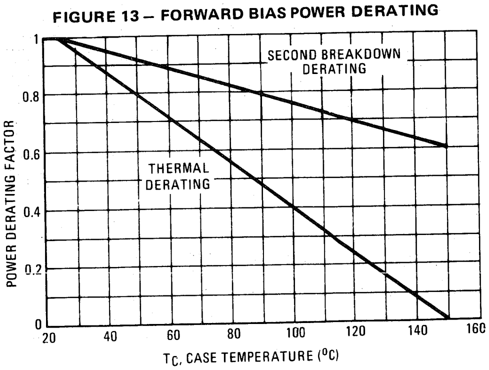
FIGURE 13 — FORWARD BIAS POWER DERATING

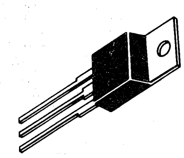


MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE13004
MJE13005

Designers Data Sheet

4 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
75 WATTS

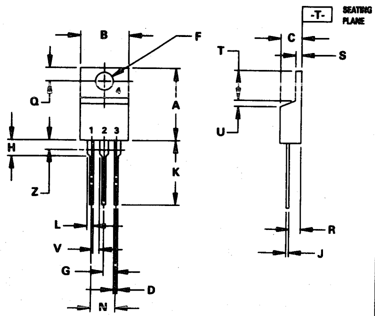


SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulator's, Inverters, Motor Controls, Solenoid / Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 2 to 4 Amp, 25 and 100°C . . . t_c @ 3A, 100°C is 180 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MJE13004	MJE13005	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	4 8		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	6 12		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 600		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ⩽ 10%.

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13004 / MJE13005	$V_{CEO(sus)}$	300 400	– –	– –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	– –	– –	1 5	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 11		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 12		
***ON CHARACTERISTICS**					
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc) (I_C = 2 Adc, V_{CE} = 5 Vdc)	h_{FE}	10 8	– –	60 40	–
Collector-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc) (I_C = 2 Adc, I_B = 0.5 Adc) (I_C = 4 Adc, I_B = 1 Adc) (I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)	$V_{CE(sat)}$	– – – –	– – – –	0.5 0.6 1 1	Vdc
Base-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc) (I_C = 2 Adc, I_B = 0.5 Adc) (I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)	$V_{BE(sat)}$	– – –	– – –	1.2 1.6 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	–	–	MHz
Output Capacitance (V_{CB} - 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	65	–	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 2)					
Delay Time (V_{CC} = 125 Vdc, I_C = 2 A, I_{B1} = I_{B2} = 0.4 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	–	0.025	0.1	μs
Rise Time	t_r	–	0.3	0.7	μs
Storage Time	t_s	–	1.7	4	μs
Fall Time	t_f	–	0.4	0.9	μs
Inductive Load, Clamped (Table 2, Figure 13)					
Voltage Storage Time (I_C = 2 A, V_{clamp} = 300 Vdc, I_{B1} = 0.4 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	0.9	4	μs
Crossover Time	t_c	–	0.32	0.9	μs
Fall Time	t_{fi}	–	0.16	–	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

3

FIGURE 1 — DC CURRENT GAIN

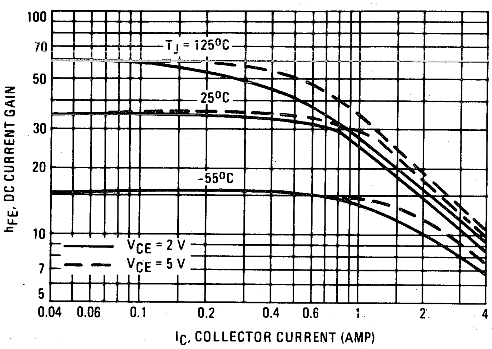


FIGURE 2 — COLLECTOR SATURATION REGION

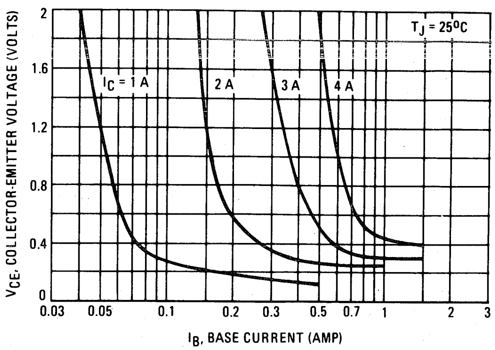


FIGURE 3 — BASE-EMITTER VOLTAGE

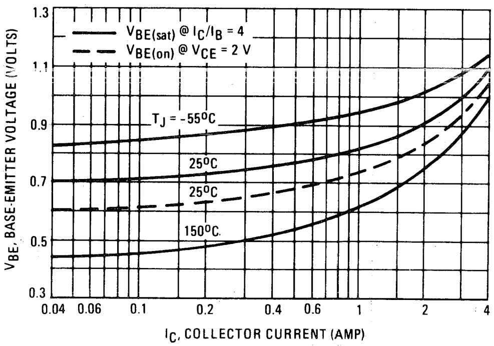


FIGURE 4 — COLLECTOR–EMITTER SATURATION VOLTAGE

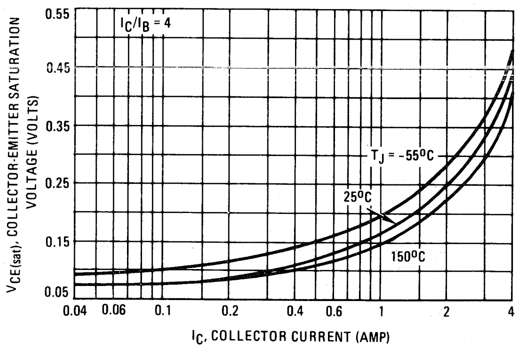


FIGURE 5 — COLLECTOR CUTOFF REGION

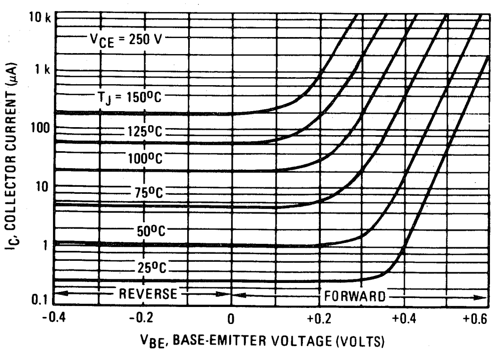


FIGURE 6 — CAPACITANCE

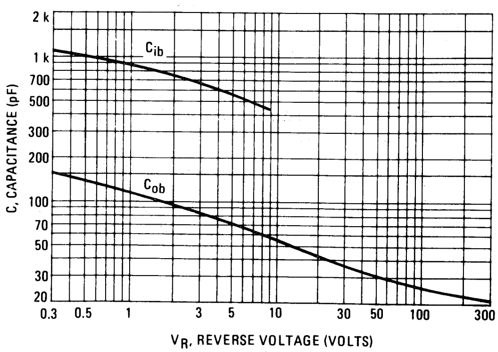


FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

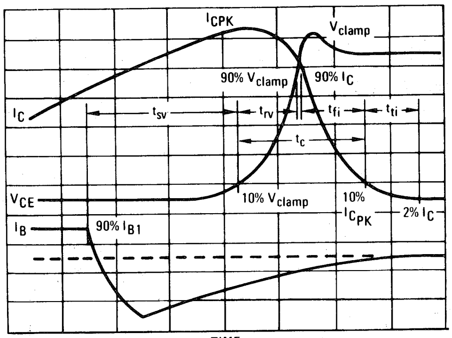


TABLE 1 — TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
2	25	600	70	100	80	180
	100	900	110	240	130	320
3	25	650	60	140	60	200
	100	950	100	330	100	350
4	25	550	70	160	100	220
	100	850	110	350	160	390

NOTE: All Data recorded in the inductive Switching Circuit in Table 2.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

3

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 — TURN-ON TIME

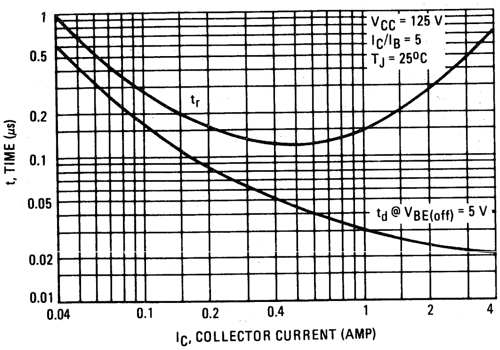


FIGURE 9 — TURN-OFF TIME

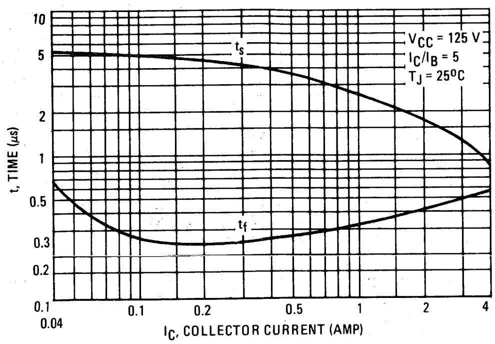


TABLE 2 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

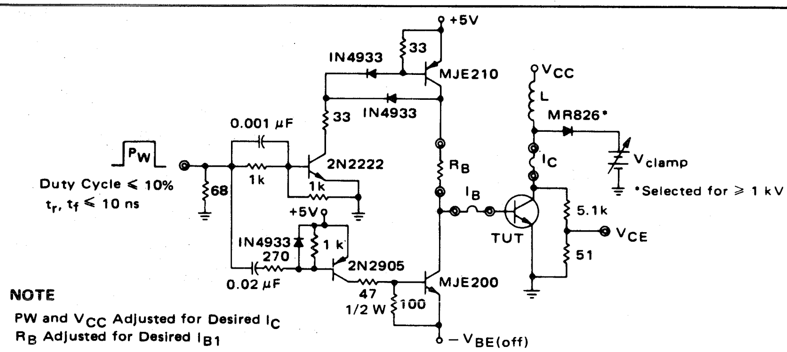
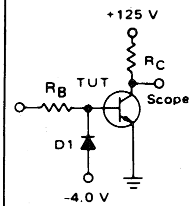
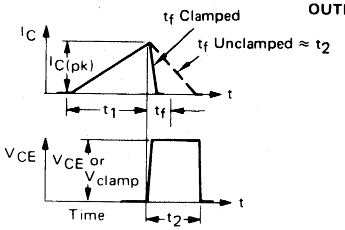
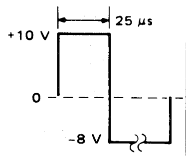
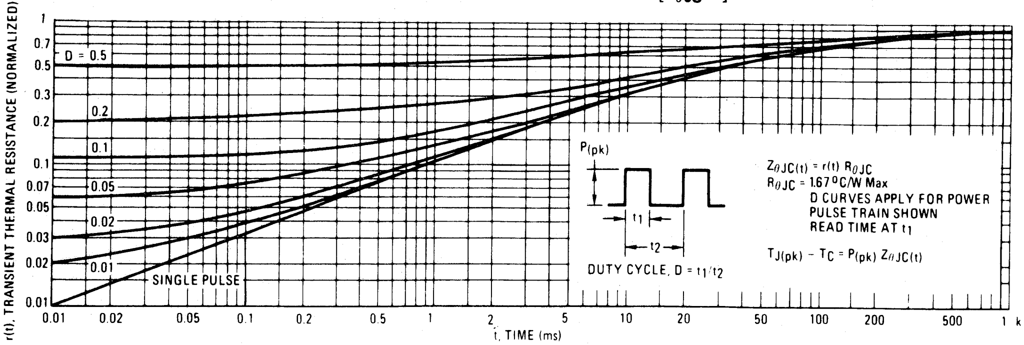
	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 NOTE: PW and V_{CC} Adjusted for Desired I_C; R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656, Full Bobbin (~16 Turns) #16; GAP for 200 µH/20A; L_{coil} = 200 µH; V_{CC} = 20 V; V_{clamp} = 300 Vdc	V_{CC} = 125 V; R_C = 62 Ω; D1 = 1N5820 or Equiv.; R_B = 22 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C; $t_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$; $t_2 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{clamp}}$; Test Equipment Scope – Tektronix 475 or Equivalent	 t_r, t_f < 10 ns; Duty Cycle = 1.0%; R_B and R_C adjusted for desired I_B and I_C

FIGURE 10 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]



3

The Safe Operating Area Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATING AREA

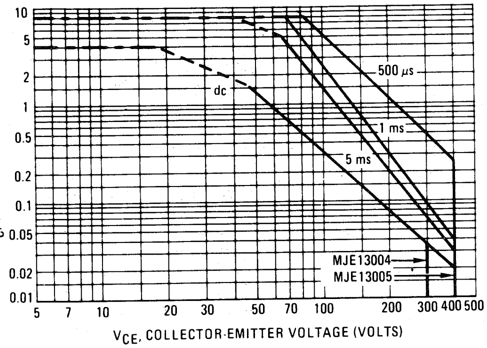
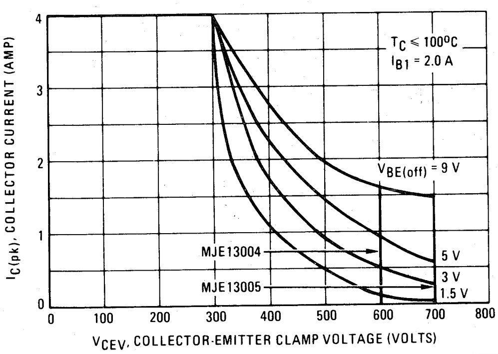


FIGURE 12— REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

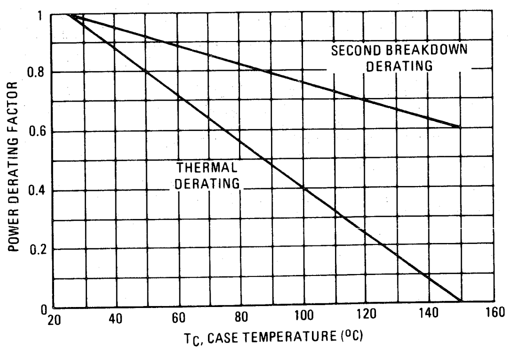
The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.

FIGURE 13 — FORWARD BIAS POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE13006
MJE13007

Designers Data Sheet

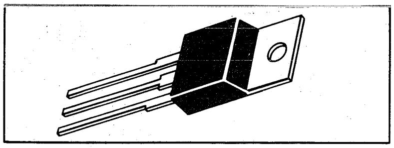
SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE13006 and MJE13007 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 8 Amp, 25 and 100°C . . . t_c @ 5A, 100°C is 136 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

8 AMPERE
NPN SILICON POWER TRANSISTORS
300 and 400 VOLTS
80 WATTS



Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

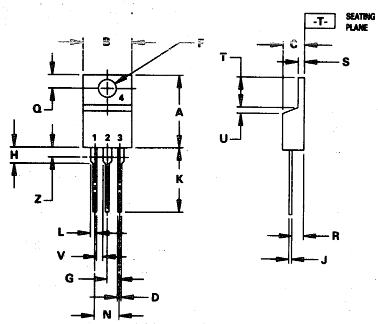
MAXIMUM RATINGS

Rating	Symbol	MJE13006	MJE13007	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8 16		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4 8		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 24		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 640		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**						
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13006		$V_{CEO(sus)}$	300	–	–	Vdc
MJE13007			400	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	–	1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased		–	See Figure 2			
***ON CHARACTERISTICS**						
DC Current Gain (I_C = 2 Adc, V_{CE} = 5 Vdc)		h_{FE}	8	–	60	–
(I_C = 5 Adc, V_{CE} = 5 Vdc)			5	–	30	
Collector-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.4 Adc)		$V_{CE(sat)}$	–	–	1	Vdc
(I_C = 5 Adc, I_B = 1 Adc)			–	–	2	
(I_C = 8 Adc, I_B = 2 Adc)			–	–	3	
(I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)			–	–	3	
Base-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.4 Adc)		$V_{BE(sat)}$	–	–	1.2	Vdc
(I_C = 5 Adc, I_B = 1 Adc)			–	–	1.6	
(I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	–	–	MHz
Output Capacitance (V_{CB} - 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	110	–	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 5 A,	t_d	–	0.05	0.1	μs
Rise Time	I_{B1} = I_{B2} = 1 A, t_p = 25 μs,	t_r	–	0.8	1.5	μs
Storage Time	Duty Cycle ⩽ 1%)	t_s	–	1	3	μs
Fall Time		t_f	–	0.15	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Voltage Storage Time	(I_C = 5 A, V_{clamp} = 300 Vdc,	t_{sv}	–	0.86	2.3	μs
Crossover Time	I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.14	0.7	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 — FORWARD BIAS SAFE OPERATING AREA

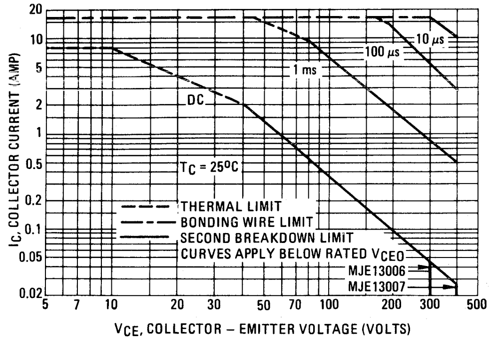
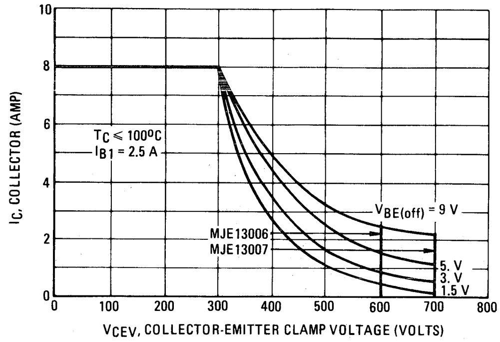
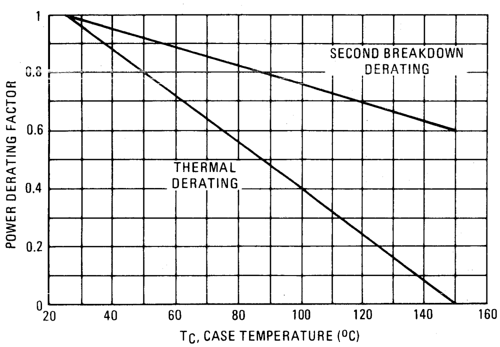


FIGURE 2 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 — FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 — TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]

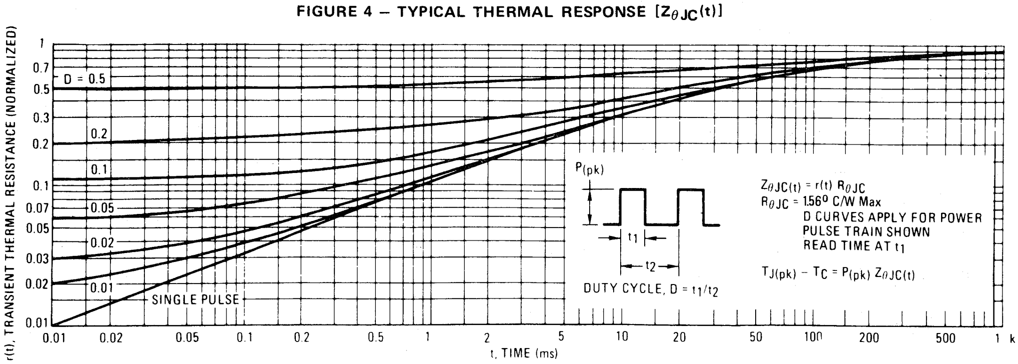


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FIGURE 5 — DC CURRENT GAIN

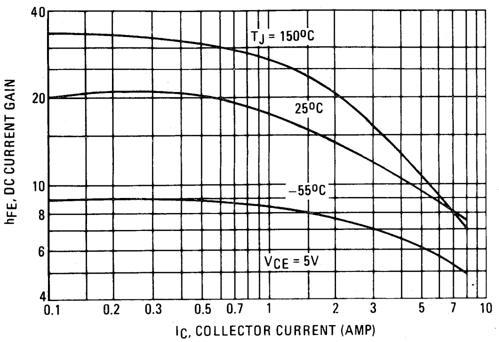

FIGURE 6 — COLLECTOR SATURATION REGION

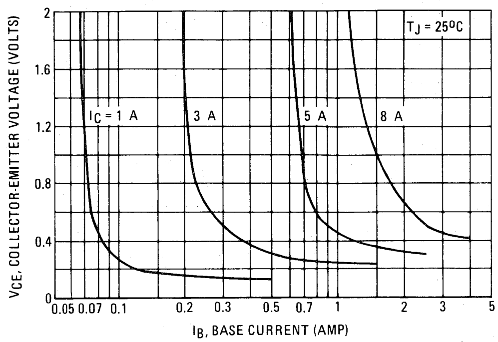

FIGURE 7 — BASE-EMITTER SATURATION VOLTAGE

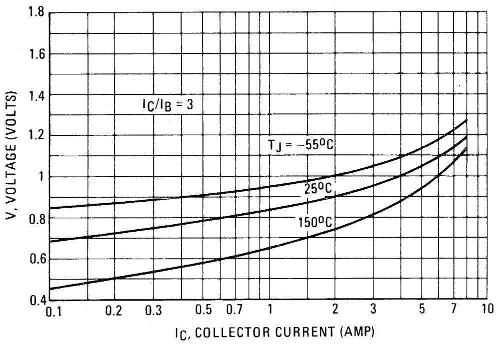

FIGURE 8 — COLLECTOR-EMITTER SATURATION VOLTAGE

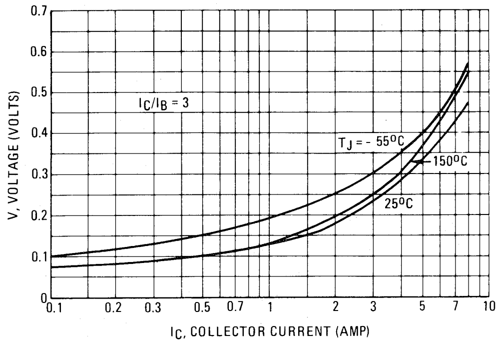

FIGURE 9 — COLLECTOR CUTOFF REGION

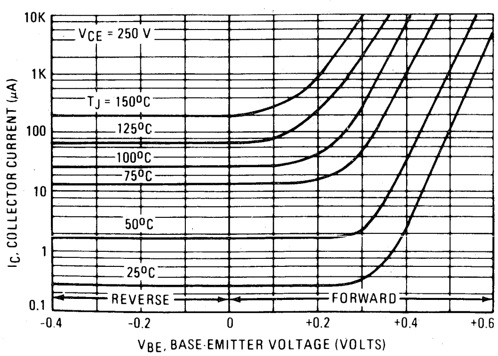

FIGURE 10 — CAPACITANCE

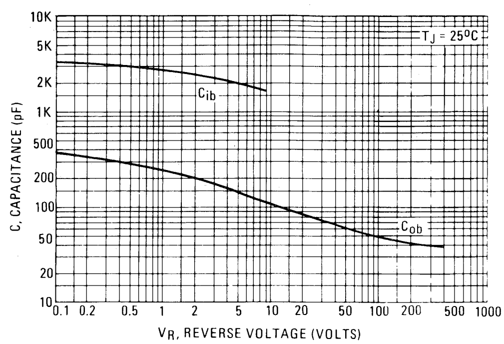

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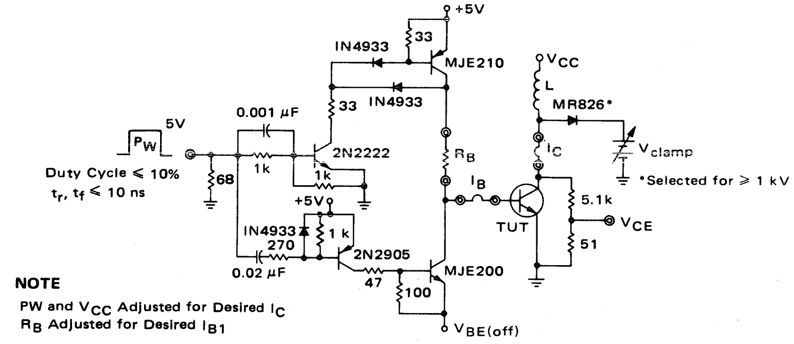
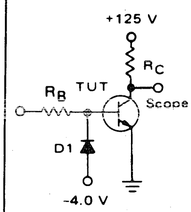
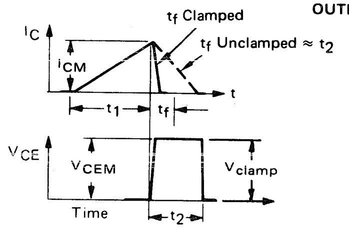
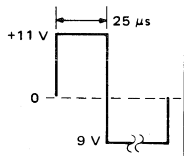
TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 μH/20A L_{coil} = 200 μH V_{CC} = 20 V V_{clamp} = 300 V	V_{CC} = 125 V R_C = 25 Ω D1 = 1N5820 or Equiv. R_B = 10Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}\,(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}\,(I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737A, AN-767, and AN-752.

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VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).

(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

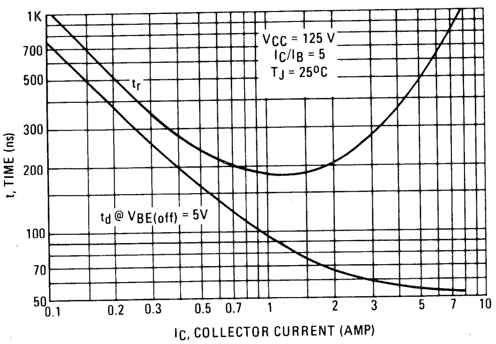


FIGURE 12 – TURN-OFF TIME

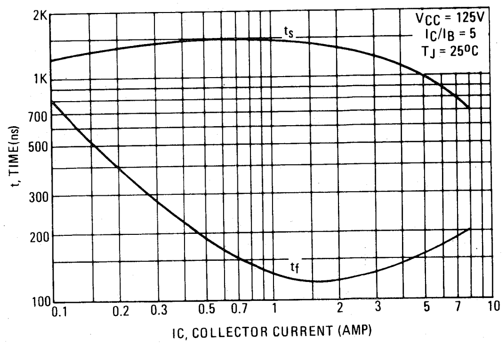


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

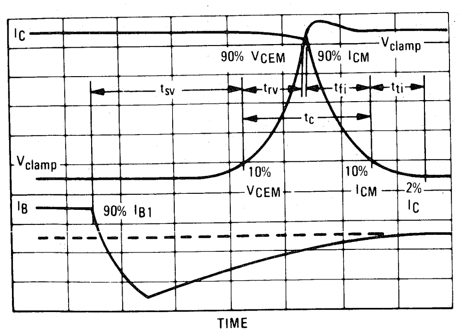


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS (at 300 V and 8A with I_{B1} = 1.6A and $V_{BE(off)}$ = 5 V)

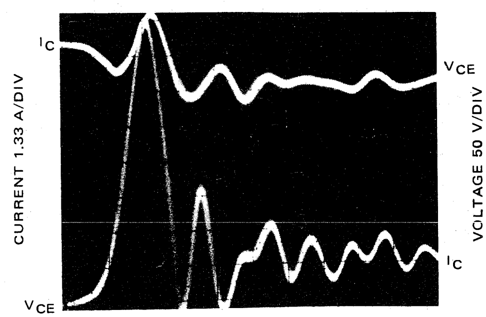
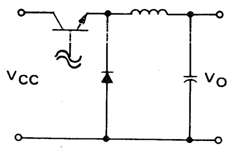
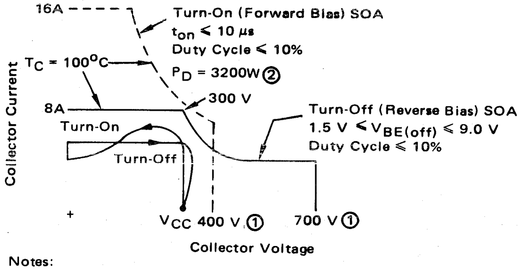


TABLE 2 — APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

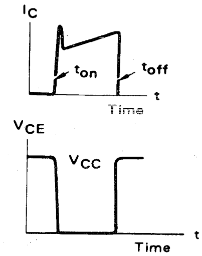
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	SERIES SWITCHING REGULATOR		
B	RINGING CHOKE INVERTER		
C	PUSH-PULL INVERTER/CONVERTER		
D	SOLENOID DRIVER		

A — SERIES SWITCHING REGULATOR

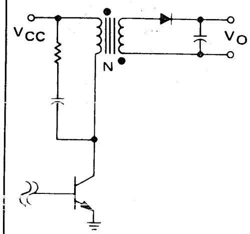


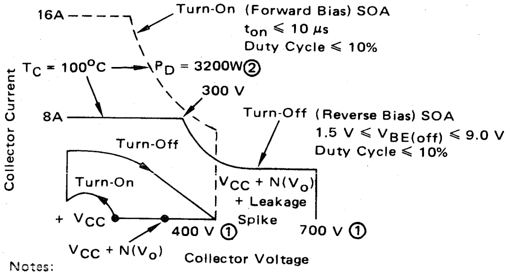


Notes:
① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13006 Ratings are 100 V Lower.
② See AN-569 for Pulse Power Derating Procedure.

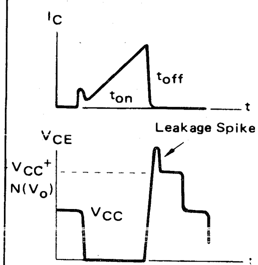


B — RINGING CHOKE INVERTER

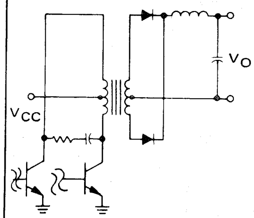


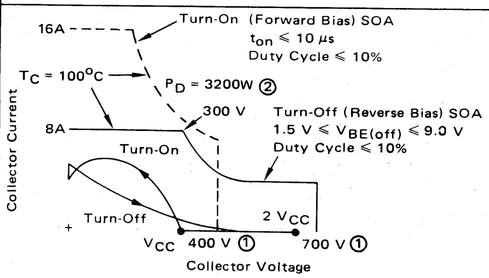


Notes:
① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown. MJE13006 Ratings Are 100 V Lower.
② See AN-569 For Pulse Power Derating Procedure

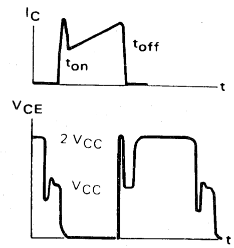


C — PUSH-PULL INVERTER/CONVERTER

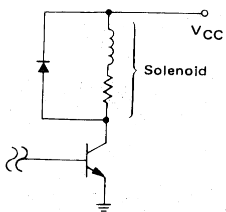


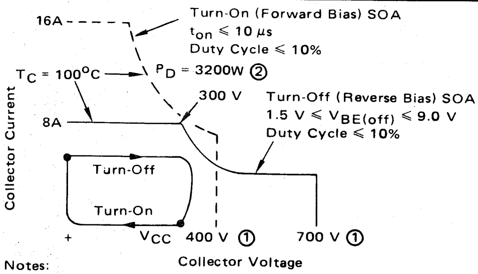


Notes:
① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower.
② See AN-569 for Pulse Power Derating Procedure.



D — SOLENOID DRIVER





Notes:
① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower.
② See AN-569 for Pulse Power Derating Procedure.

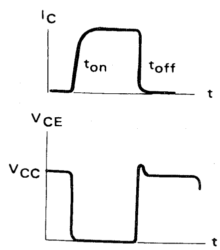


TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25	730	115	100	110	200
	100	1000	150	100	150	250
5	25	600	60	23	4	85
	100	860	84	50	10	136
8	25	650	25	26	4	42
	100	880	52	80	20	160

NOTE: All Data recorded in the inductive Switching Circuit in Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
t_{fi} = Current Fall Time, 90–10% I_{CM}
t_{ti} = Current Tail, 10–2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

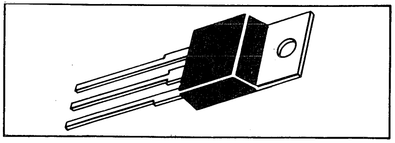
3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE13008
MJE13009

Designer's Data Sheet

12 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
100 WATTS



SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE13008 and MJE13009 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflectioncircuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 12 Amp, 25 and 100°C . . . t_c @ 8 A, 100°C is 120 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

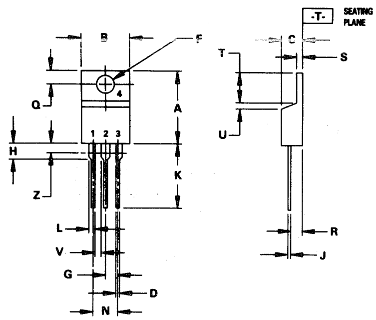
MAXIMUM RATINGS

Rating	Symbol	MJE13008	MJE13009	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	12 24		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6 12		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	18 36		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 800		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13008	$V_{CEO(sus)}$	300	–	–	Vdc
MJE13009		400	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased	–	See Figure 2			
***ON CHARACTERISTICS**					
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)	h_{FE}	8	–	40	–
(I_C = 8 Adc, V_{CE} = 5 Vdc)		6	–	30	
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1Adc)	$V_{CE(sat)}$	–	–	1	Vdc
(I_C = 8 Adc, I_B = 1.6 Adc)		–	–	1.5	
(I_C = 12 Adc, I_B = 3 Adc)		–	–	3	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		–	–	2	
Base-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc)	$V_{BE(sat)}$	–	–	1.2	Vdc
(I_C = 8 Adc, I_B = 1.6 Adc)		–	–	1.6	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		–	–	1.5	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	–	–	MHz
Output Capacitance (V_{CB} · 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	180	–	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 125 Vdc, I_C = 8 A,	t_d	–	0.06	0.1	μs
Rise Time I_{B1} = I_{B2} = 1.6 A, t_p = 25 μs,	t_r	–	0.45	1	μs
Storage Time Duty Cycle ≤ 1%)	t_s	–	1.3	3	μs
Fall Time	t_f	–	0.2	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time (I_C = 8 A, V_{clamp} = 300 Vdc,	t_{sv}	–	0.92	2.3	μs
Crossover Time I_{B1} = 1.6 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.12	0.7	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

3

FIGURE 1 — FORWARD BIAS SAFE OPERATING AREA

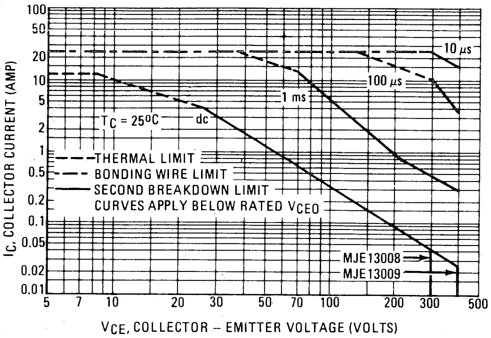
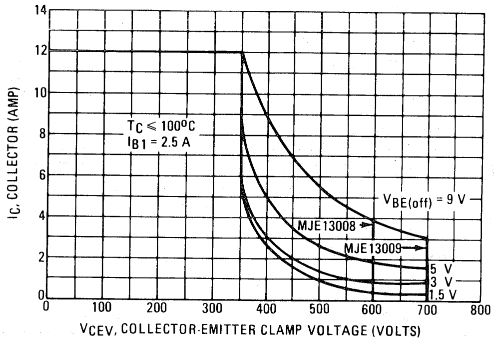
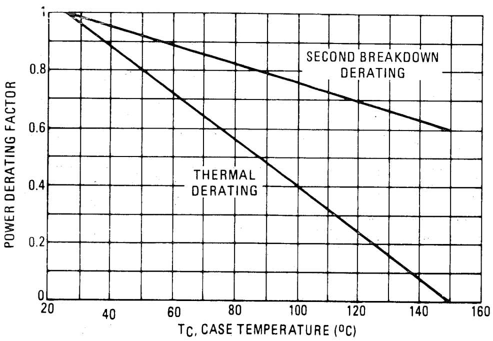


FIGURE 2 — REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 — FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^\circ C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 — TYPICAL THERMAL RESPONSE $[Z_{\theta JC}(t)]$

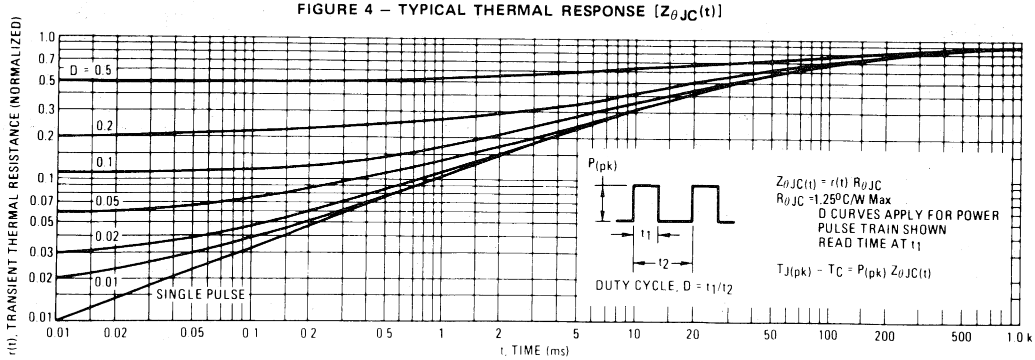


FIGURE 5 – DC CURRENT GAIN

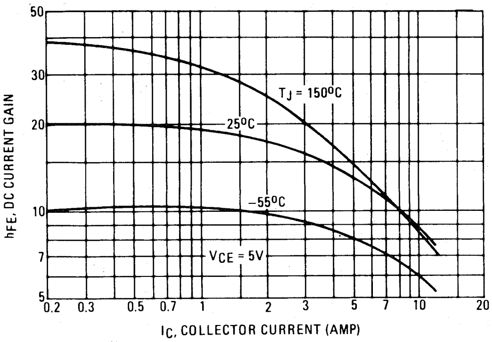


FIGURE 6 – COLLECTOR SATURATION REGION

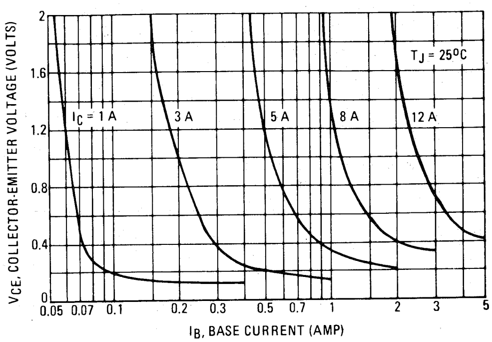


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE

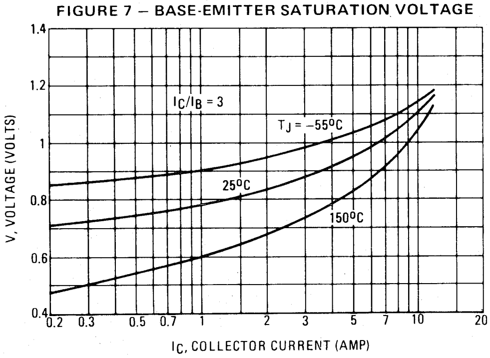


FIGURE 8 – COLLECTOR-EMITTER SATURATION VOLTAGE

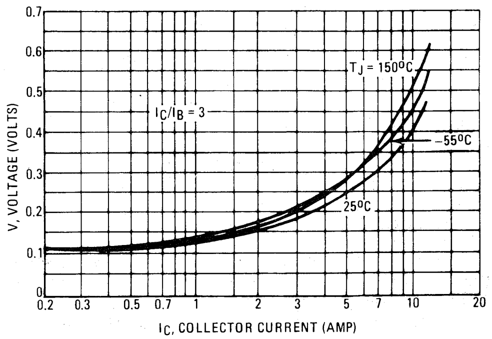


FIGURE 9 – COLLECTOR CUTOFF REGION

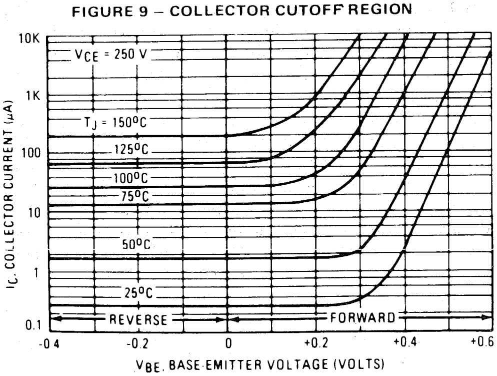


FIGURE 10 – CAPACITANCE

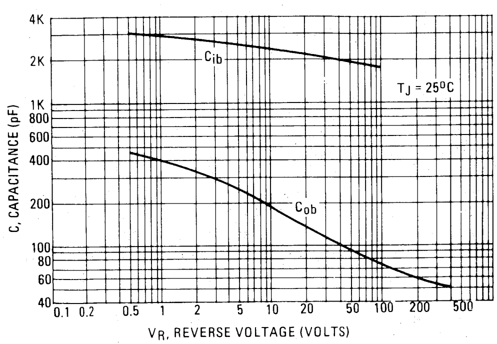
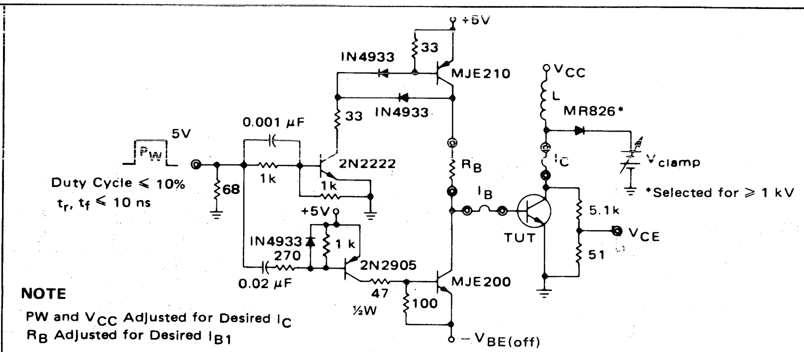
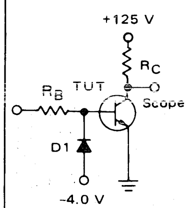
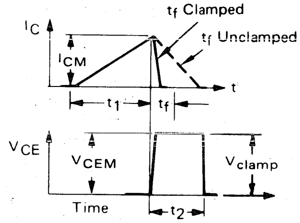
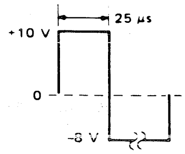


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 μH/20A L_{coil} = 200 μH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 15 Ω D1 = 1N5820 or Equiv R_B = 5.6 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes An-719, AN-737A, AN-752, AN-767.

3

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.
(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).
(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 8 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

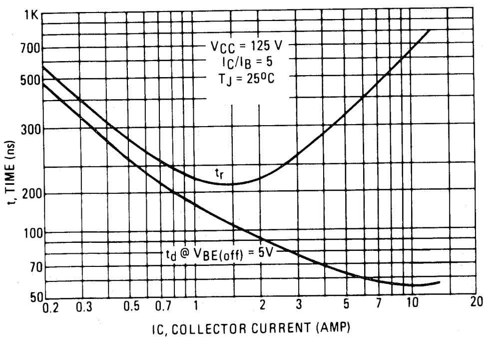


FIGURE 12 – TURN-OFF TIME

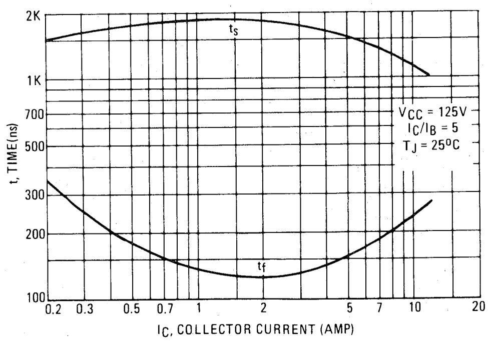


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

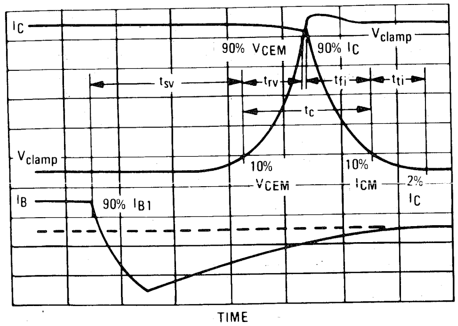


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS (at 300 V and 12 A with I_{B1} = 2.4 A and $V_{BE(off)}$ = 5 V)

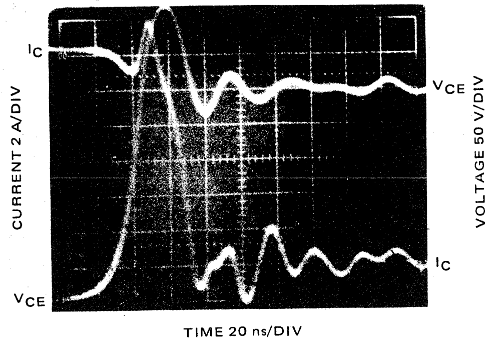
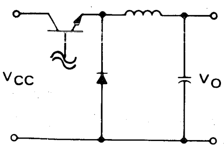
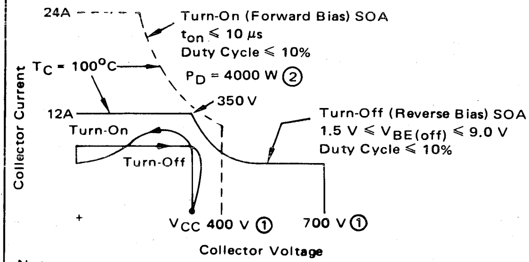


TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

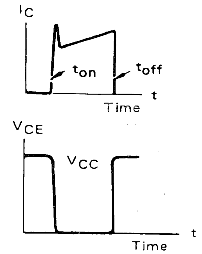
CIRCUIT | LOAD LINE DIAGRAMS | TIME DIAGRAMS

A — SERIES SWITCHING REGULATOR

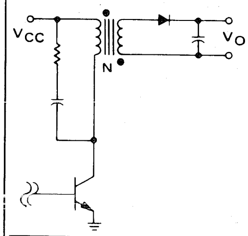


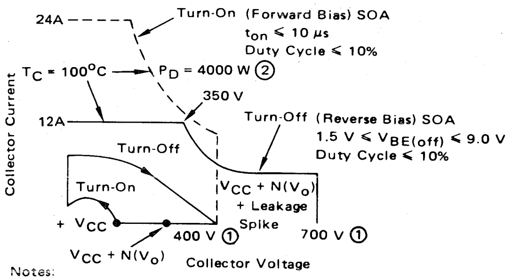


Notes:
① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower.
② See AN-569 for Pulse Power Derating Procedure.

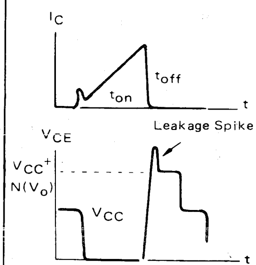


B — RINGING CHOKE INVERTER

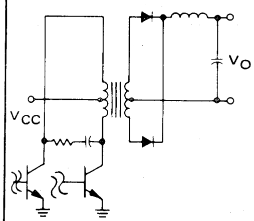


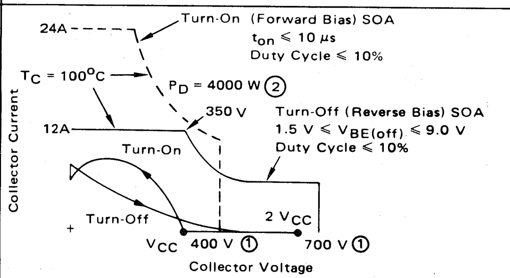


Notes:
① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower.
② See AN-569 For Pulse Power Derating Procedure

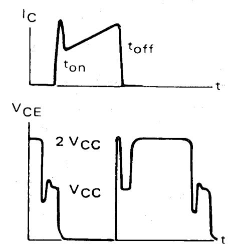


C — PUSH-PULL INVERTER/CONVERTER

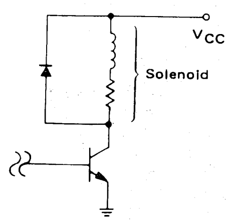


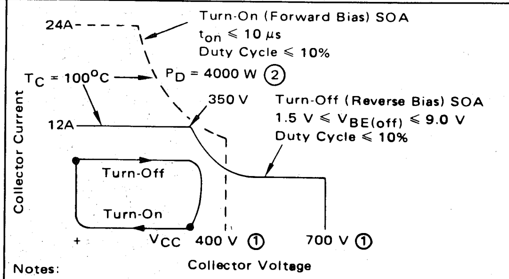


Notes:
① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower.
② See AN-569 for Pulse Power Derating Procedure.



D — SOLENOID DRIVER





Notes:
① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower.
② See AN-569 for Pulse Power Derating Procedure.

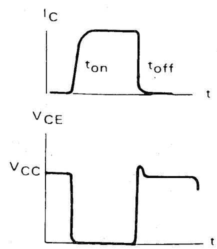


TABLE 3 — TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25	770	100	150	200	240
	100	1000	230	160	200	320
5	25	630	72	26	10	100
	100	820	100	55	30	180
8	25	720	55	27	2	77
	100	920	70	50	8	120
12	25	640	20	17	2	41
	100	800	32	24	4	54

NOTE: All Data recorded in the Inductive Switching Circuit In Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
t_{fi} = Current Fall Time, 90–10% I_{CM}
t_{ti} = Current Tail, 10–2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c)\, f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

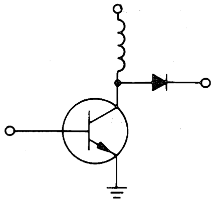
MJE13070
MJE13071

Designer's Data Sheet

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The MJE13070 and MJE13071 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
  100 ns Inductive Fall Time @ 25°C (Typ)
  150 ns Inductive Crossover Time @ 25°C (Typ)
  400 ns Inductive Storage Time @ 25°C (Typ)

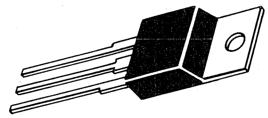
Operating Temperature Range −65 to +150°C

100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents

5 AMPERE

NPN SILICON POWER TRANSISTORS

400 AND 450 VOLTS
80 WATTS



Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

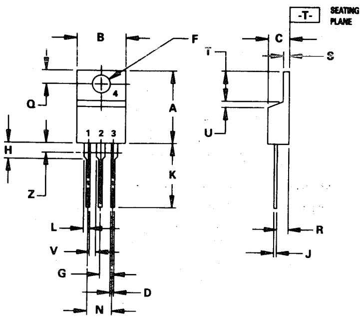
MAXIMUM RATINGS

Rating	Symbol	MJE13070	MJE13071	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	750	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 8.0		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.0 4.0		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	80 32 0.64		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJE13070	$V_{CEO(sus)}$	400	—	—	Vdc
MJE13071		450	—	—	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	—	0.5	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)	$V_{CE(sat)}$	—	—	1.0	Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)		—	—	3.0	
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		—	—	2.0	
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	250	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time — (V_{CC} = 250 Vdc, I_C = 3.0 Adc, I_{B1} = 0.4 Adc, t_p = 30 μs, Duty Cycle ≤2%, $V_{BE(off)}$ = 5.0 Vdc)	t_d	—	0.03	0.05	μs
Rise Time	t_r	—	0.10	0.40	
Storage Time	t_s	—	0.40	1.50	
Fall Time	t_f	—	0.175	0.50	
Inductive Load, Clamped (Table 1)					
Storage Time — ($I_{C(pk)}$ = 3.0 A, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V) (T_J = 100°C)	t_{sv}	—	0.70	2.0	μs
Crossover Time (T_J = 100°C)	t_c	—	0.28	0.50	
Fall Time (T_J = 100°C)	t_{fi}	—	0.15	0.30	
Storage Time (T_J = 25°C)	t_{sv}	—	0.40	—	
Crossover Time (T_J = 25°C)	t_c	—	0.15	—	
Fall Time (T_J = 25°C)	t_{fi}	—	0.10	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$\beta_f = \frac{I_C}{I_B}$

3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

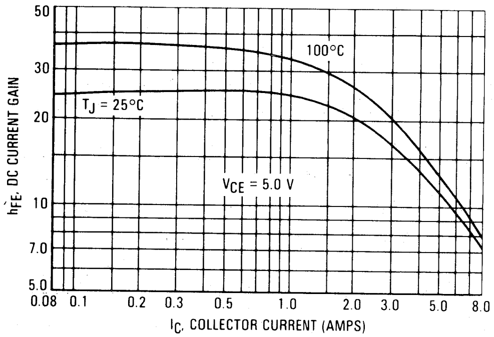


FIGURE 2 — COLLECTOR SATURATION REGION

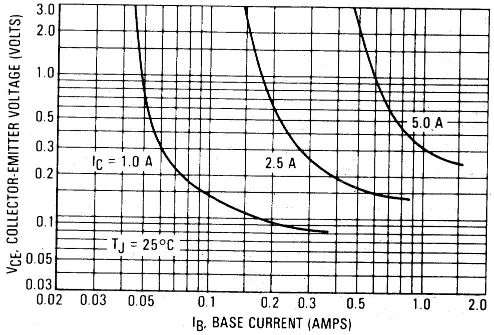


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

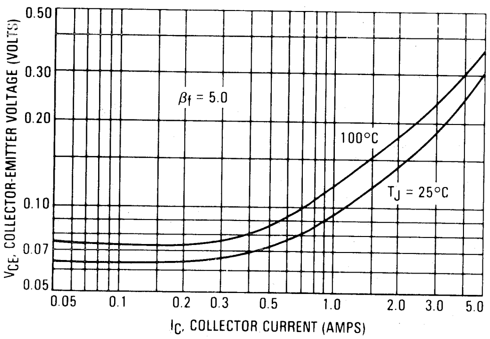


FIGURE 4 — BASE-EMITTER VOLTAGE

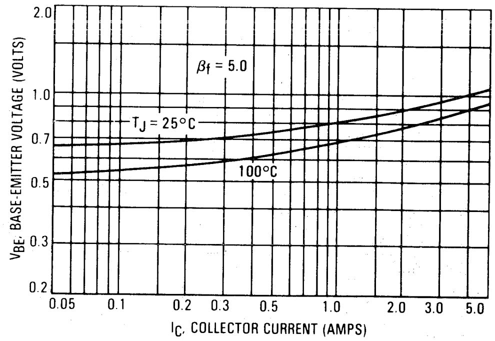


FIGURE 5 — COLLECTOR CUTOFF REGION

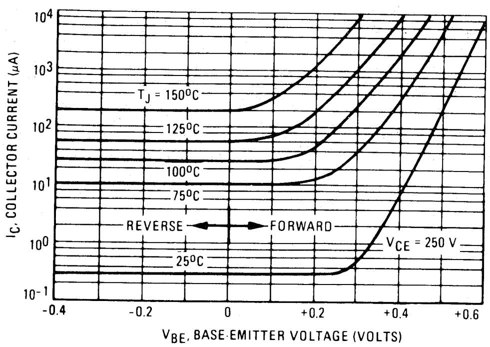


FIGURE 6 — CAPACITANCE

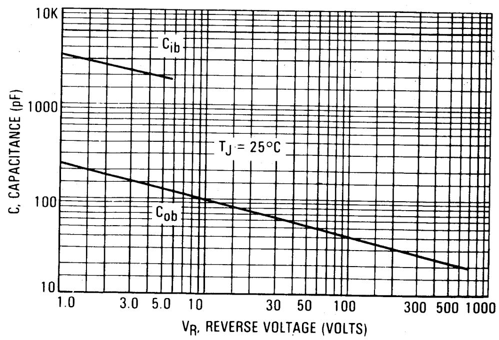


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TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

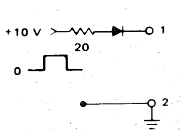
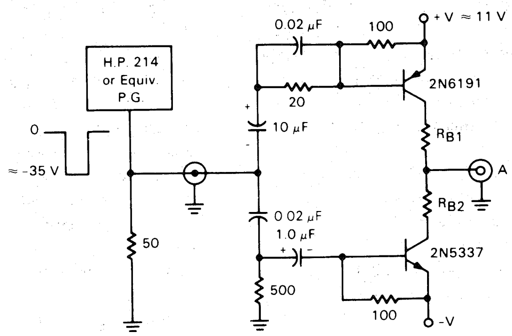
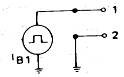
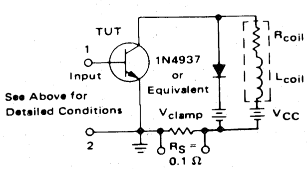
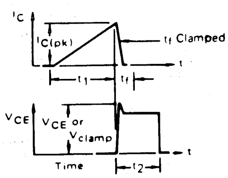
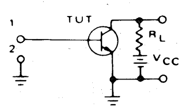
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 Adjust R_{B1} to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_{B1} adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

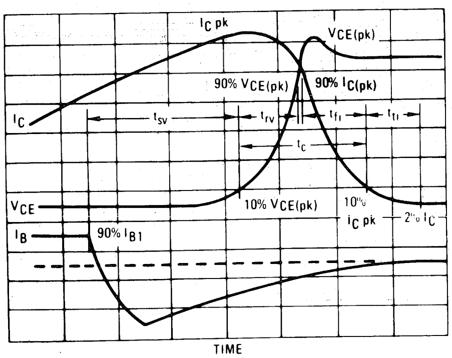
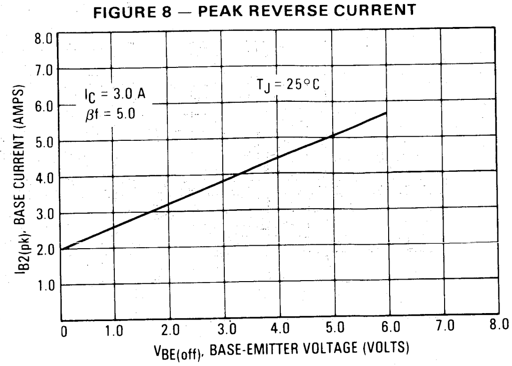


FIGURE 8 — PEAK REVERSE CURRENT



3

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\, V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

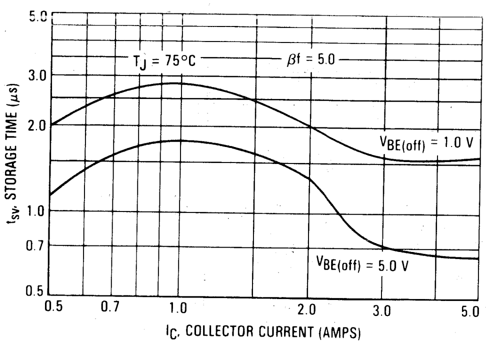


FIGURE 10 — CROSSOVER AND FALL TIMES

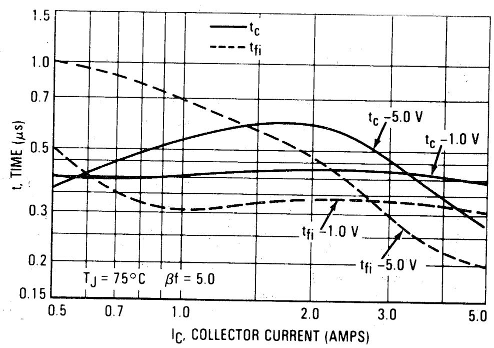


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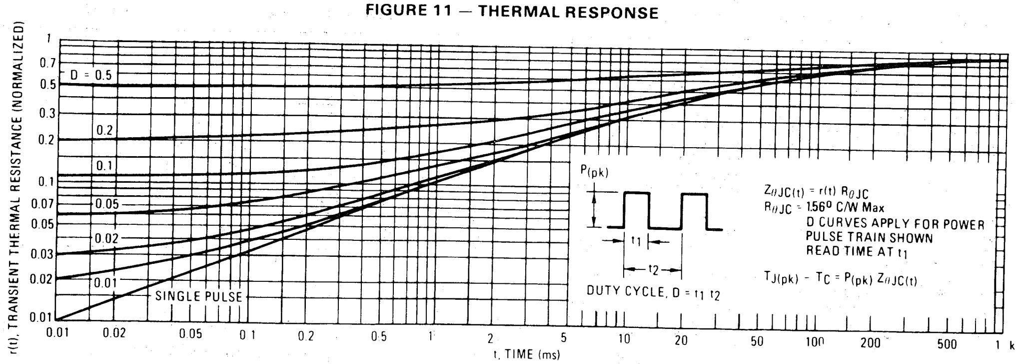
FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

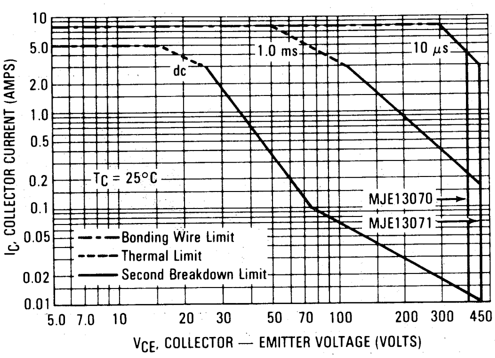
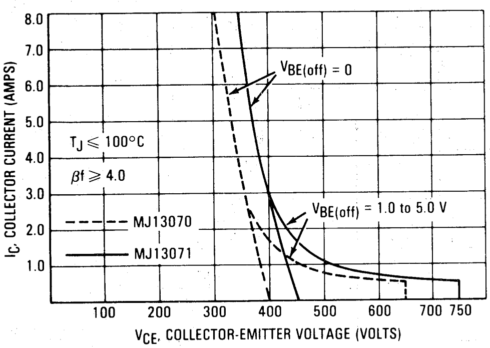


FIGURE 13 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

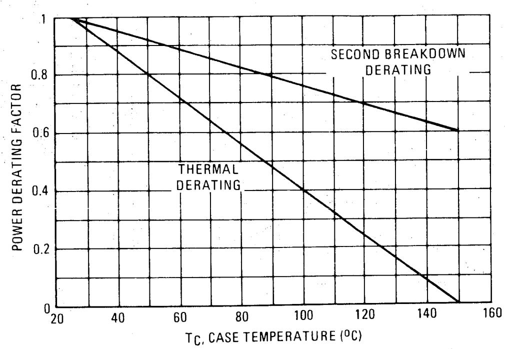
The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 14 — POWER DERATING



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
MJE15028	**MJE15029**
MJE15030	**MJE15031**

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

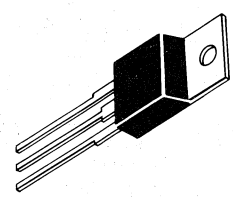
. . . designed for use as high-frequency drivers in audio amplifiers.

- DC Current Gain Specified to 4.0 Amperes
  h_{FE} = 40(Min) @ I_C = 3.0 Adc
  = 20(Min) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 120 Vdc (Min) — MJE15028, MJE15029
  = 150 Vdc (Min) — MJE15030, MJE15031
- High Current Gain — Bandwidth Product
  f_T = 30 MHz (Min) @ I_C = 500 mAdc
- TO-220AB Compact Package
- TO-66 Leadform Also Available

8 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

120–150 VOLTS
50 WATTS



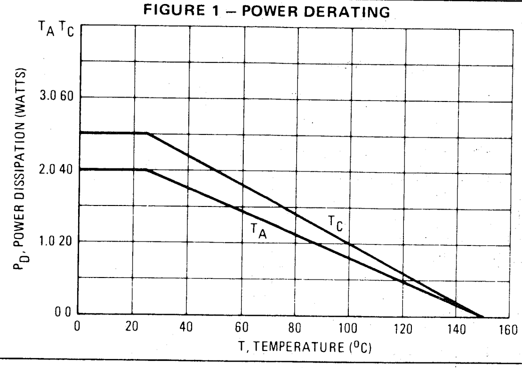
MAXIMUM RATINGS

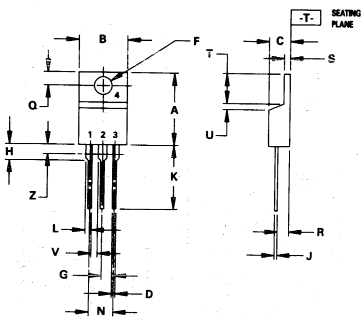
Rating	Symbol	MJE15028 MJE15029	MJE15030 MJE15031	Unit
Collector-Emitter Voltage	V_{CEO}	120	150	Vdc
Collector-Base Voltage	V_{CB}	120	150	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous — Peak	I_C	8.0 16		Adc
Base Current	I_B	2.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.40		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 — POWER DERATING





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	MJE15028, MJE15029	$V_{CEO(sus)}$	120	–	Vdc
	MJE15030, MJE15031		150	–	
Collector Cutoff Current (V_{CE} = 120 Vdc, I_B = 0)	MJE15028, MJE15029	I_{CEO}	–	0.1	mAdc
(V_{CE} = 150 Vdc, I_B = 0)	MJE15030, MJE15031		–	0.1	
Collector Cutoff Current (V_{CB} = 120 Vdc, I_E = 0)	MJE15028, MJE15029	I_{CBO}	–	10	μAdc
(V_{CB} = 150 Vdc, I_E = 0)	MJE15030, MJE15031		–	10	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	10	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	40	–	–
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)			20	–	
DC Current Gain Linearity		h_{FE}	Typ		
(V_{CE} From 2.0V to 20V, I_C From 0.1A to 3A)			2		
(NPN TO PNP)			3		
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	30	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 — THERMAL RESPONSE

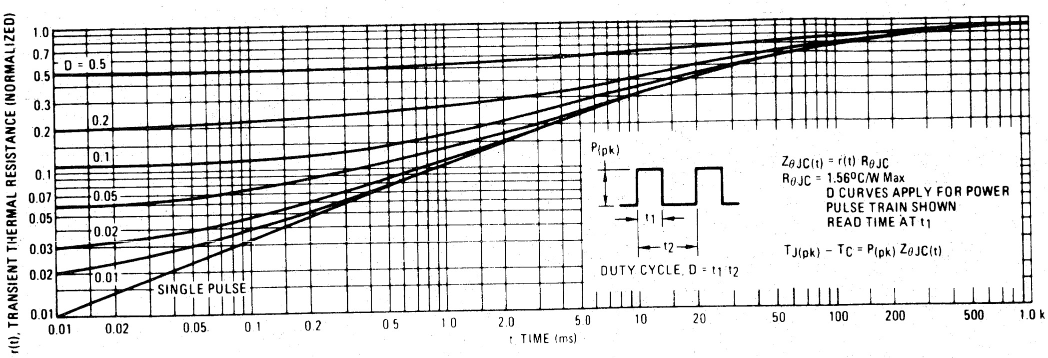


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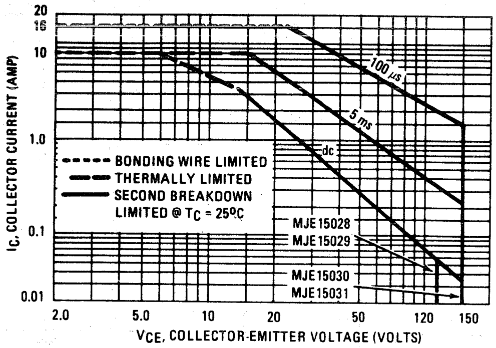
FIGURE 3 — FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150$°C. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 — REVERSE-BIAS SWITCHING SAFE OPERATING AREA

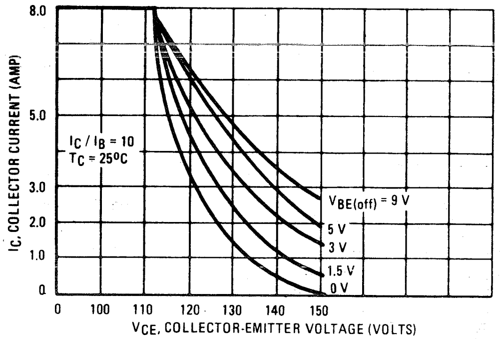


FIGURE 5 — CAPACITANCES

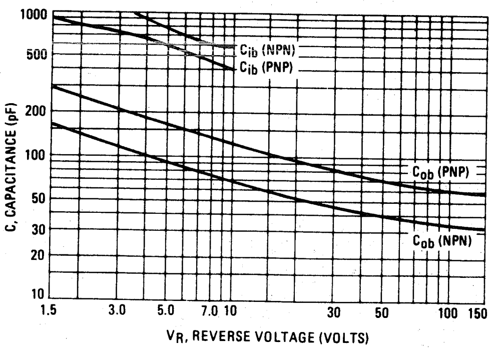


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FIGURE 6 — SMALL-SIGNAL CURRENT GAIN

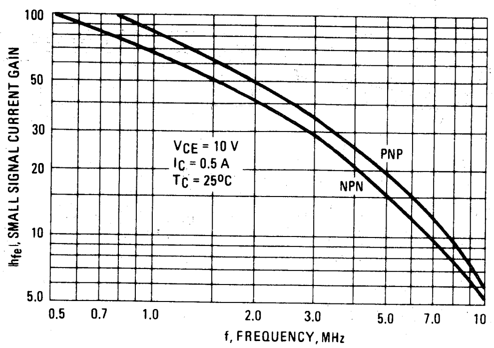
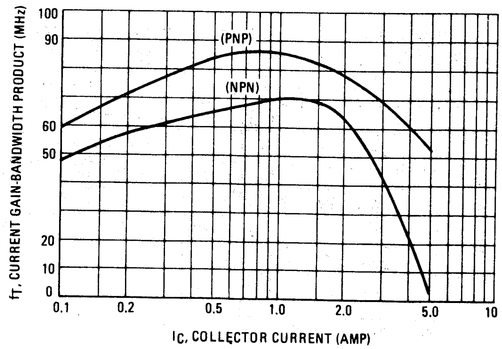


FIGURE 7 — CURRENT GAIN-BANDWIDTH PRODUCT



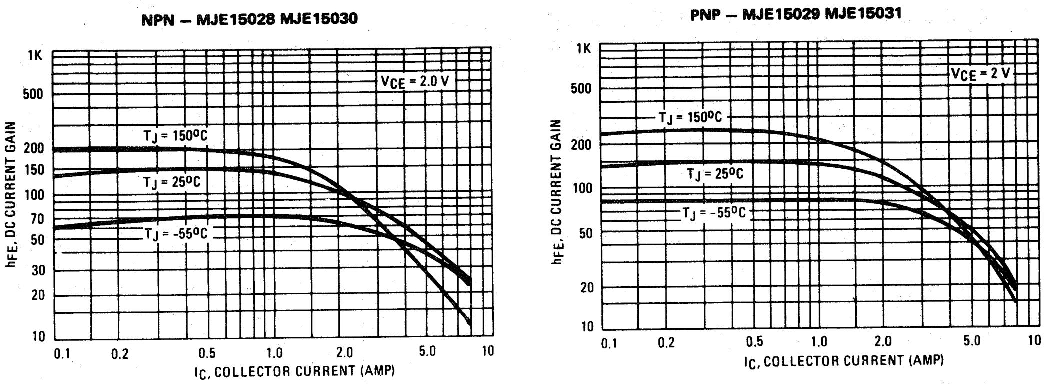


FIGURE 8 — DC CURRENT GAIN

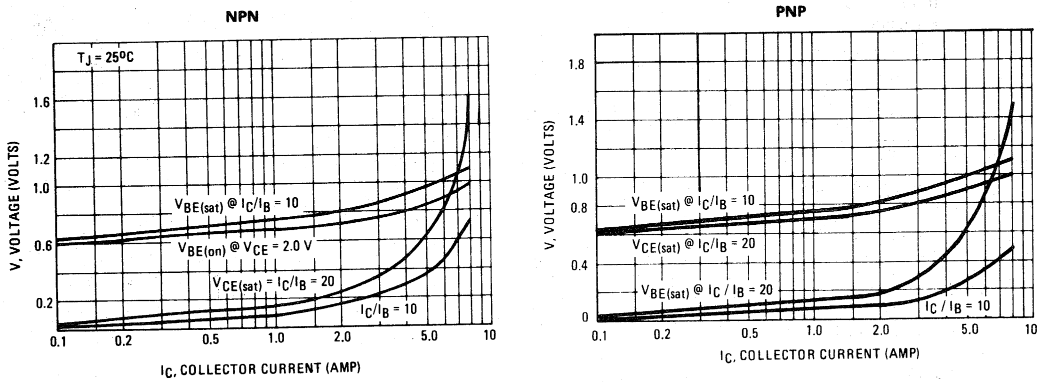


FIGURE 9 — "ON" VOLTAGE

FIGURE 10 — TURN-ON TIMES

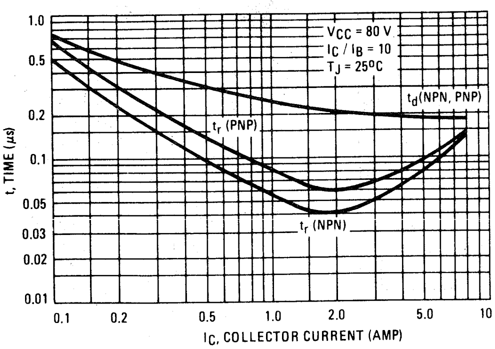
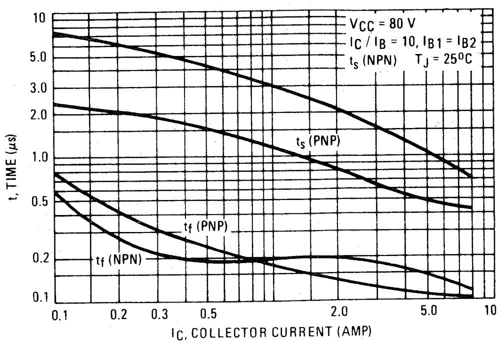


FIGURE 11 — TURN-OFF TIMES



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE16002
MJE16004
MJH16002
MJH16004

Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed switching of inductive circuits where fall time and RBSOA are critical. They are particularly well-suited for line-operated switchmode applications.

The MJE16004 and MJH16004 are high-gain versions of the MJE16002 and MJH16002 for applications where drive current is limited.

Typical Applications:

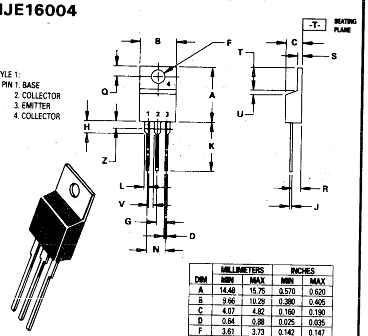
- Switching Regulators
- High Resolution Deflection Circuits
- Inverters
- Motor Drives
- Fast Switching Speeds
  50 ns Inductive Fall Time @ 75°C (Typ)
  70 ns Crossover Time @ 75°C (Typ)
- 100°C Performance Specified for:
  Reverse-Biased SOA
  Inductive Switching Times
  Saturation Voltages
  Leakage Currents

5.0 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
80 and 100 WATTS

MJE16002
MJE16004



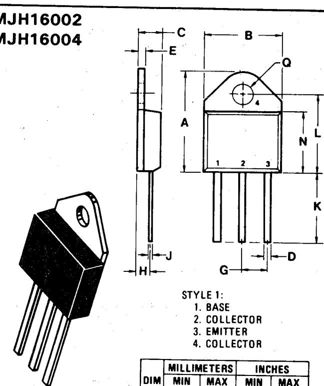
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MJH16002
MJH16004



STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MJE16002 MJE16004	MJH16002 MJH16004	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450		Vdc
Collector-Emitter Voltage	V_{CEV}	850		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 10		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4.0 8.0		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above $T_C = 25°C$	P_D	80 32 0.64	100 40 0.8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	1.25	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ⩽ 10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.25	
(V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	1.5	
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 17 or 18		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 19		
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 1.5 Adc, I_B = 0.2 Adc) MJE16002/MJH16002		—	—	1.0	
(I_C = 1.5 Adc, I_B = 0.15 Adc) MJE16004/MJH16004		—	—	1.0	
(I_C = 3.0 Adc, I_B = 0.4 Adc) MJE16002/MJH16002		—	—	2.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc) MJE16004/MJH16004		—	—	2.5	
(I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C) MJE16002/MJH16002		—	—	2.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc, T_C = 100°C) MJE16004/MJH16004		—	—	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 3.0 Adc, I_B = 0.4 Adc) MJE16002/MJH16002		—	—	1.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc) MJE16004/MJH16004		—	—	1.5	
(I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C) MJE16002/MJH16002		—	—	1.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc, T_C = 100°C) MJE16004/MJH16004		—	—	1.5	
DC Current Gain	h_{FE}				—
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc) MJE16002/MJH16002		5.0	—	—	
MJE16004/MJH16004		7.0	—	—	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	200	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1) MJE16002/MJH16002	Conditions		Symbol	Min	Typ	Max	Unit
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.4 Adc, PW = 30 µs, Duty Cycle ≤2.0%)	(I_{B2} = 0.8 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100	ns
Rise Time			t_r	—	100	300	
Storage Time			t_s	—	1000	3000	
Fall Time			t_f	—	60	300	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	400	—	
Fall Time			t_f	—	130	—	

Resistive Load (Table 1) MJE16004/MJH16004	Conditions		Symbol	Min	Typ	Max	Unit
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.3 Adc, PW = 30 µs, Duty Cycle ≤2.0%)	(I_{B2} = 0.6 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100	ns
Rise Time			t_r	—	130	300	
Storage Time			t_s	—	800	2700	
Fall Time			t_f	—	80	350	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	250	—	
Fall Time			t_f	—	60	—	

(1) Pulse Test: PW - 300 µs, Duty Cycle ≤2%.

$^*\beta_f = \frac{I_C}{I_{B1}}$

3

SWITCHING CHARACTERISTICS (continued)

Characteristics			Symbol	Min	Typ	Max	Unit
Inductive Load (Table 2) MJE16002/MJH16002							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	500	1600	ns
Fall Time			t_{fi}	—	100	200	
Crossover Time			t_c	—	120	250	
Storage Time		(T_J = 150°C)	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	
Inductive Load (Table 2) MJE16004/MJH16004							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.3 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	400	1300	ns
Fall Time			t_{fi}	—	80	150	
Crossover Time			t_c	—	90	200	
Storage Time		(T_J = 150°C)	t_{sv}	—	450	—	
Fall Time			t_{fi}	—	100	—	
Crossover Time			t_c	—	110	—	

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤2%.

$^*\beta_f = \frac{I_C}{I_{B1}}$

FIGURE 1 — DC CURRENT GAIN

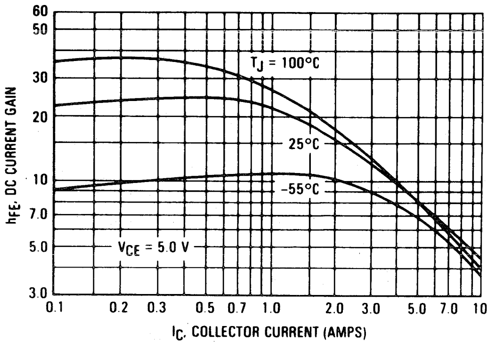


FIGURE 2 — COLLECTOR SATURATION REGION

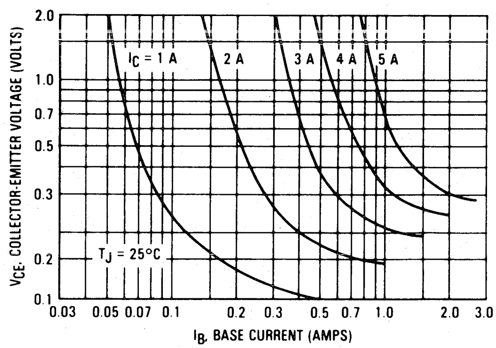


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

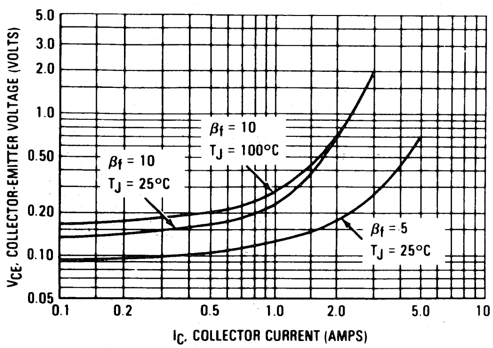
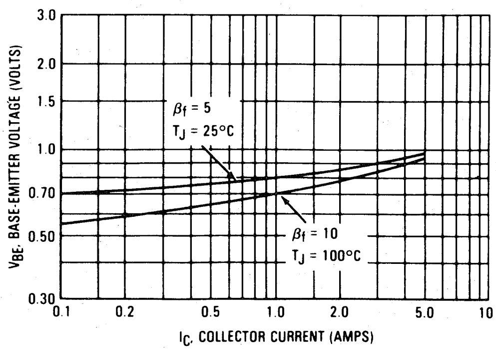


FIGURE 4 — BASE-EMITTER VOLTAGE



TYPICAL STATIC CHARACTERISTICS (continued)

FIGURE 5 — COLLECTOR CUTOFF REGION

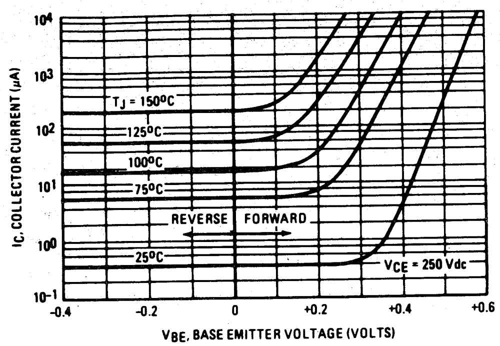
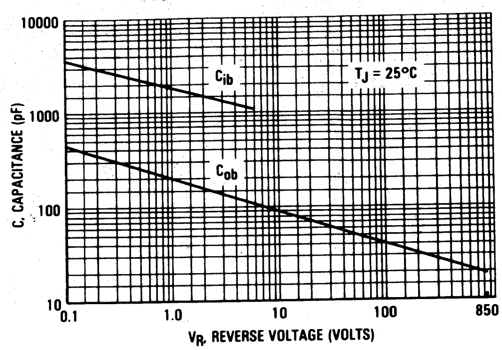


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

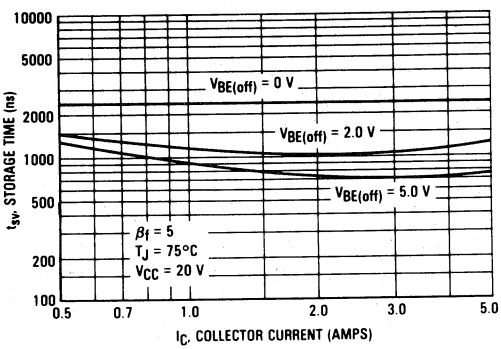


FIGURE 8 — STORAGE TIME

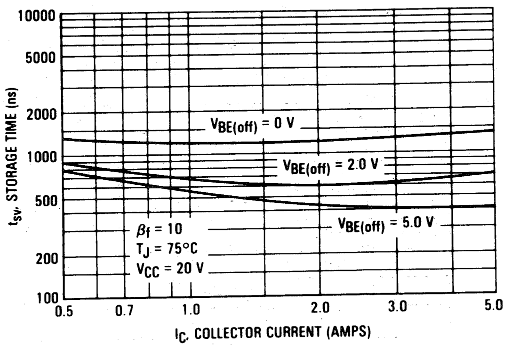


FIGURE 9 — COLLECTOR CURRENT FALL TIME

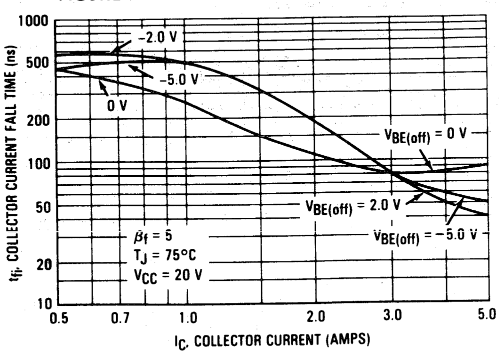
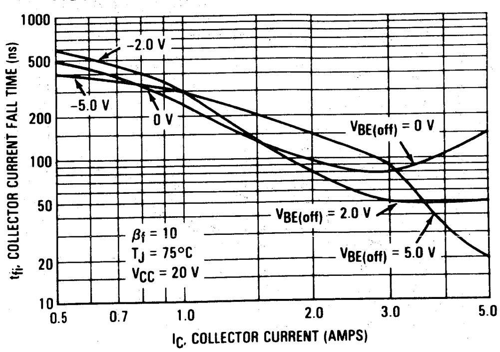


FIGURE 10 — COLLECTOR CURRENT FALL TIME



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TYPICAL DYNAMIC CHARACTERISTICS (continued)

FIGURE 11 — CROSSOVER TIME

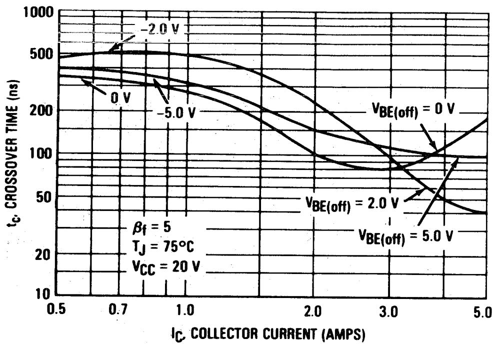
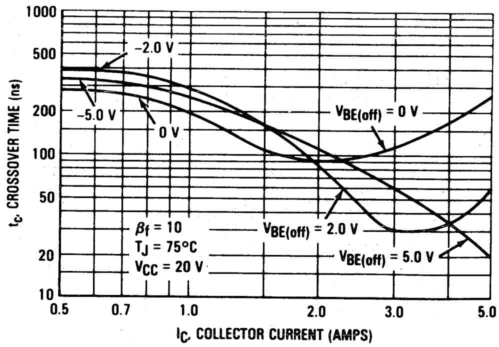


FIGURE 12 — CROSSOVER TIME



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

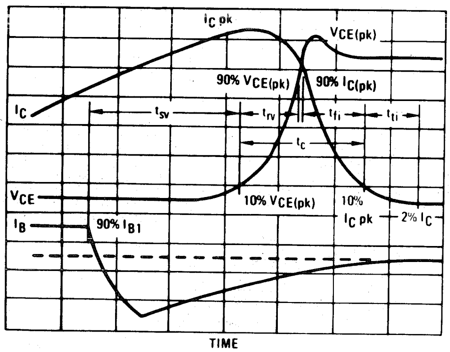


FIGURE 14 — PEAK REVERSE BASE CURRENT

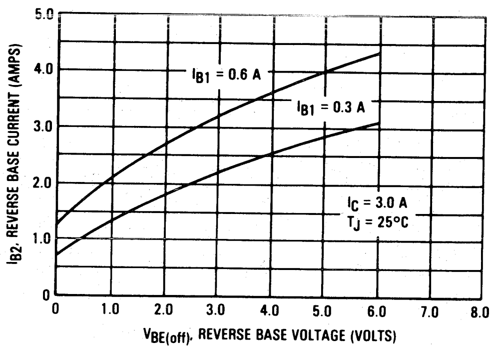
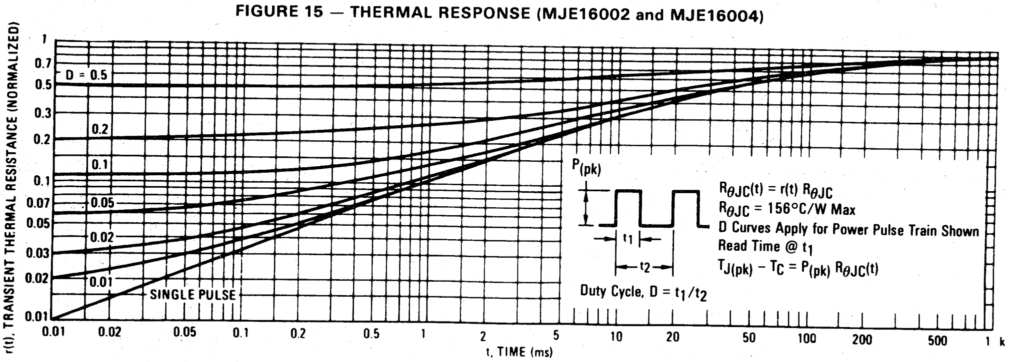
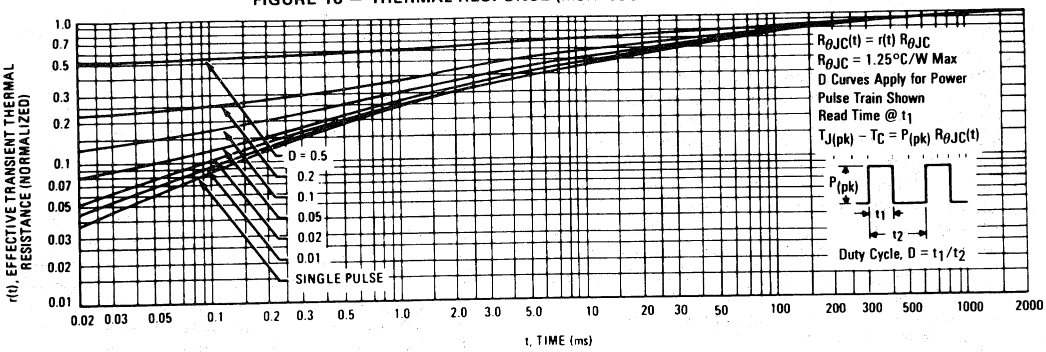


FIGURE 15 — THERMAL RESPONSE (MJE16002 and MJE16004)



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 16 — THERMAL RESPONSE (MJH16002 and MJH16004)



SAFE OPERATING AREA INFORMATION

FIGURE 17 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (MJE16002 and MJE16004)

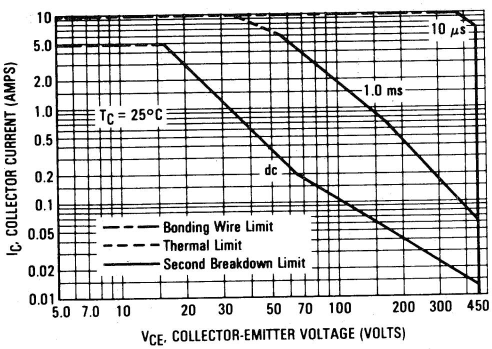


FIGURE 18 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (MJH16002 and MJH16004)

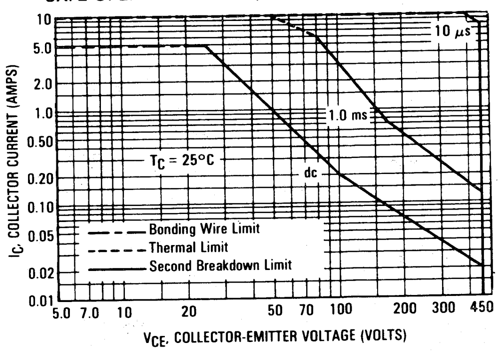


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FIGURE 19 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

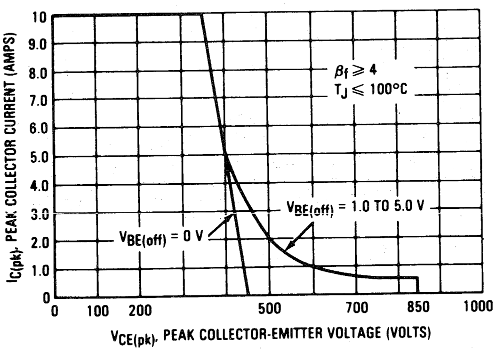
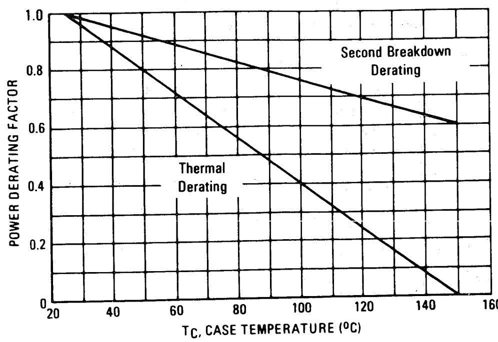


FIGURE 20 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

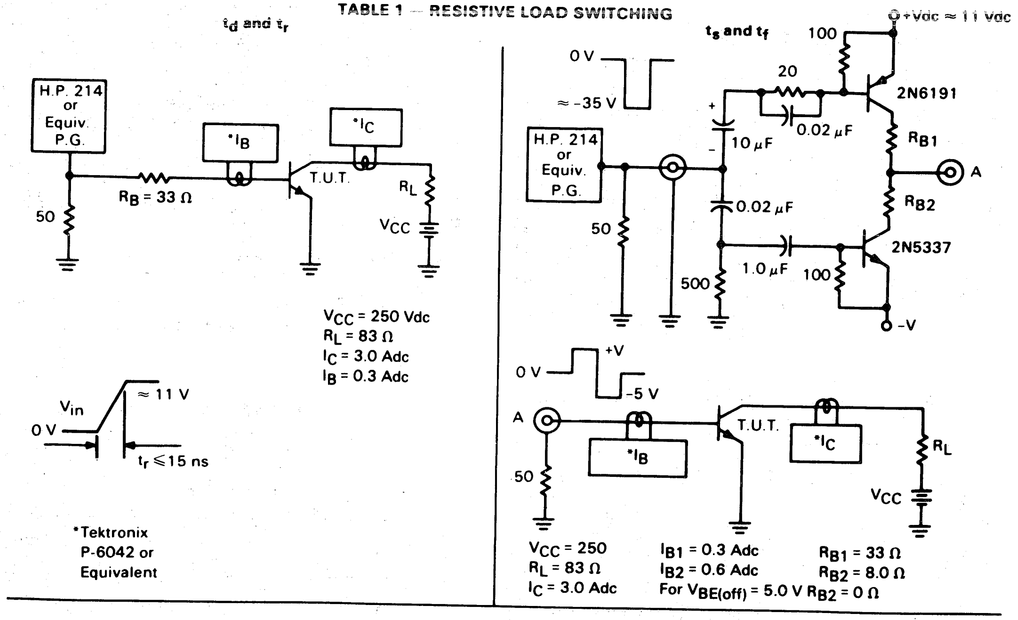
The data of Figures 17 and 18 are based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 17 and 18 may be found at any case temperature by using the appropriate curve on Figure 20.

$T_{J(pk)}$ may be calculated from the data in Figures 15 or 16. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

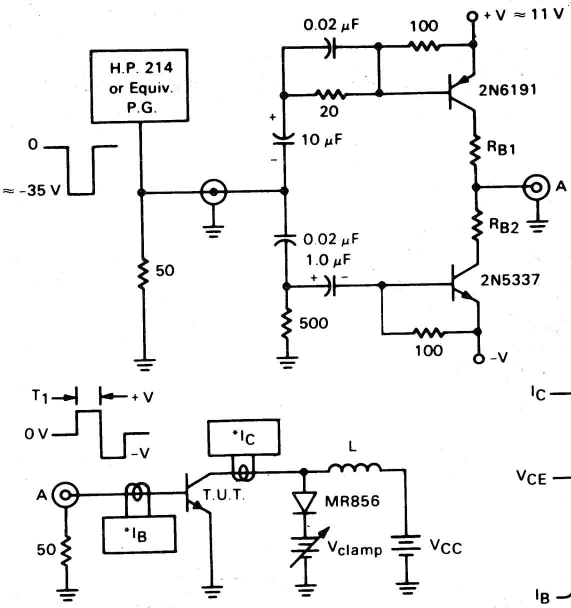
For inductive loads, high voltage and high current must be sustained simultaneousl during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable putting reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 19 gives the RBSOA characteristics.

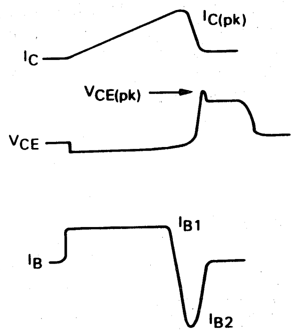
TABLE 1 — RESISTIVE LOAD SWITCHING



*Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING





$T_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

BV_{CEO}
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

*Tektronix P-6042 or Equivalent

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Scope - Tektronix 7403 or Equivalent

RBSOA
L = 200 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

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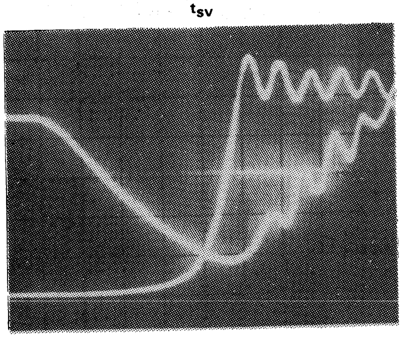
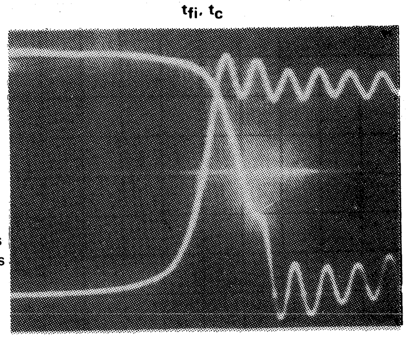
TYPICAL INDUCTIVE SWITCHING WAVEFORMS

t_{sv}



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.3 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 300 Volts
T_C = 25°C
Time Base = 20 ns/cm

t_{fi}, t_c



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.3 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 300 Volts
T_C = 25°C
Time Base = 20 ns/cm

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE16032
MJE16034
MJH16032
MJH16034

Designer's Data Sheet

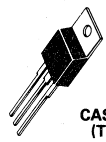
NPN Silicon Power Transistors

Switchmode III Series

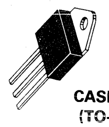
POWER TRANSISTORS
3 AMPERES
750 and 850 VOLTS
80 and 125 WATTS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  150 ns Inductive Fall Time: 25°C (Typ)
  150 ns Inductive Crossover Time: 25°C (Typ)
  500 ns Inductive Storage Time: 25°C (Typ)
- Operating Temperature Range: −65 to +150°C
- 100°C Performance Specified for:
  Reverse-Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents



CASE 221A-04
(TO-220AB)



CASE 340-01
(TO-218AC)

MAXIMUM RATINGS

Rating	Symbol	MJE16032 MJH16032	MJE16034 MJH16034	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	750	850	Vdc
Collector-Emitter Voltage	V_{CEV}	1500		Vdc
Emitter Base Voltage	V_{EB}	9		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	3 6		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	2 4		Adc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C
		MJE16032 MJE16034	MJH16032 MJH16034	
Total Power Dissipation @ T_C = +25°C @ T_C = +100°C Derate above 25°C	P_D	80 32 0.64	125 50 1	Watts W/°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0) MJE16032, MJH16032 / MJE16034, MJH16034	$V_{CEO(sus)}$	750 850	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	0.005 0.020	0.25 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	0.020	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	—	0.002	0.25	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 17			
ON CHARACTERISTICS(1)					
DC Current Gain (V_{CE} = 5 Vdc) I_C = 0.5 Adc / I_C = 3 Adc	h_{FE}	10 4	15 7	— —	— —
Collector-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.33 Adc) (I_C = 3 Adc, I_B = 1 Adc) (I_C = 1 Adc, I_B = 0.33 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	0.15 1 0.5	1 2.5 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.33 Adc) (I_C = 1 Adc, I_B = 0.33 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	0.8 0.7	1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	80	—	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(V_{CC} = 400 Vdc, I_C = 2 A I_{B1} = 333 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%)		t_d	—	0.06	0.2	μs
Rise Time			t_r	—	0.15	1	μs
Storage Time			t_s	—	1.5	2	μs
Fall Time			t_f	—	0.15	1.5	μs
Inductive Load, Clamped (Table 2)							
Storage Time	(I_C = 2 A, V_{clamp} = 400 Vdc, $V_{BE(off)}$ = 5 Vdc, I_{B1} = 333 mA)	T_C = 100°C	t_{sv}	—	0.5	1.5	μs
Crossover Time			t_c	—	0.2	1	μs
Storage Time		T_C = 25°C	t_{sv}	—	0.5	—	μs
Crossover Time			t_c	—	0.15	—	μs
Fall Time			t_{fi}	—	0.15	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL STATIC CHARACTERISTICS

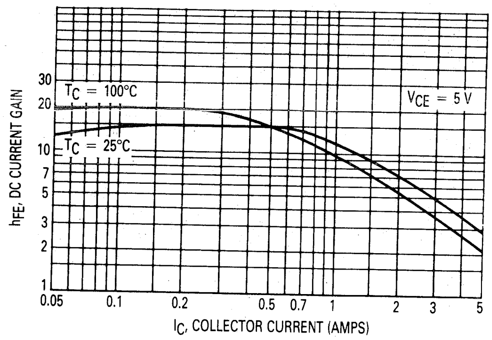


Figure 1. DC Current Gain

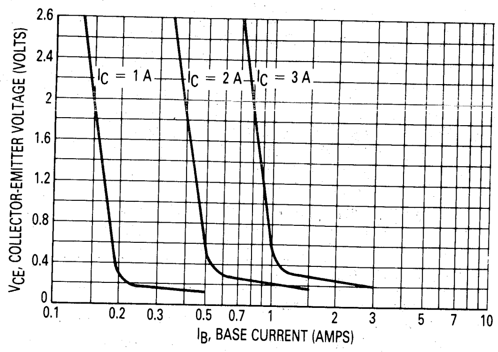


Figure 2. Collector Saturation Region

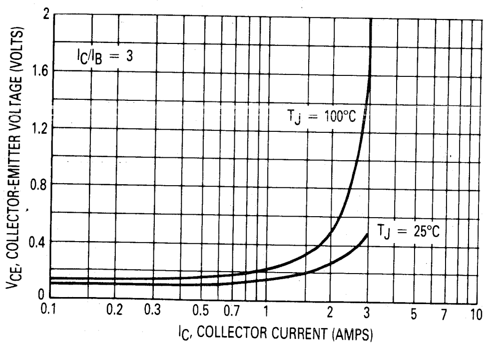


Figure 3. Collector-Emitter Saturation Voltage

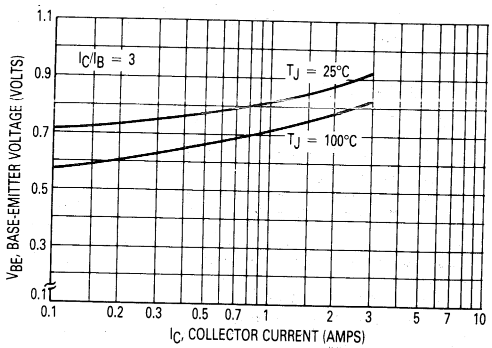


Figure 4. Base-Emitter Saturation Voltage

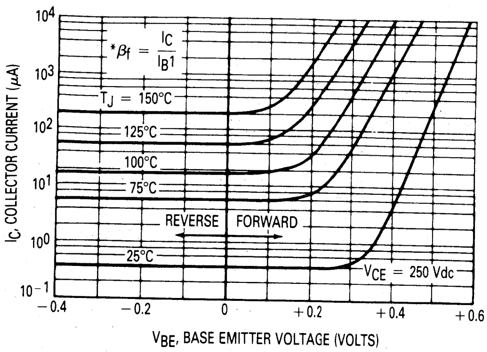


Figure 5. Collector Cutoff Region

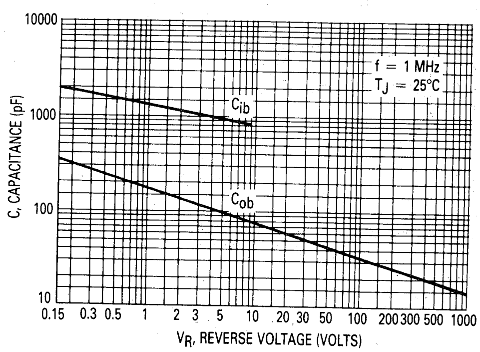


Figure 6. Capacitance Variation

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TYPICAL DYNAMIC CHARACTERISTICS

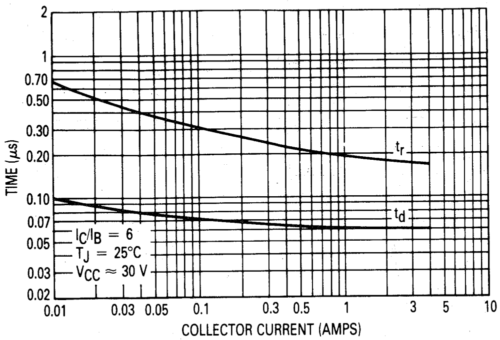


Figure 7. Resistive Turn-On Time

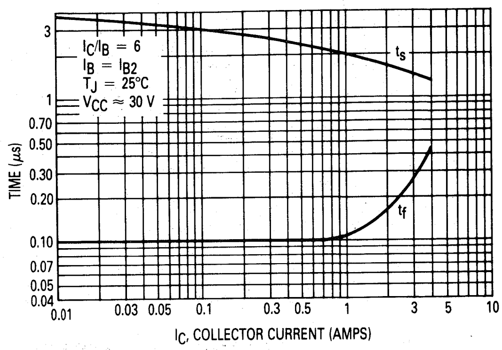


Figure 8. Resistive Turn-Off Time

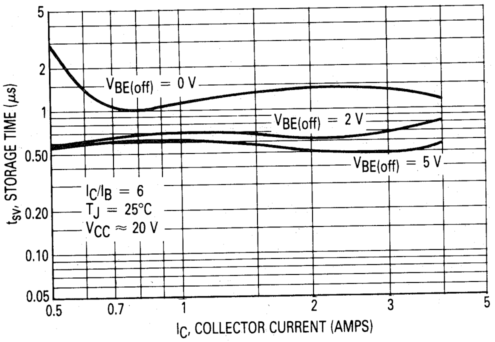


Figure 9. Inductive Storage Time
T_J = 25°C

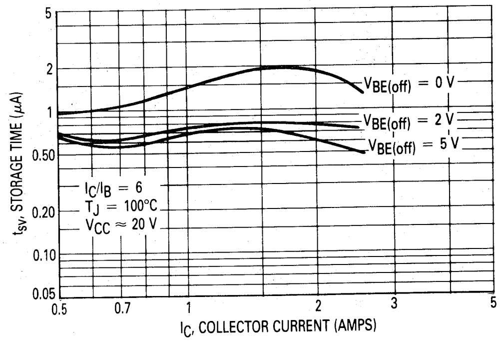


Figure 10. Inductive Storage Time
T_J = 100°C

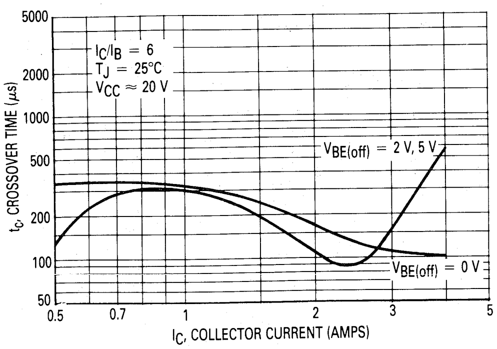


Figure 11. Inductive Crossover Time
T_J = 25°C

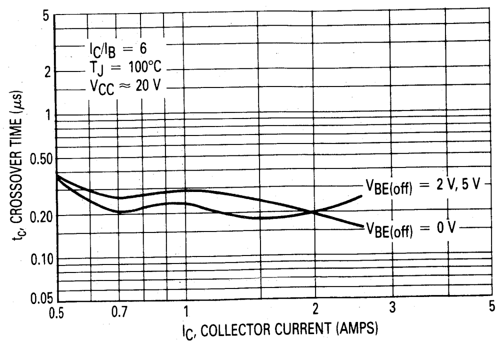


Figure 12. Inductive Crossover Time
T_J = 100°C

3

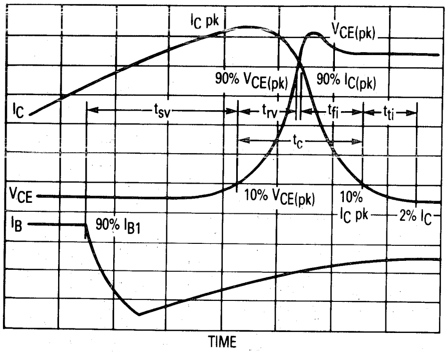


Figure 13. Inductive Switching Measurements

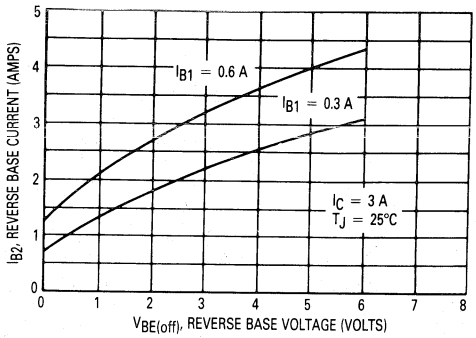
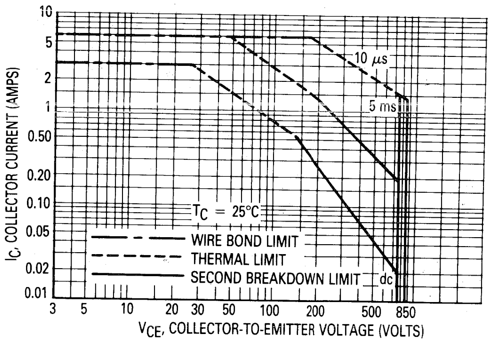
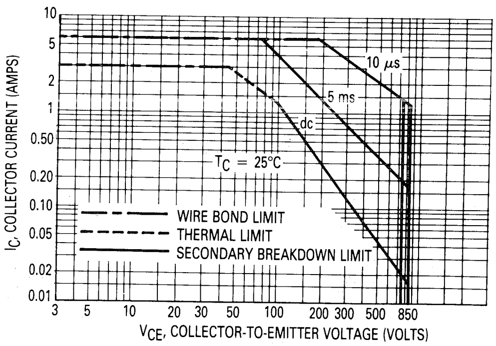


Figure 14. Peak Reverse Base Current

GUARANTEED SAFE OPERATING AREA LIMITS



a. MJE16032, MJE16034



b. MJH16032, MJH16034

Figure 15. Maximum Rated Forward Bias Safe Operating Area

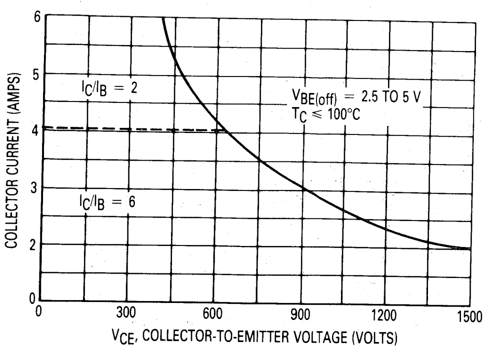


Figure 16. Maximum Rated Reverse Bias Safe Operating Area

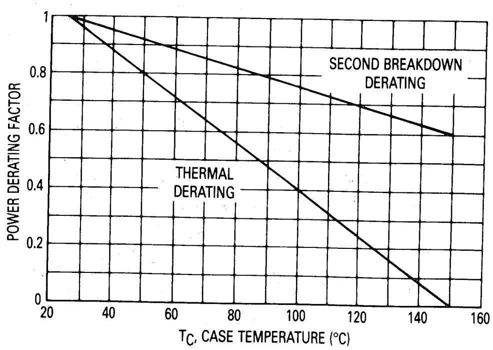


Figure 17. Power Derating

3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

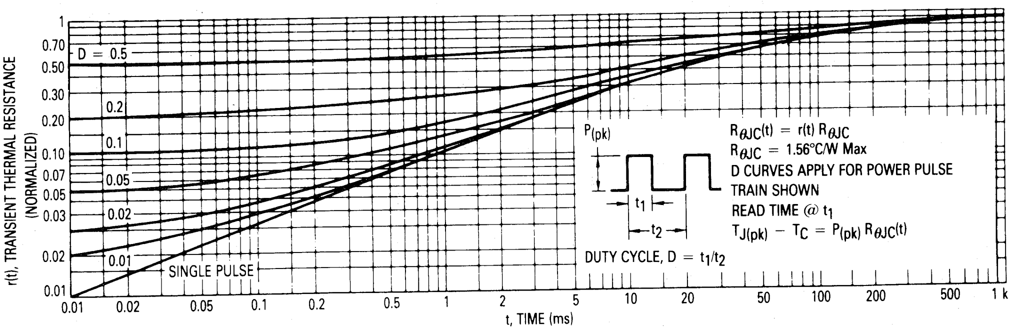
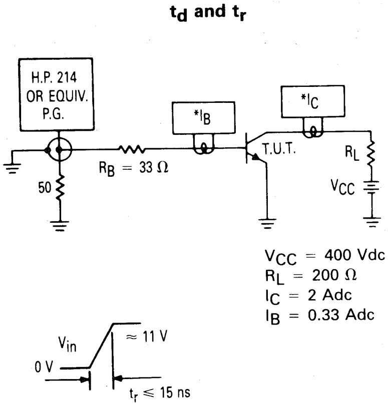


Figure 18. Thermal Response

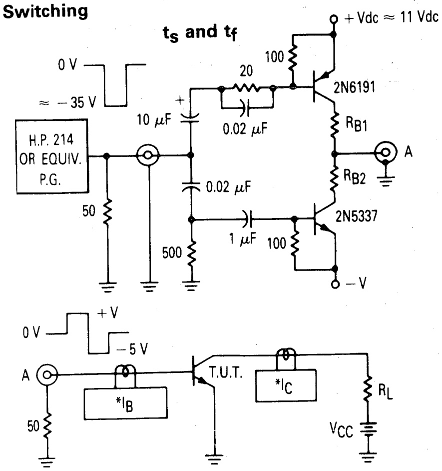
Table 1. Resistive Load Switching

t_d and t_r



*Tektronix AM503
P6302 or Equivalent

t_s and t_f

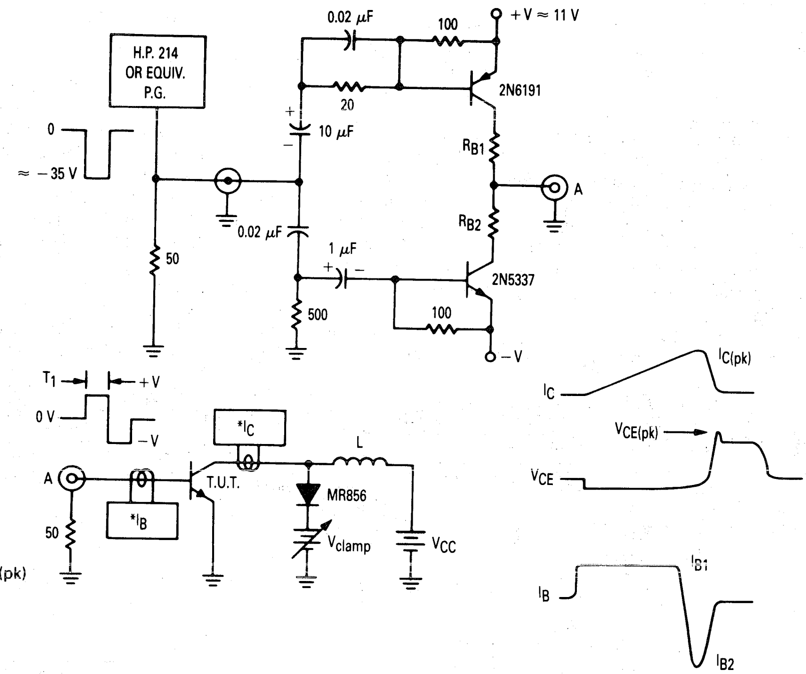


$V_{CC} = 400$ $I_{B1} = 0.3$ Adc, $R_{B1} = 33\ \Omega$
$R_L = 200\ \Omega$ For $V_{BEoff} = 5$ V, $R_{B2} = 0\ \Omega$
$I_C = 2$ Adc

Note: Adjust −V to obtain desired $V_{BE(off)}$ at point A.

3

Table 2. Inductive Load Switching



$T_1 \approx \frac{L_{coil}\ (I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
$L = 10$ mH
$R_{B2} = \infty$
$V_{CC} = 20$ Volts

*Tektronix
AM503
P6302 or Equivalent

Inductive Switching
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

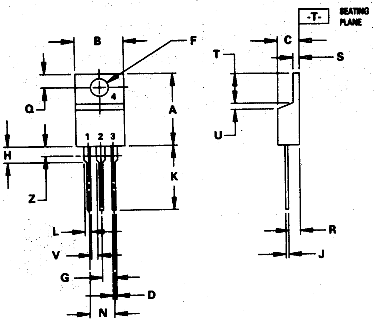
Scope — Tektronix
7403 or
Equivalent

RBSOA
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

3

OUTLINE DIMENSIONS

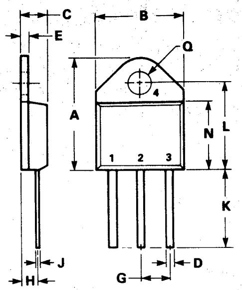


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
(TO-220AB)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
(TO-218AC)

3

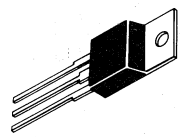
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE16080
MJE16081

Designer's Data Sheet

NPN Silicon Power Transistors
Switchmode III Series

POWER TRANSISTORS
8 AMPERES
400 and 450 VOLTS
80 WATTS



CASE 221A-04
(TO-220AB)

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  - 10 ns Inductive Fall Time − 100°C (Typ)
  - 80 ns Inductive Crossover Time − 100°C (Typ)
  - 900 ns Inductive Storage Time − 100°C (Typ)
- Operating Temperature Range − 65 to + 150°C
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

MAXIMUM RATINGS

Rating	Symbol	MJE16080	MJE16081	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	800	850	Vdc
Emitter Base Voltage	V_{EB}	9		Vdc
Collector Current — Continuous Peak(1)	I_C I_{CM}	8 16		Adc
Base Current — Continuous Peak(1)	I_B I_{BM}	4 8		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	80 32 0.64		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) MJE16080 (I_C = 100 mA, I_B = 0) MJE16081	$V_{CEO(sus)}$	400 450	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	0.020 —	0.25 2.5	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	—	0.05	50	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 13			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 14			
ON CHARACTERISTICS(1)					
DC Current Gain (V_{CE} = 5 Vdc) I_C = 1.0 Adc I_C = 8 Adc	h_{FE}	15 5	25 10	— —	— —
Collector-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.25 Adc) (I_C = 5 Adc, I_B = 0.625 Adc) (I_C = 8 Adc, I_B = 1.6 Adc) (I_C = 5 Adc, I_B = 0.625 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — — —	0.2 0.4 0.6 0.5	0.5 1.2 1.5 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.25 Adc) (I_C = 5 Adc, I_B = 0.625 Adc) (I_C = 5 Adc, I_B = 0.625 Adc, T_C = 100°C)	$V_{BE(sat)}$	— — —	0.9 1 1	1.2 1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	120	—	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 125 Vdc, I_C = 5 A, I_{B1} = I_{B2} = 0.625 Adc, t_p = 25 μs, Duty Cycle ≤ 2%)	t_d	—	0.07	0.15	μs
Rise Time	t_r	—	0.03	0.08	μs
Storage Time	t_s	—	0.5	2	μs
Fall Time	t_f	—	0.2	0.5	μs
Inductive Load, Clamped (Table 2)					
Storage Time					
Crossover Time					
Storage Time (I_C = 5 A, V_{clamp} = 350 Vdc, $V_{BE(off)}$ = 5 Vdc, I_{B1} = 0.625 Adc) T_C = 100°C	t_{sv}	—	0.90	2	μs
Crossover Time	t_c	—	0.08	0.20	μs
Fall Time	t_{fi}	—	0.01	0.10	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL STATIC CHARACTERISTICS

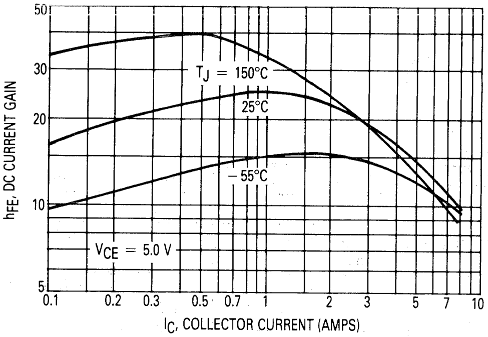


Figure 1. DC Current Gain

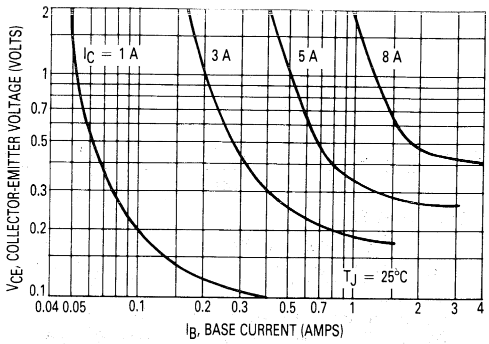


Figure 2. Collector Saturation Region

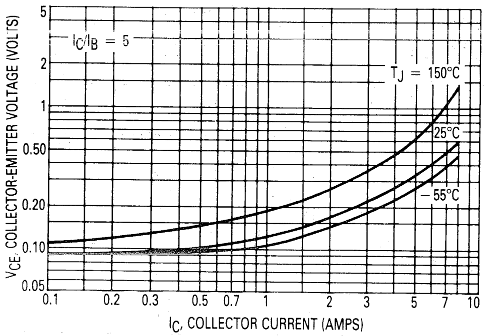


Figure 3. Collector-Emitter Saturation Voltage

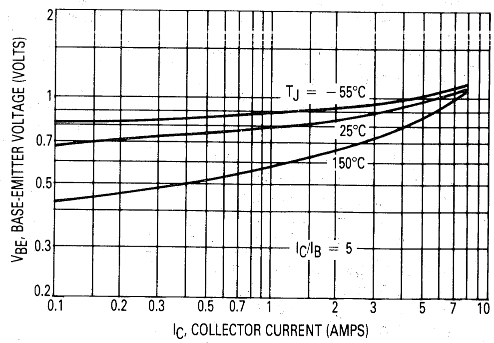


Figure 4. Base-Emitter Saturation Voltage

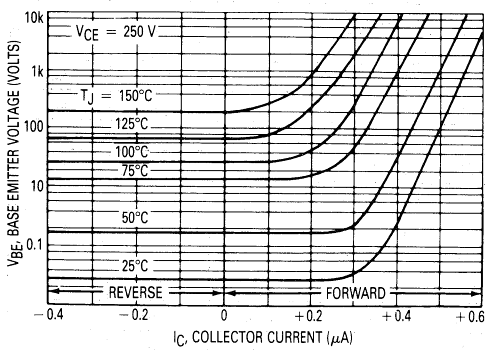


Figure 5. Collector Cutoff Region

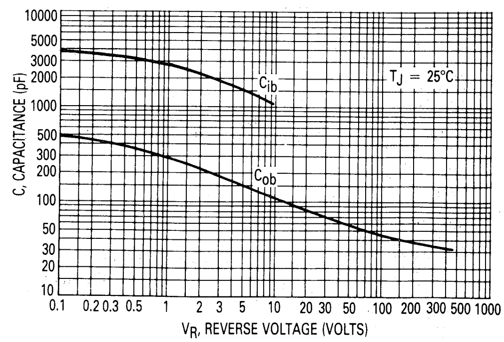


Figure 6. Capacitance Variation

TYPICAL DYNAMIC CHARACTERISTICS

T_J = 25°C | **T_J = 100°C**

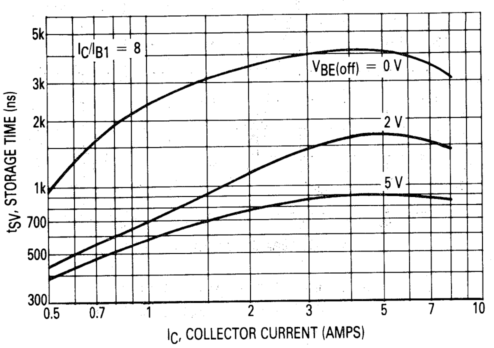


Figure 7. Inductive Storage Time

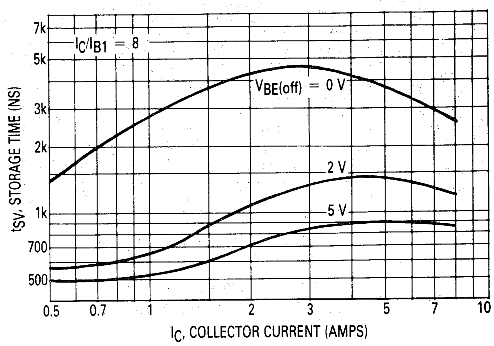


Figure 8. Inductive Storage Time

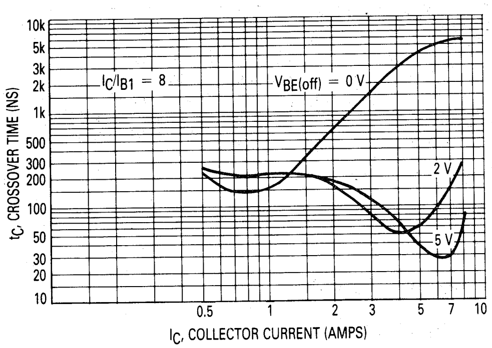


Figure 9. Inductive Crossover Time

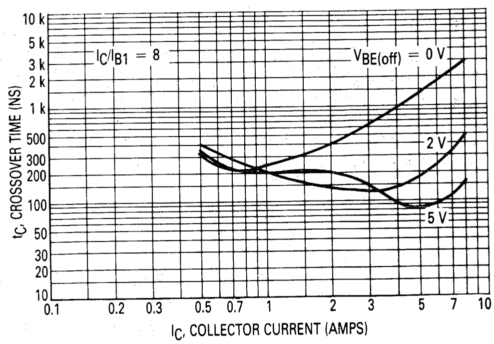


Figure 10. Inductive Crossover Time

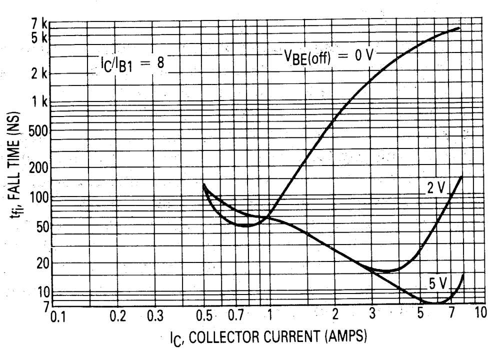


Figure 11. Inductive Fall Time

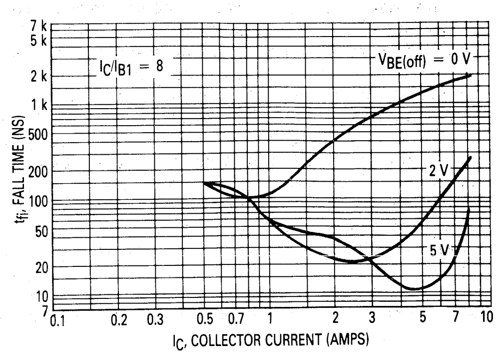


Figure 12. Inductive Fall Time

3

GUARANTEED SAFE OPERATING AREA LIMITS

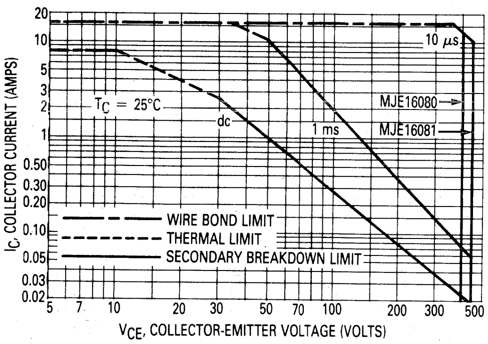


Figure 13. Maximum Rated Forward Bias Safe Operating Area

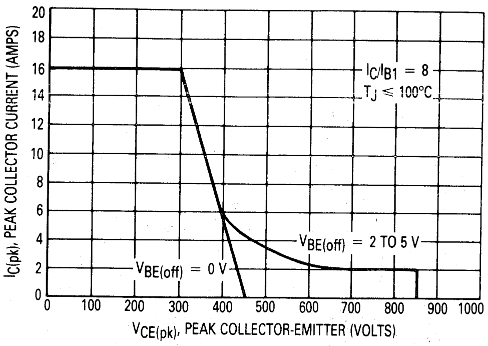


Figure 14. Maximum Rated Reverse Bias Safe Operating Area

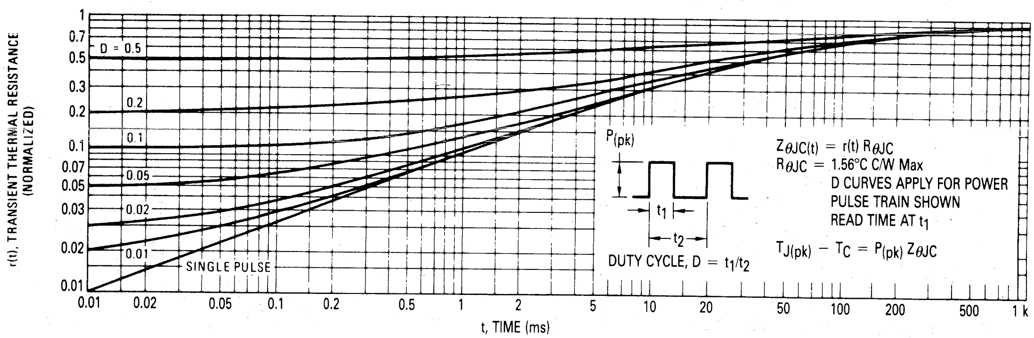


Figure 15. Typical Thermal Response [$Z_{\theta JC}(t)$]

3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 15. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

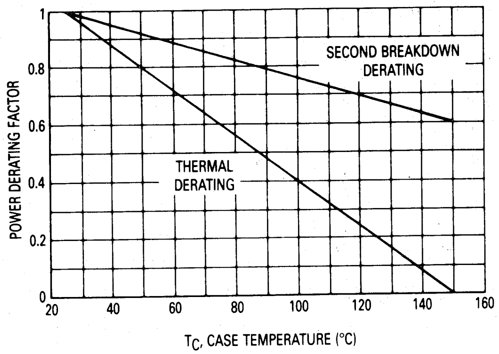


Figure 16. Power Derating

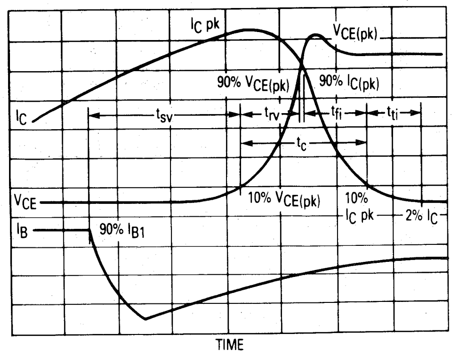
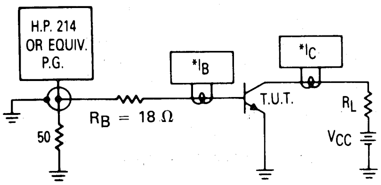


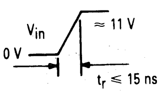
Figure 17. Inductive Switching Measurements

Table 1. Resistive Load Switching

t_d and t_r

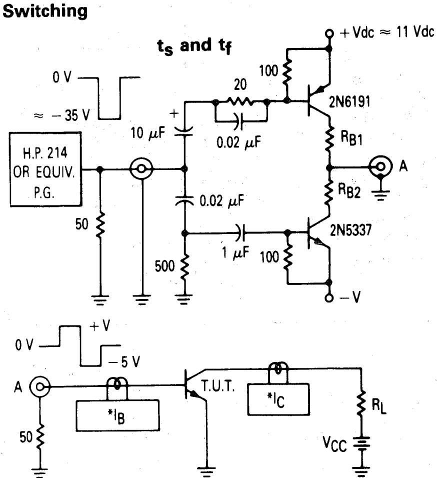


V_{CC} = 125 Vdc
R_L = 25 Ω
I_C = 5 Adc
I_B = 0.625 Adc



*Tektronix AM503
P6302 or Equivalent

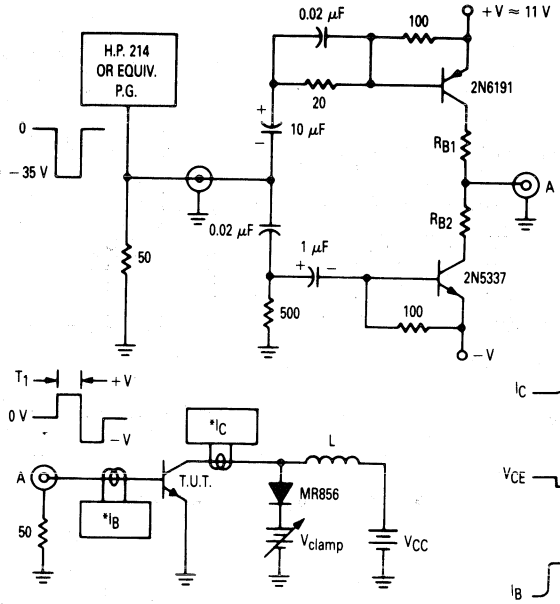
t_s and t_f

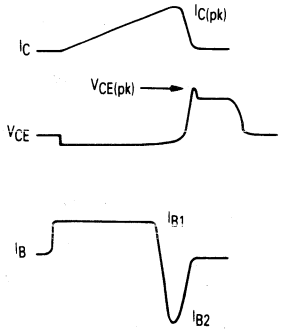


V_{CC} = 125 I_{B1} = 0.625 Adc, R_{B1} = 18 Ω
R_L = 25 Ω I_{B2} = 0.625 Adc, R_{B2} = 8 Ω
I_C = 5 Adc For $V_{BE(off)}$ = 5 V R_{B2} = 0 Ω
Note: Adjust −V to obtain desired $V_{BE(off)}$ at point A.

3

Table 2. Inductive Load Switching





$T_1 \approx \dfrac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
$L = 10$ mH
$R_{B2} = \infty$
$V_{CC} = 20$ Volts

*Tektronix
P-6042 or
Equivalent

Inductive Switching
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

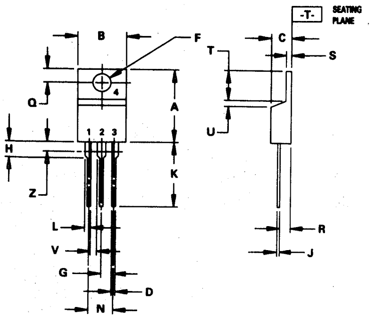
Scope — Tektronix
7403 or
Equivalent

RBSOA
$L = 200\ \mu H$
$R_{B2} = 0$
$V_{CC} = 20$ Volts
R_{B1} selected for desired I_{B1}

Note: Adjust −V to obtain desired $V_{BE(off)}$ at Point A.

3

CASE 221A-04
(TO-220AB)



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

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N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NPN MJH6282 MJH6283 MJH6284 / PNP MJH6285 MJH6286 MJH6287

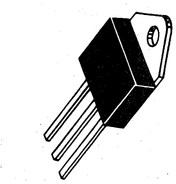
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

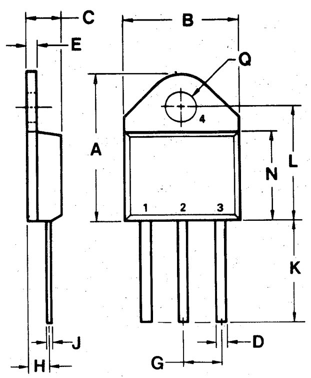
. . . designed for general-purpose amplifier and low-speed switching motor control applications.

- Similar to the Popular NPN 2N6282, 2N6283, 2N6284 and the PNP 2N6285, 2N6286, 2N6287
- Rugged RBSOA Characteristics
- Monolithic Construction with Built-In Collector-Emitter Diode

DARLINGTON 20 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60, 80, 100 VOLTS
160 WATTS





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

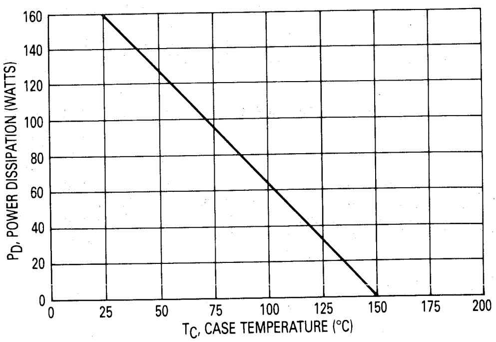
MAXIMUM RATINGS

Rating	Symbol	MJH6282 MJH6285	MJH6283 MJH6286	MJH6284 MJH6287	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous Peak	I_C		20 40		Adc
Base Current	I_B		0.5		Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D		160 1.28		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.78	°C/W

FIGURE 1 — POWER DERATING



3

MJH6282, MJH6283, MJH6284 NPN
MJH6285, MJH6286, MJH6287 PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

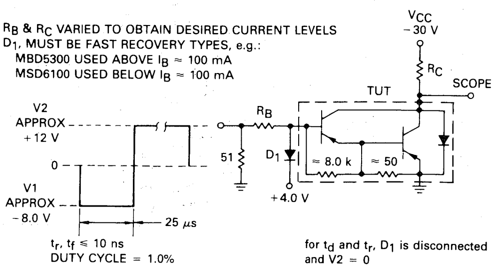
Chracteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 0.1 Adc, I_B = 0)	MJH6282, MJH6285 MJH6283, MJH6286 MJH6284, MJH6287	$V_{CEO(sus)}$	60 80 100	— — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	MJH6282, MJH6285 MJH6283, MJH6286 MJH6284, MJH6287	I_{CEO}	— — —	1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	— —	0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc) (I_C = 20 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	750 100	18,000 —	—
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 40 mAdc) (I_C = 20 Adc, I_B = 200 mAdc)		$V_{CE(sat)}$	— —	2.0 3.0	Vdc
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJH6282, 83, 84 MJH6285, 86, 87	C_{ob}	— —	400 600	pF
Small-Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	—	—

SWITCHING CHARACTERISTICS

Resistive Load		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	V_{CC} = 30 Vdc, I_C = 10 Adc I_{B1} = I_{B2} = 100 mA Duty Cycle = 1.0%	t_d	0.1	0.1	μs
Rise Time		t_r	0.3	0.3	
Storage Time		t_s	1.0	1.0	
Fall Time		t_f	3.5	2.0	

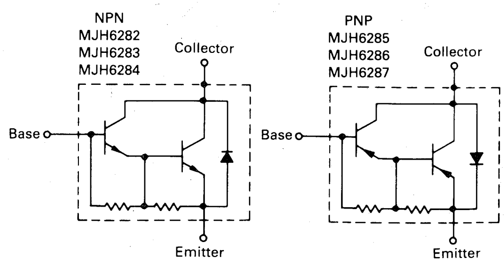
(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



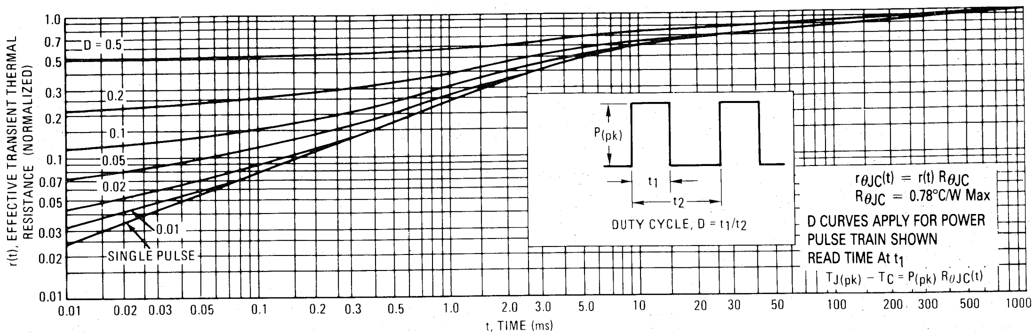
For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 — DARLINGTON SCHEMATIC



3

FIGURE 4 — THERMAL RESPONSE



FBSOA, FORWARD BIAS SAFE OPERATING AREA

FIGURE 5 — MJH6282, MJH6285

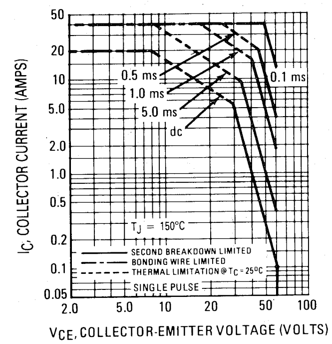


FIGURE 6 — MJH6283, MJH6286

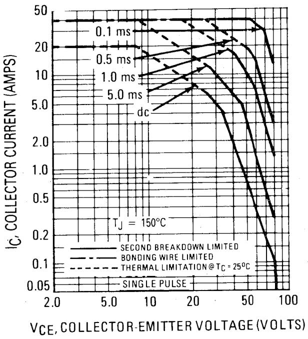


FIGURE 7 — MJH6284, MJH6287

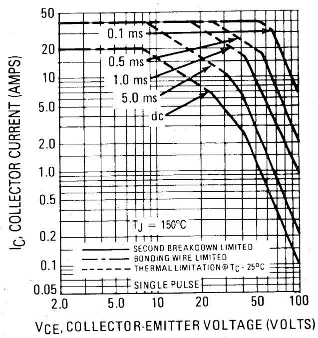
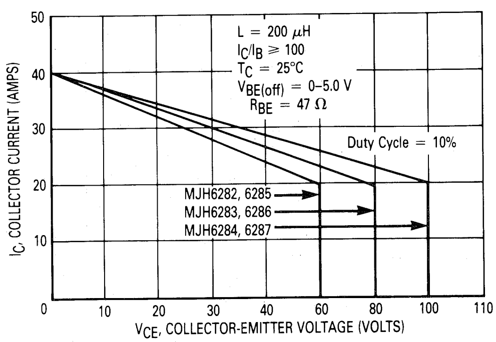


FIGURE 8 — MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5, 6 and 7 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 9 — DC CURRENT GAIN

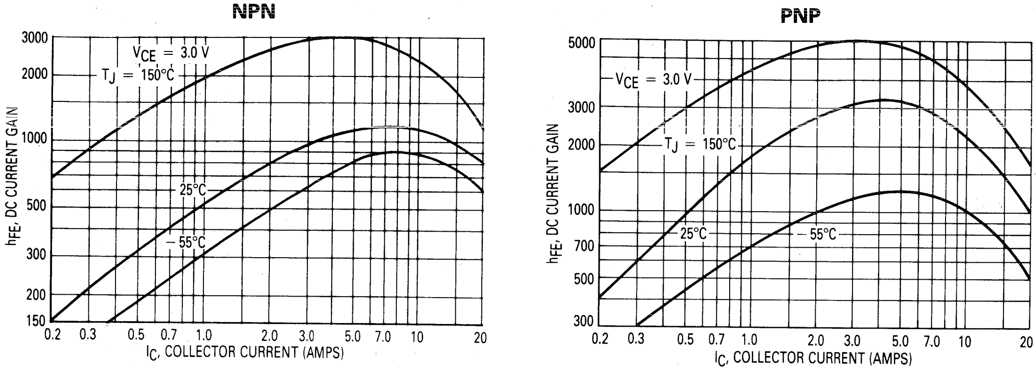


FIGURE 10 — COLLECTOR SATURATION REGION

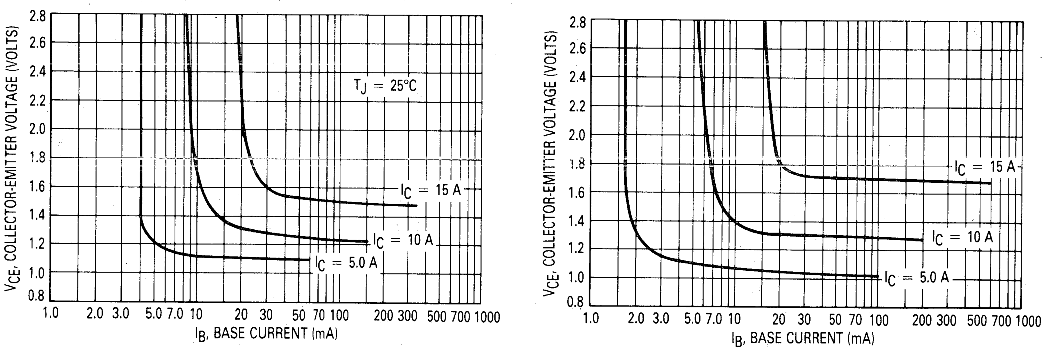
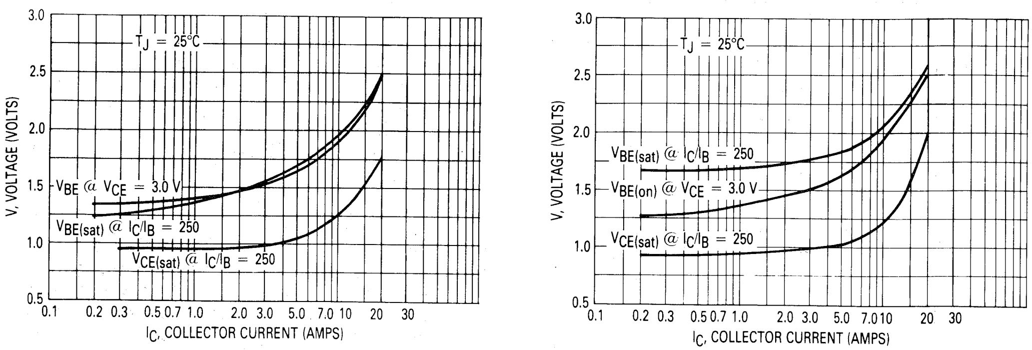


FIGURE 11 — "ON" VOLTAGES



MJH6676 thru MJH6678
See Page 3-250

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP	NPN
MJH11017	MJH11018
MJH11019	MJH11020
MJH11021	MJH11022

COMPLEMENTARY DARLINGTON SILICON POWER TRANSISTORS

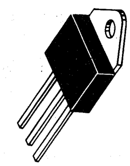
. . . designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High DC Current Gain @ 10 Adc — h_{FE} = 400 Min (All Types)
- Collector-Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 150 Vdc (Min) — MJH11018, 17
  = 200 Vdc (Min) — MJH11020, 19
  = 250 Vdc (Min) — MJH11022, 21
- Low Collector-Emitter Saturation Voltage
  $V_{CE(sat)}$ = 1.2 V (Typ) @ I_C = 5.0 A
  = 1.8 V (Typ) @ I_C = 10 A
- Monolithic Construction

15 AMPERE

DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

150, 200, 250 VOLTS
150 WATTS



MAXIMUM RATINGS

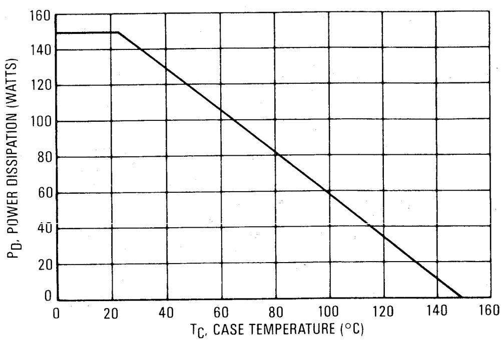
Rating	Symbol	MJH 11018 11017	MJH 11020 11019	MJH 11022 11021	Unit
Collector-Emitter Voltage	V_{CEO}	150	200	250	Vdc
Collector-Base Voltage	V_{CB}	150	200	250	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous — Peak (1)	I_C		15 30		Adc
Base Current	I_B		0.5		Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D		150 1.2		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +150		°C

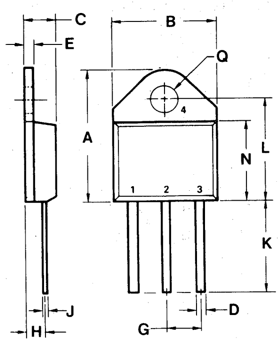
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.83	°C/W

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
(TO-218AC)

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C Unless Otherwise Noted)

Characteristics		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	MJH11017, MJH11018 MJH11019, MJH11020 MJH11021, MJH11022	$V_{CEO(sus)}$	150 200 250	— — —	Vdc
Collector Cutoff Current (V_{CE} = 75 Vdc, I_B = 0) (V_{CE} = 100 Vdc, I_B = 0) (V_{CE} = 125 Vdc, I_B = 0)	MJH11017, MJH11018 MJH11019, MJH11020 MJH11021, MJH11022	I_{CEO}	— — —	1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_J = 150°C)		I_{CEV}	— —	0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	400 100	15,000 —	—
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 100 mA) (I_C = 15 Adc, I_B = 150 mA)		$V_{CE(sat)}$	— —	2.5 4.0	Vdc
Base-Emitter On Voltage (I_C = 10 A, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
Base-Emitter Saturation Voltage (I_C = 15 Adc, I_B = 150 mA)		$V_{BE(sat)}$	—	3.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	3.0	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJH11018, MJH11020, MJH11022 MJH11017, MJH11019, MJH11021	C_{ob}	— —	400 600	pF
Small-Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	100	—	—

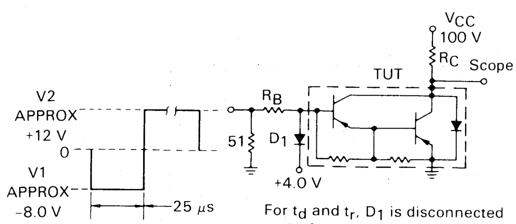
SWITCHING CHARACTERISTICS

Characteristics		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	(V_{CC} = 100 V, I_C = 10 A, I_B = 100 mA $V_{BE(off)}$ = 5.0 V) (See Figure 2)	t_d	150	75	ns
Rise Time		t_r	1.2	0.5	μs
Storage Time		t_s	4.4	2.7	μs
Fall Time		t_f	2.5	2.5	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT

R_B & R_C varied to obtain desired current levels
D_1, must be fast recovery types, e.g.:
MBD5300 used above $I_B \approx$ 100 mA
MSD6100 used below $I_B \approx$ 100 mA



t_r, $t_f \leq$ 10 ns
Duty Cycle = 1.0%

For t_d and t_r, D_1 is disconnected and V2 = 0

For NPN test circuit, reverse diode and voltage polarities.

FIGURE 3 — THERMAL RESPONSE

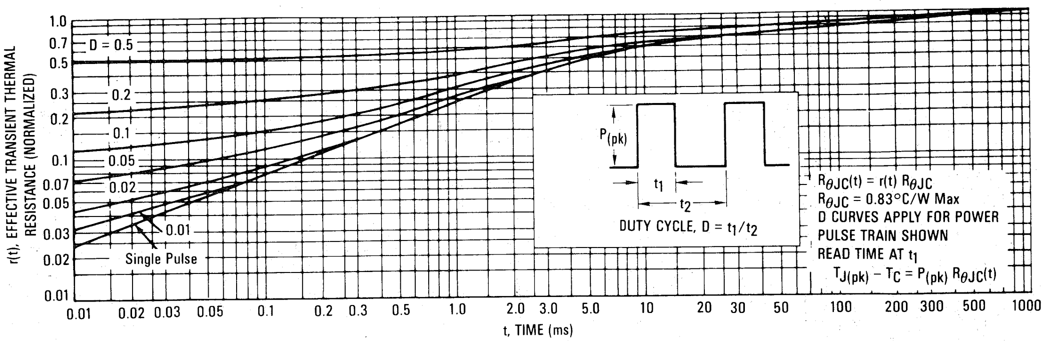
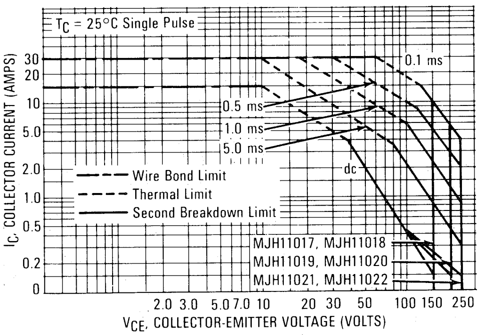


FIGURE 4 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (FBSOA)

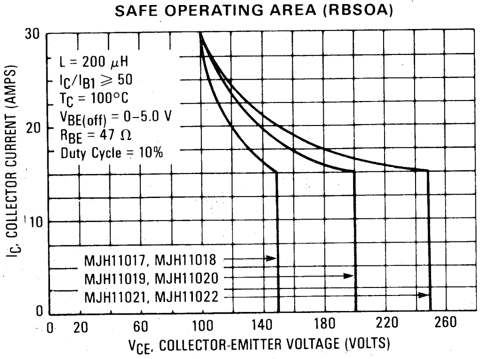


FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 5 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA (RBSOA)



REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives RBSOA characteristics.

FIGURE 6 — DC CURRENT GAIN

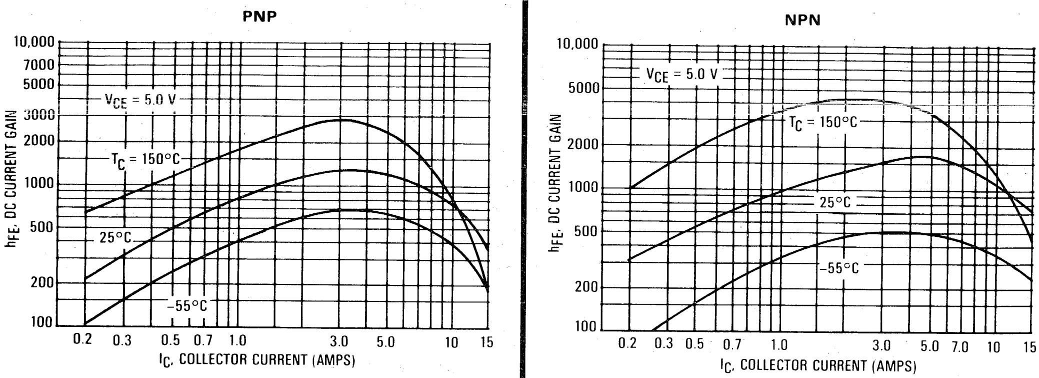


FIGURE 7 — COLLECTOR SATURATION REGION

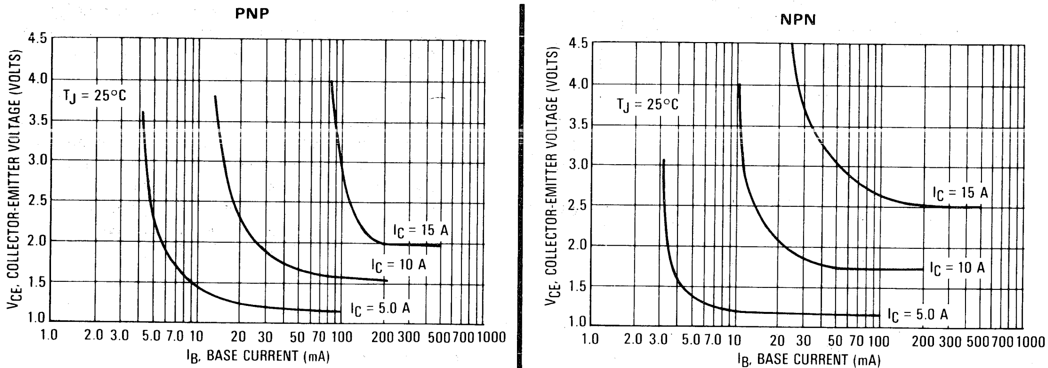
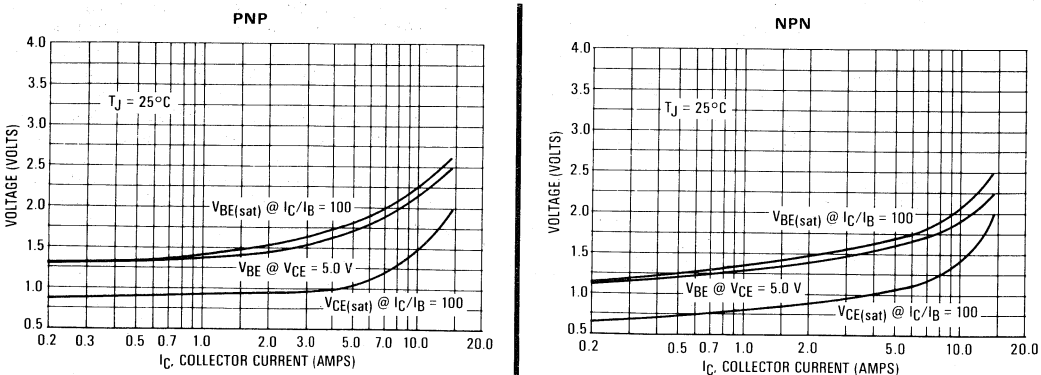
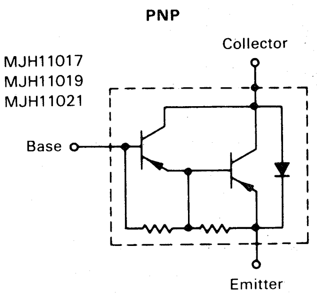


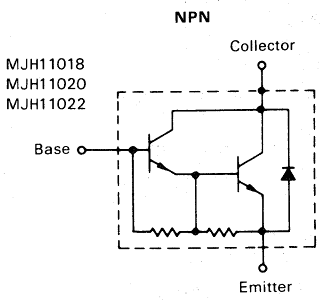
FIGURE 8 — "ON" VOLTAGES



3

FIGURE 9 — DARLINGTON SCHEMATIC





MJH13090
MJH13091
See Page 3-816

MJH16010
MJH16012
See Page 3-890

MJH16002
MJH16004
See Page 3-1090

MJH16010A
See Page 3-898

MJH16002A
See Page 3-866

MJH16018
See Page 3-914

MJH16006
MJH16008
See Page 3-874

MJH16032
MJH16034
See Page 3-1098

MJH16006A
See Page 3-882

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

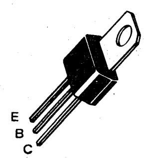
MPS-U01
MPS-U01A

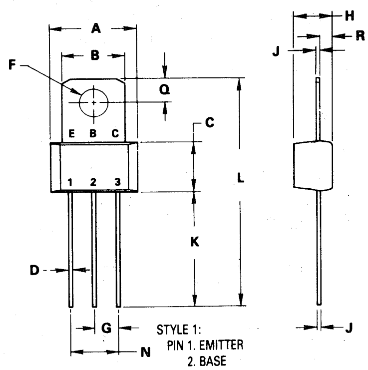
NPN SILICON ANNULAR TRANSISTORS

. . . designed for complementary symmetry audio circuits to 10 Watts output.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 1.0 Adc
- Complements to PNP MPS-U51 and MPS-U51A
- Uniwatt Package for Excellent Thermal Properties — 1.0 Watt @ T_A = 25°C

NPN SILICON AUDIO TRANSISTORS





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	MPS-U01	MPS-U01A	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Base Voltage	V_{CB}	40	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	2.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	125	°C/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

Uniwatt packages can be To-5 lead formed by adding -5 to the device title and tab formed for flush mounting by adding -1 to the device title.

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)	MPS-U01 MPS-U01A	$V_{(BR)CEO}$	30 40	– –	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	MPS-U01 MPS-U01A	$V_{(BR)CBO}$	40 50	– –	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0)	MPS-U01 MPS-U01A	I_{CBO}	– –	0.1 0.1	μAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 1.0 Vdc) (I_C = 100 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	 55 60 50	 – – –	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	50	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	20	pF

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 – DC CURRENT GAIN

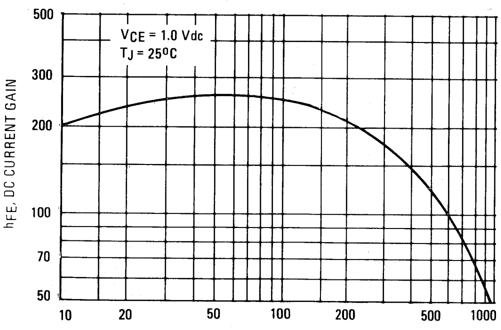


FIGURE 2 – "ON" VOLTAGES

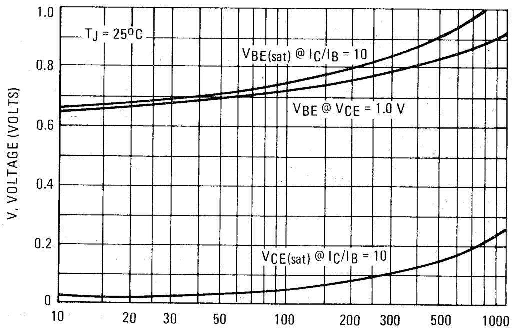
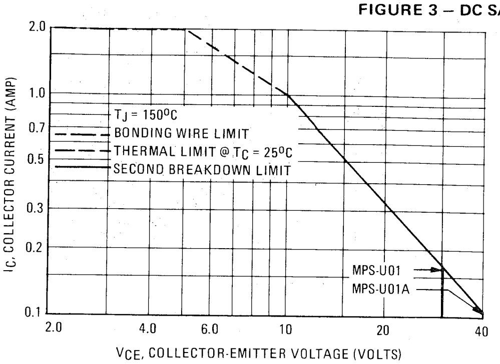


FIGURE 3 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

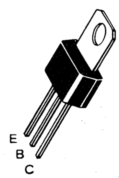
MPS-U02

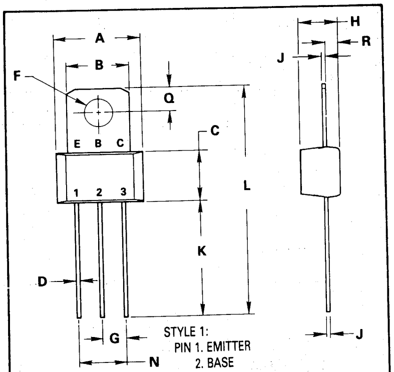
NPN SILICON ANNULAR AMPLIFIER TRANSISTOR

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complement to PNP MPS-U52

NPN SILICON AMPLIFIER TRANSISTOR





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	[illegible]	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	800	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	60	-	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	-	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 150 mAdc, V_{CE} = 10 Vdc) (I_C = 500 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 50 50 30	 - 300 -	
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$	-	0.4	Vdc
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$	-	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	100	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	-	20	pF

3

FIGURE 1 – NORMALIZED DC CURRENT GAIN

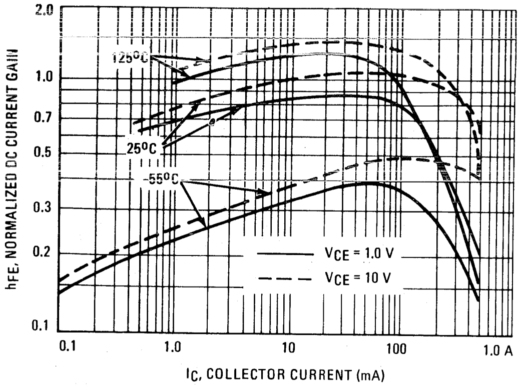


FIGURE 2 – COLLECTOR-EMITTER SATURATION VOLTAGE versus BASE CURRENT

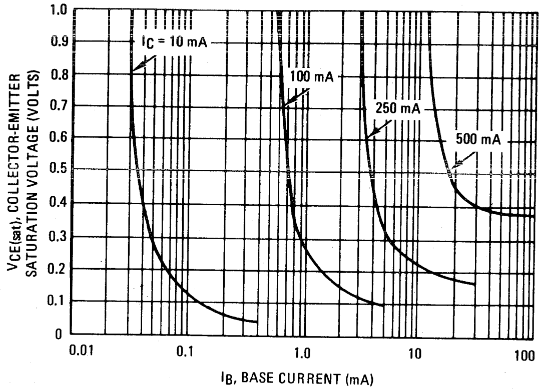


FIGURE 3 – BASE-EMITTER VOLTAGE versus COLLECTOR CURRENT

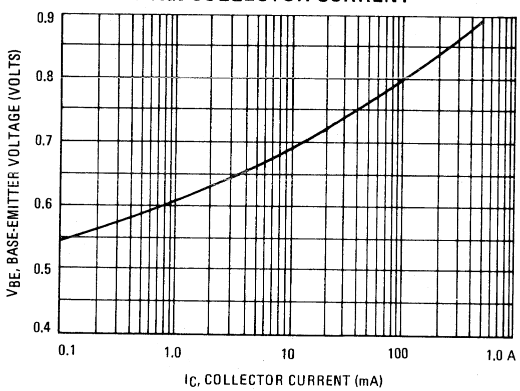


FIGURE 4 – CAPACITANCE versus VOLTAGE

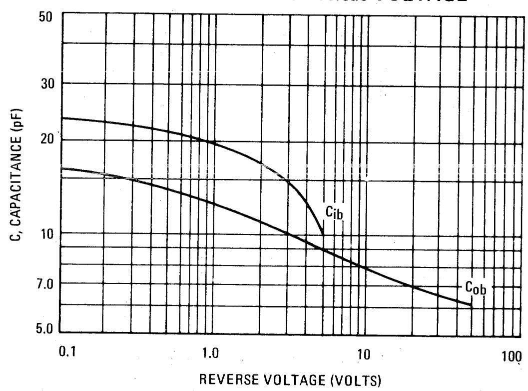


FIGURE 5 – CURRENT-GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

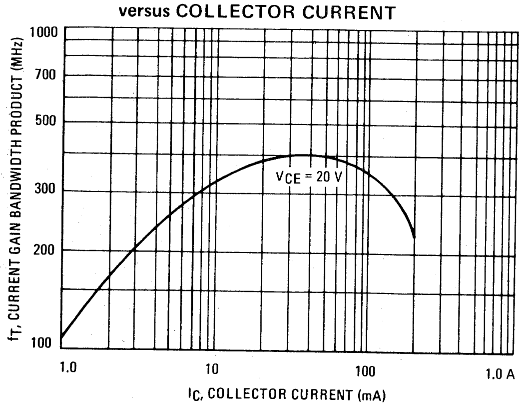
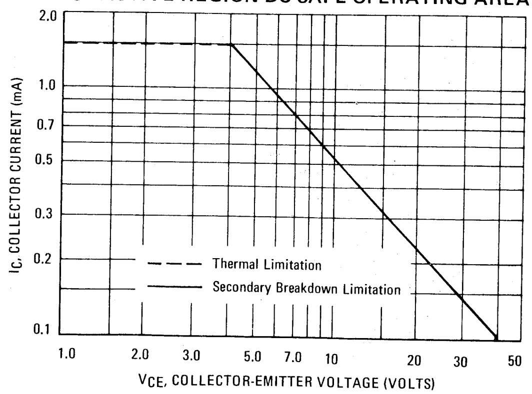


FIGURE 6 – ACTIVE REGION DC SAFE OPERATING AREA



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

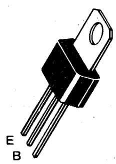
MPS-U03
MPS-U04

NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for horizontal drive applications, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage — $V_{(BR)CEO}$ = 180 Vdc (Min) @ I_C = 1 mAdc — MPS-U04
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 200 mAdc
- High Power Dissipation — P_D = 10 W @ T_C = 25°C

NPN SILICON AMPLIFIER TRANSISTORS

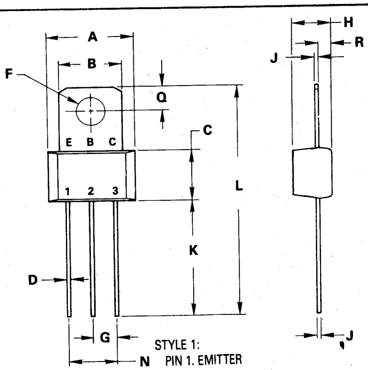


MAXIMUM RATINGS

Rating	Symbol	MPS-U03	MPS-U04	Unit
Collector-Emitter Voltage	V_{CEO}	120	180	Vdc
Collector-Base Voltage	V_{CB}	120	180	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current	I_C	1		Adc
Total Power Dissipation @ T_A = 25°C Derate Above 25°C	P_D	1 8		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C
Solder Temperature, 1/16″ From Case for 10 Seconds	—	260		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	MPS-U03 MPS-U04	$V_{(BR)CEO}$	120 180	– –	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	MPS-U03 MPS-U04	$V_{(BR)CBO}$	120 180	– –	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 150 Vdc, I_E = 0)	MPS-U03 MPS-U04	I_{CBO}	– –	0.1 0.1	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc)		h_{FE}	40	–	–
Collector-Emitter Saturation Voltage (I_C = 200 mAdc, I_B = 20 mAdc)		$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter On Voltage (I_C = 200 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	35	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	12	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)		C_{ib}	–	110	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

TYPICAL CHARACTERISTICS

FIGURE 1 — CURRENT-GAIN — BANDWIDTH PRODUCT

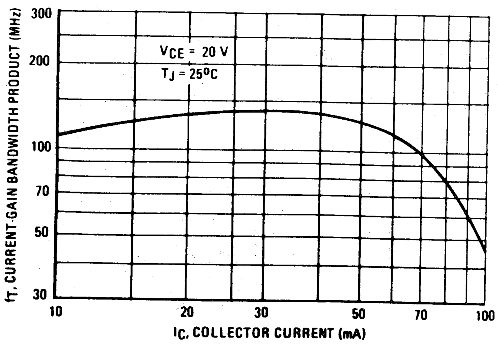
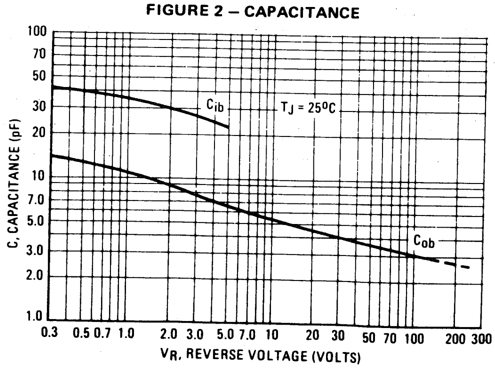


FIGURE 2 — CAPACITANCE



TYPICAL CHARACTERISTICS (Continued)

FIGURE 3 – DC CURRENT GAIN

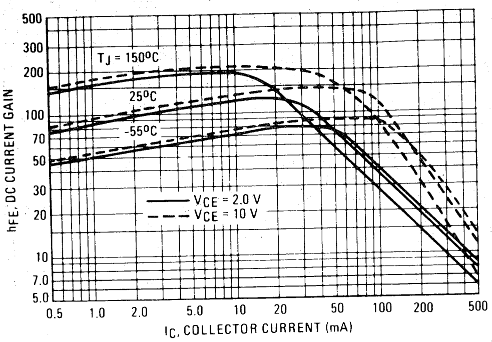


FIGURE 4 – "ON" VOLTAGE

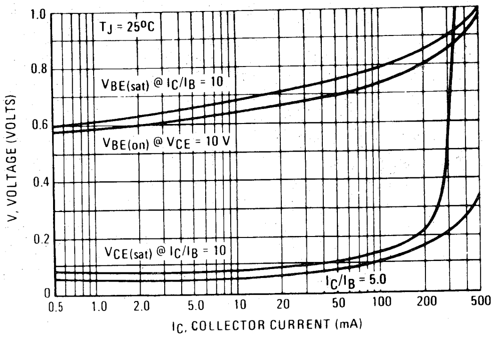


FIGURE 5 – COLLECTOR SATURATION REGION

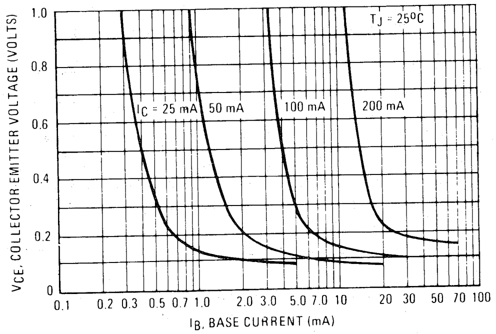


FIGURE 6 – TEMPERATURE COEFFICIENTS

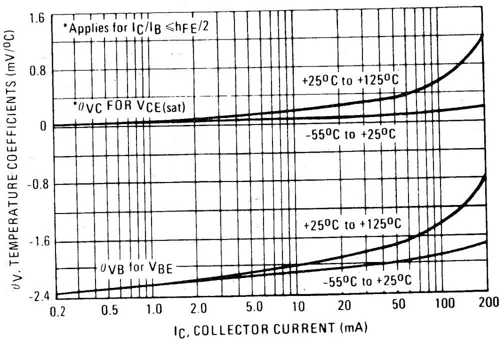


FIGURE 7 – COLLECTOR CHARACTERISTICS

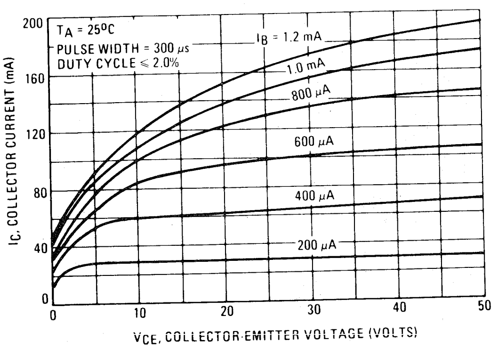
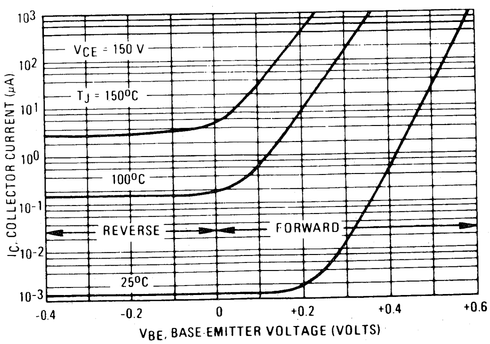


FIGURE 8 – COLLECTOR CUTOFF REGION



TYPICAL CHARACTERISTICS (Continued)

FIGURE 9 – THERMAL RESPONSE

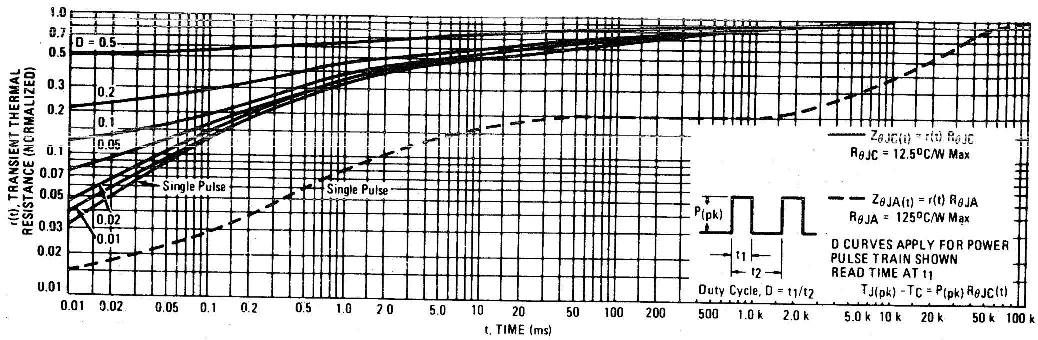
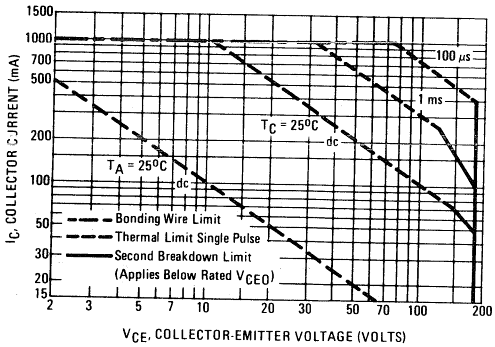


FIGURE 10 – ACTIVE REGION SAFE-OPERATING AREA

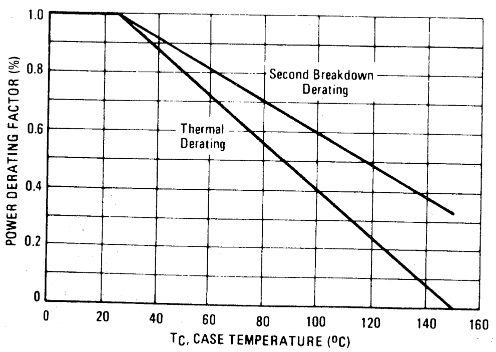


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

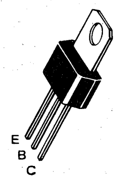
MPS-U05
MPS-U06

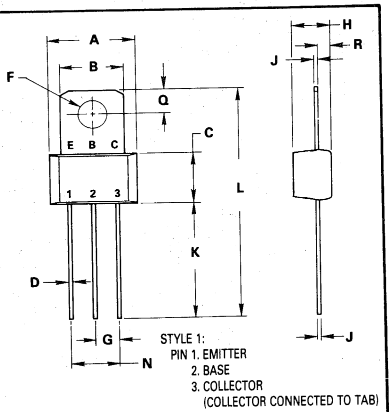
NPN SILICON ANNULAR AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage — $V_{(BR)CEO}$ = 60 Vdc (Min) @ I_C = 1.0 mAdc — MPS-U05
  80 Vdc (Min) @ I_C = 1.0 mAdc — MPS-U06
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complements to PNP MPS-U55 and MPS-U56

NPN SILICON AMPLIFIER TRANSISTORS





NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	MPS-U05	MPS-U06	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current — Continuous	I_C	2.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	MPS-U05 MPS-U06	$V_{(BR)CEO}$	60 80	– –	– –	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0)	MPS-U05 MPS-U06	I_{CBO}	– –	– –	100 100	nAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 250 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		h_{FE}	80 60 –	125 100 55	– – –	–
Collector-Emitter Saturation Voltage(1) (I_C = 250 mAdc, I_B = 10 mAdc) (I_C = 250 mAdc, I_B = 25 mAdc)		$V_{CE(sat)}$	– –	0.18 0.1	0.4 –	Vdc
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	0.74	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain—Bandwidth Product (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	150	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	6.0	12	pF

(1)Pulse Test: Pulse Width ≤300 μs; Duty Cycle ≤2.0%.

FIGURE 1 – DC CURRENT GAIN

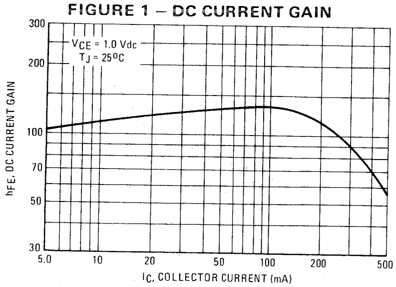


FIGURE 2 – "ON" VOLTAGES

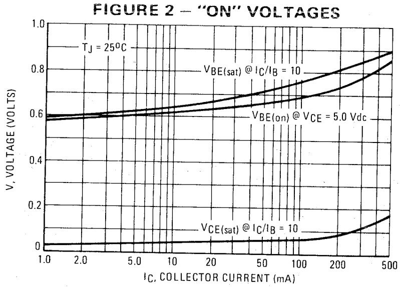


FIGURE 3 – DC SAFE OPERATING AREA

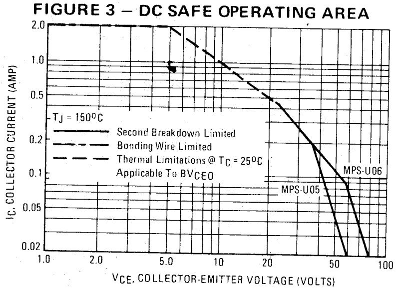
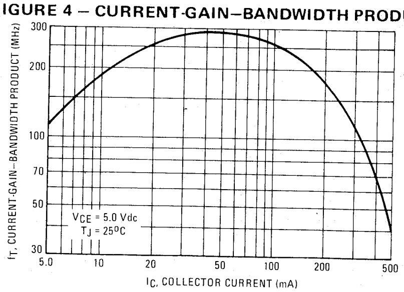


FIGURE 4 – CURRENT-GAIN–BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

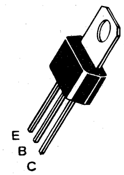
MPS-U07

NPN SILICON ANNULAR AMPLIFIER TRANSISTOR

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage — $V_{(BR)CEO}$ = 100 Vdc (Min) @ I_C = 1.0 mAdc
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complement to PNP MPS-U57

NPN SILICON AMPLIFIER TRANSISTOR

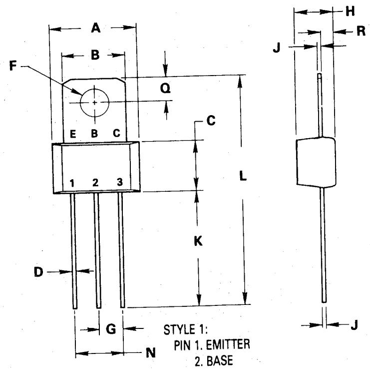


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	2.0	Adc
Total Power Dissipaton @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipaton @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	100	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (1)	h_{FE}				–
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)		60	110	–	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		30	65	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		–	33	–	
Collector-Emitter Saturation Voltage (1)	$V_{CE(sat)}$				Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)		–	0.18	0.4	
(I_C = 250 mAdc, I_B = 25 mAdc)		–	0.1	–	
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	0.76	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	50	150	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	6.0	12	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 – DC CURRENT GAIN

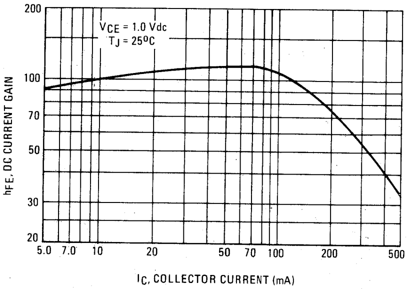


FIGURE 2 – "ON" VOLTAGES

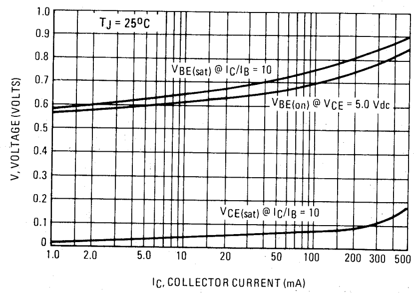


FIGURE 3 – DC SAFE OPERATING AREA

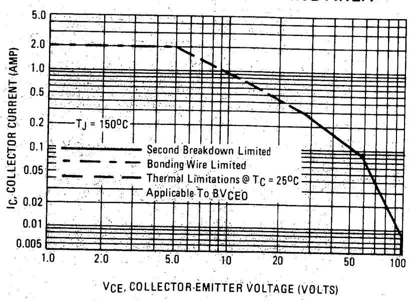
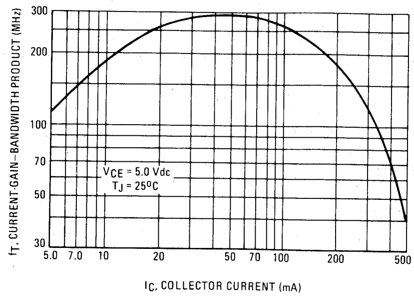


FIGURE 4 – CURRENT-GAIN–BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

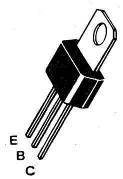
MPS-U10

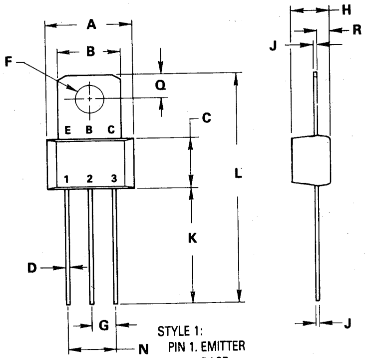
**NPN SILICON
HIGH VOLTAGE
AMPLIFIER
TRANSISTOR**

NPN SILICON ANNULAR TRANSISTOR

. . . designed for high-voltage video and luminance output stages in TV receivers.

- High Collector-Emitter Breakdown Voltage — $V_{(BR)CEO}$ = 300 Vdc (Min) @ I_C = 1.0 mAdc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.75 Vdc (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance — C_{cb} = 3.0 pF (Max) @ V_{CB} = 20 Vdc





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	0.5	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	125	°C/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

3

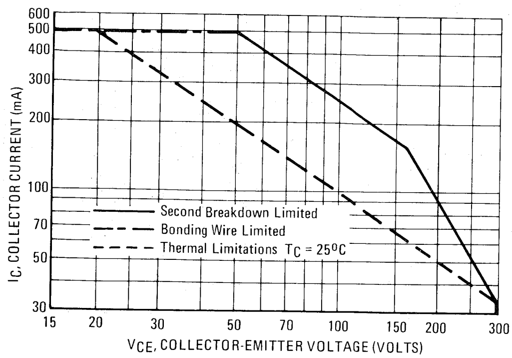
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	300	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	300	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	6.0	–	Vdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}	–	0.2	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)		25	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)		40	–	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)		40	–	
Collector-Emitter Saturation Voltage (I_C = 30 mAdc, I_B = 3.0 mAdc)	$V_{CE(sat)}$	–	0.75	Vdc
Base-Emitter On Voltage (I_C = 30 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	–	0.85	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (1) (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	45	–	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	3.0	pF

(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle≤ 2%.

3

FIGURE 1 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter second breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 — DC CURRENT GAIN

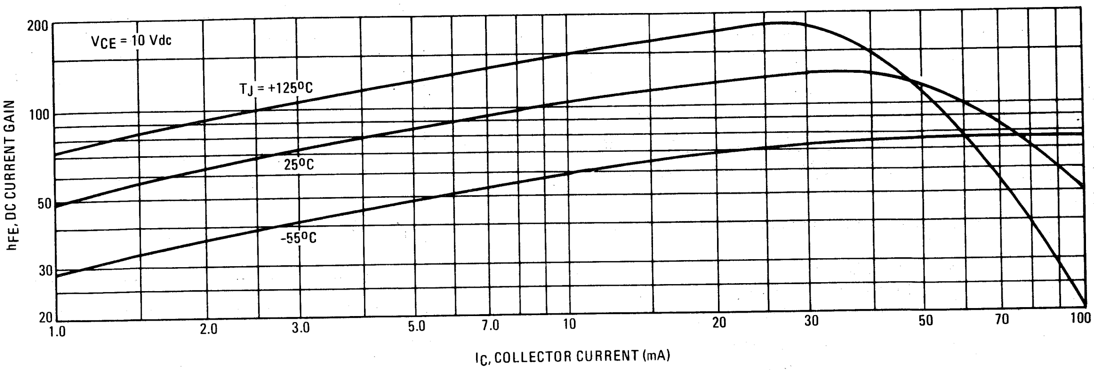


FIGURE 3 — CAPACITANCES

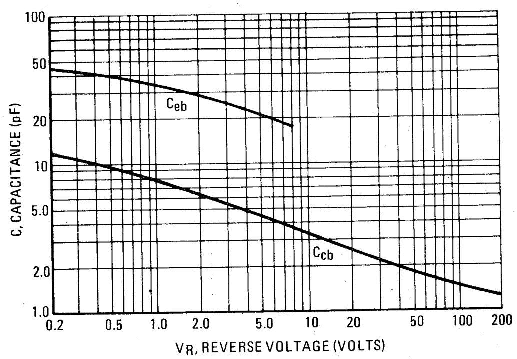


FIGURE 4 — CURRENT-GAIN—BANDWIDTH PRODUCT

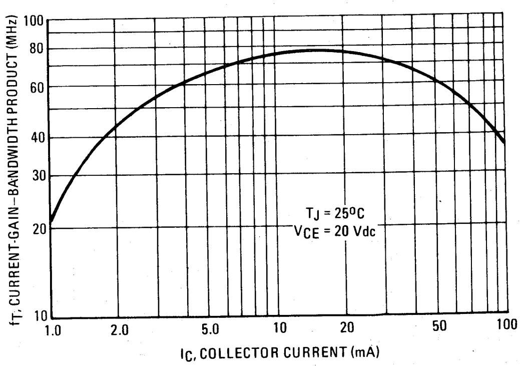
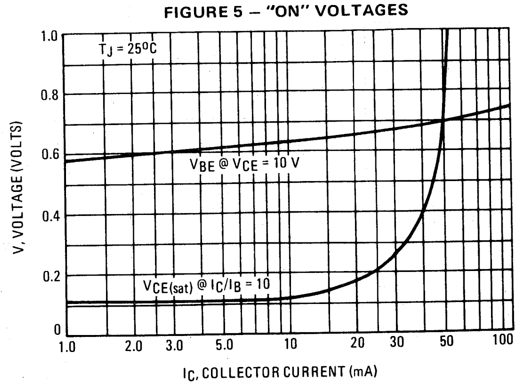


FIGURE 5 — "ON" VOLTAGES



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

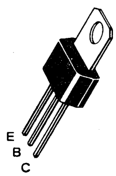
MPS-U45

NPN SILICON DARLINGTON AMPLIFIER TRANSISTOR

. . . designed for amplifier and driver applications.

- High DC Current Gain —
  h_{FE} = 25,000 (Min) @ I_C = 200 mAdc
  15,000 (Min) @ I_C = 500 mAdc
- Collector-Emitter Breakdown Voltage —
  $V_{(BR)CES}$ = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc @ I_C = 1.0 Adc
- Monolithic Construction for High Reliability
- Complement to PNP MPS-U95

NPN SILICON DARLINGTON TRANSISTOR



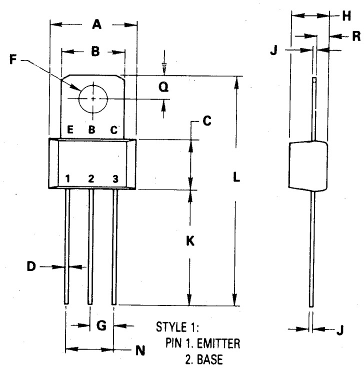
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}(1)	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	12	Vdc
Collector Current	I_C	2.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

(1) Due to the monolithic construction of this device, breakdown voltages of both transistor elements are identical. $V_{(BR)CES}$ is tested in lieu of $V_{(BR)CEO}$ in order to avoid errors caused by noise pickup. The voltage measured during the $V_{(BR)CES}$ test is the $V_{(BR)CEO}$ of the output transistor.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, V_{BE} = 0)	$V_{(BR)CES}$	40	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	50	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	12	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)	I_{EBO}	–	–	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain	h_{FE}				–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)		25,000	65,000	150,000	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)		15,000	35,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		4,000	12,000	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{CE(sat)}$	–	1.2	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{BE(sat)}$	–	1.85	2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	1.7	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (1) (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	$\|h_{fe}\|$	1.0	3.2	–	–
Collector Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	2.5	6.0	pF

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

Uniwatt darlington transistors can be used in any number of low power applications, such as relay drivers, motor control and as general purpose amplifiers. As an audio amplifier these devices, when used as a complementary pair, can drive 3.5 watts into a 3.2 ohm speaker using a 14 volt supply with less than one per cent distortion. Because of the high gain the base drive requirement is as low as 1 mA in this application. They are also useful as power drivers for high current application such as voltage regulators.

FIGURE 1 – DC CURRENT GAIN

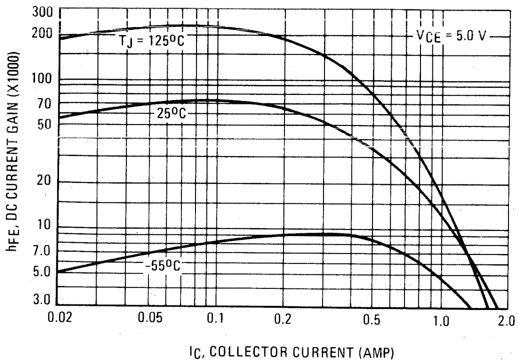


FIGURE 2 – SMALL-SIGNAL CURRENT GAIN

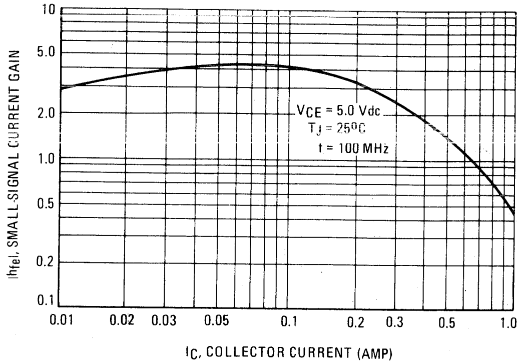


FIGURE 3 – "ON" VOLTAGES

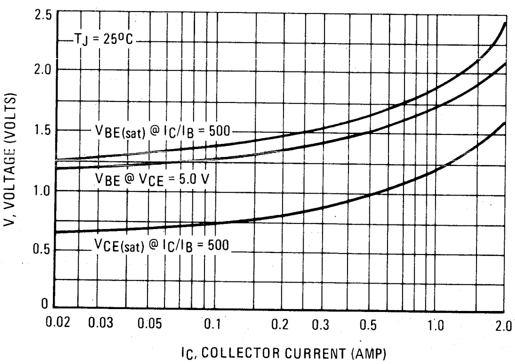
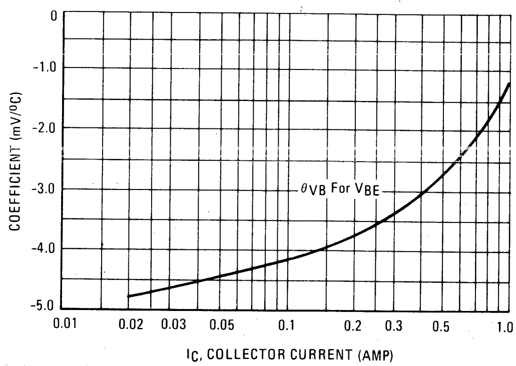
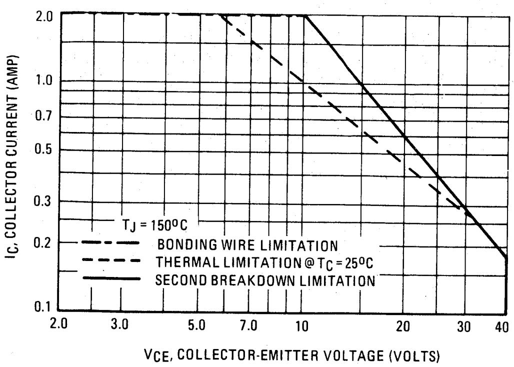


FIGURE 4 – TEMPERATURE COEFFICIENT



3

FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

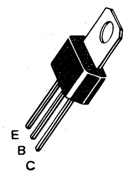
MPS-U51
MPS-U51A

PNP SILICON ANNULAR TRANSISTORS

. . . designed for complementary symmetry audio circuits to 5 Watts output.

- Excellent Current Gain Linearity — 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 1.0 Adc
- Complements to NPN MPS-U01 and MPS-U01A
- Uniwatt Package for Excellent Thermal Properties — 1.0 Watt @ T_A = 25°C

PNP SILICON AUDIO TRANSISTORS

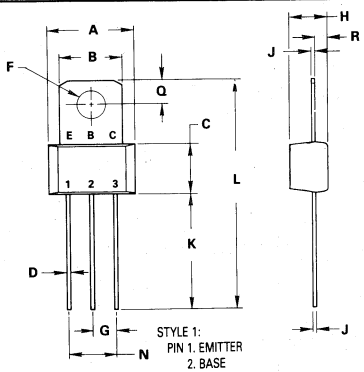


MAXIMUM RATINGS

Rating	Symbol	MPS-U51	MPS-U51A	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Base Voltage	V_{CB}	40	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	2.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W



STYLE 1:
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3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

3

MPS-U51,MPS-U51A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	MPS-U51 MPS-U51A	$V_{(BR)CEO}$	30 40	— —	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	MPS-U51 MPS-U51A	$V_{(BR)CBO}$	40 50	— —	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		$V_{(BR)EBO}$	5.0	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0)	MPS-U51 MPS-U51A	I_{CBO}	— —	0.1 0.1	μAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)		I_{EBO}	—	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 1.0 Vdc) (I_C = 100 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	 55 60 50	 — — —	—
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.7	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	50	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	30	pF

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

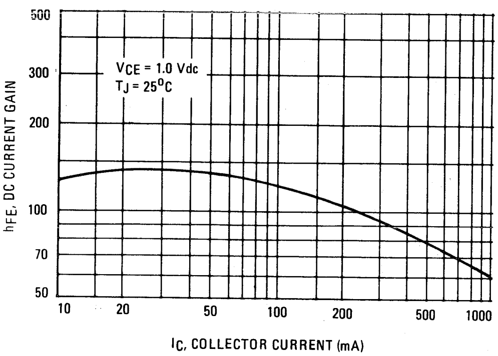


FIGURE 2 — "ON" VOLTAGES

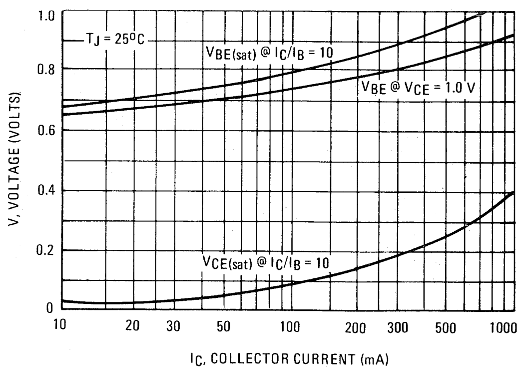
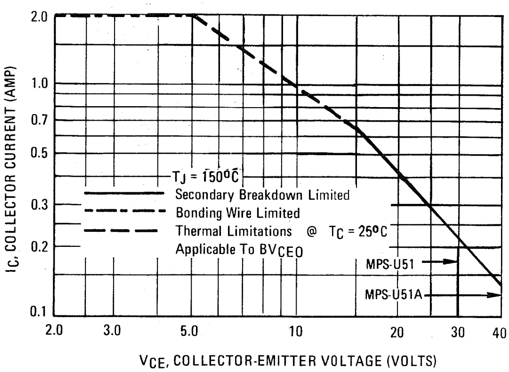


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

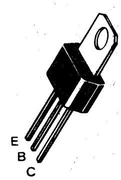
MPS-U52

PNP SILICON ANNULAR TRANSISTOR

. . . designed for general-purpose amplifier and driver applications.

- Complement to NPN MPS-U02

PNP SILICON AMPLIFIER TRANSISTOR



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	1.5	Adc
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg} (1)	-55 to +150	°C

THERMAL CHARACTERISTICS

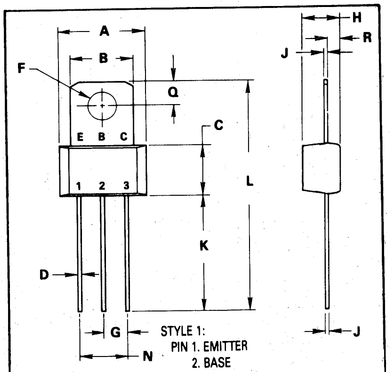
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ (1)	125	C/W

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 1.0$ mAdc, $I_B = 0$)	$V_{(BR)CEO}$	40	-	Vdc
Collector-Base Breakdown Voltage ($I_C = 100\,\mu$Adc, $I_E = 0$)	$V_{(BR)CBO}$	60	-	Vdc
Collector Cutoff Current ($V_{CB} = 40$ Vdc, $I_E = 0$)	I_{CBO}	-	100	nAdc
ON CHARACTERISTICS (2)				
DC Current Gain ($I_C = 10$ mAdc, $V_{CE} = 10$ Vdc) ($I_C = 150$ mAdc, $V_{CE} = 10$ Vdc) ($I_C = 500$ mAdc, $V_{CE} = 10$ Vdc)	h_{FE}	 50 50 30	 - 300 -	-
Collector-Emitter Saturation Voltage ($I_C = 150$ mAdc, $I_B = 15$ mAdc)	$V_{CE(sat)}$	-	0.4	Vdc
Base-Emitter Saturation Voltage ($I_C = 150$ mAdc, $I_B = 15$ mAdc)	$V_{BE(sat)}$	-	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (2) ($I_C = 20$ mAdc, $V_{CE} = 20$ Vdc, f = 100 MHz)	f_T	100	-	MHz
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, f = 100 kHz)	C_{ob}	-	24	pF

(1) $R_{\theta JA}$ is measured with device soldered into a typical printed circuit board

(2) Pulse Test: Pulse Width≤300 μs, Duty Cycle≤2.0%



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

3

FIGURE 1 — DC CURRENT GAIN

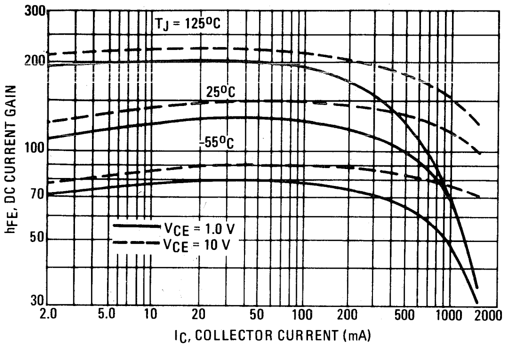


FIGURE 2 — "ON" VOLTAGES

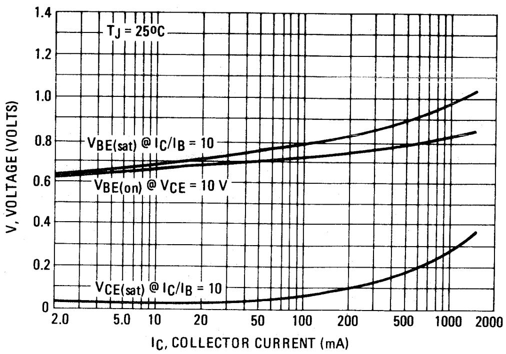


FIGURE 3 — COLLECTOR SATURATION REGION

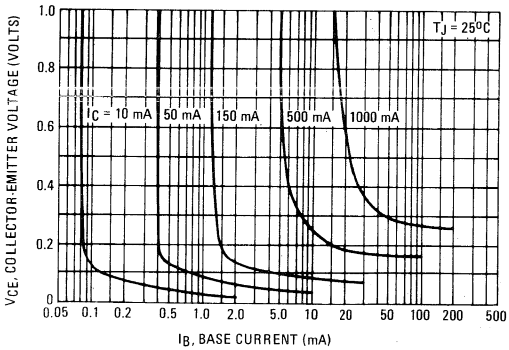


FIGURE 4 — DC SAFE OPERATING AREA

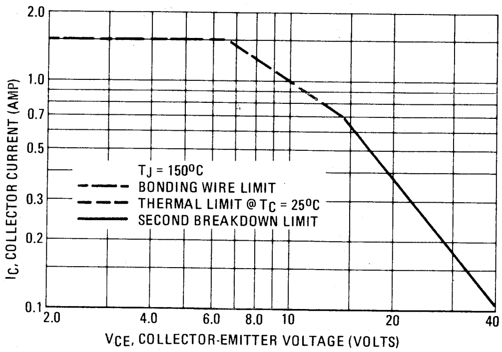


FIGURE 5 — CURRENT-GAIN BANDWIDTH PRODUCT

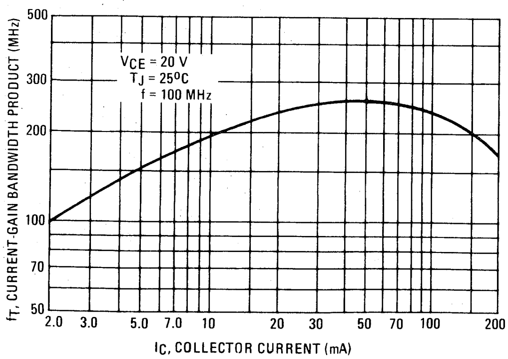
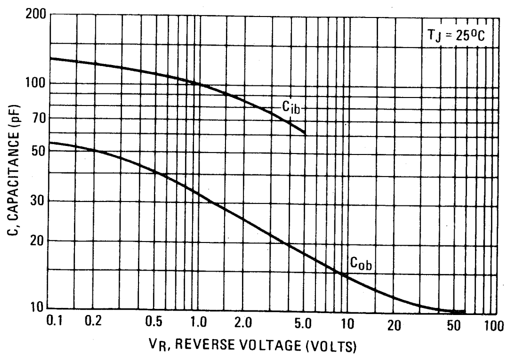


FIGURE 6 — CAPACITANCE



3

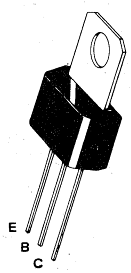
MPS-U55
MPS-U56

PNP SILICON ANNULAR AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage –
  $V_{(BR)CEO}$ = 60 Vdc (Min) @ I_C = 1.0 mAdc — MPS-U55
  80 Vdc (Min) @ I_C = 1.0 mAdc – MPS-U56
- High Power Dissipation – P_D = 10 W @ T_C = 25°C
- Complements to NPN MPS-U05 and MPS-U06

PNP SILICON AMPLIFIER TRANSISTORS



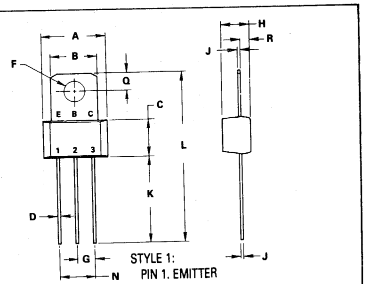
MAXIMUM RATINGS

Rating	Symbol	MPS-U55	MPS-U56	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	2.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage(1) (I_C = 1.0 mAdc, I_B = 0)	MPS-U55	$V_{(BR)CEO}$	60	—	—	Vdc
	MPS-U56		80	—	—	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	MPS-U55	I_{CBO}	—	—	100	nAdc
(V_{CB} = 60 Vdc, I_E = 0)	MPS-U56		—	—	100	
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)		h_{FE}	80	160	—	—
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			50	130	—	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			—	80	—	
Collector-Emitter Saturation Voltage(1) (I_C = 250 mAdc, I_B = 10 mAdc)		$V_{CE(sat)}$	—	0.22	0.5	Vdc
(I_C = 250 mAdc, I_B = 25 mAdc)			—	0.15	—	
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	0.78	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain—Bandwidth Product (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	100	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	10	15	pF

(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 1 — DC CURRENT GAIN

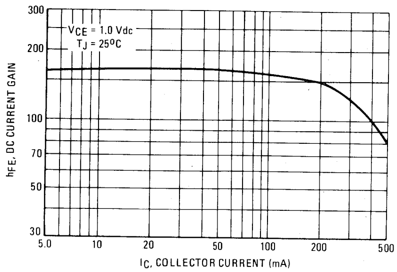


FIGURE 2 — "ON" VOLTAGES

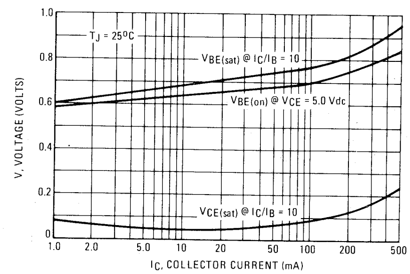


FIGURE 3 — ACTIVE-REGION SAFE OPERATING AREA

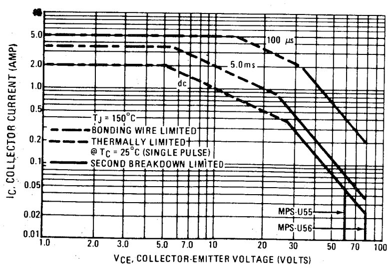
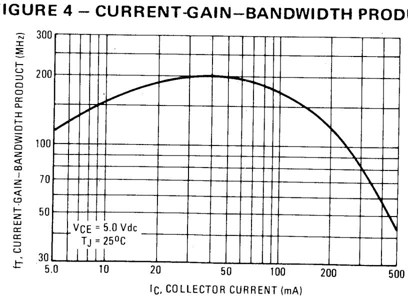


FIGURE 4 — CURRENT-GAIN—BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

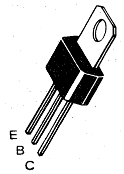
MPS-U57

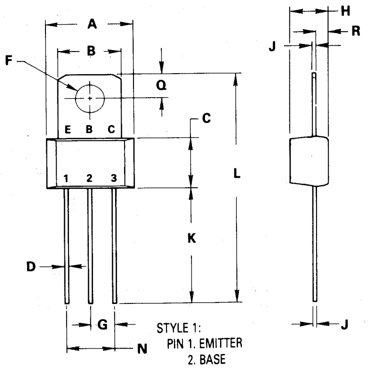
PNP SILICON ANNULAR
AMPLIFIER TRANSISTOR

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage — $V_{(BR)CEO}$ = 100 Vdc (Min) @ I_C = 1.0 mAdc
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complement to NPN MPS-U07

AMPLIFIER TRANSISTOR
PNP SILICON





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	2.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	100	–	–	Vdc
Emitter-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				–
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)		60	140	–	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		30	65	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		–	30	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)		–	0.24	0.5	
(I_C = 250 mAdc, I_B = 25 mAdc)		–	0.15	–	
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	0.78	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	50	100	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	10	15	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

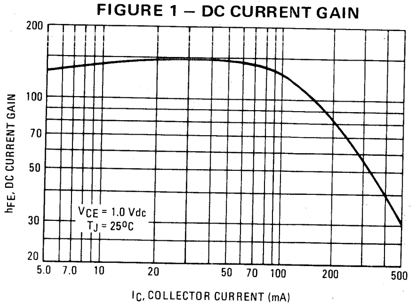


FIGURE 2 — "ON" VOLTAGES

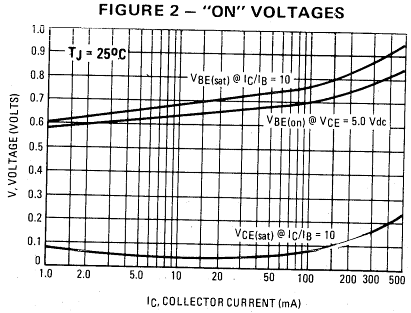


FIGURE 3 — DC SAFE OPERATING AREA

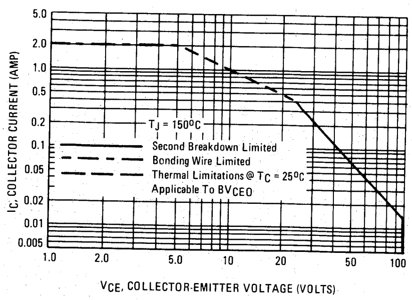
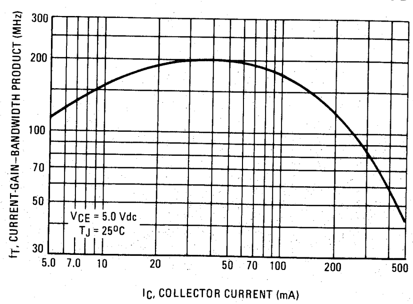


FIGURE 4 — CURRENT-GAIN—BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

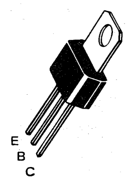
MPS-U60

PNP SILICON ANNULAR TRANSISTOR

. . . designed for general-purpose applications requiring high breakdown voltages, low saturation voltages and low capacitance.

- Complement to NPN Type MPS-U10

PNP SILICON HIGH VOLTAGE TRANSISTOR



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	1.0 8.0	Watt mW/^oC
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	10 80	Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	^oC

THERMAL CHARACTERISTICS

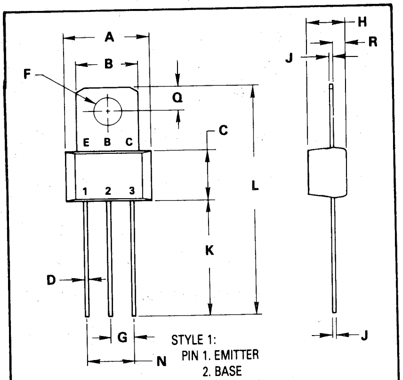
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}(1)$	125	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Breakdown Voltage (2) (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	300	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	300	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0		Vdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}		0.2	μAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}		0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (2) (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 30 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 25 30 30		
Collector-Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 2.0 mAdc)	$V_{CE(sat)}$		0.75	Vdc
Base-Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 2.0 mAdc)	$V_{BE(sat)}$	-	0.9	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (2) (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	60		MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	8.0	pF

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

3

FIGURE 1 – DC CURRENT GAIN

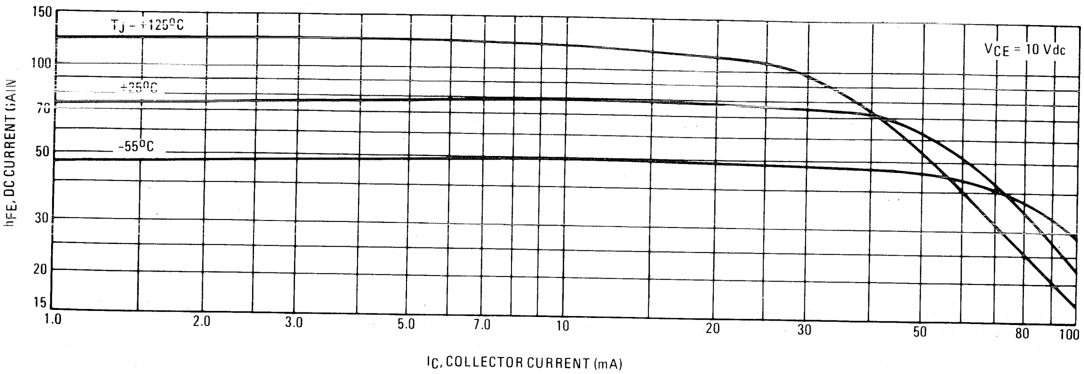


FIGURE 2 – CAPACITANCES

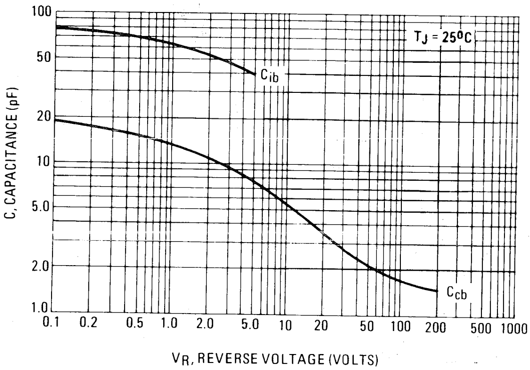
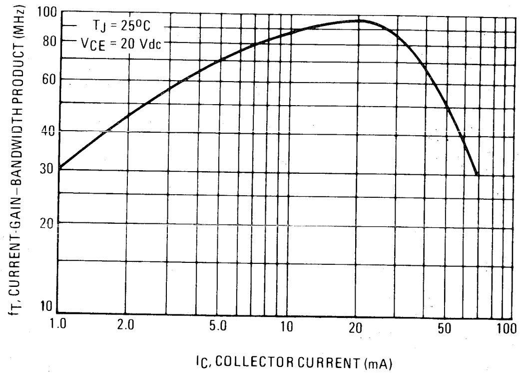


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT



3

FIGURE 4 – "ON" VOLTAGES

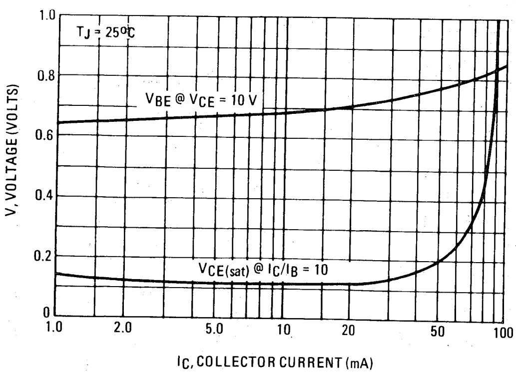
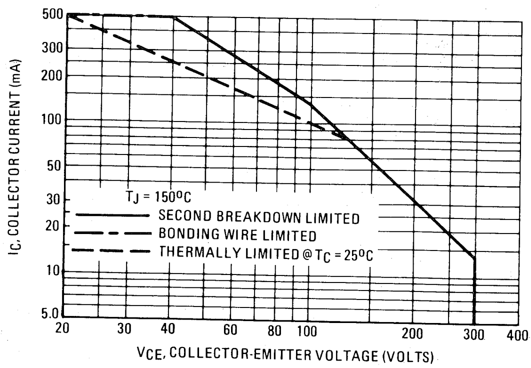


FIGURE 5 – DC SAFE OPERATING AREA



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

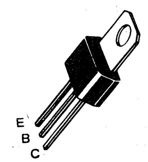
MPS-U95

PNP SILICON DARLINGTON AMPLIFIER TRANSISTOR

. . . designed for amplifier and driver applications.

- High DC Current Gain —
  h_{FE} = 25,000 (Min) @ I_C = 200 mAdc
  15,000 (Min) @ I_C = 500 mAdc
- Collector-Emitter Breakdown Voltage —
  $V_{(BR)CES}$ = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc @ I_C = 1.0 Adc
- Monolithic Construction for High Reliability
- Complement to NPN MPS-U45

PNP SILICON DARLINGTON TRANSISTOR



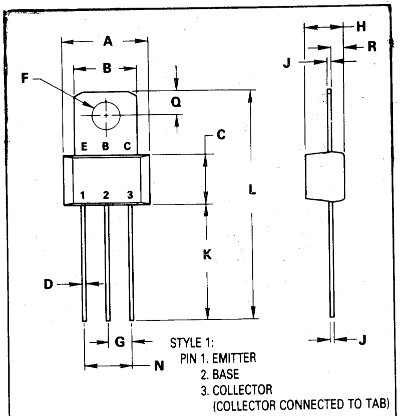
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}(1)	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current -Continuous	I_C	2.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(2)	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

(1) Due to the monolithic construction of this device, breakdown voltages of both transistor elements are identical, $V_{(BR)CES}$ is tested in lieu of $V_{(BR)CEO}$ in order to avoid errors caused by noise pickup. The voltage measured during the $V_{(BR)CES}$ test is the $V_{(BR)CEO}$ of the output transistor.
(2) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
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K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, V_{BE} = 0)	$V_{(BR)CES}$	40	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	50	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	10	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	–	–	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain	h_{FE}				–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)		25,000	43,000	150,000	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)		15,000	41,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		4,000	35,000	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{CE(sat)}$	–	1.0	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{BE(sat)}$	–	1.85	2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	1.7	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (1) (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	$\|h_{fe}\|$	0.5	1.6	–	–
Collector Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	2.5	12	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

Uniwatt Darlington transistors can be used in any number of low power applications, such as relay drivers, motor control and as general purpose amplifiers. As an audio amplifier these devices, when used as a complementary pair, can drive 3.5 watts into a 3.2 ohm speaker using a 14 volt supply with less than one percent distortion. Because of the high gain the base drive requirement is as low as 1 mA in this application. They are also useful as power drivers for high current application such as voltage regulators.

FIGURE 1 – DC CURRENT GAIN

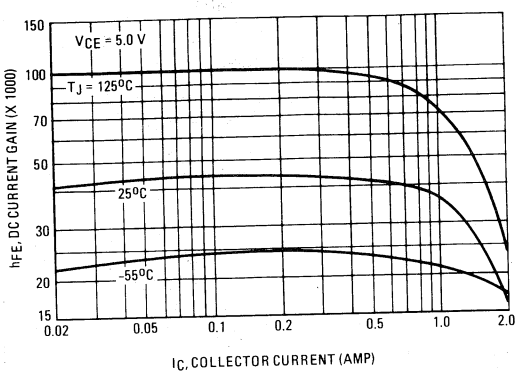


FIGURE 2 – SMALL-SIGNAL CURRENT GAIN

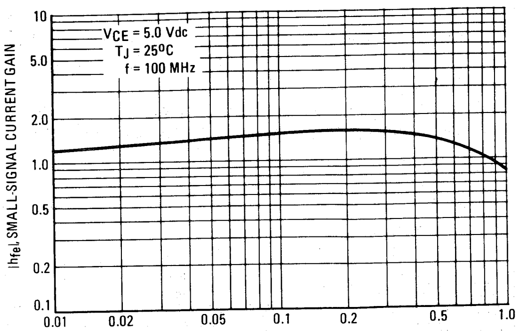


FIGURE 3 – "ON" VOLTAGES

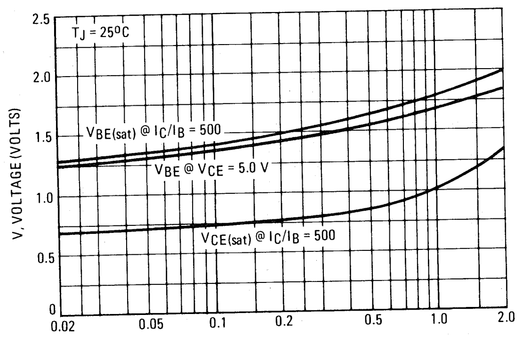


FIGURE 4 – TEMPERATURE COEFFICIENT

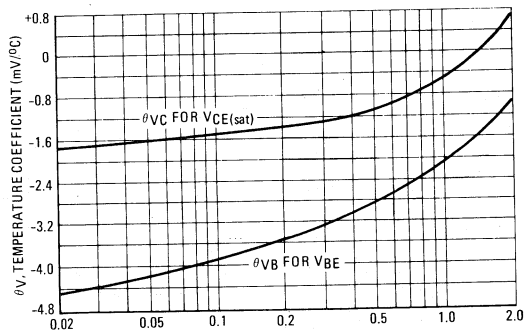
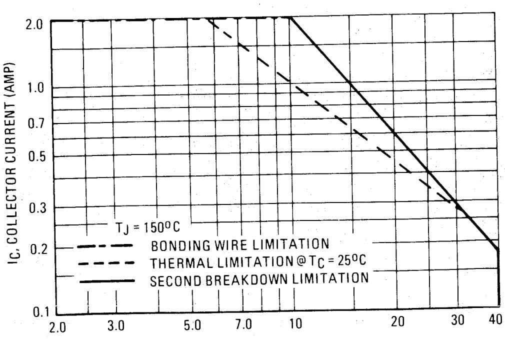


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

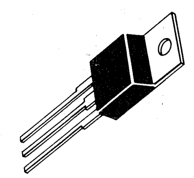
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
TIP29	TIP30
TIP29A	TIP30A
TIP29B	TIP30B
TIP29C	TIP30C

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications. Compact TO-220 AB package. TO-66 leadform also available.

1 AMPERE
POWER TRANSISTORS COMPLEMENTARY SILICON
40-60-80-100 VOLTS
30 WATTS



MAXIMUM RATINGS

Rating	Symbol	TIP29 TIP30	TIP29A TIP30A	TIP29B TIP30B	TIP29C TIP30C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current — Continuous Peak	I_C	← 1.0 → ← 3.0 →				Adc
Base Current	I_B	← 0.4 →				Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	← 30 → ← 0.24 →				Watts W/°C
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	← 2.0 → ← 0.016 →				Watts W/°C
Unclamped Inductive Load Energy (See Note 3)	E	← 32 →				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +150 →				°C

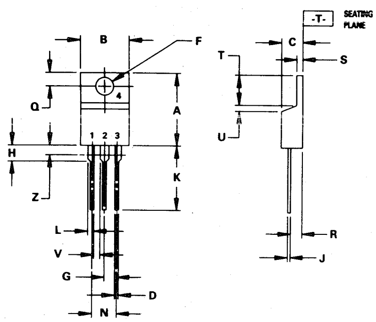
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.167	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP29, TIP30 TIP29A, TIP30A TIP29B, TIP30B TIP29C, TIP30C	$V_{CEO(sus)}$	40 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	TIP29, TIP29A, TIP30, TIP30A TIP29B, TIP29C, TIP30B, TIP30C	I_{CEO}	– –	0.3 0.3	mAdc
Collector Cutoff Current (V_{CE} = 40 Vdc, V_{EB} = 0) (V_{CE} = 60 Vdc, V_{EB} = 0) (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	TIP29, TIP30 TIP29A, TIP30A TIP29B, TIP30B TIP29C, TIP30C	I_{CES}	– – – –	200 200 200 200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.2 Adc, V_{CE} = 4.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	40 15	– 75	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 125 mAdc)		$V_{CE(sat)}$	–	0.7	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$
(3) This rating based on testing with L_C = 20 mH, R_{BE} = 100 Ω, V_{CC} = 10 V, I_C = 1.8 A, P.R.F. = 10 Hz.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

FIGURE 1 — DC CURRENT GAIN

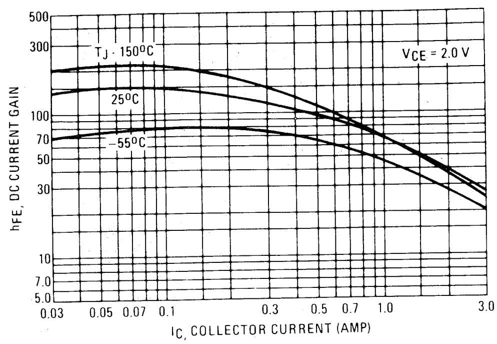


FIGURE 2 — TURN-OFF TIME

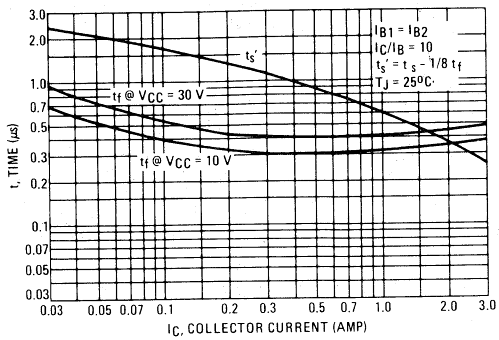


FIGURE 3 — SWITCHING TIME EQUIVALENT CIRCUIT

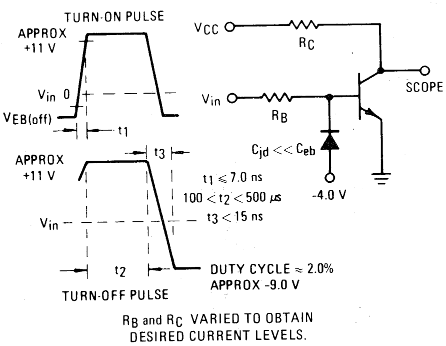


FIGURE 4 — TURN-ON TIME

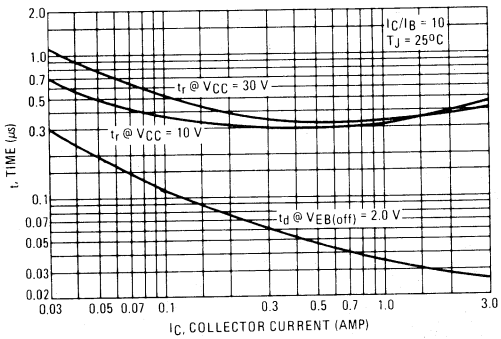
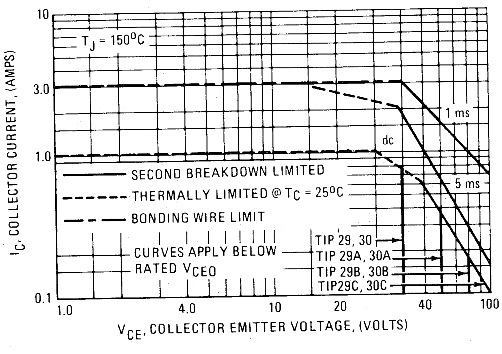


FIGURE 5 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{\circ}C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
TIP31	**TIP32**
TIP31A	**TIP32A**
TIP31B	**TIP32B**
TIP31C	**TIP32C**

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

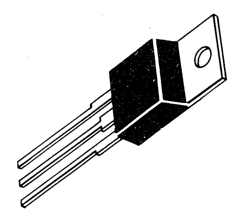
. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc (Min) — TIP31, TIP 32
  = 60 Vdc (Min) — TIP31A, TIP32A
  = 80 Vdc (Min) — TIP31B, TIP32B
  = 100 Vdc (Min) — TIP31C, TIP32C
- High Current Gain — Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220 AB Package
- TO-66 Leadform Also Available

3 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

40-60-80-100 VOLTS
40 WATTS



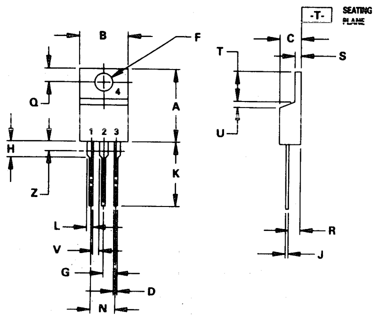
*MAXIMUM RATINGS

Rating	Symbol	TIP31 TIP32	TIP31A TIP32A	TIP31B TIP32B	TIP31C TIP32C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous Peak	I_C	3.0 5.0				Adc
Base Current	I_B	1.0				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32				Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016				Watts W/°C
Unclamped Inductive Load Energy (1)	E	32				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1.8 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP31, TIP32 TIP31A, TIP32A TIP31B, TIP32B TIP31C, TIP32C	$V_{CEO(sus)}$	40 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	TIP31, TIP31A, TIP32, TIP32A TIP31B, TIP31C, TIP32B, TIP32C	I_{CEO}	– –	0.3 0.3	mAdc
Collector Cutoff Current (V_{CE} = 40 Vdc, V_{EB} = 0) (V_{CE} = 60 Vdc, V_{EB} = 0) (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	TIP31, TIP32 TIP31A, TIP32A TIP31B, TIP32B TIP31C, TIP32C	I_{CES}	– – – –	200 200 200 200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	25 10	– 50	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 375 mAdc)		$V_{CE(sat)}$	–	1.2	Vdc
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		$\|h_{fe}\|$	20	–	–

(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 1 — POWER DERATING

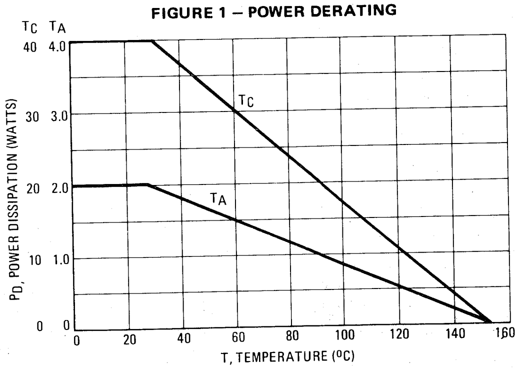
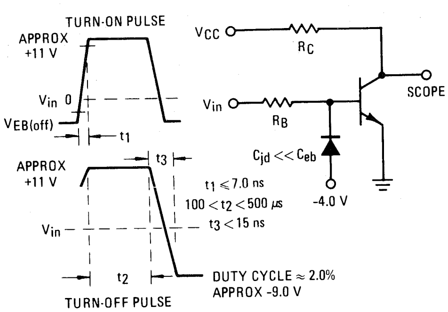
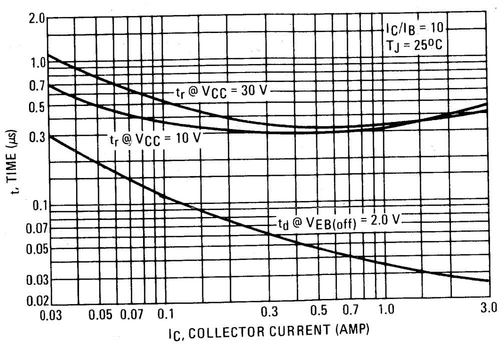


FIGURE 2 — SWITCHING TIME EQUIVALENT CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS.

FIGURE 3 — TURN-ON TIME



3

FIGURE 4 – THERMAL RESPONSE

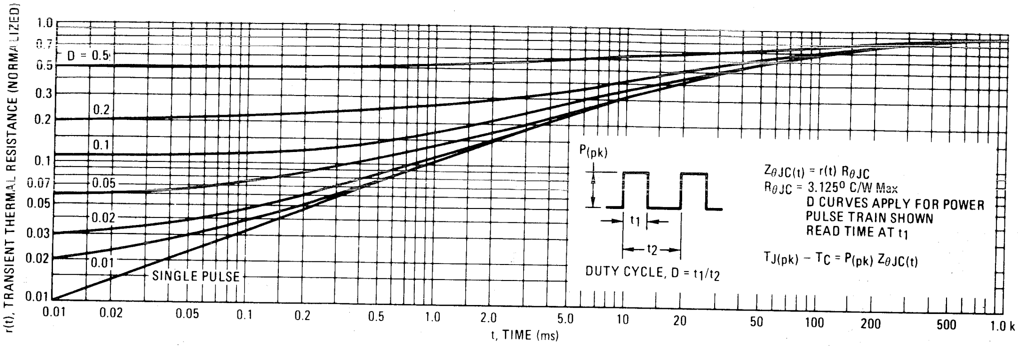
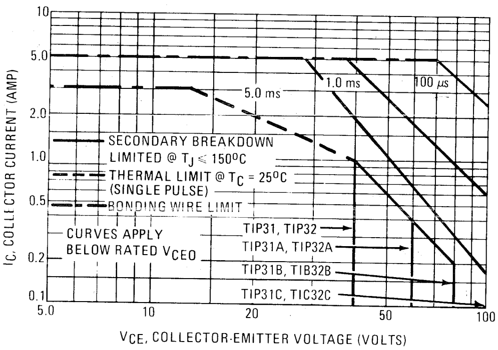


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

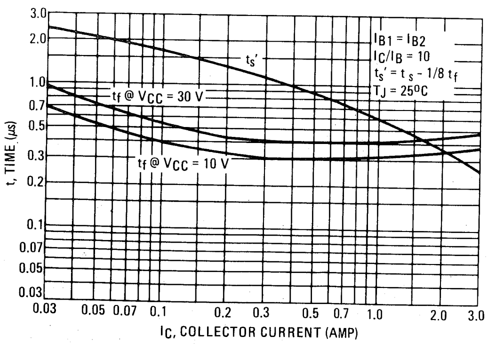


FIGURE 7 – CAPACITANCE

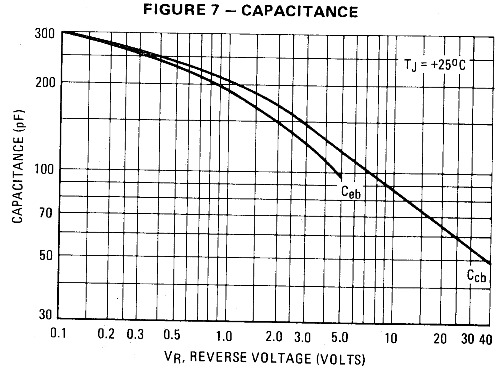


FIGURE 8 — DC CURRENT GAIN

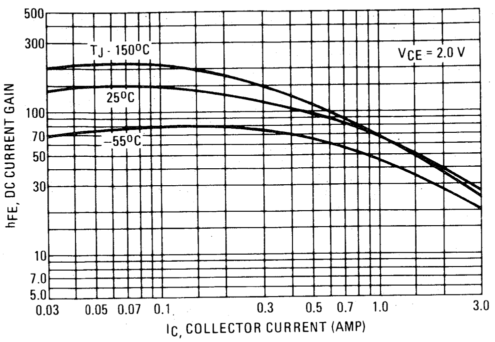


FIGURE 9 — COLLECTOR SATURATION REGION

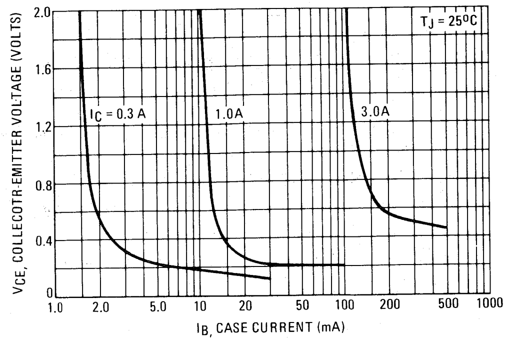


FIGURE 10 — "ON" VOLTAGES

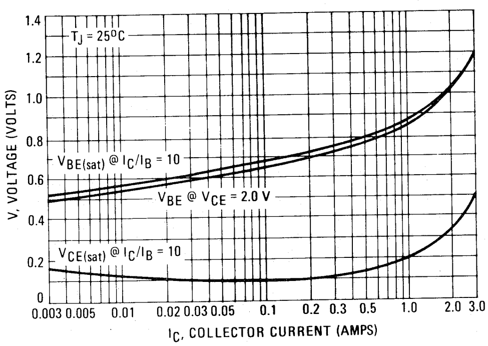


FIGURE 11 — TEMPERATURE COEFFICIENTS

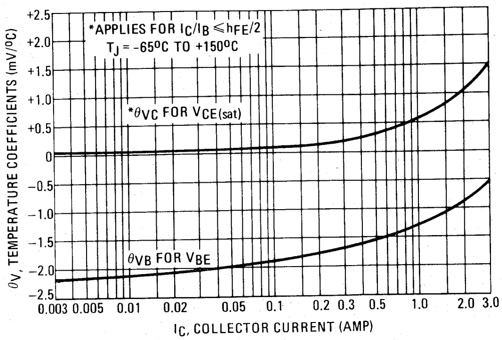


FIGURE 12 — COLLECTOR CUT-OFF REGION

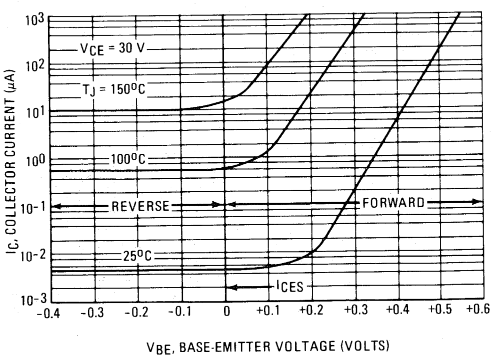
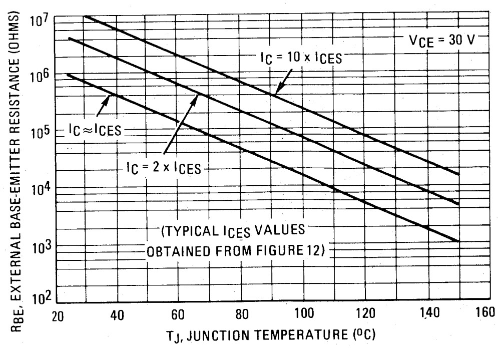


FIGURE 13 — EFFECTS OF BASE-EMITTER RESISTANCE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
TIP33	TIP34
TIP33A	TIP34A
TIP33B	TIP34B
TIP33C	TIP34C

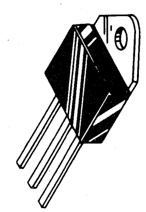
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . for general-purpose power amplifier and switching applications.

- 10 A Collector Current
- Low Leakage Current — I_{CEO} = 0.7 mA @ 30 and 60 V
- Excellent dc Gain — h_{FE} = 40 Typ @ 3.0 A
- High Current Gain Bandwidth Product — h_{fe} = 3.0 min @ I_C = 0.5 A, f = 1.0 MHz

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

40–100 VOLTS
80 WATTS



MAXIMUM RATINGS

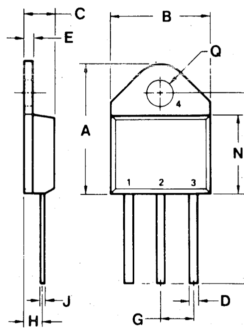
Rating	Symbol	TIP33 TIP34	TIP33A TIP34A	TIP33B TIP34B	TIP33C TIP34C	Unit
Collector-Emitter Voltage	V_{CEO}	40 V	60 V	80 V	100 V	Vdc
Collector-Base Voltage	V_{CB}	40 V	60 V	80 V	100 V	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current — Continuous Peak (1)	I_C	← 10 → ← 15 →				Adc
Base Current — Continous	I_B	← 3.0 →				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 80 → ← 0.64 →				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Junction-To-Free-Air Thermal Resistance	$R_{\theta JA}$	35.7	°C/W

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle ≤10%.

3

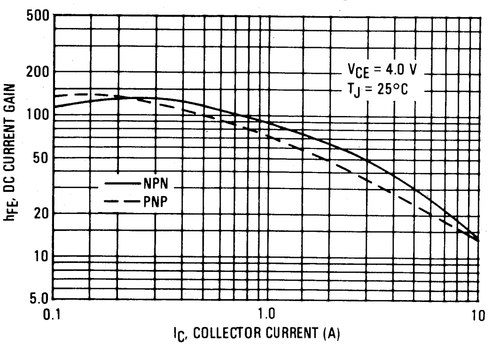


STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

FIGURE 1 — DC CURRENT GAIN



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mA, I_B = 0) TIP33, TIP34 / TIP33A, TIP34A / TIP33B, TIP34B / TIP33C, TIP34C	$V_{CEO(sus)}$	40 / 60 / 80 / 100	— / — / — / —	Vdc
Collector-Emitter Cutoff Current (V_{CE} = 30 V, I_B = 0) TIP33, TIP33A, TIP34, TIP34A / (V_{CE} = 60 V, I_B = 0) TIP33B, TIP33C, TIP34B, TIP34C	I_{CEO}	— / —	0.7 / 0.7	mA
Collector-Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)	I_{CES}	—	0.4	mA
Emitter-Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)	I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 1.0 A, V_{CE} = 4.0 V) / (I_C = 3.0 A, V_{CE} = 4.0 V)	h_{FE}	40 / 20	— / 100	—
Collector-Emitter Saturation Voltage (I_C = 3.0 A, I_B = 0.3 A) / (I_C = 10 A, I_B = 2.5 A)	$V_{CE(sat)}$	— / —	1.0 / 4.0	Vdc
Base-Emitter On Voltage (I_C = 3.0 A, V_{CE} = 4.0 V) / (I_C = 10 A, V_{CE} = 4.0 V)	$V_{BE(on)}$	— / —	1.6 / 3.0	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I_C = 0.5 A, V_{CE} = 10 V, f = 1.0 kHz)	h_{fe}	20	—	—
Current-Gain—Bandwidth Product (2) (I_C = 0.5 A, V_{CE} = 10 V, f = 1.0 MHz)	f_T	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

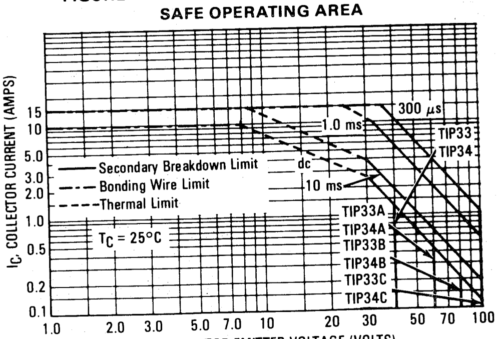
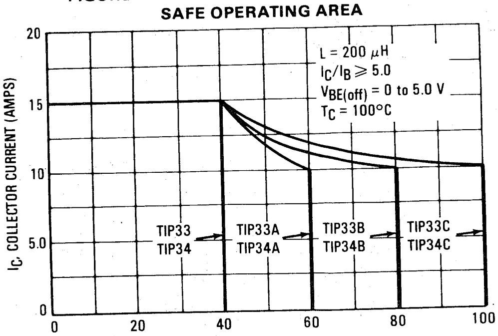


FIGURE 3 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



FORWARD BIAS

The Forward Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during forward bias. The data is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%, and must be derated thermally for T_C > 25°C.

REVERSE BIAS

The Reverse Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during reverse biased turn-off. This rating is verified under clamped conditions so the device is never subjected to an avalanche mode.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
TIP35	**TIP36**
TIP35A	**TIP36A**
TIP35B	**TIP36B**
TIP35C	**TIP36C**

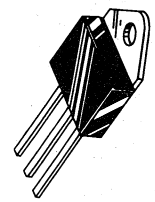
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . for general-purpose power amplifier and switching applications.

- 25 A Collector Current
- Low Leakage Current — I_{CEO} = 1.0 mA @ 30 and 60 V
- Excellent dc Gain — h_{FE} = 40 Typ @ 15 A
- High Current Gain Bandwidth Product — (h_{fe} = 3.0 min @ I_C = 1.0 A, f = 1.0 MHz

25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

40-100 VOLTS
125 WATTS



MAXIMUM RATINGS

Rating	Symbol	TIP35 TIP36	TIP35A TIP36A	TIP35B TIP36B	TIP35C TIP36C	Unit
Collector-Emitter Voltage	V_{CEO}	40 V	60 V	80 V	100 V	Vdc
Collector-Base Voltage	V_{CB}	40 V	60 V	80 V	100 V	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current — Continuous Peak (1)	I_C	← 25 → ← 40 →				Adc
Base Current — Continous	I_B	← 5.0 →				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 125 → ← 1.0 →				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C
Unclamped Inductive Load	E_{SB}	90				mJ

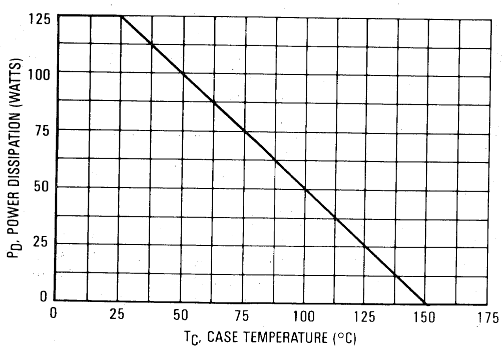
THERMAL CHARACTERISTICS

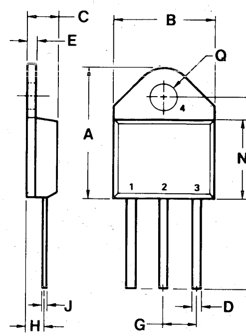
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Junction-To-Free-Air Thermal Resistance	$R_{\theta JA}$	35.7	°C/W

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle ≤10%.

3

FIGURE 1 — POWER DERATING





STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

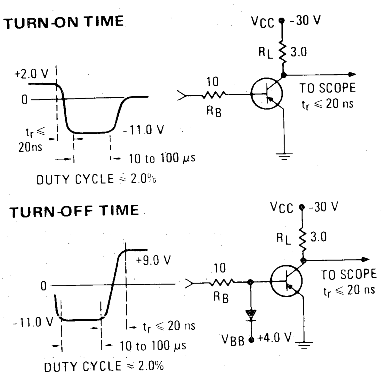
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mA, I_B = 0) TIP35, TIP36	$V_{CEO(sus)}$	40	—	Vdc
TIP35A, TIP36A		60	—	
TIP35B, TIP36B		80	—	
TIP35C, TIP36C		100	—	
Collector-Emitter Cutoff Current (V_{CE} = 30 V, I_B = 0) TIP35, TIP35A, TIP36, TIP36A	I_{CEO}	—	1.0	mA
(V_{CE} = 60 V, I_B = 0) TIP35B, TIP35C, TIP36B, TIP36C		—	1.0	
Collector-Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)	I_{CES}	—	0.7	mA
Emitter-Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)	I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 1.5 A, V_{CE} = 4.0 V)	h_{FE}	25	—	—
(I_C = 15 A, V_{CE} = 4.0 V)		15	75	
Collector-Emitter Saturation Voltage (I_C = 15 A, I_B = 1.5 A)	$V_{CE(sat)}$	—	1.8	Vdc
(I_C = 25 A, I_B = 5.0 A)		—	4.0	
Base-Emitter On Voltage (I_C = 15 A, V_{CE} = 4.0 V)	$V_{BE(on)}$	—	2.0	Vdc
(I_C = 25 A, V_{CE} = 4.0 V)		—	4.0	
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 kHz)	h_{fe}	25	—	—
Current-Gain—Bandwidth Product (2) (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 MHz)	f_T	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$

3

FIGURE 2 — SWITCHING TIME EQUIVALENT TEST CIRCUITS



FOR CURVES OF FIGURES 3 & 4, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES.

FIGURE 3 — TURN-ON TIME

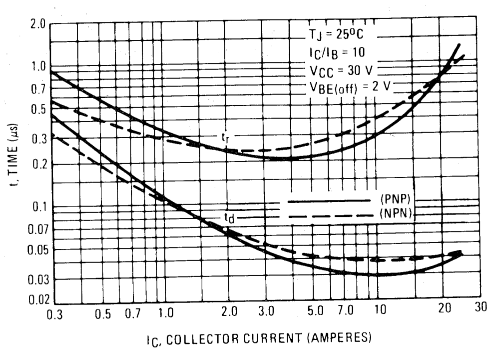


FIGURE 4 — TURN-OFF TIME

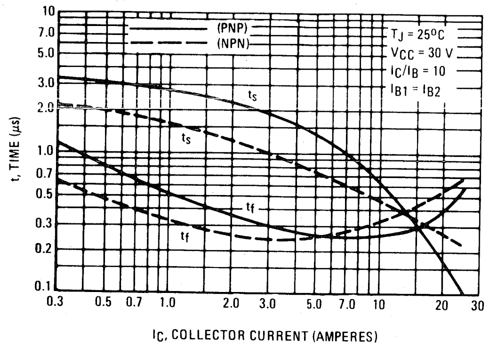
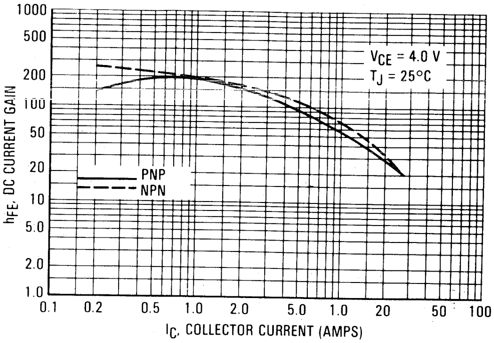


FIGURE 5 — DC CURRENT GAIN

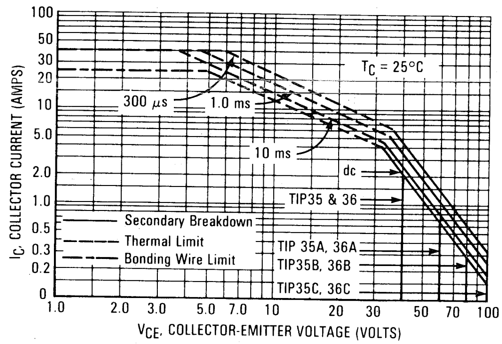


FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations.

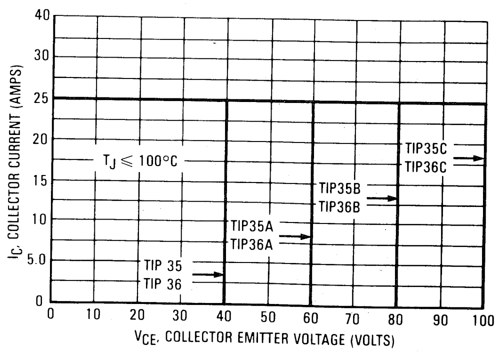
FIGURE 6 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



REVERSE BIAS

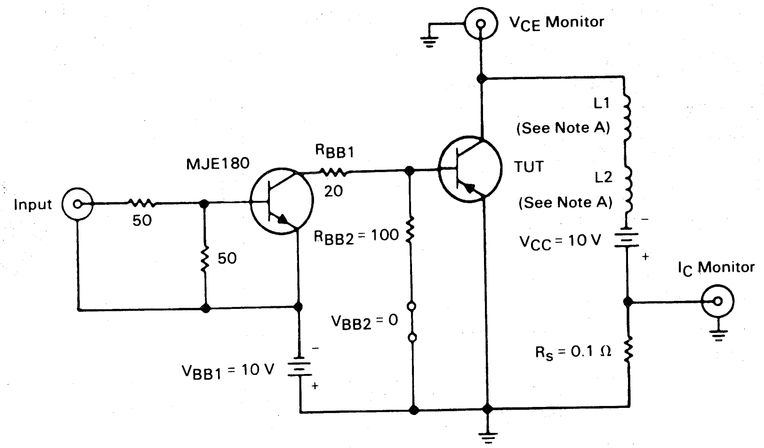
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.

FIGURE 7 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

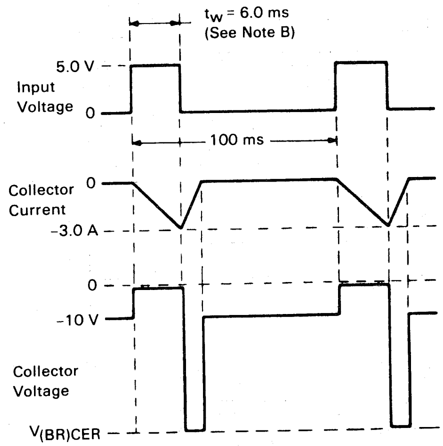


3

FIGURE 8 — INDUCTIVE LOAD SWITCHING



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES:

A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C-2688, or equivalent.

B. Input pulse width is increased until $I_{CM} = -3.0$ A.

C. For NPN, reverse all polarities.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
TIP41	TIP42
TIP41A	TIP42A
TIP41B	TIP42B
TIP41C	TIP42C

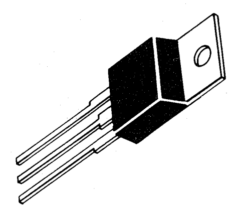
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc (Min) – TIP41, TIP42
  = 60 Vdc (Min) – TIP41A, TIP42A
  = 80 Vdc (Min) – TIP41B, TIP42B
  = 100 Vdc (Min) – TIP41C, TIP42C
- High Current Gain — Bandwidth Product f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220AB Package
- TO-66 Leadform Also Available

6 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

40-60-80-100 VOLTS
65 WATTS



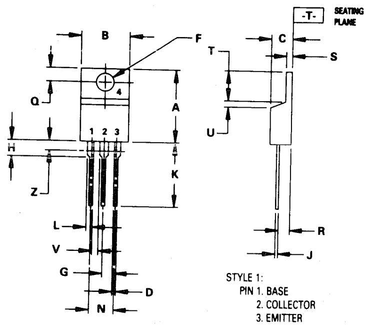
*MAXIMUM RATINGS

Rating	Symbol	TIP41 TIP42	TIP41A TIP42A	TIP41B TIP42B	TIP41C TIP42C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current - Continuous	I_C	← 6 →				Adc
Peak		← 10 →				
Base Current	I_B	← 2.0 →				Adc
Total Power Dissipation @ T_C = 25°C	P_D	← 65 →				Watts
Derate above 25°C		← 0.52 →				W/°C
Total Power Dissipation @ T_A = 25°C	P_D	← 2.0 →				Watts
Derate above 25°C		← 0.016 →				W/°C
Unclamped Inductive Load Energy (1)	E	← 62.5 →				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +150 →				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 2.5 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10V, R_{BE} = 100 Ω.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	$V_{CEO(sus)}$	40 60 80 100	— — — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	TIP41, TIP41A, TIP42, TIP42A TIP41B, TIP41C, TIP42B, TIP42C	I_{CEO}	— —	0.7 0.7	mAdc
Collector Cutoff Current (V_{CE} = 40 Vdc, V_{EB} = 0) (V_{CE} = 60 Vdc, V_{EB} = 0) (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	I_{CES}	— — — —	400 400 400 400	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	30 15	— 75	—
Collector-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 600 mAdc)		$V_{CE(sat)}$	—	1.5	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	—	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		$\|h_{fe}\|$	20	—	—

(1) Pulse Test: Pulsewidth ⩽ 300 μs, Duty Cycle ⩽ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 1 — POWER DERATING

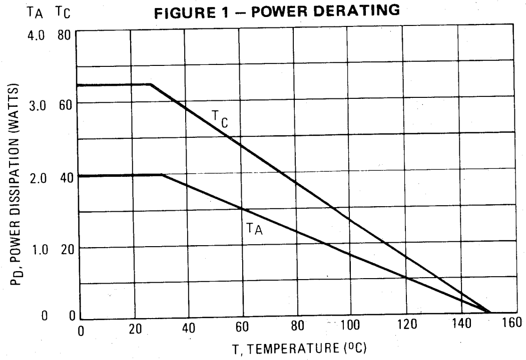


FIGURE 2 — SWITCHING TIME TEST CIRCUIT

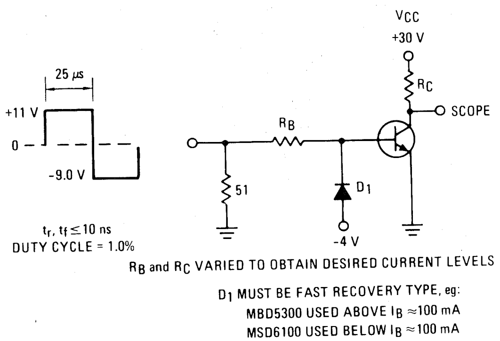


FIGURE 3 — TURN-ON TIME

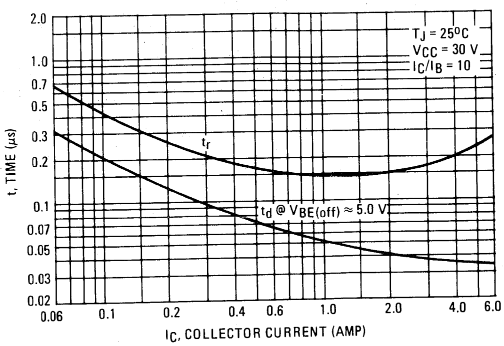


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FIGURE 4 — THERMAL RESPONSE

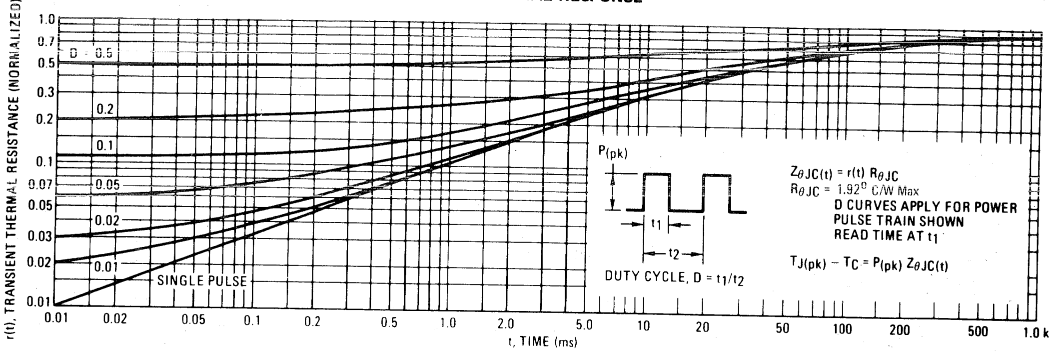
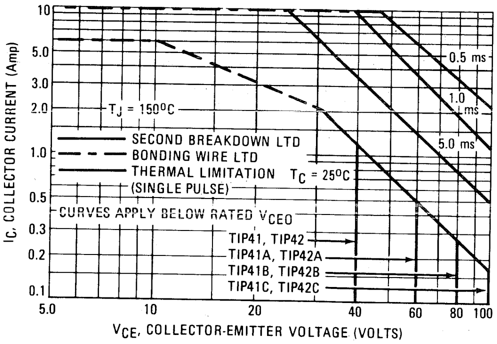


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 — TURN-OFF TIME

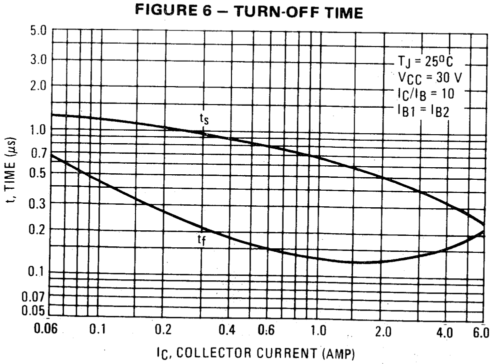


FIGURE 7 — CAPACITANCE

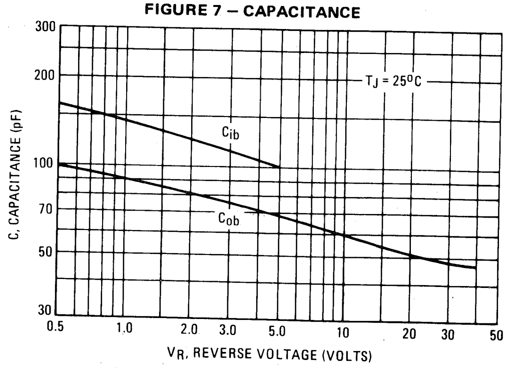


FIGURE 8 — DC CURRENT GAIN

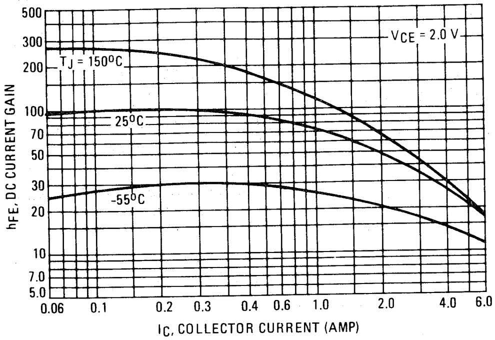


FIGURE 9 — COLLECTOR SATURATION REGION

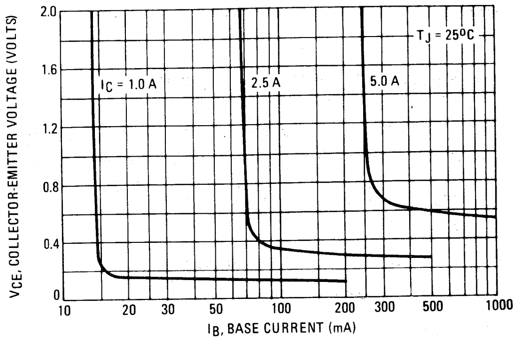


FIGURE 10 — "ON" VOLTAGES

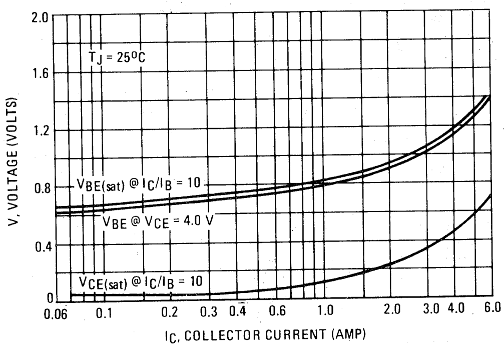


FIGURE 11 — TEMPERATURE COEFFICIENTS

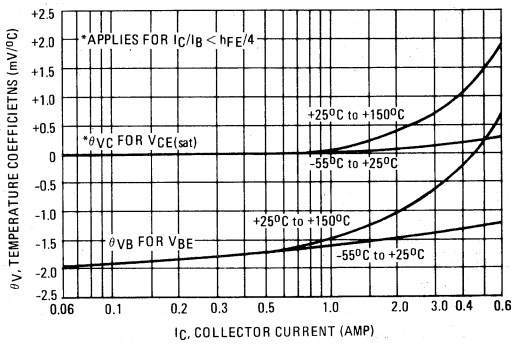


FIGURE 12 — COLLECTOR CUT-OFF REGION

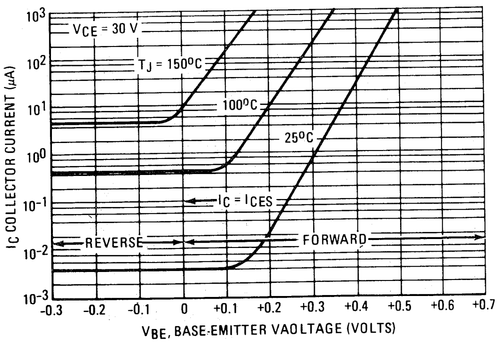
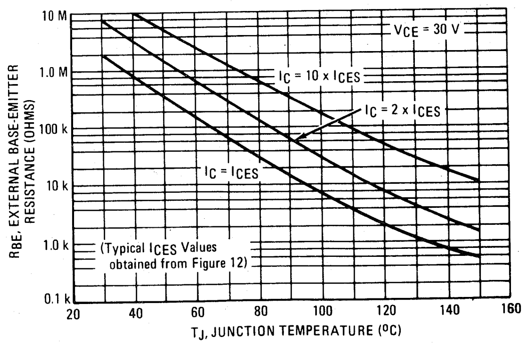


FIGURE 13 — EFFECTS OF BASE-EMITTER RESISTANCE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

TIP47 TIP48 TIP49 TIP50

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

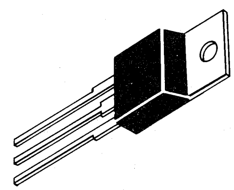
. . . designed for line operated audio output amplifier, Switchmode power supply drivers and other switching applications.

- 250 V to 400 V (Min) — $V_{CEO(sus)}$
- 1 A Rated Collector Current
- Popular TO-220 Plastic Package
- TO-66 Leadform Available

1.0 AMPERE

POWER TRANSISTORS NPN SILICON

250-300-350-400 VOLTS
40 WATTS



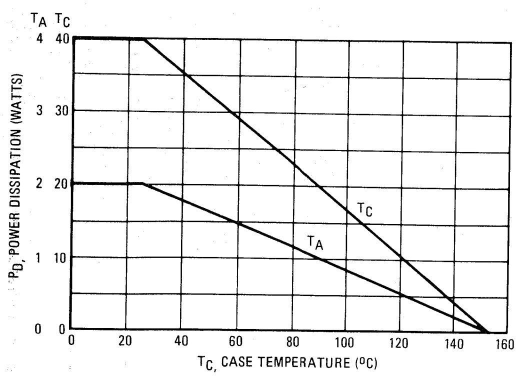
MAXIMUM RATINGS

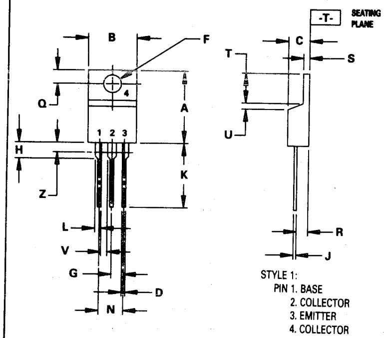
Rating	Symbol	TIP47	TIP48	TIP49	TIP50	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	400	Vdc
Collector-Base Voltage	V_{CB}	350	400	450	500	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current—Continuous Peak	I_C	← 1.0 → ← 2.0 →				Adc
Base Current	I_B	← 0.6 →				Adc
Total Power Dissipation @ T_C = 25° C Derate above 25° C	P_D	← 40 → ← 0.32 →				Watts W/°C
Total Power Dissipation @ T_A = 25° C Derate above 25° C	P_D	← 2.0 → ← 0.016 →				Watts W/°C
Unclamped Inducting Load Energy (See Figure 8)	E	← 20 →				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP47 TIP48 TIP49 TIP50	$V_{CEO(sus)}$	250 300 350 400	— — — —	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0) (V_{CE} = 250 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	TIP47 TIP48 TIP49 TIP50	I_{CEO}	— — — —	1.0 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0) (V_{CE} = 400 Vdc, V_{BE} = 0) (V_{CE} = 450 Vdc, V_{BE} = 0) (V_{CE} = 500 Vdc, V_{BE} = 0)	TIP47 TIP48 TIP49 TIP50	I_{CES}	— — — —	1.0 1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		h_{FE}	30 10	150 —	—
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	—	1.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)		f_T	10	—	MHz
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

FIGURE 2 — SWITCHING TIME EQUIVALENT CIRCUIT

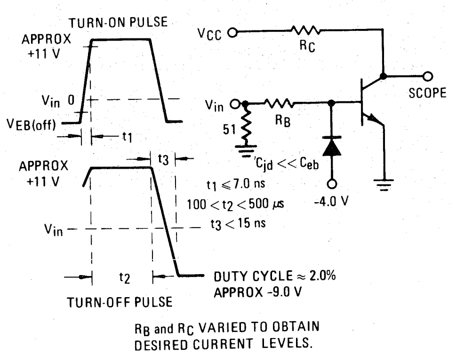


FIGURE 3 — TURN-ON TIME

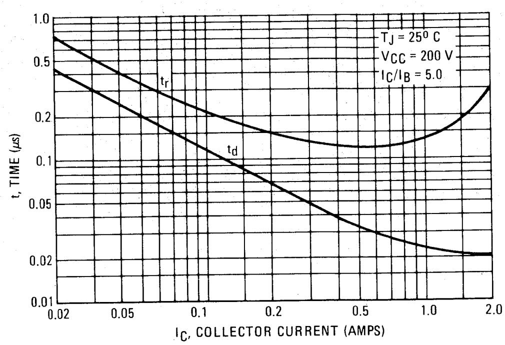


FIGURE 4 – THERMAL RESPONSE

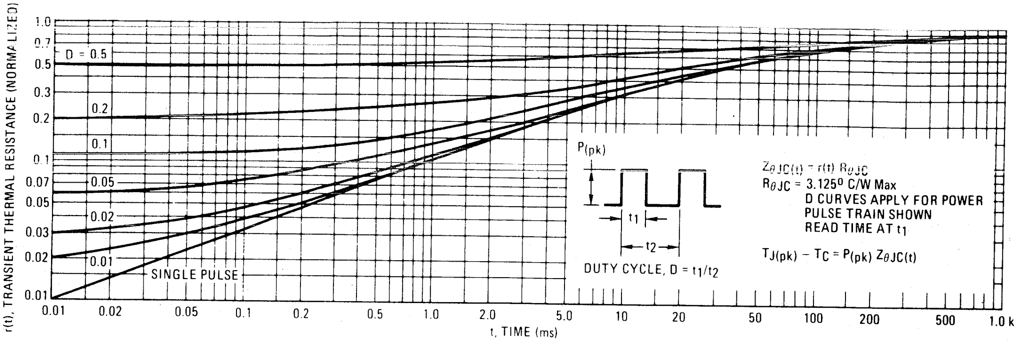
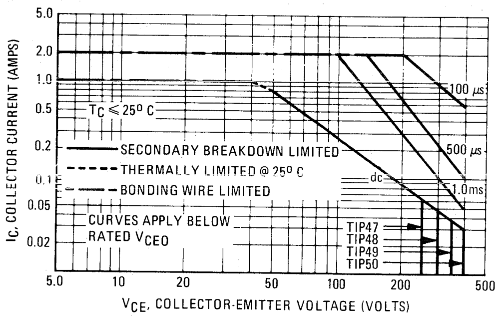


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

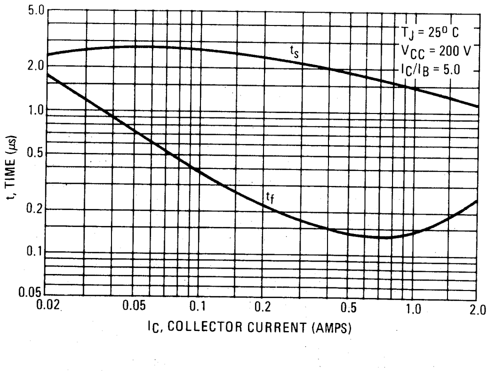


FIGURE 7 – TEMPERATURE COEFFICIENTS

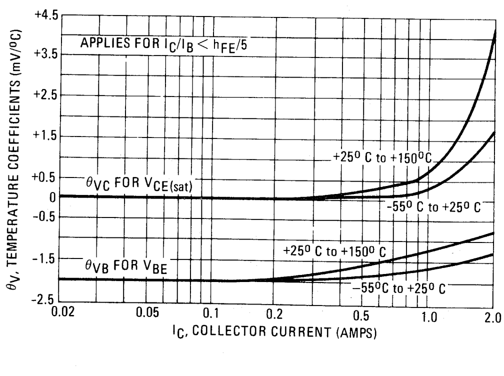
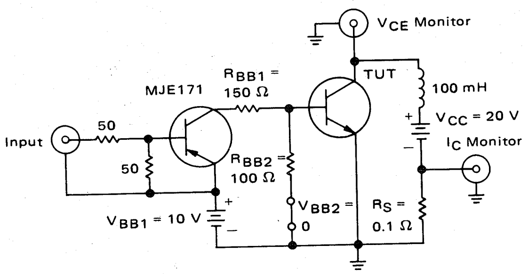


FIGURE 8 – INDUCTIVE LOAD SWITCHING

Test Circuit



Note A: Input pulse width is increased until I_{CM} = 0.63 A.

Voltage and Current Waveforms

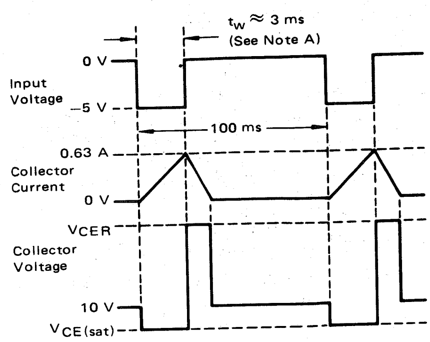


FIGURE 9 – DC CURRENT GAIN

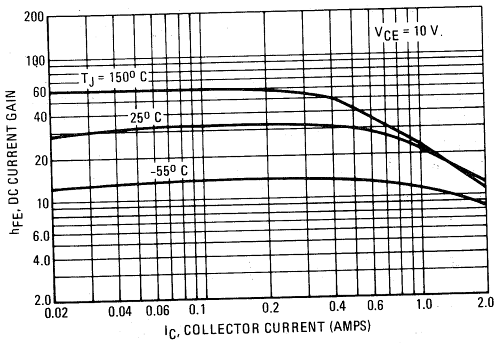
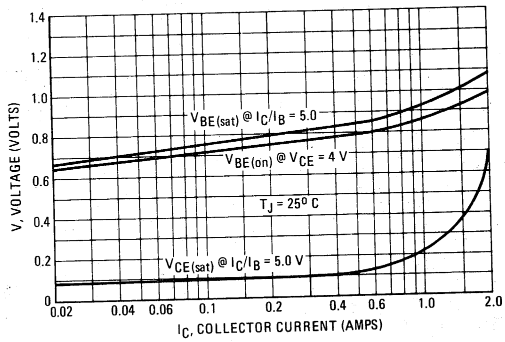


FIGURE 10 – "ON" VOLTAGES



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

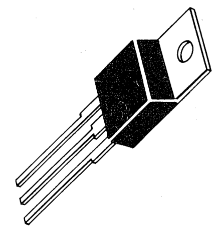
NPN	PNP
TIP100	**TIP105**
TIP101	**TIP106**
TIP102	**TIP107**

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP100, TIP105
  = 80 Vdc (Min) — TIP101, TIP106
  = 100 Vdc (Min) — TIP102, TIP107
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 2.5 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
80 WATTS



*MAXIMUM RATINGS

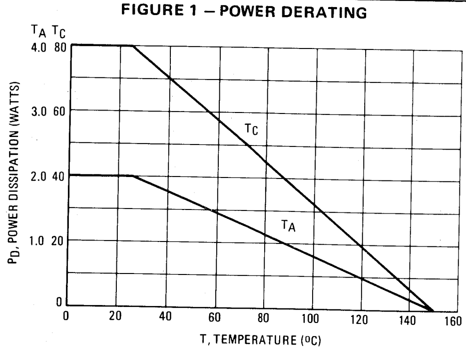
Rating	Symbol	TIP100, TIP105	TIP101, TIP106	TIP102, TIP107	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous	I_C	← 8.0 →			Adc
Peak		← 15 →			
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ T_C = 25°C	P_D	← 80 →			Watts
Derate above 25°C		← 0.64 →			W/°C
Unclamped Inductive Load Energy (1)	E	← 30 →			mJ
Total Power Dissipation @ T_A = 25°C	P_D	← 2.0 →			Watts
Derate above 25°C		← 0.016 →			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

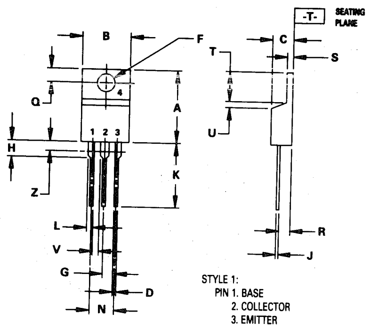
THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1.1 A, L = 50 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
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DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP100, TIP105 TIP101, TIP106 TIP102, TIP107	$V_{CEO(sus)}$	60 80 100	– – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	TIP100, TIP105 TIP101, TIP106 TIP102, TIP107	I_{CEO}	– – –	50 50 50	μAdc
Collector Cuttoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	TIP100, TIP105 TIP101, TIP106 TIP102, TIP107	I_{CBO}	– – –	50 50 50	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	8.0	mAdc
ON-CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	1000 200	20,000 –	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 6.0 mAdc) (I_C = 8.0 Adc, I_B = 80 mAdc)		$V_{CE(sat)}$	– –	2.0 2.5	Vdc
Base-Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP105, TIP106, TIP107 TIP100, TIP101, TIP102	C_{ob}	– –	300 200	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

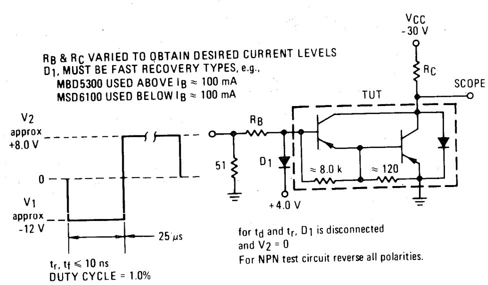


FIGURE 3 – SWITCHING TIMES

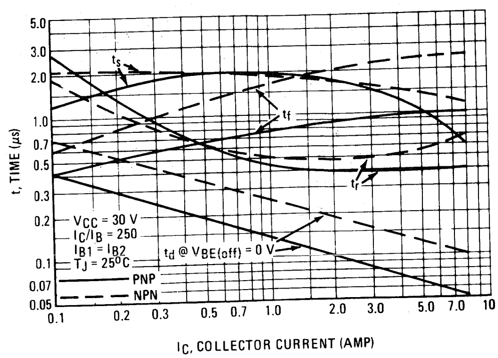


FIGURE 4 – THERMAL RESPONSE

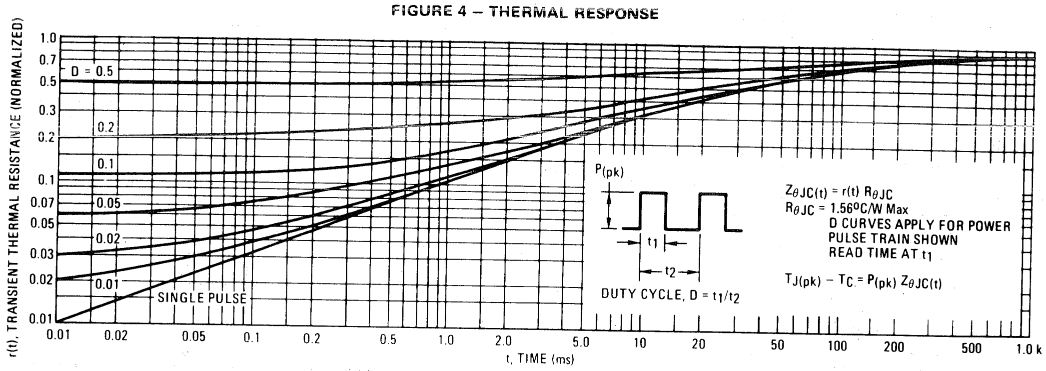
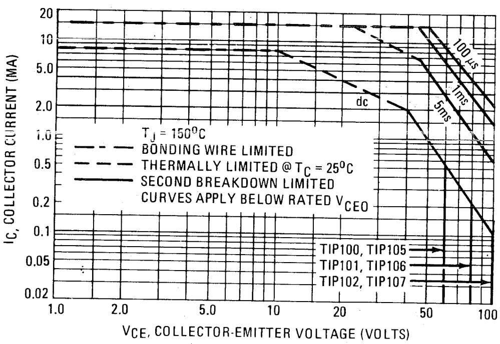


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

3

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

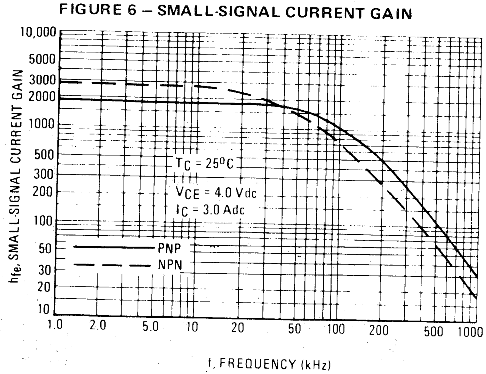
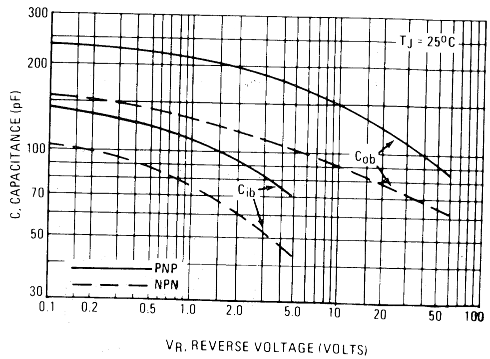


FIGURE 7 – CAPACITANCE



NPN	PNP
TIP100, TIP101, TIP102	TIP105, TIP106, TIP107

FIGURE 8 — DC CURRENT GAIN

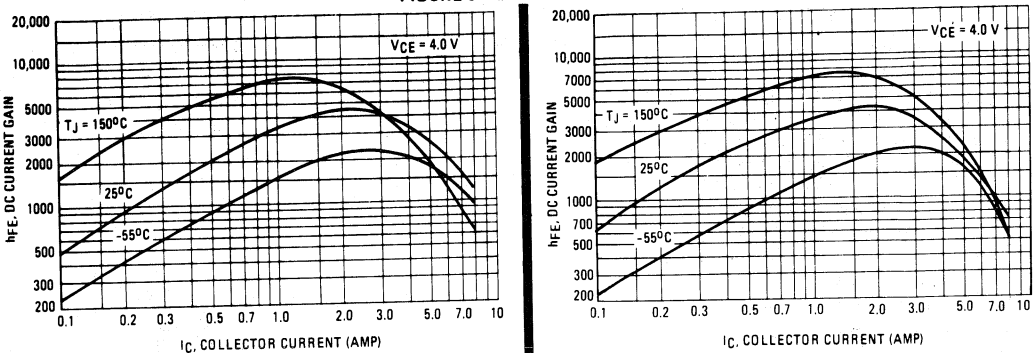


FIGURE 9 — COLLECTOR SATURATION REGION

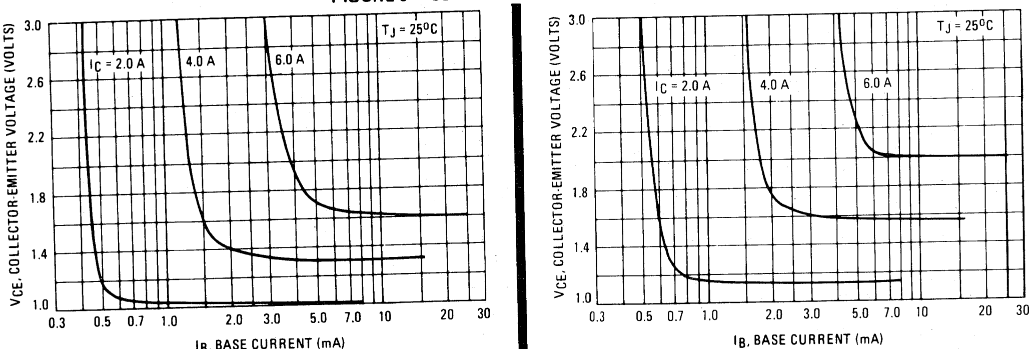
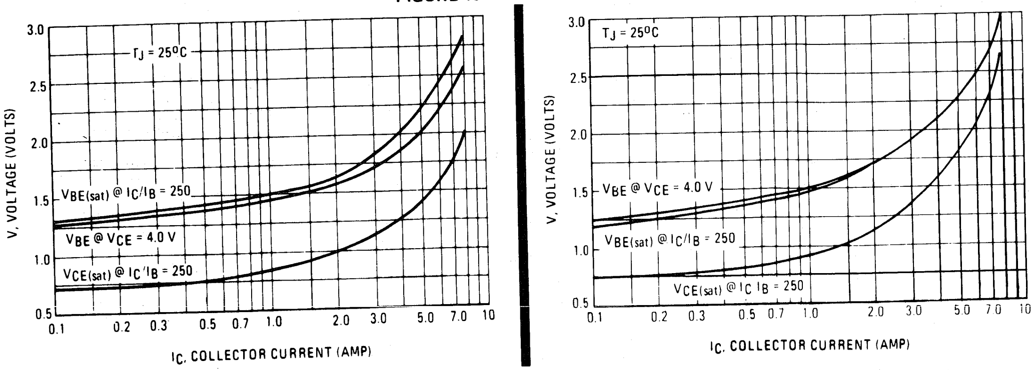


FIGURE 10 — "ON" VOLTAGES



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
TIP110	TIP115
TIP111	TIP116
TIP112	TIP117

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

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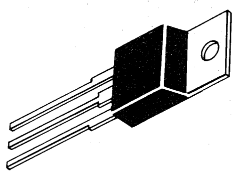
DARLINGTON
2 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
50 WATTS



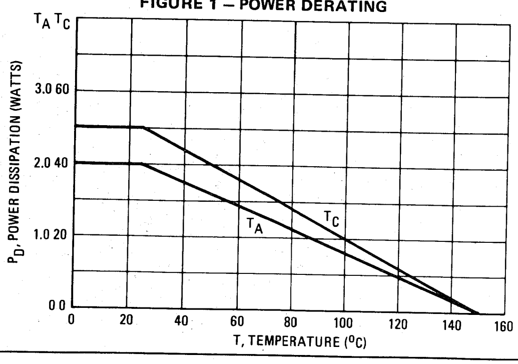
*MAXIMUM RATINGS

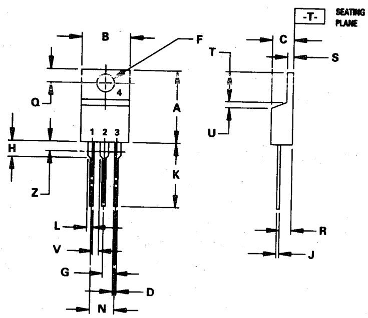
Rating	Symbol	TIP110, TIP115	TIP111, TIP116	TIP112, TIP117	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 2.0 → ← 4.0 →			Adc
Base Current	I_B	← 50 →			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 50 → ← 0.4 →			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 0.016 →			Watts W/°C
Unclamped Inductive Load Energy — Figure 13	E	← 25 →			mJ
Operating and Storage Junction,	T_J, T_{stg}	← −65 to +150 →			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 — POWER DERATING





NOTES:
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STYLE 1:
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3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
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B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
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H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP110, TIP115 TIP111, TIP116 TIP112, TIP117	$V_{CEO(sus)}$	60 80 100	— — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	TIP110, TIP115 TIP111, TIP116 TIP112, TIP117	I_{CEO}	— — —	2.0 2.0 2.0	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	TIP110, TIP115 TIP111, TIP116 TIP112, TIP117	I_{CBO}	— — —	1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	1000 500	— —	—
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 8.0 mAdc)		$V_{CE(sat)}$	—	2.5	Vdc
Base-Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	25	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP115, TIP116, TIP117 TIP110, TIP111, TIP112	C_{ob}	— —	200 100	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

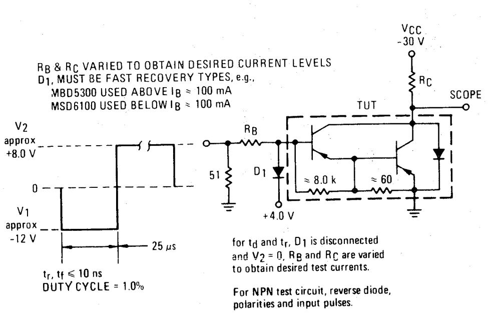


FIGURE 3 – SWITCHING TIMES

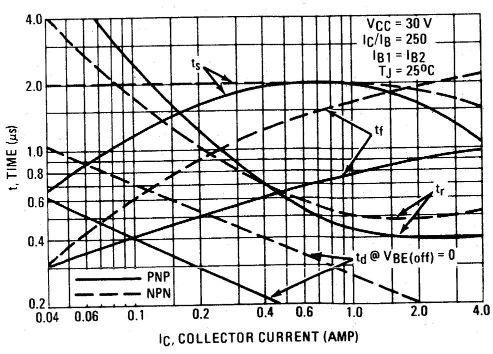
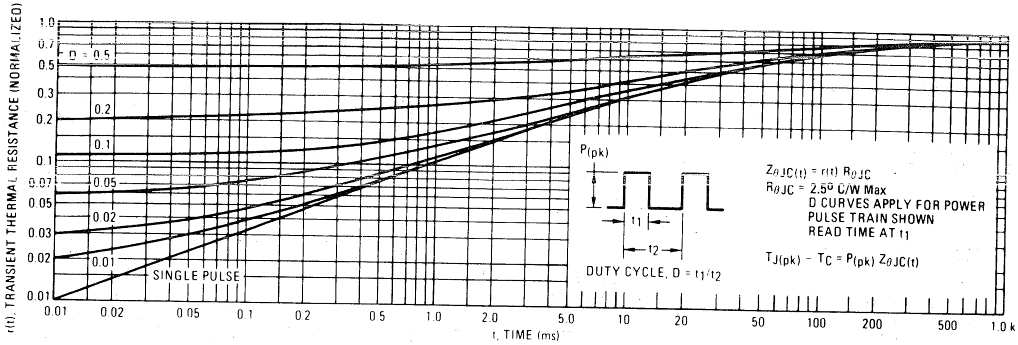


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 5 – TIP115, 116, 117

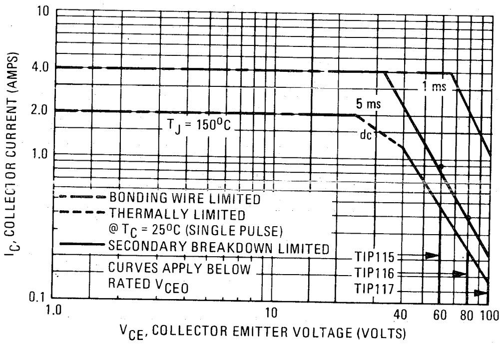
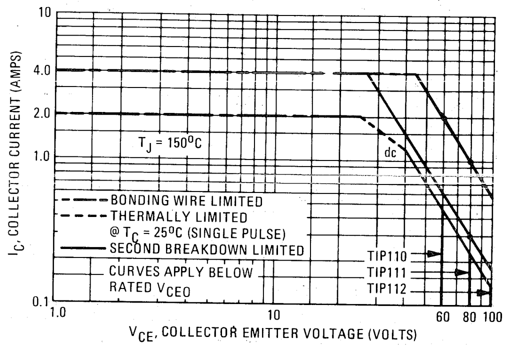


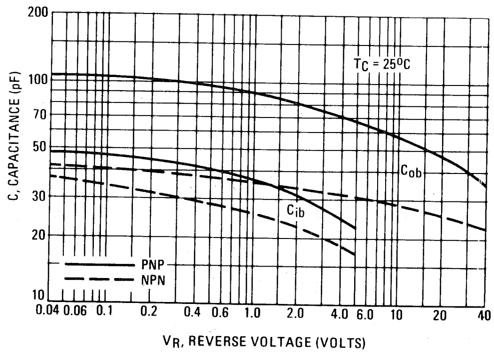
FIGURE 6 – TIP110, 111, 112



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 – CAPACITANCE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
TIP120	**TIP125**
TIP121	**TIP126**
TIP122	**TIP127**

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  = 80 Vdc (Min) — TIP121, TIP126
  = 100 Vdc (Min) — TIP122, TIP127
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DARLINGTON
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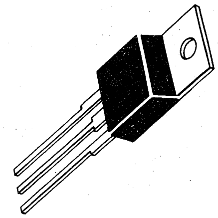
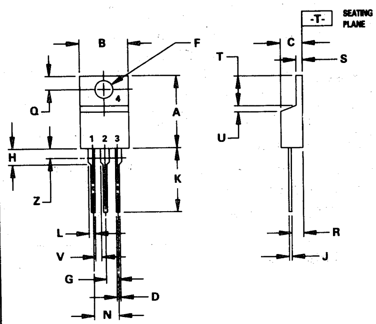
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
65 WATTS





NOTES:
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3. EMITTER
4. COLLECTOR

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T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

*MAXIMUM RATINGS

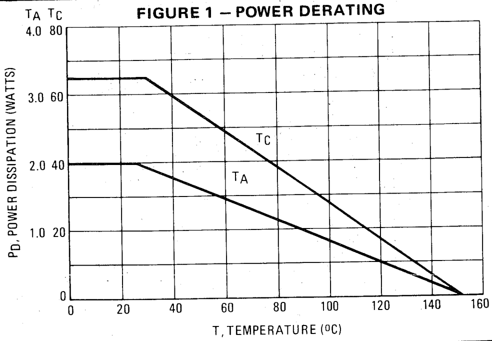
Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 5.0 → ← 8.0 →			Adc
Base Current	I_B	← 120 →			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 65 → ← 0.52 →			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 0.016 →			Watts W/°C
Unclamped Inductive Load Energy (1)	E	← 50 →			mJ
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1 A, L = 100 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

FIGURE 1 — POWER DERATING



3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	$V_{CEO(sus)}$	60 80 100	– – –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	I_{CEO}	– – –	0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	I_{CBO}	– – –	0.2 0.2 0.2	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000 1000	– –	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc) (I_C = 5.0 Adc, I_B = 20 mAdc)		$V_{CE(sat)}$	– –	2.0 4.0	Vdc
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP125, TIP126, TIP127 TIP120, TIP121, TIP122	C_{ob}	– –	300 200	pF

(1) Pulse Test: Pulse Width ⩽ 300 μs, Duty Cycle ⩽ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

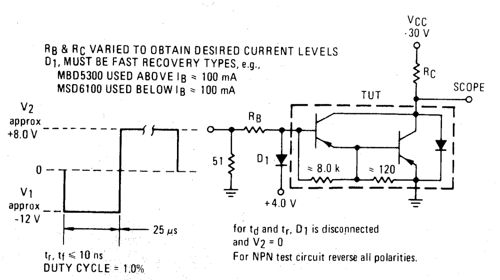


FIGURE 3 – SWITCHING TIMES

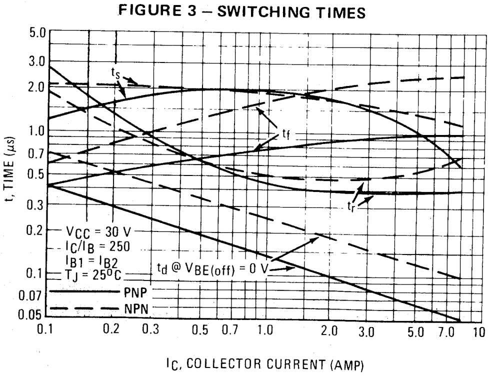


FIGURE 4 – THERMAL RESPONSE

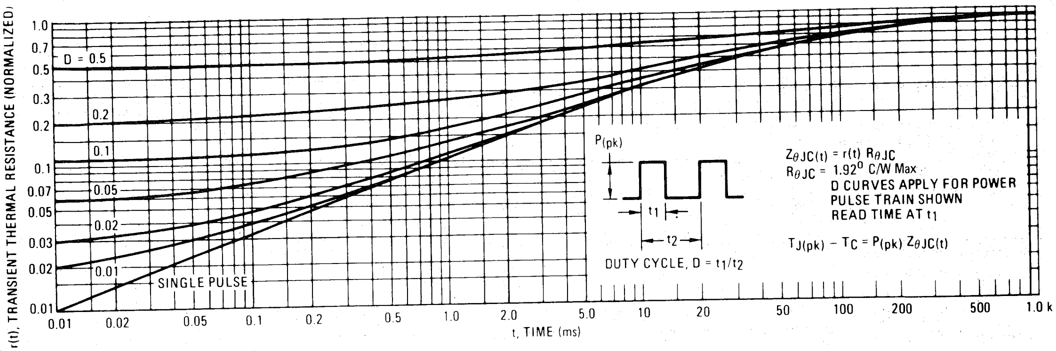
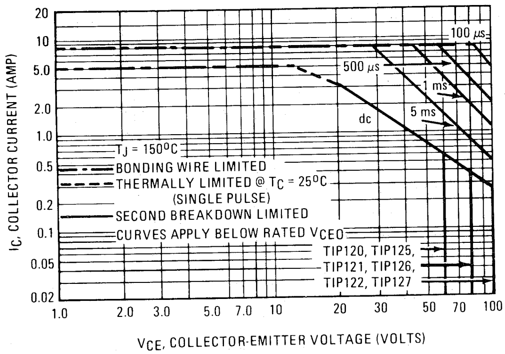


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

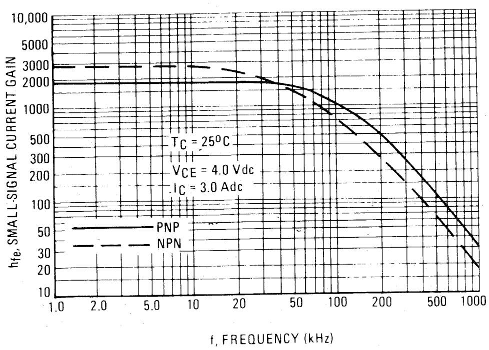
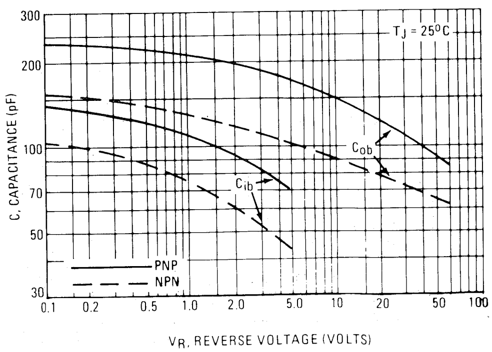


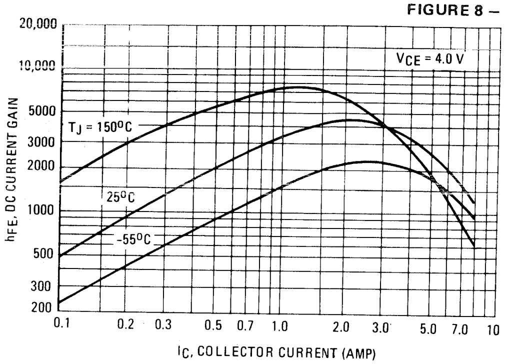
FIGURE 7 – CAPACITANCE



3

FIGURE 8 – DC CURRENT GAIN

NPN
TIP120, TIP121, TIP122



PNP
TIP125, TIP126, TIP127

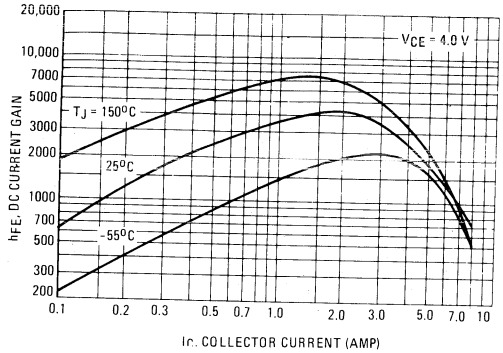
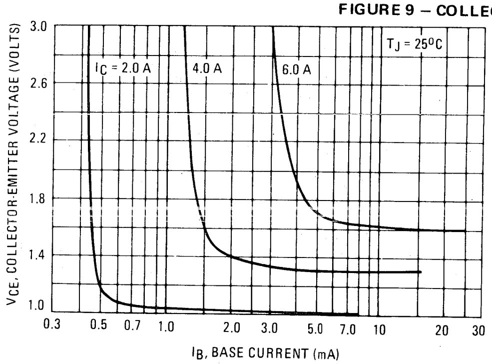


FIGURE 9 – COLLECTOR SATURATION REGION



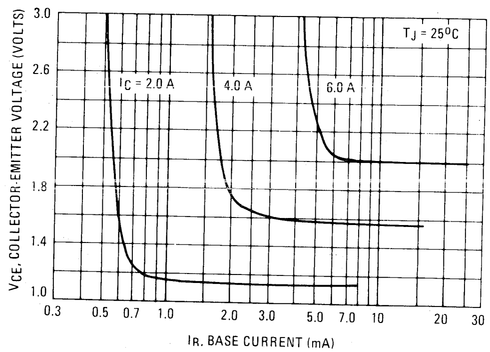
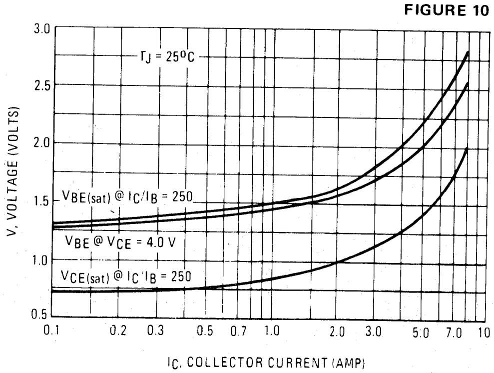
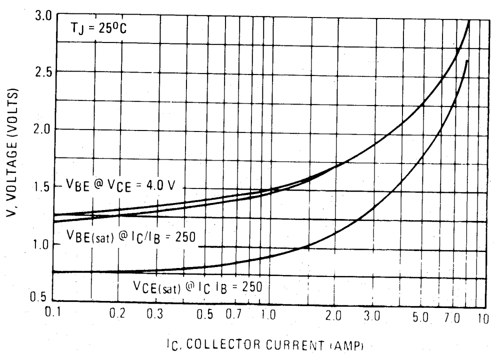


FIGURE 10 – "ON" VOLTAGES





3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN — **TIP140**, **TIP141**, **TIP142**

PNP — **TIP145**, **TIP146**, **TIP147**

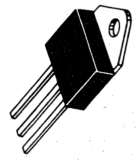
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain — Min h_{FE} = 1000 @ I_C = 5 A, V_{CE} = 4 V
- Collector-Emitter Sustaining Voltage — @ 30 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP140, TIP145
  80 Vdc (Min) — TIP141, TIP146
  100 Vdc (Min) — TIP142, TIP147
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor

10 AMPERE DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

60-100 VOLTS
125 WATTS



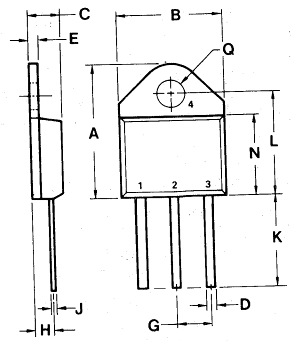
MAXIMUM RATINGS

Rating	Symbol	TIP140 TIP145	TIP141 TIP146	TIP142 TIP147	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous Peak (1)	I_C		10 15		Adc
Base Current — Continuous	I_B		0.5		Adc
Total Device Dissipation @ T_C = 25°C	P_D		125		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Case to Ambient	$R_{\theta JA}$	35.7	°C/W

(1) 5 ms, ≤10% Duty Cycle

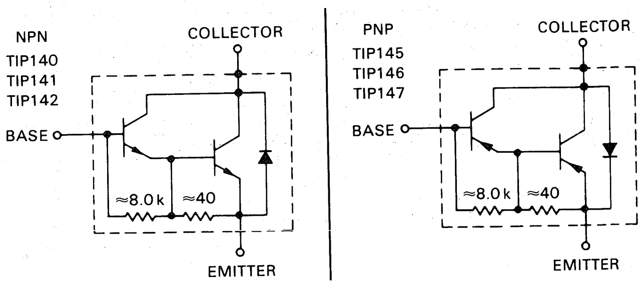


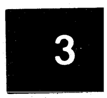
STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

CASE 340-01
TO-218AC

DARLINGTON SCHEMATICS





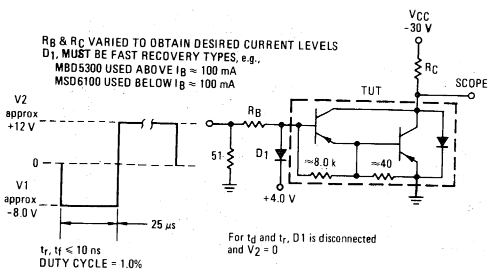
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mA, I_B = 0)	TIP140, TIP145 TIP141, TIP146 TIP142, TIP147	$V_{CEO(sus)}$	60 80 100	— — —	— — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	TIP140, TIP145 TIP141, TIP146 TIP142, TIP147	I_{CEO}	— — —	— — —	2.0 2.0 2.0	mA
Collector Cutoff Current (V_{CB} = 60 V, I_E = 0) (V_{CB} = 80 V, I_E = 0) (V_{CB} = 100 V, I_E = 0)	TIP140, TIP145 TIP141, TIP146 TIP142, TIP147	I_{CBO}	— — —	— — —	1.0 1.0 1.0	mA
Emitter Cutoff Current V_{BE} = 5.0 V		I_{EBO}	—	—	2.0	mA
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 5.0 A, V_{CE} = 4.0 V) (I_C = 10 A, V_{CE} = 4.0 V)		h_{FE}	1000 500	— —	— —	—
Collector-Emitter Saturation Voltage (I_C = 5.0 A, I_B = 10 mA) (I_C = 10 A, I_B = 40 mA)		$V_{CE(sat)}$	— —	— —	2.0 3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 A, I_B = 40 mA)		$V_{BE(sat)}$	—	—	3.5	Vdc
Base-Emitter On Voltage (I_C = 10 A, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	—	3.0	Vdc
SWITCHING CHARACTERISTICS						
Resistive Load (See Figure 1)						
Delay Time	(V_{CC} = 30 V, I_C = 5.0 A, I_B = 20 mA, Duty Cycle ≤ 2.0%, I_{B1} = I_{B2}, R_C & R_B Varied, T_J = 25°C)	t_d	—	0.15	—	μs
Rise Time		t_r	—	0.55	—	μs
Storage Time		t_s	—	2.5	—	μs
Fall Time		t_f	—	2.5	—	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

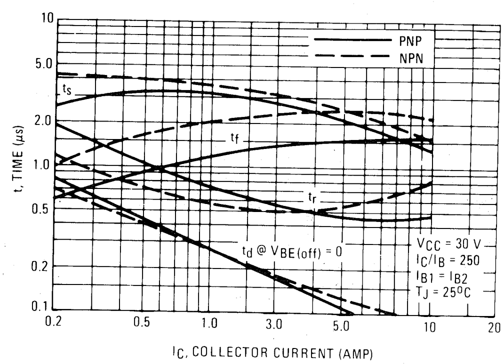
3

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

FIGURE 2 — SWITCHING TIMES



TYPICAL CHARACTERISTICS

NPN — **TIP140, TIP141, TIP142** | **PNP** — **TIP145, TIP146, TIP147**

FIGURE 3 — DC CURRENT GAIN versus COLLECTOR CURRENT

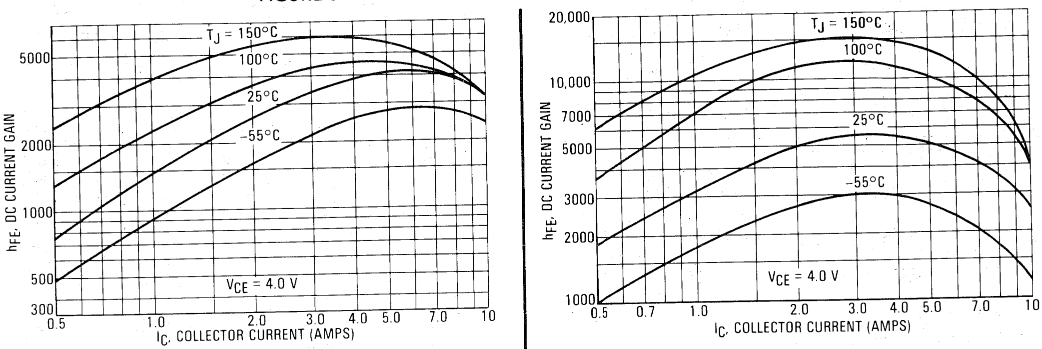


FIGURE 4 — COLLECTOR-EMITTER SATURATION VOLTAGE

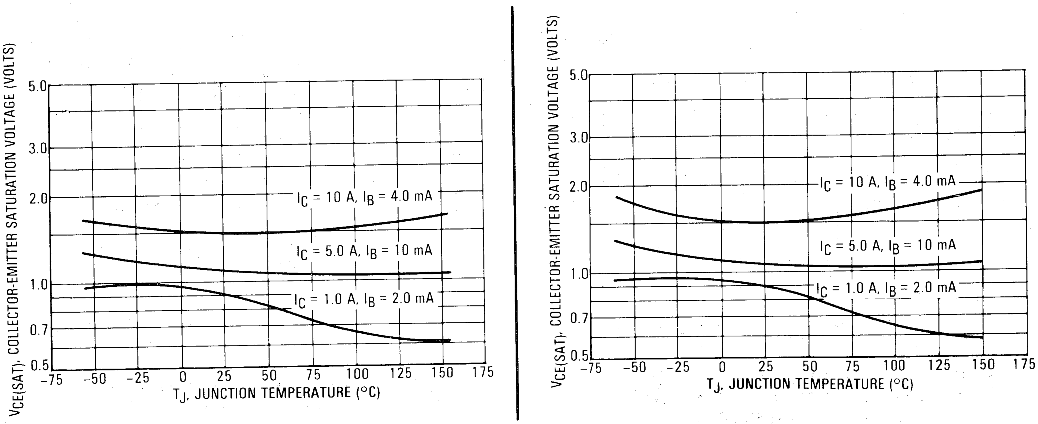
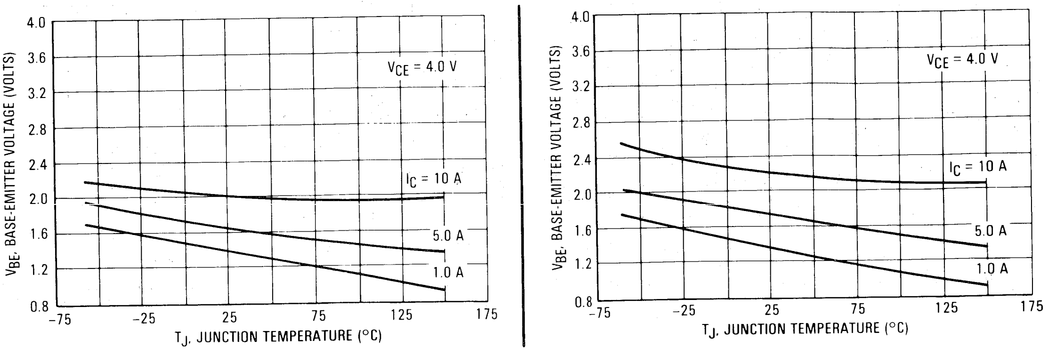


FIGURE 5 — BASE-EMITTER VOLTAGE



ACTIVE-REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — ACTIVE-REGION SAFE OPERATING AREA

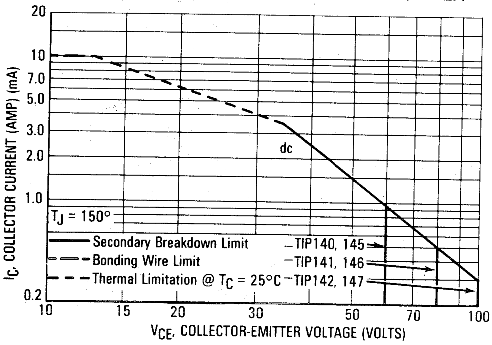


FIGURE 7 — UNCLAMPED INDUCTIVE LOAD

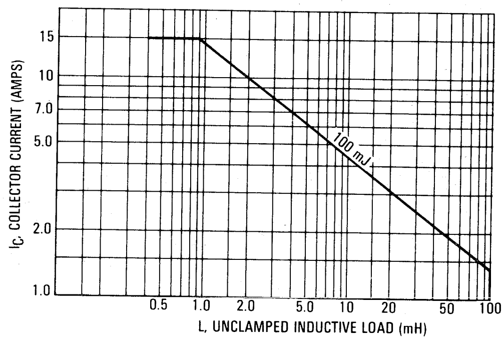
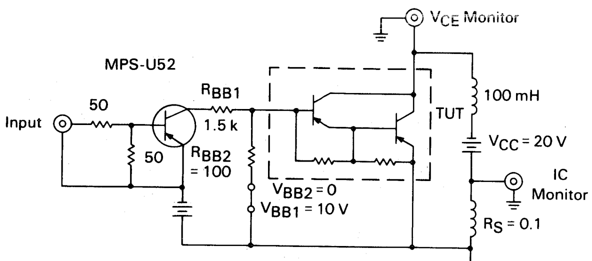
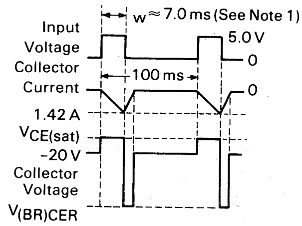


FIGURE 8 — INDUCTIVE LOAD



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTE 1: Input pulse width is increased until I_{CM} = 1.42 A.
NOTE 2: For NPN test circuit reverse polarities.

FIGURE 9 — MAGNITUDE OF COMMON EMITTER SMALL-SIGNAL SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO

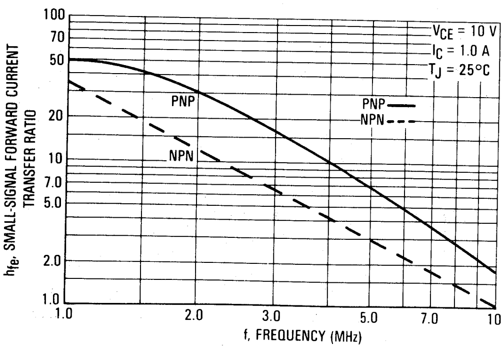
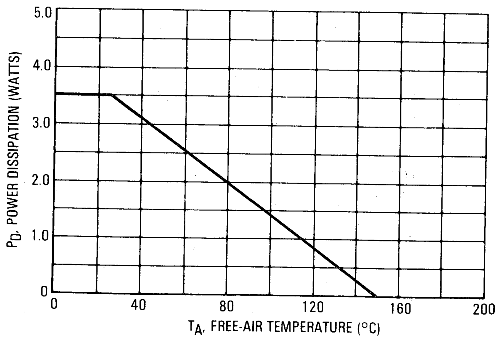


FIGURE 10 — FREE-AIR TEMPERATURE POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
TIP3055
PNP
TIP2955

COMPLEMENTARY SILICON POWER TRANSISTORS

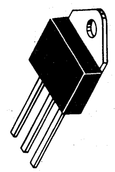
. . . designed for general-purpose switching and amplifier applications.

- DC Current Gain — h_{FE} = 20–70 @ I_C = 4.0 Adc
- Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4.0 Adc
- Excellent Safe Operating Area

15 AMPERE POWER TRANSISTORS

COMPLEMENTARY SILICON

60 VOLTS
90 WATTS

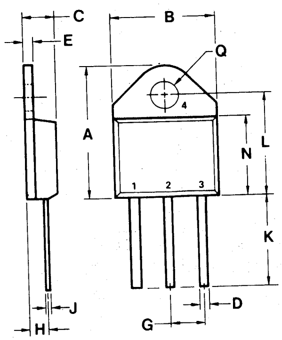


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Emitter Voltage	V_{CER}	70	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current	I_B	7.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	90 0.72	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.39	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	35.7	°C/W

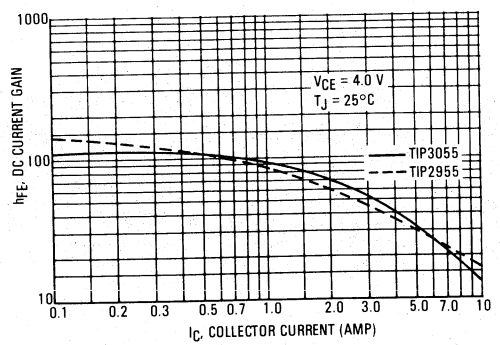


STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01 (TO-218AC)

FIGURE 1 — DC CURRENT GAIN



3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

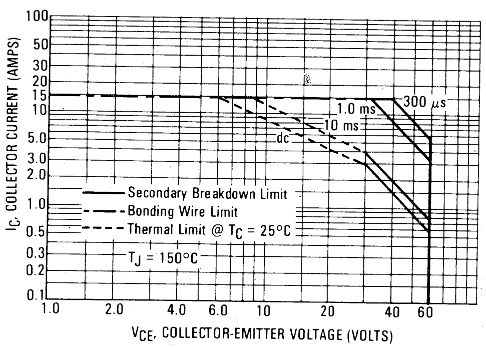
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 70 Vdc, R_{BE} = 100 Ohms)	I_{CER}	—	1.0	mAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	70 —	—
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	— —	1.1 3.0	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.8	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 30 Vdc, t = 1.0 s; Nonrepetitive)	$I_{s/b}$	3.0	—	Adc
DYNAMIC CHARACTERISTICS				
Current Gain—Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	—	MHz
Small-Signal Current Gain (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	h_{fe}	15	—	kHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2.0%.

Note: For additional design curves, refer to electrical characteristics curves of 2N3055.

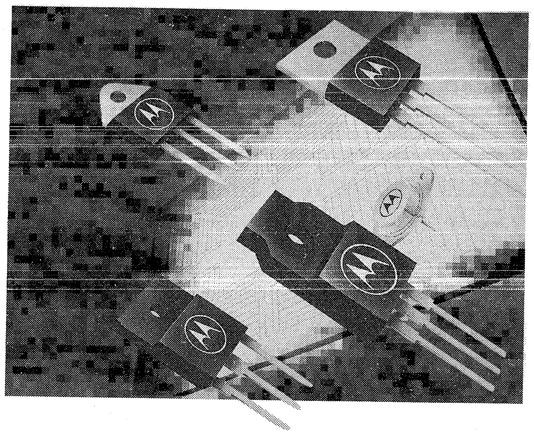
3

FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature.



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2 Selector Guide

3 Data Sheets

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